2Ω Max On Resistance, ±15 V/12 V/±5 V *i*CMOS™ Dual SPDT Switch

Preliminary Technical Data

ADG1436

FEATURES

2Ω Max On Resistance
0.5Ω Max On Resistance Flatness
200mA continious current
33 V supply range
Fully specified at +12 V, ±15 V, ±5 V
No V_L supply required
3 V logic-compatible inputs
Rail-to-rail operation
16-lead TSSOP and 16-lead LFCSP packages

APPLICATIONS

Automatic test equipment
Data aquisition systems
Battery-powered systems
Sample-and-hold systems
Audio signal routing
Communication systems
Relay Replacement

FUNCTIONAL BLOCK DIAGRAM

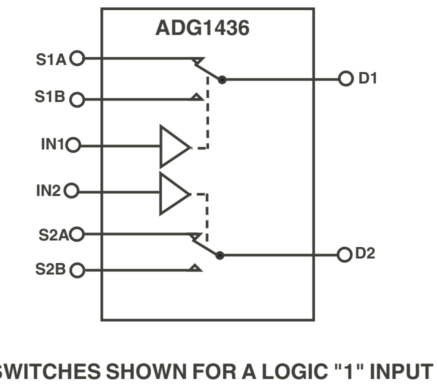

Figure 1.TSSOP package

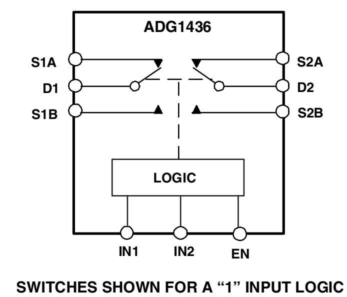

Figure 2.LFCSP package

GENERAL DESCRIPTION

The ADG1436 is a monolithic CMOS device containing two independently selectable SPDT switches. An EN input on the LFCSP package is used to enable or disable the device. When disabled, all channels are switched off. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

It is designed on an *i*CMOS process. *i*CMOS (industrial-CMOS) is a modular manufacturing process combining high voltage CMOS (complementary metal-oxide semiconductor) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages, while providing increased performance, dramatically lower power consumption, and reduced package size.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals. *i*CMOS construction ensures ultralow power dissipation, making the part ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 2Ω Max On Resistance over temperature.
2. Minimum distortion
3. 3 V logic-compatible digital inputs: V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. No V_L logic power supply required.
5. Ultralow power dissipation: <0.03 μW.
6. 16-lead TSSOP and 16-lead 4 mm × 4mm LFCSP packages.

Rev. PrC

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SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

	25°C	-40°C to +85°C	-40°C to +125°C		
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	1.5			Ω typ	V_S = ±10 V, I_S = −10 mA; Figure 23
		2		Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match between Channels (ΔR_{ON})	0.1			Ω typ	V_S = ±10 V, I_S = −10 mA
		0.5		Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.1			Ω typ	V_S = −5 V/0 V/+5 V; I_S = −10 mA
		0.5		Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = ±10 V, V_s = ±10 V; Figure 23
	±0.5	±2.5	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = ±10 V, V_s = ±10 V;; Figure 23
	±0.5	±2.5	±5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = ±10 V; Figure 23
	±1	±2.5	±5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.5	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, t_{TRANS}	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	150		200	ns max	V_S = +10 V; Figure 25
t_{ON} (EN)	85			ns typ	R_L = 300 Ω, C_L = 35 pF
	105	130	140	ns max	V_S = 10 V; see Figure 25
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	125	150	170	ns max	V_S = 10 V; see Figure 25
Break-before-Make Time Delay, t_D	15		40	ns typ	R_L = 300 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = +10 V; Figure 27
Charge Injection	50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; Figure 29
Off Isolation	50			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 30
Channel-to-Channel Crosstalk	60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 31
Total Harmonic Distortion + Noise	0.015			% typ	R_L = 110Ω, 5 V rms, f = 20 Hz to 20 kHz
−3 dB Bandwidth	100			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 32
C_S (Off)	35			pF typ	f = 1 MHz; V_S = 0 V
C_D (Off)	35			pF typ	f = 1 MHz; V_S = 0 V
C_D, C_S (On)	70			pF typ	f = 1 MHz; V_S = 0 V
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			µA typ	Digital Inputs = 0 V or V_{DD}
			1	µA max	
I_{DD}	150			µA typ	Digital Input = 5 V
			300	µA max	
I_{SS}	0.001			µA typ	Digital Inputs = 0 V, 5V or V_{DD}
			1.0	µA max	

	25°C	-40°C to +85°C	-40°C to +125°C		
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	Gnd = 0V

[1] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

	25°C	-40°C to +85°C	-40°C to +125°C		
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	2.5			Ω typ	V_S = +10 V, I_S = −10 mA; Figure 23
	3	4		Ω max	
On Resistance Match between Channels (ΔR_{ON})	0.1			Ω typ	V_S = +10 V, I_S = −10 mA
		0.5		Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.1			Ω typ	V_S = +3 V/+6 V/+9 V, I_S = −10 mA
		0.5			
LEAKAGE CURRENTS					V_{DD} = 12 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; Figure 24
	±0.5	±2.5	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; Figure 24
	±0.5	±2.5	±5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = 1 V or 10 V, Figure 25
	±1	±2.5	±5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.5	µA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, t_{TRANS}	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	150		200	ns max	V_S = 8 V; Figure 25
t_{ON} (EN)	85			ns typ	R_L = 300 Ω, C_L = 35 pF
	105	130	140	ns max	V_S = 8 V; Figure 25
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	125	150	170	ns max	V_S = 8 V; Figure 25
Break-before-Make Time Delay, t_D	15			ns typ	R_L = 300 Ω, C_L = 35 pF
			1	ns min	V_{S1} = V_{S2} = 8 V; Figure 27
Charge Injection	30			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; Figure 29
Off Isolation	50			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 30;
Channel-to-Channel Crosstalk	60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 31
Total Harmonic Distortion + Noise	0.015			% typ	R_L = 110Ω, 5 V rms, f = 20 Hz to 20 kHz
−3 dB Bandwidth	100			MHz typ	R_L = 50 Ω, C_L = 5 pF; Figure 32
C_S (Off)	35			pF typ	f = 1 MHz; V_S = 6V
C_D (Off)	35			pF typ	f = 1 MHz; V_S = 6V
C_D, C_S (On)	70			pF typ	f = 1 MHz; V_S = 6 V

	25°C	**-40°C to +85°C**	**-40°C to +125°C**		
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			μA typ	Digital Inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	150			μA typ	Digital Inputs = 5 V
			300	μA max	
V_{DD}			5/16.5	V min/max	Gnd = 0V, Vss = 0V

[1] Guaranteed by design, not subject to production test.

DUAL SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = -5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	3			Ω typ	V_S = ±3.3V, I_S = −10 mA; See figure x
		4		Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance Match Between Channels (ΔR_{ON})	0.1			Ω typ	V_S = ±3.3 V , I_S = −10 mA
				Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.1			Ω typ	V_S = −3 V/0 V/+3 V; I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; See figure x
	±0.5	±2.5	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.01			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; See figure x
	±0.5	±2.5	±5	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = ±4.5V; See figure x
	±1	±5	±5	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.5	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, t_{TRANS}	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	190		265	ns max	V_S = 3 V; Figure 25
t_{ON} (EN)	85			ns typ	R_L = 300 Ω, C_L = 35 pF
	105	130	140	ns max	V_S = 3 V; Figure 25
t_{OFF} (EN)	105			ns typ	R_L = 300 Ω, C_L = 35 pF
	125	150	170	ns max	V_S = 3 V; Figure 25
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 3 V; See figure 25
Charge Injection	50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; See figure x
Off Isolation	50			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; See figure x
Channel-to-Channel Crosstalk	60			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; See figure x

	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Total Harmonic Distortion + Noise	0.002			% typ	R_L = 110Ω, 5 V pp, f = 20 Hz to 20 kHz
−3 dB Bandwidth	200			MHz typ	R_L = 50 Ω, C_L = 5 pF; See figure x
C_S (Off)	35			pF typ	Vs = 0V, f = 1 MHz
C_D (Off)	35			pF typ	Vs = 0V, f = 1 MHz
C_D, C_S (On)	150			pF typ	Vs = 0V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V , Vss = -5.5V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	Gnd = 0V

[1] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Ratings
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	300 mA (pulsed at 1 ms, 10% duty cycle max)
Continuous Current, S or D	200 mA
Operating Temperature Range	
Automotive (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
16-Lead TSSOP, θ_{JA} Thermal Impedance	150.4°C/W
16-Lead LFCSP, θ_{JA} Thermal Impedance	72.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

[1] Over voltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition s above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

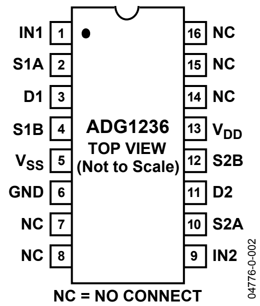

Figure 3.TSSOP Pin Configuration

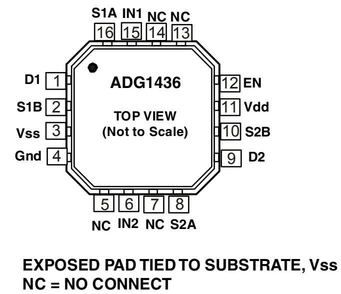

Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Function**
1	15	IN1	Logic Control Input.
2	16	S1A	Source Terminal. Can be an input or output.
3	1	D1	Drain Terminal. Can be an input or output.
4	2	S1B	Source Terminal. Can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14–16	5,7,13,14	NC	No Connect.
9	6	IN2	Logic Control Input.
10	8	S2A	Source Terminal. Can be an input or output.
11	9	D2	Drain Terminal. Can be an input or output.
12	10	S2B	Source Terminal. Can be an input or output.
13	11	V_{DD}	Most Positive Power Supply Potential.
-	12	EN	Active High Digital Input. When low, the device is disabled and all switches are off. When high, INx logic inputs determine the on switches.

TRUTH TABLE FOR SWITCHES

Table 6. ADG1436 TSSOP Truth Table

INx	Switch xA	Switch xB
0	Off	On
1	On	Off

Table 7. ADG1436 LFCSPTruth Table

EN	INx	SxA	SxB
0	X	Off	Off
1	0	Off	On
1	1	On	Off

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminals D and S.

R_{ON}
The ohmic resistance between D and S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{TRANS}
The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

Figure 6, On Resistance as a Function of V_D (V_S) for Single l Supply

Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

Figure 9. Leakage Current as a Function of V_D (V_S)

Figure 10. Leakage Currents as a Function of V_D (V_S)

Figure 11. Leakage Current as a Function of V_D (V_S)

Figure 12. Leakage Currents as a Function of Temperature

Figure 13. I_{DD} vs. Logic Level

Figure 14. Logic Threshold Voltage vs Supply Voltage

Figure 15. Charge Injection vs. Source Voltage

Figure 16. $t_{TRANSITION}$ Times vs. Temperature

Figure 17. Off Isolation vs. Frequency

Figure 18. Crosstalk vs. Frequency

Figure 19. On Response vs. Frequency

Figure 20. THD + N vs. Frequency

Figure 211. Capacitance vs. Source Voltage for Dual Supply

Figure 222. Capacitance vs. Source Voltage for Single Supply

TEST CIRCUITS

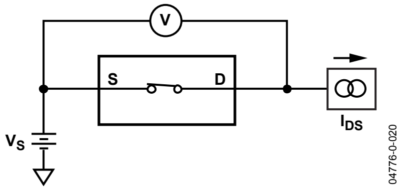

Figure 23. On Resistance

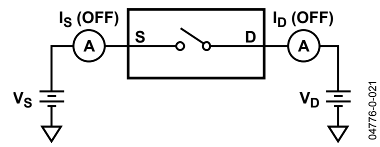

Figure 24. Off Resistance

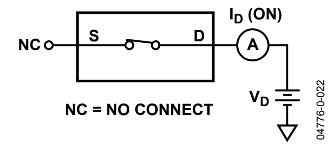

Figure 25. On Leakage

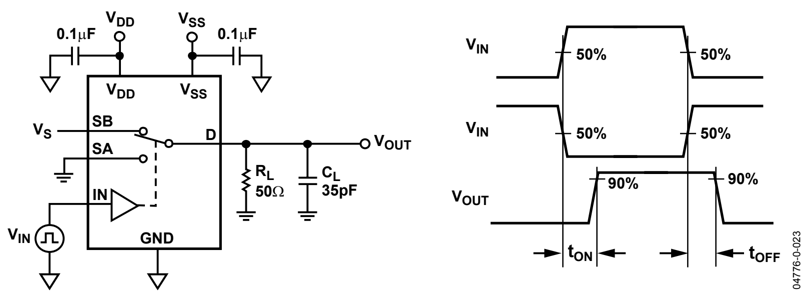

Figure 26. Switching Times

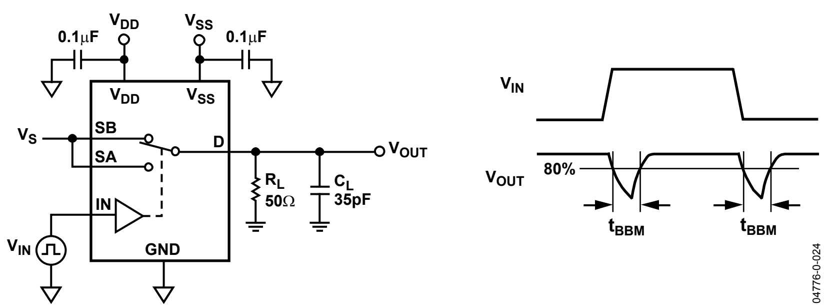

Figure 27. Break-before-Make Time Delay

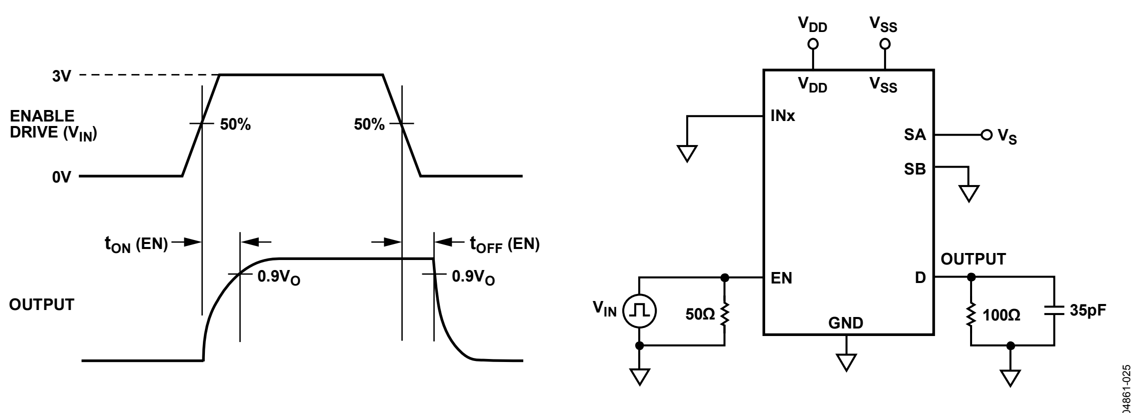

Figure 28. . Enable Delay, t_{ON} (EN), t_{OFF} (EN)

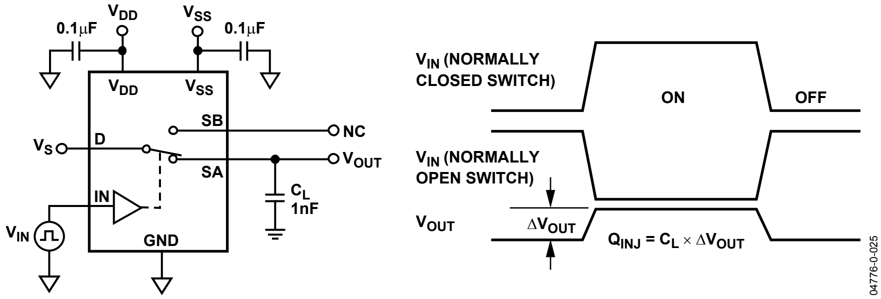

Figure 29. Charge Injection

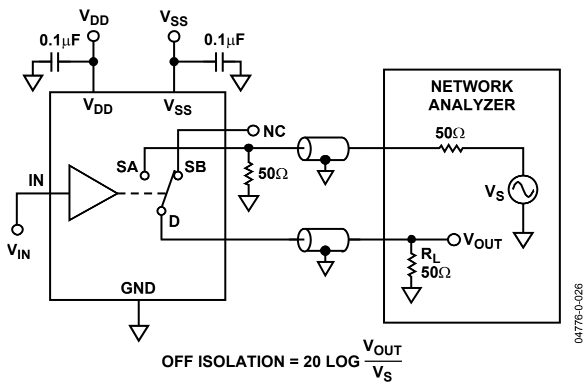

Figure 30. Off Isolation

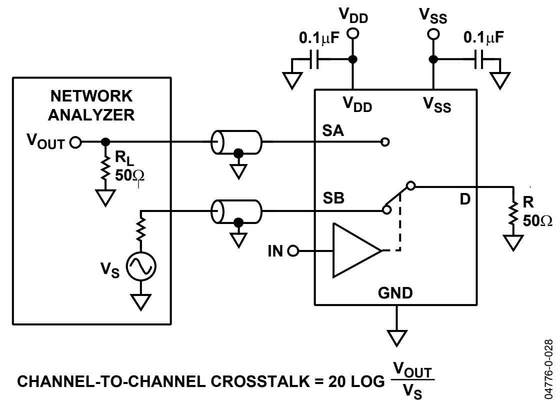

Figure 32. Bandwidth

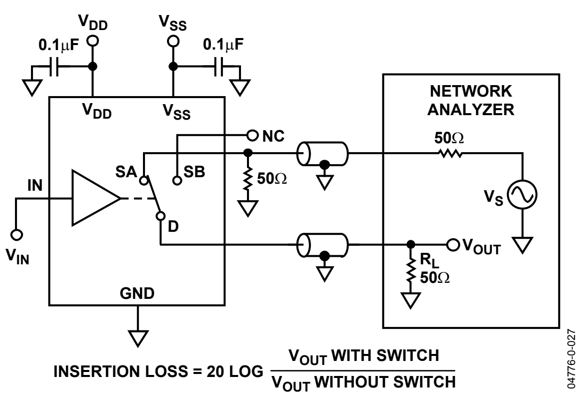

Figure 31. Channel-to-Channel Crosstalk

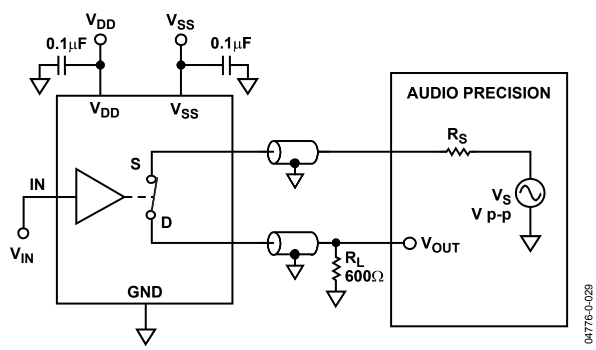

Figure 33. THD + Noise

OUTLINE DIMENSIONS

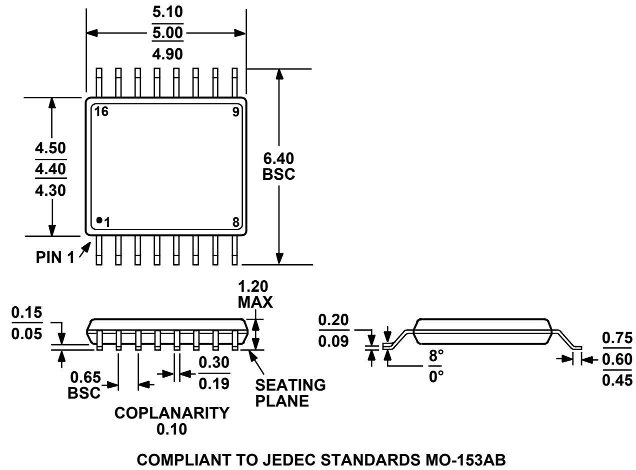

Figure 34. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in inches and (millimeters

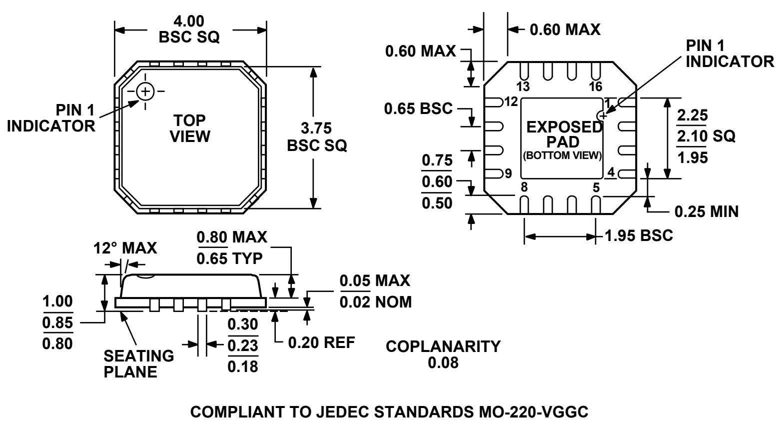

Figure 35. 16-Lead Lead Frame Chip Scale Package [VQ_LFCSP]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1436YRUZ	–40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1436YRUZ-REEL	–40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1436YRUZ-REEL7	–40°C to +125°C	Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1436YCPZ-500RL7	–40°C to +125°C	Lead Frame Chip Scale Package (LFCSP)	CP-16-4
ADG1436YCPZ-REEL7	–40°C to +125°C	Lead Frame Chip Scale Package (LFCSP)	CP-16-4

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