XR75100
40V Synchronous Step Down COT Controller

General Description

The XR75100 is a synchronous step-down controller for point-of load supplies up to 20A. A wide 5.5V to 40V input voltage range allows for single supply operation from industry standard 12V, 18V, and 24V DC and AC rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR75100 provides extremely fast line and load transient response using ceramic output capacitors. It requires no loop compensation hence simplifying circuit implementation and reducing overall component count. The control loop also provides exceptional load and line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in discontinuous mode (DCM) at light current loads thereby significantly increasing the converter efficiency.

A host of protection features, including over-current, over-temperature, short-circuit and UVLO, help achieve safe operation under abnormal operating conditions.

The XR75100 is available in RoHS compliant, green/halogen free space-saving 16-pin 3x3 QFN package.

FEATURES

- 20A Capable Step Down Controller
  - □ Wide 5.5V to 40V Input Voltage Range
  - □ Integrated High Current 2A/3A Drivers
  - □ 0.6 to 30V Adjustable Output Voltage
- Proprietary Constant On-Time Control
  - □ No Loop Compensation Required
  - □ Stable Ceramic Output Capacitor Operation
  - □ Programmable 200ns to 2µs On-Time
  - □ Constant 100kHz to 800kHz Frequency
  - □ Selectable CCM or CCM/DCM Operation
- Programmable Hiccup Current Limit with Thermal Compensation
- Precision Enable and Power Good flag
- Programmable Soft-start
- Integrated Bootstrap diode
- 16-pin QFN package

APPLICATIONS

- Networking and Communications
- Fast Transient Point-of-Loads
- Industrial and Medical Equipment
- Embedded High Power FPGA

Ordering Information – back page

Typical Application
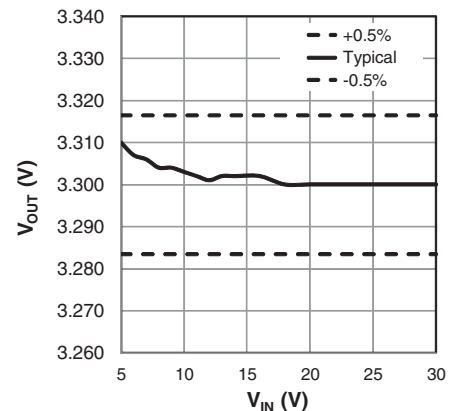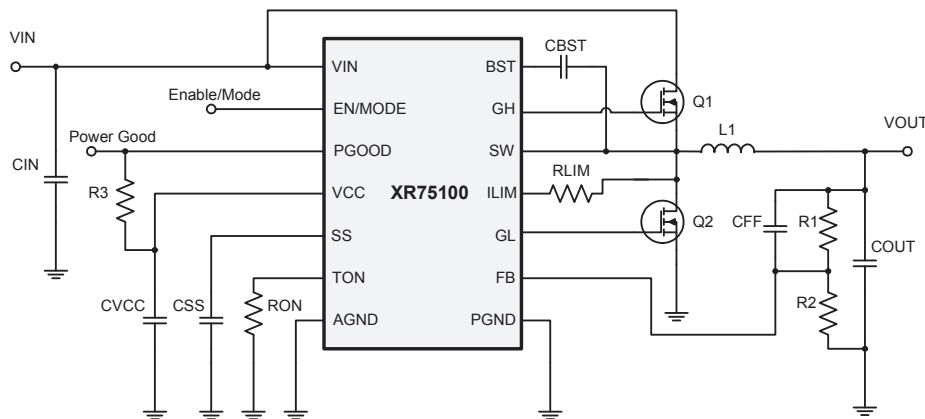
Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

V_{IN}···-0.3V to 43V

V_{CC}···-0.3V to 6.0V

BST···-0.3V to 48V[2]

BST-SW···-0.3V to 6V

SW, ILIM··-5V to 43V[1, 2]

GH··-0.3V to BST+0.3V

GH-SW··-0.3V to 6V

ALL other pins································-0.3V to VCC+0.3V

Storage Temperature····················-65°C to +150°C

Junction Temperature····················150°C

Power Dissipation·························Internally Limited

Lead Temperature (Soldering, 10 sec)················300°C

ESD Rating (HBM - Human Body Model)··············2kV

Operating Conditions

V_{IN}···-0.3V to 40V

V_{CC}···-0.3V to 5.5V

SW, ILIM··-1V to 40V[1]

PGOOD, VCC, TON, SS, EN, GL, FB··············-0.3V to 5.5V

Switching Frequency·····················100kHz to 800kHz[3]

Junction Temperature Range··············-40°C to +125°C

Note 1: SW pin's minimum DC range is -1V, transient is -5V for less than 50ns.

Note 2: No external voltage applied.

Note 3: Recommended

Electrical Characteristics

Unless otherwise noted: T_J= 25°C, V_{IN}=24V, BST=V_{CC}, SW=AGND=PGND=0V, CGH=CGL=3.3nF, 4.7uF at VCC-AGND. Limits applying over the full operating temperature range are denoted by a "•"

| Symbol	Parameter	Conditions		Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input Voltage Range	VCC regulating	•	5.5		40	V
I_{VIN}	VIN Input Supply Current	Not switching, V_{IN} = 24V, VFB = 0.7V	•		0.7	2	mA
		f=300kHz, RON=215k, VFB=0.58V			11		mA
I_{OFF}	Shutdown Current	Enable = 0V, V_{IN} = 24V			0.1		µA
Enable and Under-Voltage Lock-Out UVLO							
V_{IH_EN}	EN Pin Rising Threshold		•	1.8	1.9	2.0	V
V_{EN_HYS}	EN Pin Hysteresis				50		mV
V_{IH_EN}	EN Pin Rising Threshold for DCM/CCM operation		•	2.9	3.0	3.1	V
V_{EN_HYS}	EN Pin Hysteresis				100		mV
	VCC UVLO Start Threshold, Rising Edge		•	4.00	4.25	4.50	V

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	VCC UVLO Hysteresis				200		mV
Reference Voltage							
V_{REF}	Reference Voltage	V_{IN} = 5.5V to 40V		0.597	0.600	0.603	V
			•	0.594	0.600	0.606	V
	DC Line Regulation	CCM, closed loop, V_{IN}=5.5V-30V, applies to any C_{OUT}			±0.3		%
	DC Load Regulation	CCM, closed loop, I_{OUT}=0A-10A, applies to any C_{OUT}			±0.15		%
Programmable Constant On-Time							
	Maximum Recommended On-Time	R_{ON} = 237k, V_{IN} = 40V			2.0		us
	On-Time 1	R_{ON} = 237k, V_{IN} = 40V	•	1.7	2.0	2.3	us
	f Corresponding to On-Time 1	V_{IN} = 40V, V_{OUT} = 24V		261	300	353	kHz
	Minimum Programmable On-Time	R_{ON} = 14k, V_{IN} = 40V			120		ns
		R_{ON} = 14k, V_{IN} = 24V			200	230	ns
	On-Time 2	R_{ON} = 14k, V_{IN} = 24V	•	170	200	230	ns
	f Corresponding to On-Time 2	V_{OUT} = 5V		906	1042	1225	kHz
		V_{OUT} = 3.3V		598	688	809	kHz
	On-Time 3	R_{ON} = 35.7k, V_{IN} = 24V	•	430	506	582	ns
	Minimum Off-Time		•		250	350	ns
Diode Emulation Mode							
	Zero Crossing Threshold	DC value measured during test			-1		mV
Soft-start							
	SS Charge Current		•	-14	-10	-6	µA
	SS Discharge Current	Fault present	•	1			mA
VCC Linear Regulator							
	VCC Output Voltage	V_{IN} = 6V to 40V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 5.5V, I_{LOAD} = 0 to 20mA	•	4.8	5.0	5.2	V
Power Good Output							
	Power Good Threshold			-10	-7.5	-5	%
	Power Good Hysteresis				2	4	%
	Power Good Sink Current			1			mA
Protection: OCP, OTP, Short-Circuit							
	Hiccup Timeout				110		ms
	ILIM Pin Source Current			45	50	55	µA
	ILIM Current Temperature Coefficient				0.4		%/°C

Symbol	Parameter	Conditions		Min	Typ	Max	Units
	OCP Comparator Offset		•	-8	0	+8	mV
	Current Limit Blanking	GL rising>1V			100		ns
	Thermal Shutdown Threshold[1]	Rising temperature			150		°C
	Thermal Hysteresis[1]				15		°C
	VSCTH Feedback Pin Short-Circuit Threshold	Percent of VREF, short circuit is active after PGOOD is up	•	50	60	70	%
Output Gate Drivers							
	GH Pull-Down Resistance	IGH = 200mA			1.35	2.0	Ω
	GH Pull-Up Resistance	IGH = 200mA			1.8	2.8	Ω
	GL Pull-Down Resistance	IGL = 200mA			1.35	1.9	Ω
	GL Pull-Up Resistance	IGL = 200mA			1.7	2.7	Ω
	GH and GL Pull-down Resistance				50		kΩ
	GH and GL Rise Time	10% to 90%			35	50	ns
	GH and GL Fall Time	90% to 10%			30	40	ns
	GL to GH Non-Overlap Time	Measured GL falling edge = 1V to GH rising edge = 1V, BST=VCC, SW = 0V			30	60	ns
	GH to GL Non-Overlap Time	Measured GH falling edge = 1V to GL rising edge = 1V			20	40	ns

Note 1: Guaranteed by design

Pin Configuration
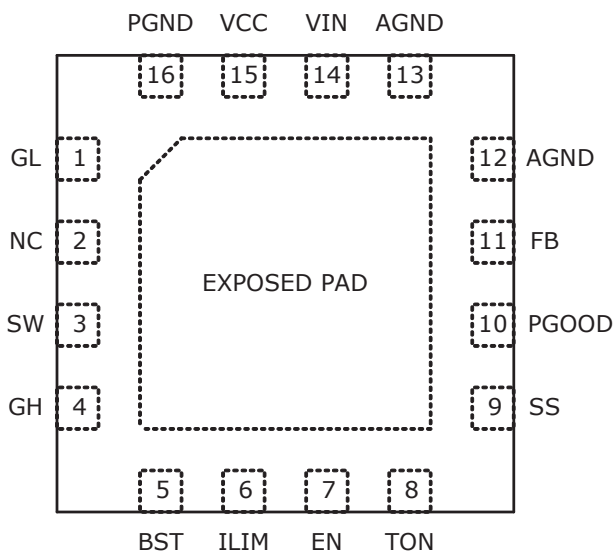
Pin Assignments

Pin No.	Pin Name	Type	Description
1	GL	O	Driver output for Low-side N-channel synchronous MOSFET.
2	NC		Internally not connected. Leave this pin floating.
3	SW	A	Lower supply rail for high-side gate driver GH. Connect this pin to the junction between the two external N-channel MOSFETs.
4	GH	O	Driver output for high-side N-channel switching MOSFET.
5	BST	A	High-side driver supply pin. Connect a 0.1uF bootstrap capacitor between BST and SW.
6	ILIM	A	Over-current protection programming. Connect with a resistor to the drain of the low-side MOS-FET.
7	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the IC on and it will operate in Forced CCM. If the voltage is raised above 3.0V, then the IC will operate in DCM or CCM depending on load.
8	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
9	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10uA internal source current.
10	PGOOD	OD	Power-good output. This open-drain output is pulled low when VOUT is outside the regulation.
11	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and GND in order to program VOUT.
12, 13	AGND	A	Analog ground. Control circuitry of the IC is referenced to this pin.
14	VIN	PWR	IC supply input. Provides power to internal LDO.
15	VCC	PWR	The output of LDO. For operation using a 5V rail, VCC should be shorted to VIN.
16	PGND	PWR	Low side driver ground
	Exposed Pad	A	Thermal pad for heat dissipation. Connect to AGND with a short trace.

Type: A = Analog, I = Input, O = Output, I/O = Input/Output, PWR = Power, OD = Open-Drain

Functional Block Diagram

XR75100
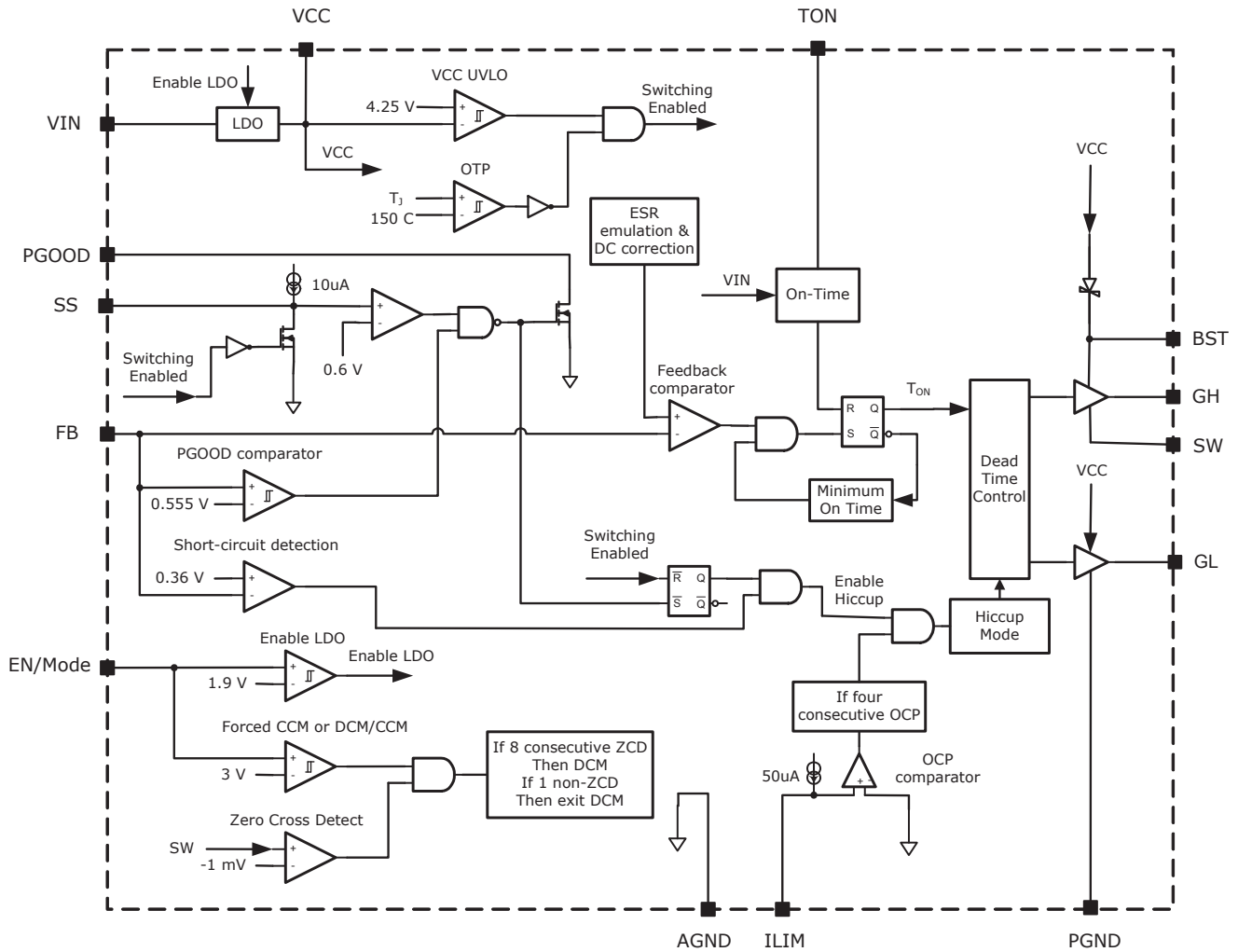
Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 24V, V_{OUT}=3.3V, I_{OUT}=10A, f=500kHz, T_A = 25°C. Schematic from the application information section.
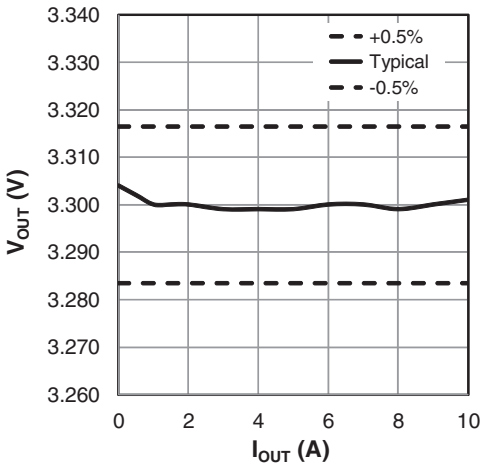

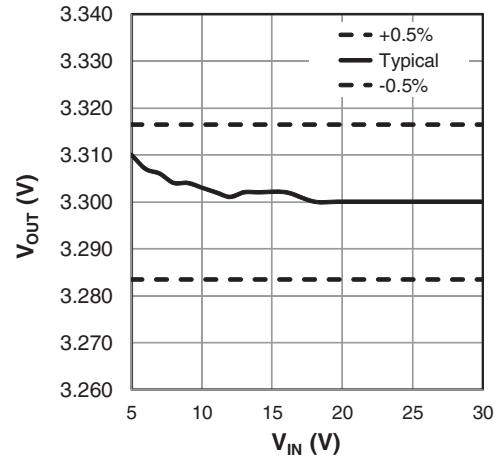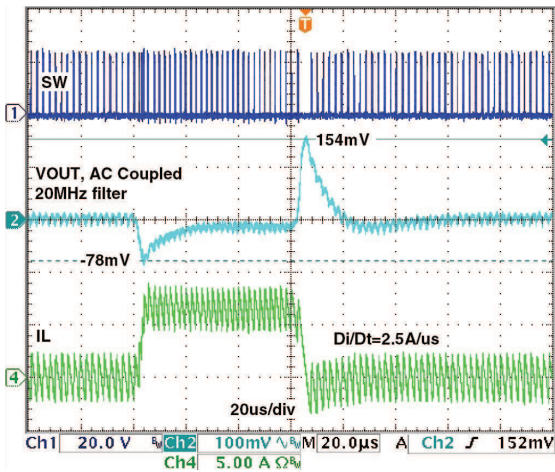Figure 1: Load Regulation

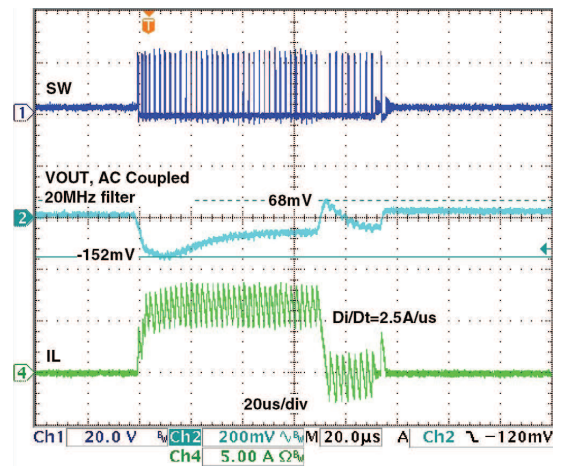Figure 2: Line regulation

Figure 3: Load step, Forced CCM, 0A-6.5A-0A
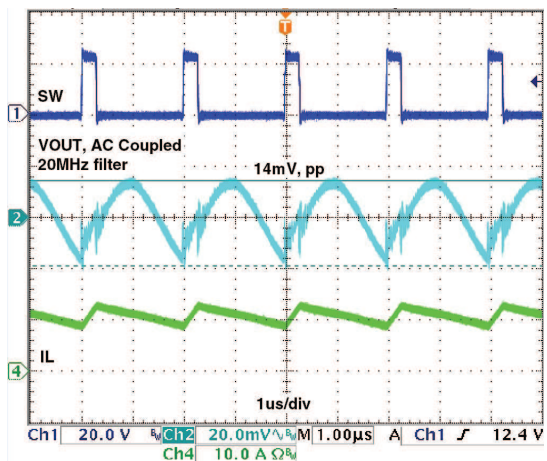

Figure 4: Load step, DCM/CCM, 0A-6.5A-0A

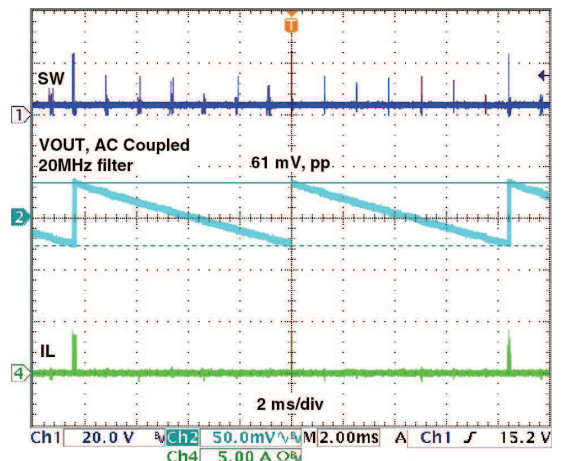Figure 5: Steady state, $V_{OUT,ripple}$=14mV, I_{OUT}=10A
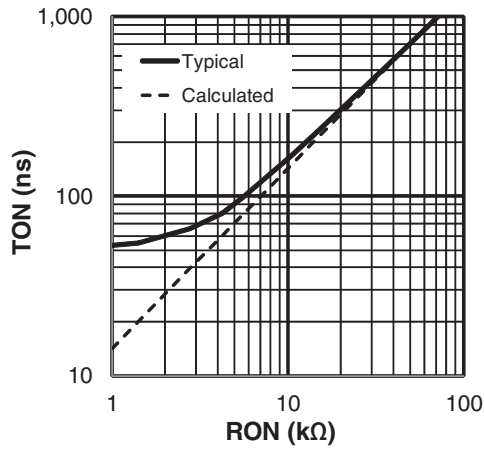

Figure 6: Steady state, DCM, $V_{OUT,ripple}$=61mV, I_{OUT}=0A

Figure 7: TON versus V$_{IN}$=24V
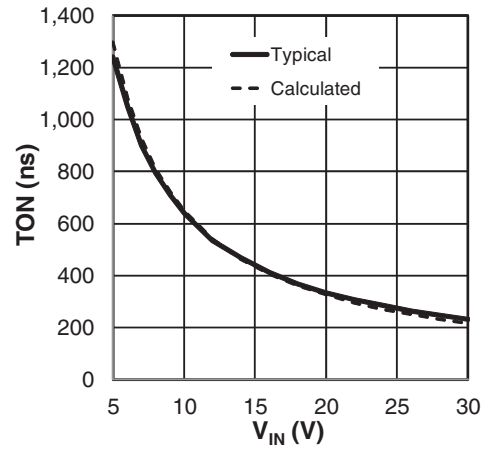
Figure 8: TON versus V$_{IN}$, RON=19.1k
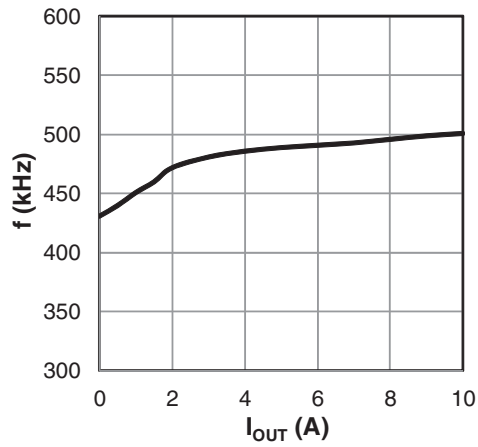
Figure 9: frequency versus I$_{OUT}$, V$_{IN}$=24V
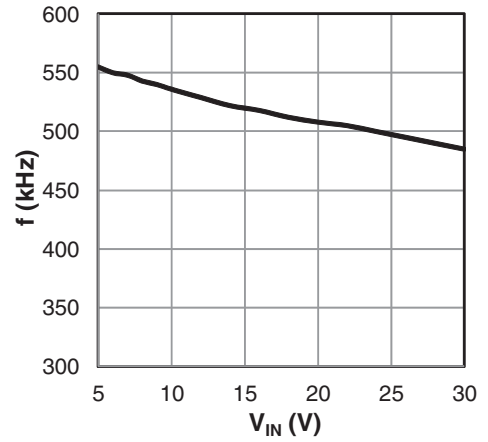
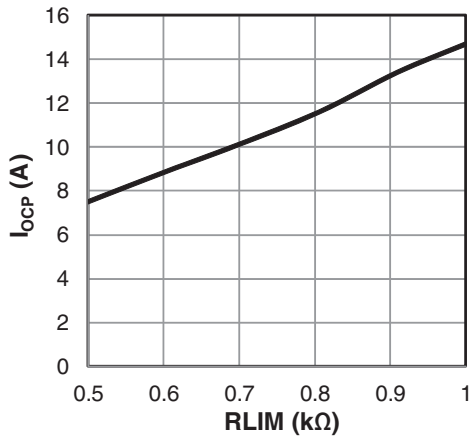Figure 10: frequency versus V$_{IN}$, I$_{OUT}$=10A
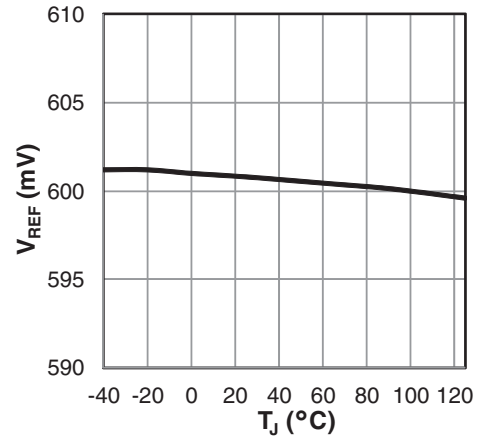

Figure 11: I$_{OCP}$ versus RLIM

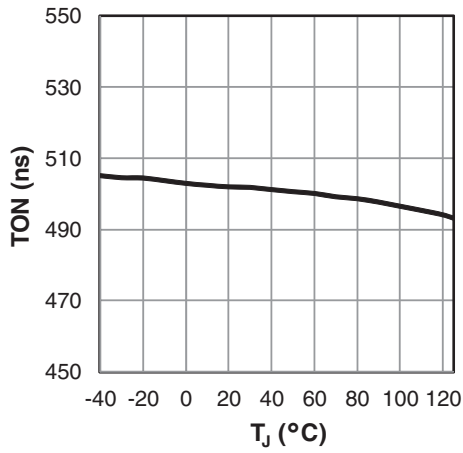Figure 12: V$_{REF}$ versus temperature
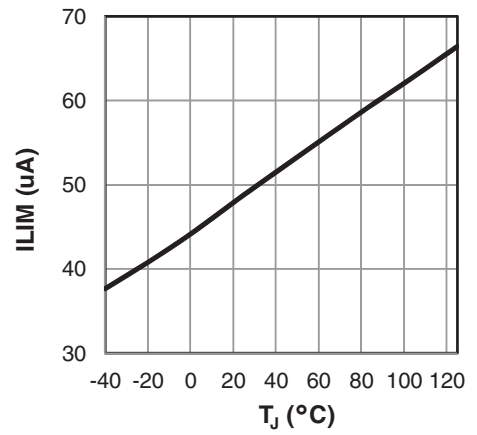
Figure 13: TON versus temperature

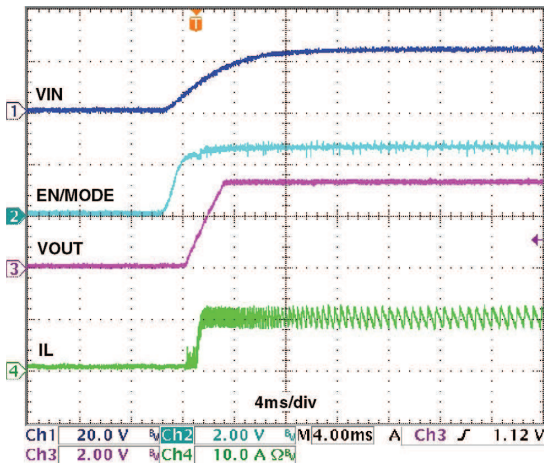Figure 14: ILIM versus temperature
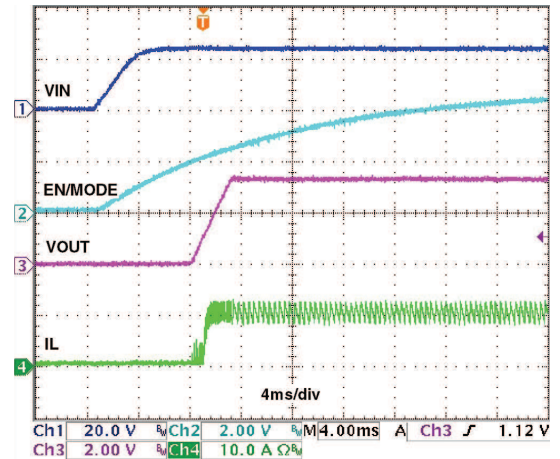

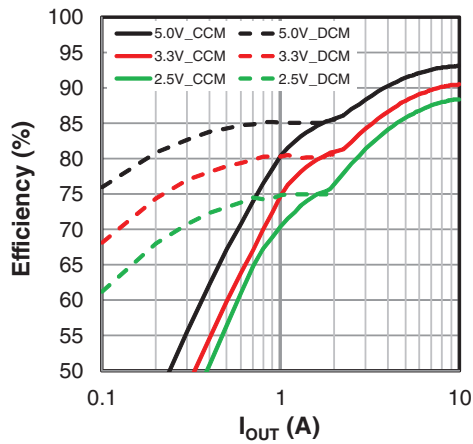Figure 15: Powerup, Forced CCM

Figure 16: Powerup, DCM/CCM

Figure 17: Efficiency, V_{IN}=24V, f=500kHz

Functional Description

XR75100 is a synchronous step-down proprietary emulated current-mode Constant On-Time (COT) controller. The on-time, which is programmed via RON, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control allows the use of ceramic output capacitors.

Each switching cycle begins with GH signal turning the high-side (switching) FET for a preprogrammed time. At the end of the on-time the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the minimum off-time the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When VFB drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable/Mode Input (EN/MODE)

EN/MODE pin accepts a tri-level signal that is used to control turn on/off. It also selects between two modes of operation: 'Forced CCM' and 'DCM/CCM'. If EN is pulled below 1.8V the IC shuts down. A voltage between 2.0V and 2.9V selects the Forced CCM mode, which will run the converter in continuous conduction at all times. A voltage higher than 3.1V selects the DCM/CCM mode, which will run the converter in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the controller to operate in Forced CCM a voltage between 2.0V and 2.9V has to be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. The EN/MODE can be derived from V_{IN} where an external control is not available. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.45V. If V_{IN} varies over a wide range, the circuit shown in figure 18 can be used to generate the required voltage.

Selecting the DCM/CCM Mode

In order to set the controller operation to DCM/CCM a voltage between 3.1V and 5.5V has to be applied to EN/MODE pin. This voltage must be sequenced with respect to V_{OUT} such that $2.0V \leq V_{EN} < 2.9V$ when V_{OUT} completes softstart.

If an external 5V control signal is available use a low-pass RC and set the time constant to RC=5.5tss where tss is the softstart time. R should be in the 100k-200k range. Time t1 can be calculated from t1=2.8tss. The timing circuit and diagram are shown in figure 19.

If an external 3.3V control signal is available, use a low-pass RC and set th time constant to RC=2.1tss where tss is the softstart time. R should be in the 100k-200k range. Time t1 can be calculated from t1=1.9tss (figure 19).
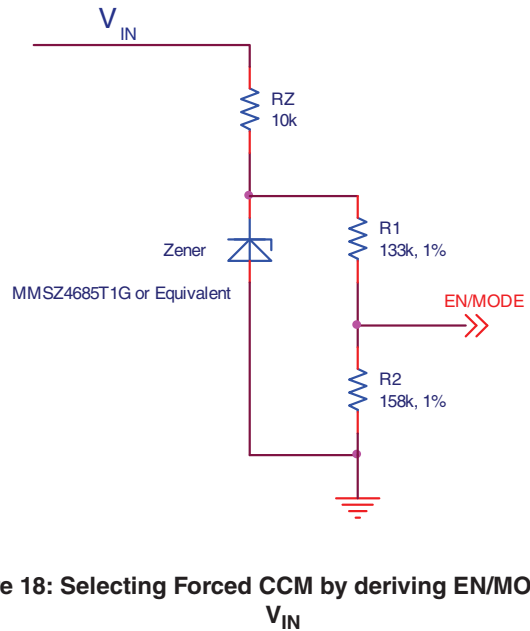

Figure 18: Selecting Forced CCM by deriving EN/MODE from V_{IN}
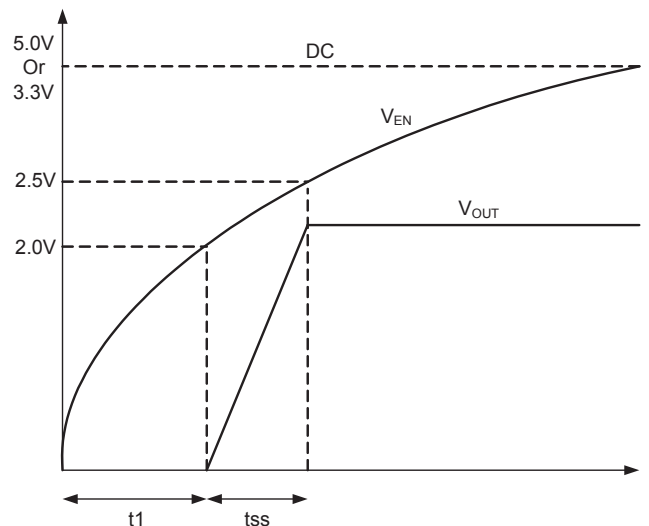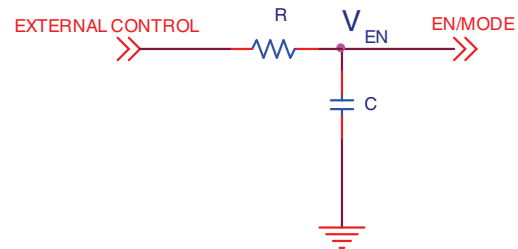

Figure 19: Timing circuit and diagram for selecting DCM/CCM by using an external enable signal.

EN/MODE input has to be derived from V_{IN} in applications where an external control is not available. The timing circuit and diagram are shown in figure 20. Calculate the time constant from RC=4.7tss. The value of R should be between 100k and 200k. t1 can be calculated from t1=2.7tss. The R and C in figure 20 correspond to 2.8ms softstart of the application circuit. The powerup waveforms are shown in figure 16.
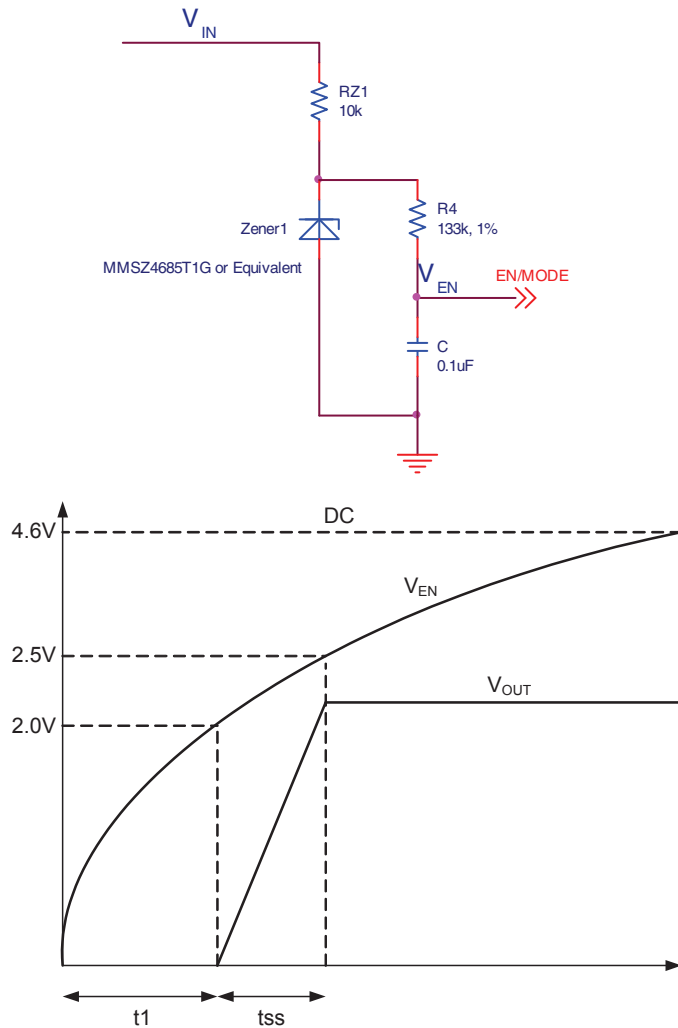

Figure 20: Timing circuit and diagram for selecting DCM/CCM by deriving EN/MODE from V_{IN}.

Programming the On-Time

The on-time TON is programmed via resistor RON according to following equation:

$$RON = \frac{V_{IN} \times TON}{3.4 \times 10^{-10}}$$

where TON is calculated from:

$$TON = \frac{V_{OUT}}{V_{IN} \times f}$$

As an example the calculated TON for the application circuit is 275ns. An RON of 19.4k is required in order to set TON to 275ns. A graph of typical TON versus RON is shown in figure 7.

Over-Current Protection (OCP)

If load current exceeds the programmed over-current I_{OCP} for four consecutive switching cycles, then IC enters hiccup mode of operation. In hiccup the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout a soft-start is attempted. If OCP persists, hiccup timeout will repeat. The IC will remain in hiccup mode until load current is reduced below the programmed I_{OCP} In order to program over-current protection use the following equation:

$$RLIM = \frac{(I_{OCP} \times RDS) + 8mV}{ILIM}$$

Where:

RLIM is resistor value for programming I_{OCP}

I_{OCP} is the over-current threshold to be programmed

RDS is the MOSFET rated on resistance

8mV is the OCP comparator offset

ILIM is the internal current that generates the necessary OCP comparator threshold (use 45µA).

Note that ILIM has a positive temperature coefficient of 0.4%/°C. This is meant to roughly match and compensate for positive temperature coefficient of the synchronous FET. In order for this feature to be effective the temperature rise of the IC should approximately match the temperature rise of the FET. A graph of typical I_{OCP} versus RLIM is shown in figure 11.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the IC will enter hiccup mode. Hiccup will persist until short-circuit is removed. SCP circuit becomes active after PGOOD asserts high.

Over-Temperature (OTP)

OTP triggers at a nominal die temperature of 150°C. The gate of switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in the application circuit to program the output voltage V_{OUT}.

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.6} - 1 \right)$$

where R2 has a nominal value of 2kΩ.

Programming the Soft-start

Place a capacitor CSS between the SS and GND pins to program the soft-start. In order to program a soft-start time of TSS, calculate the required capacitance CSS from the following equation:

$$CSS = TSS \times \left(\frac{10\mu A}{0.6V} \right)$$

Feed-Forward Capacitor (CFF)

The voltage divider R1-R2 attenuates the output voltage ripple that is fed back to controller's FB pin. The steady-state voltage ripple at FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for controller to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV, a CFF should not be used. COUT should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

It is recommended to use a feed-forward capacitor (CFF) if output voltage ripple is less than 50mV. CFF provides a low-impedance/high-frequency path for the output voltage ripple to be transmitted to FB. It also helps get an optimum load transient response. Calculate CFF from:

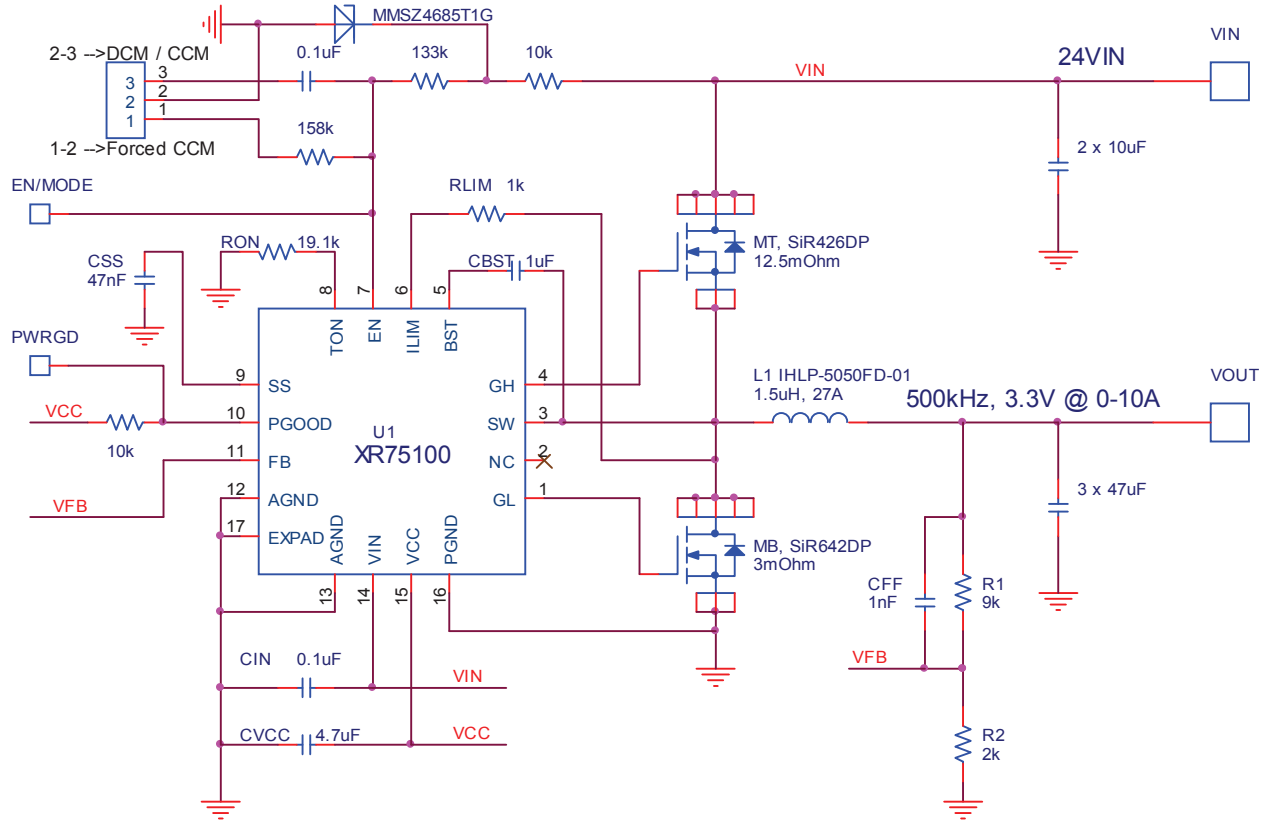$$CFF = \frac{1}{2 \times \pi \times f \times 0.1 \times R1}$$

A load step test should be performed and if necessary CFF can be adjusted in order to get a critically damped load transient response.

Feed-Forward Resistor (RFF)

In order to prevent switching noise from coupling to the FB pin it may be necessary to place a resistor RFF in series with CFF. Calculate RFF from:
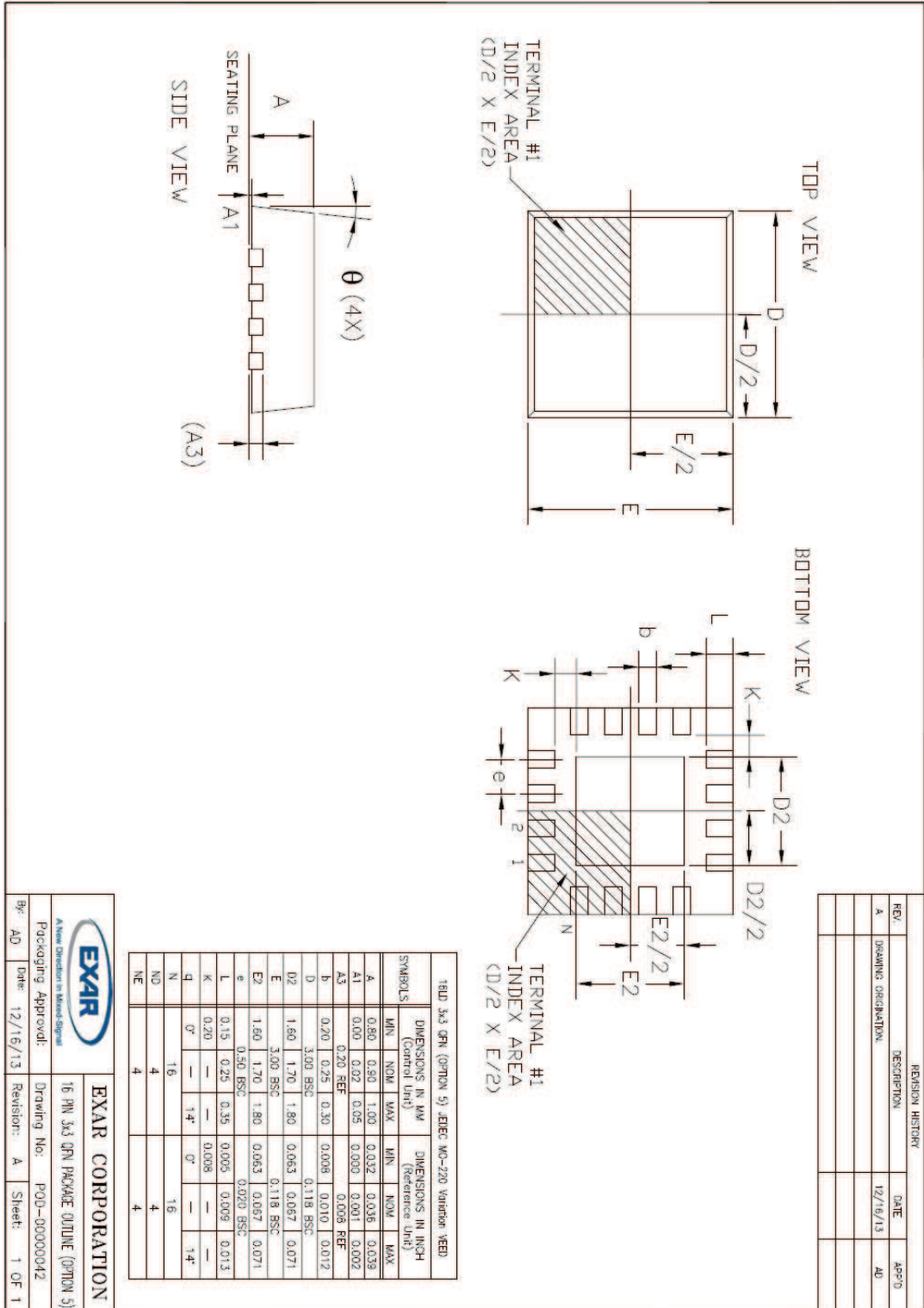
$$RFF = \frac{20ns}{CFF}$$

Application Circuit

Application Circuit for XR75100, 500kHz, 3.3V @ 0-10A, 24VIN to VOUT

Key components and labels:
- 24VIN, VIN, VOUT
- MMSZ4685T1G
- 2-3 --> DCM / CCM
- 1-2 --> Forced CCM
- EN/MODE
- CSS 47nF
- RON 19.1k
- RLIM 1k
- CBST 1uF
- PWRGD
- VCC 10k
- VFB
- 0.1uF, 133k, 10k, 158k
- 2 x 10uF
- MT, SiR426DP 12.5mOhm
- MB, SiR642DP 3mOhm
- L1 IHLP-5050FD-01 1.5uH, 27A
- 3 x 47uF
- CFF 1nF
- R1 9k
- R2 2k
- CIN 0.1uF
- CVCC 4.7uF

U1 XR75100 pin labels:
- TON (8), EN (7), ILIM (6), BST (5)
- SS (9), PGOOD (10), FB (11), AGND (12), EXPAD (17)
- AGND (13), VIN (14), VCC (15), PGND (16)
- GH (4), SW (3), NC (2), GL (1)

Mechanical Dimensions

16-Pin QFN

16LD 3x3 QFN (OPTION 5) JEDEC MO-220 Variation VEED

SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.036	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.006 REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.00 BSC			0.118 BSC		
D2	1.60	1.70	1.80	0.063	0.067	0.071
E	3.00 BSC			0.118 BSC		
E2	1.60	1.70	1.80	0.063	0.067	0.071
e	0.50 BSC			0.020 BSC		
L	0.15	0.25	0.35	0.005	0.009	0.013
K	0.20	–	–	0.008	–	–
q	0°	–	14°	0°	–	14°
N	16			16		
ND	4			4		
NE	4			4		

EXAR CORPORATION

A New Direction in Mixed-Signal
Packaging Approval:
By: AD   Date: 12/16/13

16 PIN 3x3 QFN PACKAGE OUTLINE (OPTION 5)
Drawing No: POD-00000042
Revision: A   Sheet: 1 OF 1

ECN: 1351-04 12/16/2013

REVISION HISTORY

REV.	DESCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	12/16/13	AD

Ordering Information

Part Number	Package	JEDEC Compliant	Operating Temperature Range	Packaging Quantity	Marking
XR75100EL-F	16-pin QFN	Yes	-40°C to +125°C	Bulk	75100 YYWW XXXXX
XR75100ELMTR-F	16-pin QFN	Yes	-40°C to +125°C	250 / Reel	
XR75100ELTR-F	16-pin QFN	Yes	-40°C to +125°C	3000 / Reel	
XR75100EVB	Evaluation Board	N/A	N/A	N/A	N/A

"YY" = Year (last two digits)- "WW" = Work Week- "X" = Lot Number; when applicable

Revision History

Revision	Date	Description
1A	June 2014	Initial release [ECN1426-21_6/27/2014]

For Further Assistance:

Technical Support: techsupport.exar.com

Technical Documentation: www.exar.com/techdoc

Exar Corporation Headquarters and Sales Offices
48720 Kato Road   Tel.: +1 (510) 668-7000
Fremont, CA 95438 - USA   Fax: +1 (510) 668-7001

EXAR
A New Direction in Mixed-Signal

exar.com/XR75100
Rev 1A