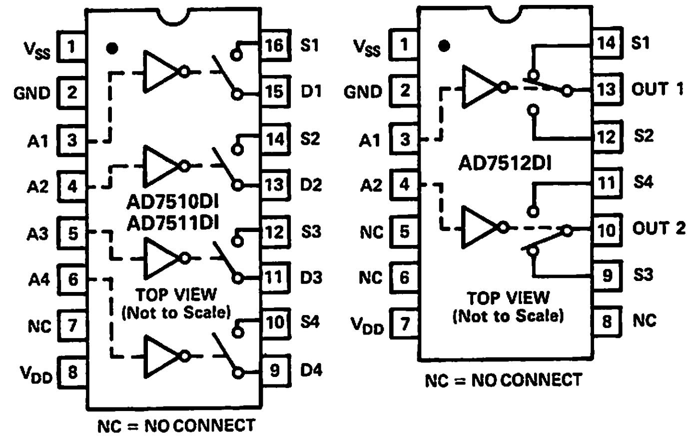
DI CMOS Protected Analog Switches

AD7511

FEATURES
- **Latch-Proof**
- **Overvoltage-Proof: ±25V**
- **Low R_{ON}: 75Ω**
- **Low Dissipation: 3mW**
- **TTL/CMOS Direct Interface**
- **Silicon-Nitride Passivated**
- **Monolithic Dielectrically-Isolated CMOS**
- **Standard 14-/16-Pin DIPs and 20-Terminal Surface Mount Packages**

AD7510 and AD7512 are obsolete

DIP FUNCTIONAL DIAGRAMS



GENERAL DESCRIPTION

The AD7510DI, AD7511DI and AD7512DI are a family of latch proof dielectrically isolated CMOS switches featuring overvoltage protection up to ±25V above the power supplies. These benefits are obtained without sacrificing the low "ON" resistance (75Ω) or low leakage current (500pA), the main features of an analog switch.

The AD7510DI and AD7511DI consist of four independent SPST analog switches packaged in either a 16-pin DIP or a 20-terminal surface mount package. They differ only in that the digital control logic is inverted. The AD7512DI has two independent SPDT switches packaged either in a 14-pin DIP or a 20-terminal surface mount package.

Very low power dissipation, overvoltage protection and TTL/CMOS direct interfacing are achieved by combining a unique circuit design and a dielectrically isolated CMOS process. Silicon nitride passivation ensures long term stability while monolithic construction provides reliability.

The AD7510 and AD7512 are no longer available.

CONTROL LOGIC

AD7510DI: Switch "ON" for Address "HIGH"

AD7511DI: Switch "ON" for Address "LOW"

AD7512DI: Address "HIGH" makes S1 to Out 1 and S3 to Out 2

REV. B

Document Feedback

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(V_{DD} = +15V, V_{SS} = −15V, unless otherwise noted.)

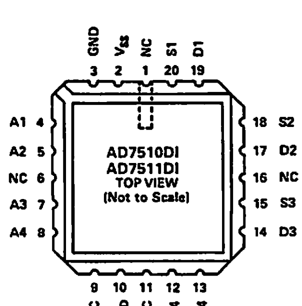
INDUSTRIAL VERSION (K)

PARAMETER	MODEL	VERSION	+25°C (N, P, Q)	0 to +70°C (N, P) -25°C to +85°C (Q)	TEST CONDITIONS
ANALOG SWITCH					
R_{ON}[1]	All	K	75Ω typ, 100Ω max	175Ω max	-10V ≤ V_D ≤ +10V
R_{ON} vs V_D (V_S)	All	K	20% typ		I_{DS} = 1.0mA
R_{ON} Drift	All	K	+0.5%/°C typ		
R_{ON} Match	All	K	1% typ		V_D = 0, I_{DS} = 1.0mA
R_{ON} Drift Match	All	K	0.01%/°C typ		
I_D (I_S)OFF[1]	All	K	0.5nA typ, 5nA max	500nA max	V_D = -10V, V_S = +10V and V_D = +10V, V_S = -10V
I_D (I_S)ON[1]	All	K	10nA max		V_S = V_D = +10V V_S = V_D = -10V
I_{OUT}[1]	AD7512DI	K	15nA max	1500nA max	V_{S1} = V_{OUT} = ±10V, V_{S2} = ∓10V and V_{S2} = V_{OUT} = ±10V, V_{S1} = ∓10V
DIGITAL CONTROL					
V_{INL}[1]	All	K		0.8V max	
V_{INH}[1]	All			2.4V min	
C_{IN}	All	K	7pF typ		
I_{INH}[1]	All	K	10nA max		V_{IN} = V_{DD}
I_{INL}[1]	All	K	10nA max		V_{IN} = 0
DYNAMIC CHARACTERISTICS					
t_{ON}	AD7510DI	K	180ns typ		
	AD7511DI	K	350ns typ		
t_{OFF}	AD7510DI	K	350ns typ		V_{IN} = 0 to +3.0V
	AD7511DI	K	180ns typ		
$t_{TRANSITION}$	AD7512DI	K	300ns typ		
C_S (C_D)OFF	All	K	8pF typ		
C_S (C_D)ON	All	K	17pF typ		
C_{DS} (C_{S-OUT})	All	K	1pF typ		V_D (V_S) = 0V
C_{DD} (C_{SS})	All	K	0.5pF typ		
C_{OUT}	AD7512DI	K	17pF typ		
Q_{INJ}	All	K	30pC typ		Measured at S or D terminal. C_L = 1000pF, V_{IN} = 0 to 3V, V_D (V_S) = +10V to -10V
POWER SUPPLY					
I_{DD}[1]	All	K	800µA max	800µA max	All digital inputs = V_{INH}
I_{SS}[1]	All	K	800µA max	800µA max	
I_{DD}[1]	All	K	500µA max	500µA max	All digital inputs = V_{INL}
I_{SS}[1]	All	K	500µA max	500µA max	

NOTES
[1] 100% tested.
Specifications subject to change without notice.

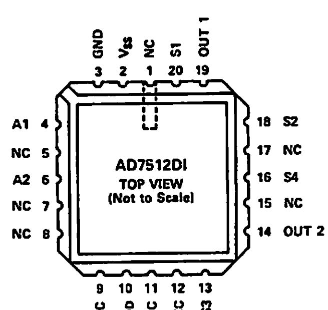
PIN CONFIGURATIONS

LCCC



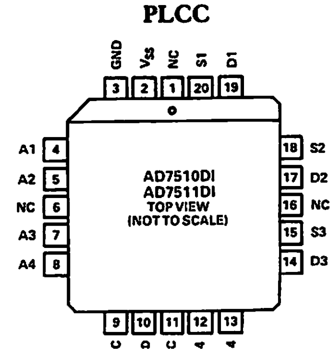
NC = NO CONNECT

LCCC



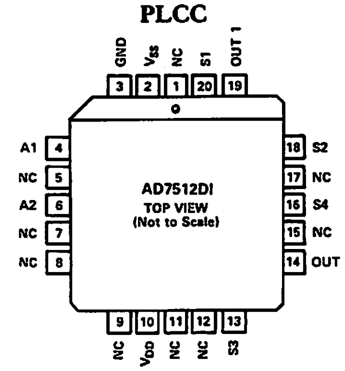
NC = NO CONNECT

PLCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

EXTENDED VERSIONS (S, T)

PARAMETER	MODEL	VERSION	+25°C	-55°C to +125°C	TEST CONDITIONS
ANALOG SWITCH					
R_{ON} [1]	All	S, T	100Ω max	175Ω max	$-10V \leq V_D \leq +10V$ $I_{DS} = 1mA$
I_D $(I_S)_{OFF}$ [1]	All	S, T	3nA max	200nA max	$V_D = -10V$, $V_S = +10V$ and $V_D = +10V$, $V_S = -10V$
I_D $(I_S)ON$ [1]	All	S, T	10		$V_S = V_D = +10V$ and $V_S = V_D = -10V$
I_{OUT} [1]	AD7512DI	S, T	9nA max	600nA max	$V_{S1} = V_{OUT} = \pm 10V$ $V_{S2} = \mp 10V$ and $V_{S2} = V_{OUT} = \pm 10V$ $V_{S1} = \mp 10V$
DIGITAL CONTROL					
V_{INL} [1]	All	S, T		0.8V max	
V_{INH} [1,2]	AD7510DI AD7511DI AD7512DI AD7511DI AD7512DI	S T T S S		2.4V min 2.4V min 2.4V min 3.0V min 3.0V min	
I_{INH} [1] I_{INL} [1]	All All	S, T S, T	10nA max 10nA max		$V_{IN} = V_{DD}$ $V_{IN} = 0$
DYNAMIC CHARACTERISTICS					
t_{ON} [3]	AD7510DI AD7511DI	S, S, T	1.0μs max 1.0μs max		$V_{IN} = 0$ to $+3V$
t_{OFF} [3]	AD7510DI AD7511DI	S, T S, T	1.0μs max 1.0μs max		
$t_{TRANSITION}$ [3]	AD7512DI	S, T	1.0μs max		
POWER SUPPLY					
I_{DD} [1] I_{SS} [1]	All All	S, T S, T		800μA max 800μA max	All digital inputs = V_{INH}
I_{DD} [1] I_{SS} [1]	All All	S, T S, T		500μA max 500μA max	All digital inputs = V_{INL}

NOTES
[1] 100% tested.
[2] A pullup resistor, typically 1-2kΩ is required to make AD7511DISQ and AD7512DISQ TTL compatible.
[3] Guaranteed, not production tested.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

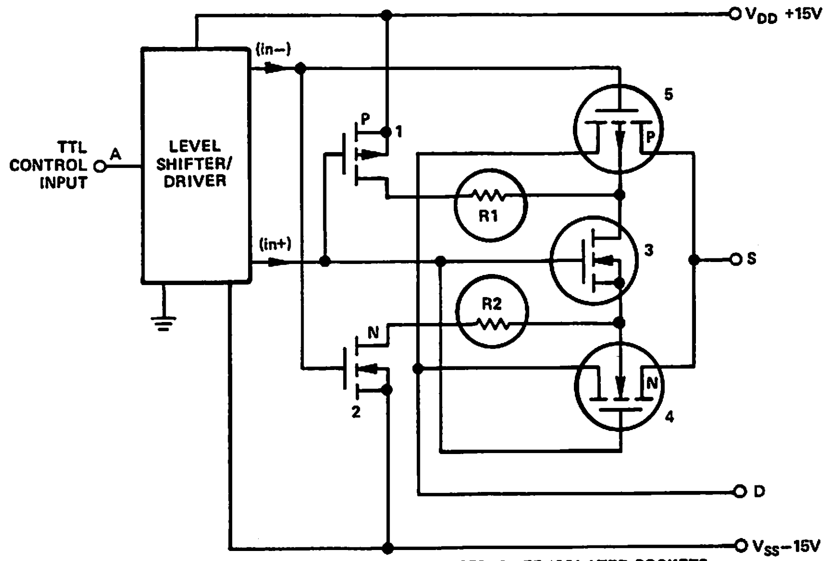
V_{DD} to GND . . . . +17V
V_{SS} to GND . . . . −17V
Overvoltage at V_D (V_S)
(1 second surge) . . . . V_{DD} +25V or V_{SS} −25V
(Continuous) . . . . V_{DD} +20V or V_{SS} −20V or 20mA, Whichever Occurs First
Switch Current (I_{DS}, Continuous) 50mA
Switch Current (I_{DS}, Surge)
1ms Duration, 10% Duty Cycle 150mA
Digital Input Voltage Range . . . . 0V to V_{DD} +0.3V
Power Dissipation (Any Package)
Up to +75°C 450mW
Derates above +75°C by . . . . 6mW/°C

Lead Temperature (Soldering, 10sec) . . . . +300°C
Storage Temperature . . . . −65°C to +150°C
Operating Temperature
Commercial (KN, KP Versions) . . . . 0 to +70°C
Industrial (KQ Versions) . . . . −25°C to +85°C
Extended (SQ, TQ, SE, TE Versions) . . −55°C to +125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



NOTE: CIRCLED DEVICES IN SEPARATE ISOLATED POCKETS.

Figure 1. Typical Output Switch Circuitry of AD7510DI Series

CIRCUIT DESCRIPTION

CMOS devices make excellent analog switches; however, problems with overvoltage and latch-up phenomenon necessitated protection circuitry. These protection circuits, however, either caused degradation of important switch parameters such as R_{ON} or leakage, or provided only limited protection in the event of overvoltage.

The AD7510DI series switches utilize a dielectrically isolated CMOS fabrication process to eliminate the four-layer substrate found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 2. The output switching element is comprised of device numbers 4 and 5. Operation is as follows: for an "ON" switch, (in+) is V_{DD} and (in−) is V_{SS} from the driver circuits. Device numbers 1 and 2 are "OFF" and number 3 in "ON". Hence, the backgates of the P- and N-channel output devices (numbers 4 and 5) are tied together and floating. The circled devices are located in separate dielectrically isolated pockets. Floating the output switch backgates with the signal input increases the effective threshold voltage for an applied analog signal, thus providing a flatter R_{ON} versus V_S response.

For an "OFF" switch, device number 3 is "OFF," and the backgates of devices 4 and 5 are tied through 1kΩ resistors (R1 and R2) to the respective supply voltages through the "ON" devices 1 and 2.

If a voltage is applied to the S or D (OUT) terminal which exceeds V_{DD} or V_{SS}, the S- or D-to-backgate diode is forward biased; however, R1 and R2 provide current limiting action to the supplies.

An equivalent circuit of the output switch element in Figure 3 shows that, indeed, the 1kΩ limiting resistors are in series with the backgates of the P- and N-channel output devices – *not* in series with the signal path between the S and D terminals.

It is possible to turn on an "OFF" switch by applying a voltage in excess of V_{DD} or V_{SS} to the S or D terminal. If a positive stress voltage is applied to the S or D terminal which exceeds V_{DD} by a threshold, then the P-channel (device 5) will turn on creating a low impedance path between the S and D terminals. A similar situation exists for negative stress voltages which exceed V_{SS}. In this case the N-channel provides the low impedance path between the S and D terminals. The limiting factor on the overvoltage protection is the power dissipation of the package and is ±20V continuous (or 20mA whichever occurs first) above the supply voltages.

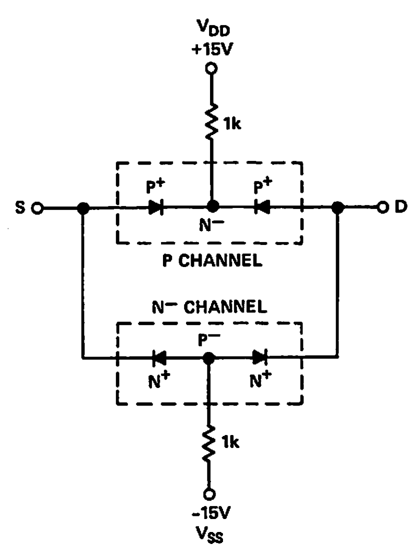
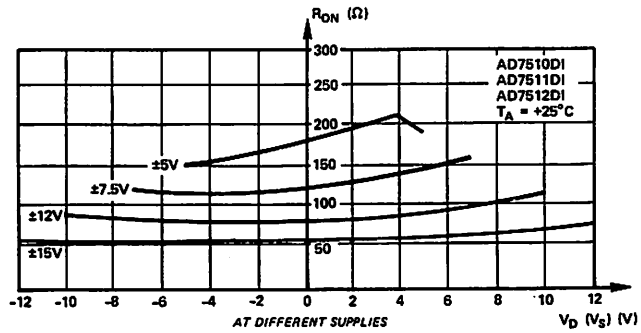
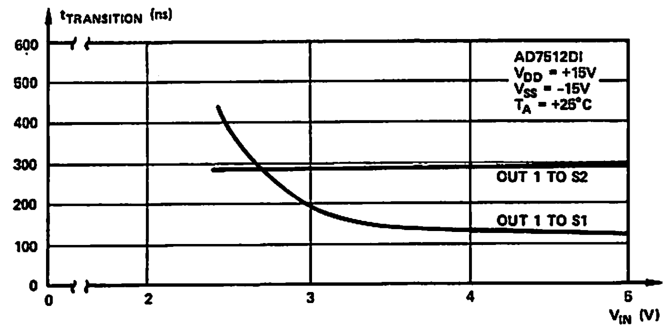


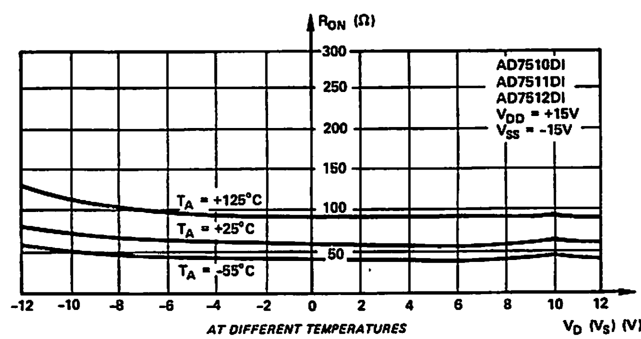
Figure 2. AD7510DI Series Output Switch Diode Equivalent Circuit



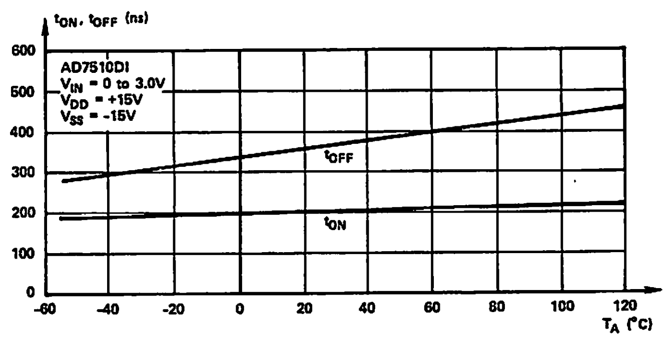
R_{ON} as a Function of V_D (V_S)



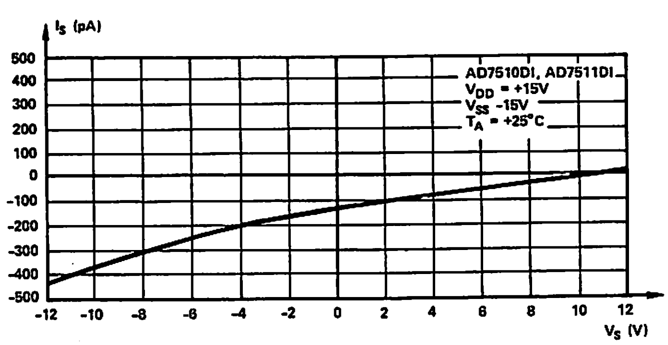
$t_{TRANSITION}$ as a Function of Digital Input Voltage



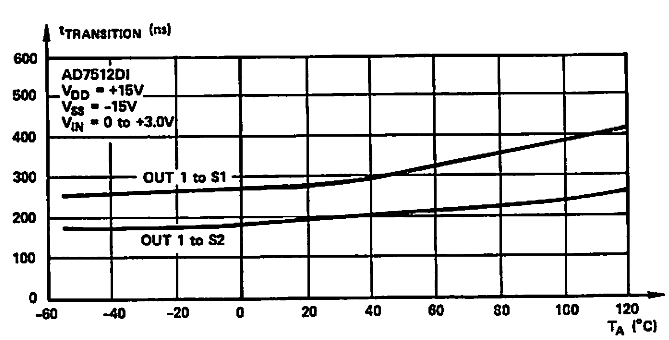
R_{ON} as a Function of V_D (V_S)



t_{ON}, t_{OFF} as a Function of Temperature

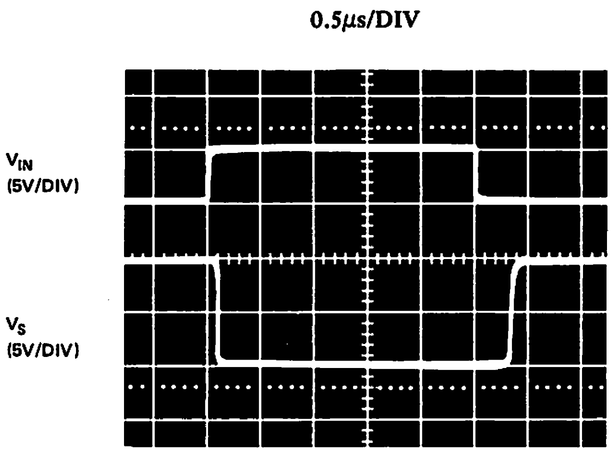


I_S, $(I_D)_{OFF}$ vs V_S

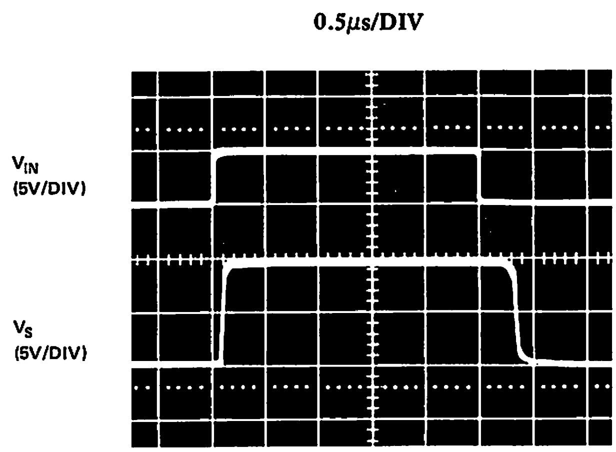


$t_{TRANSITION}$ as a Function of Temperature

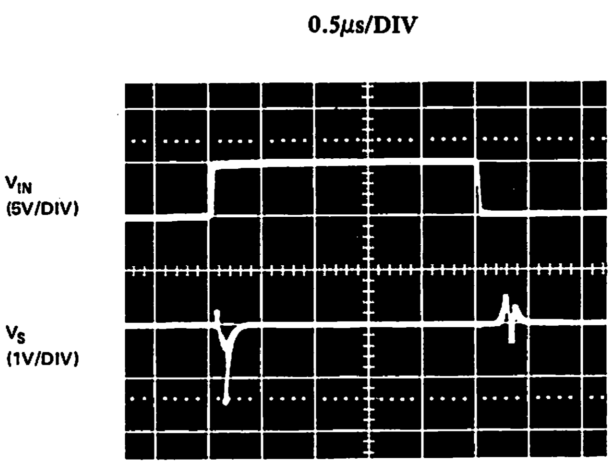
TYPICAL SWITCHING CHARACTERISTICS AD7510DI, AD7511DI



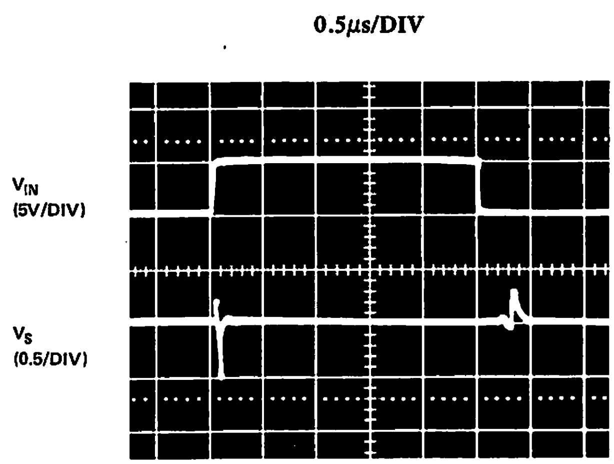
Switching Waveforms for V_D = −10V



Switching Waveforms for V_D = +10V

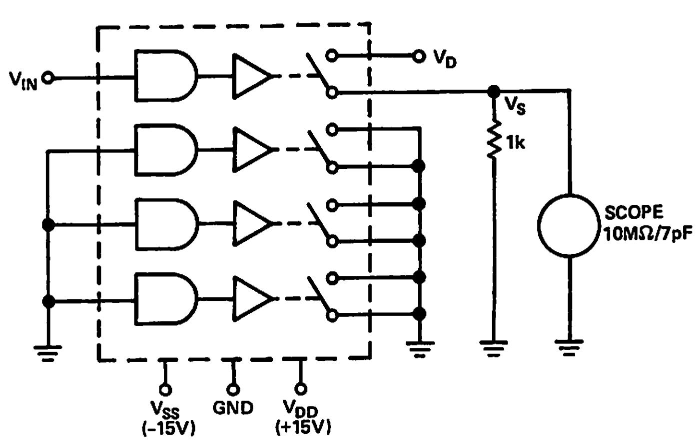


Switching Waveforms for V_D = Open



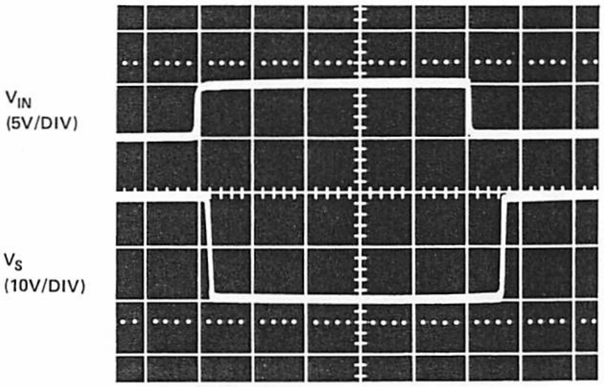
Switching Waveforms for V_D = 0V

AD7510DI, AD7511DI TEST CIRCUIT



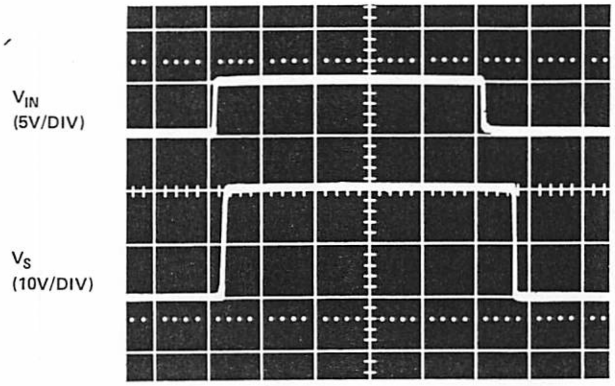
AD7512DI

0.5μs/DIV



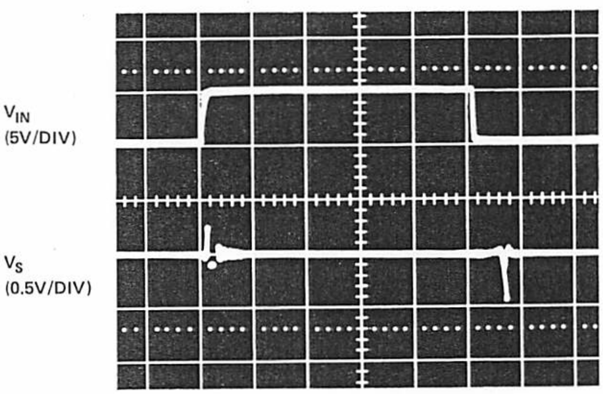
Switching Waveforms for
V_{S1} = -10V, V_{S2} = +10V, R_L = 1k

0.5μs/DIV



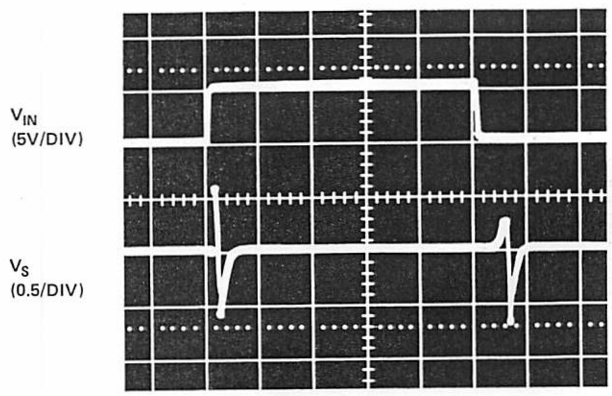
Switching Waveforms for
V_{S1} = +10V, V_{S2} = -10V, R_L = ∞

0.5μs/DIV



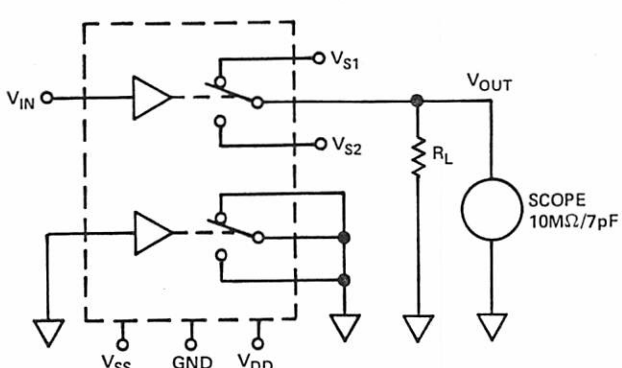
Switching Waveforms for
V_{S1} and V_{S2} = 0V, R_L = ∞

0.5μs/DIV



Switching Waveforms for
V_{S1} and V_{S2} = Open, R_L = 1k

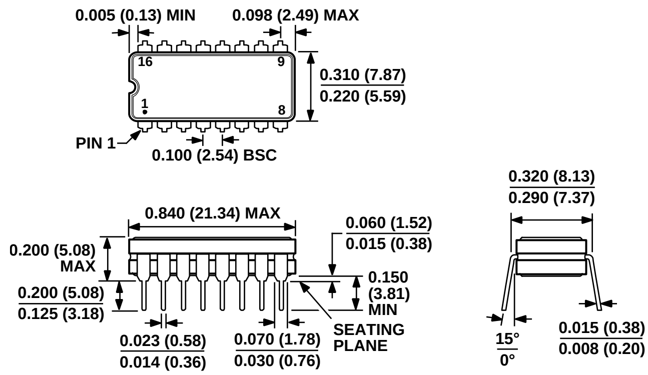
AD7512DI TEST CIRCUIT



TERMINOLOGY

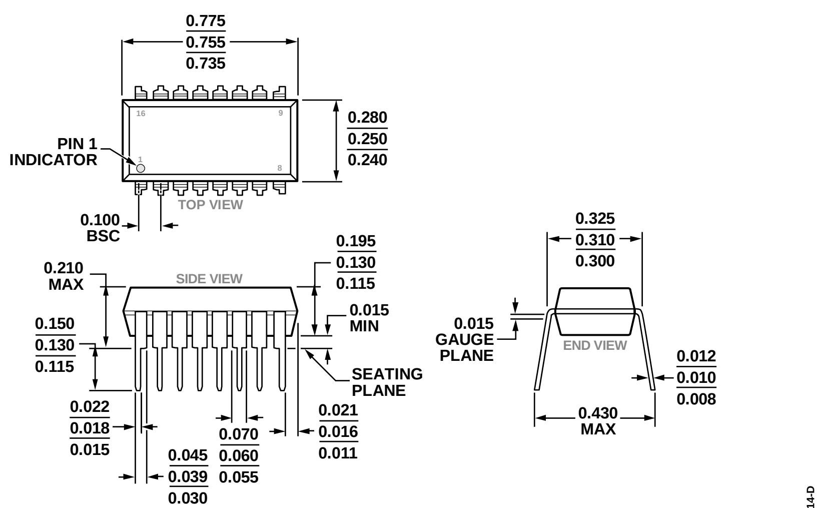
R_{ON}	Ohmic resistance between terminals D and S.
R_{ON} Drift Match	Difference between the R_{ON} drift of any two switches.
R_{ON} Match	Difference between the R_{ON} of any two switches.
$I_D (I_S)_{OFF}$	Current at terminals D or S. This is a leakage current when the switch is "OFF".
$I_D (I_S)_{ON}$	Leakage current that flows from the closed switch into the body. (This leakage will show up as the difference between the current I_D going into the switch and the outgoing current I_S.)
$V_D (V_S)$	Analog voltage on terminal D (S).
$C_S (C_D)$	Capacitance between terminal S (D) and ground. (This capacitance is specified for the switch open and closed.)
C_{DS}	Capacitance between terminals D and S. (This will determine the switch isolation over frequency.)
$C_{DD} (C_{SS})$	Capacitance between terminals D (S) of any two switches. (This will determine the cross coupling between switches vs. frequency.)
t_{ON}	Delay time between the 50% points of the digital input and switch "ON" condition.
t_{OFF}	Delay time between the 50% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time when switching from one address state to another.
V_{INL}	Maximum input voltage for a logic low.
V_{INH}	Minimum input voltage for a logic high.
$I_{INL} (I_{INH})$	Input current of the digital input.
C_{IN}	Input capacitance to ground of the digital input.
V_{DD}	Most positive voltage supply.
V_{SS}	Most negative voltage supply.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

OUTLINE DIMENSIONS



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 3. 16-Lead Ceramic Dual In-Line Package [CERDIP]
(Q-16)
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MS-001-BB

Figure 4. 16-Lead Plastic Dual In-Line Package [PDIP]
Narrow Body
(N-16)
Dimensions shown in inches

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD7511DIJN	0°C to 70°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD7511DIJNZ	0°C to 70°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD7511DIKNZ	0°C to 70°C	16-Lead Plastic Dual In-Line Package [PDIP]	N-16
AD7511DIKQ	−25°C to +85°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16
AD7511DISQ/883B	−55°C to +125°C	16-Lead Ceramic Dual In-Line Package [CERDIP]	Q-16

[1] Z = RoHS Compliant Part.
[2] AD7511DISQ/883B is a MIL-STD-883, Class B, processed part.

REVISION HISTORY

12/2016—Rev. A to Rev. B

Added AD7510 and AD7512 Obsolete Note 1
Updated Outline Dimensions 9
Changes to Ordering Guide.. 9

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