maxim integrated™

MAX8934G

Dual-Input Linear Charger, Smart Power Selector with Advanced Battery Temperature Monitoring

General Description

The MAX8934G dual-input Li+/Li-Poly linear battery charger with Smart Power Selector™ safely charges a single Li+/Li-Poly cell in accordance with JEITA* recommendations. The MAX8934G monitors the battery temperature (T_{BATT}) while charging, and automatically adjusts the fast-charge current and charge termination voltage as the battery temperature varies. The MAX8934G also monitors the battery temperature while the battery is discharging, and provides a warning flag ($\overline{OT}$) to the system in the event that the battery is over temperature. Safety region 2 is supported (see Figure 6 for details). An ultra-low I_Q, always-on LDO provides an additional 3.3V supply for system power.

The MAX8934G operates with either separate inputs for USB and AC adapter power, or from a single input that accepts both. All power switches for charging and switching the load between battery and external power are included on-chip. No external MOSFETs are required.

The MAX8934G features a Smart Power Selector to make the best use of limited USB or adapter power. Input current limit and battery charge current limit are independently set. Input power not used by the system charges the battery. Charge current limit and DC current limit can be set up to 1.5A and 2A, respectively, while USB input current can be set to 100mA or 500mA. Automatic input selection switches the system load from battery to external power.

The MAX8934G provides a SYS output voltage of 4.35V.

Other features include overvoltage protection (OVP), open-drain charge status and fault outputs, power-OK monitors, charge timers, and a battery thermistor monitor. Additionally, on-chip thermal limiting reduces the battery charge-rate to prevent charger overheating. The MAX8934G is available in a 28-pin, 4mm x 4mm, TQFN package.

Applications

PDAs, Palmtop, and Wireless Handhelds
Portable Media, MP3 Players, and PNDs
Digital Still Cameras and Digital Video Cameras
Handheld Game Systems

**JEITA (Japan Electronics and Information Technology Industries Association) Standard, A Guide to the Safe Use of Secondary Lithium Ion Batteries on Notebook–Type Personal Computers, April 20, 2007.*

Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

Features

- **Li+ Charger with Smart Power Selector, No External MOSFETs Needed**
- **Monitors Battery Temperature and Adjusts Charge Current and Termination Voltage Automatically per JEITA Recommendations**
- **$\overline{OT}$ Flags System of a Hot Battery During Discharge**
- **Ultra-Low I_Q, Always-On 3.3V LDO**
- **Common or Separate USB and Adapter Inputs**
- **Automatic Adapter/USB/Battery Switchover**
- **Load Peaks in Excess of Adapter Rating are Supported by Battery**
- **Input OVP to 16V (DC) and 9V (USB)**
- **40mΩ SYS-to-BATT Switch**
- **Thermal Regulation Prevents Overheating**
- **4.35V SYS Regulation Voltage**

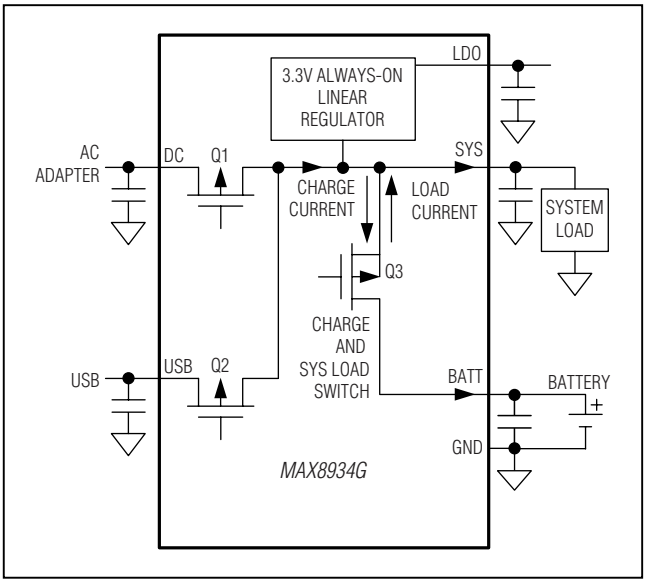
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8934GETI+	-40°C to +85°C	28 Thin QFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.

***EP = Exposed pad.*

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5296; Rev 0; 6/10

ABSOLUTE MAXIMUM RATINGS

DC, PEN1 to GND ..... -0.3V to +16V
USB to GND ..... -0.3V to +9V
V_L to GND ..... -0.3V to +4V
LDO to GND ..... -0.3V to the lower of +4V and (V_{SYS} + 0.3V)
THMEN, THMSW to GND ..... -0.3V to +(V_{LDO} + 0.3V)
THM to GND ..... -0.3V to (V_{THMSW} + 0.3V)
PSET, ISET, CT to GND ..... -0.3V to (V_L + 0.3V)
BATT, SYS, $\overline{CEN}$, $\overline{CHG}$, $\overline{OT}$, $\overline{DOK}$, $\overline{UOK}$, $\overline{FLT}$, $\overline{DONE}$, USUS, PEN2 to GND ..... -0.3V to +6V
EP (Exposed Pad) to GND ..... -0.3V to +0.3V
DC Continuous Current (total in two pins) ..... $2.4A_{RMS}$
SYS Continuous Current (total in two pins) ..... $2.4A_{RMS}$
USB Continuous Current (total in two pins) ..... $2.0A_{RMS}$
BATT Continuous Current (total in two pins) ..... $2.4A_{RMS}$
LDO Continuous Current ..... $50mA_{RMS}$
LDO Short-Circuit Duration ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Single-Layer Board
(derate 20.8mW/°C above +70°C) 1666.7mW
Multilayer Board
(derate 28.6mW/°C above +70°C) 2285.7mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... -40°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DC} = V_{PEN1} = V_{PEN2} = 5V, $\overline{CEN}$ = USUS = THMEN = GND, V_{BATT} = 4V, V_{THM} = 1.65V, USB, THMSW, $\overline{CHG}$, $\overline{DONE}$, $\overline{OT}$, $\overline{DOK}$, $\overline{UOK}$, $\overline{FLT}$ are unconnected, C_{CT} = 0.068µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC-to-SYS PREREGULATOR						
DC Operating Voltage Range			4.1		6.6	V
DC Withstand Voltage	V_{BATT} = V_{SYS} = 0V				14	V
DC Undervoltage Threshold	When $V_{\overline{DOK}}$ goes low, V_{DC} rising, 500mV hysteresis		3.95	4.0	4.05	V
DC Overvoltage Threshold	When $V_{\overline{DOK}}$ goes high, V_{DC} rising, 360mV hysteresis		6.8	6.9	7.0	V
DC Operating Supply Current	I_{SYS} = I_{BATT} = 0mA, $V_{\overline{CEN}}$ = 0V			1	2	mA
	I_{SYS} = I_{BATT} = 0mA, $V_{\overline{CEN}}$ = 5V			0.8	1.5	
DC Suspend Current	V_{DC} = $V_{\overline{CEN}}$ = V_{USUS} = 5V, V_{PEN1} = 0V			195	340	µA
DC-to-SYS On-Resistance	I_{SYS} = 400mA, $V_{\overline{CEN}}$ = 5V			0.2	0.35	Ω
DC to BATT Dropout Voltage	When SYS regulation and charging stops, V_{DC} falling, 150mV hysteresis		10	50	90	mV
DC Current Limit	V_{DC} = 5V, V_{SYS} = 4V, T_A = +25°C	R_{PSET} = 1.5kΩ	1800	2000	2200	mA
		R_{PSET} = 3kΩ	900	1000	1100	
		R_{PSET} = 6.3kΩ	450	475	500	
		V_{PEN1} = 0V, V_{PEN2} = 5V (500mA USB mode)	450	475	500	
		V_{PEN1} = V_{PEN2} = 0V (100mA USB mode)	80	95	100	
PSET Resistance Range			1.5		6.3	kΩ
SYS Regulation Voltage	V_{DC} = 6V, I_{SYS} = 1mA to 1.75A, $V_{\overline{CEN}}$ = 5V		4.29	4.35	4.4	V
Input Current Soft-Start Time	Connecting DC with USB not present			1.5		ms
	Connecting DC with USB present			50		µs
Thermal-Limit Temperature	Die temperature at when the charging current and input current limits are reduced			100		°C
Thermal-Limit Gain	I_{SYS} reduction with die temperature (above +100°C)			5		%/C
V_L Voltage	I_{VL} = 0 to 5mA, USB = unconnected		3	3.3	3.6	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DC} = V_{PEN1} = V_{PEN2} = 5V, $\overline{CEN}$ = USUS = THMEN = GND, V_{BATT} = 4V, V_{THM} = 1.65V, USB, THMSW, $\overline{CHG}$, $\overline{DONE}$, $\overline{OT}$, $\overline{DOK}$, $\overline{UOK}$, $\overline{FLT}$ are unconnected, C_{CT} = 0.068µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
USB-TO-SYS PREREGULATOR						
USB Operating Voltage Range			4.1		6.6	V
USB Withstand Voltage	V_{BATT} = V_{SYS} = 0V				8	V
USB Undervoltage Threshold	When $V_{\overline{UOK}}$ goes low, V_{USB} rising, 500mV hysteresis		3.95	4.0	4.05	V
USB Overvoltage Threshold	When $V_{\overline{UOK}}$ goes high, V_{USB} rising, 360mV hysteresis		6.8	6.9	7.0	V
USB Operating Supply Current	I_{SYS} = I_{BATT} = 0mA, $V_{\overline{CEN}}$ = V_{PEN2} = 0V			1	2	mA
	I_{SYS} = I_{BATT} = 0mA, $V_{\overline{CEN}}$ = 5V, V_{PEN2} = 0V			0.9	1.5	
USB Suspend Current	DC = unconnected, V_{USB} = $V_{\overline{CEN}}$ = V_{USUS} = 5V			190	340	µA
USB to SYS On-Resistance	DC unconnected, V_{USB} = $V_{\overline{CEN}}$ = 5V, I_{SYS} = 400mA			0.22	0.33	Ω
USB-to-BATT Dropout Voltage	When SYS regulation and charging stops, V_{USB} falling, 150mV hysteresis		10	50	90	mV
USB Current Limit (See Table 2)	DC unconnected, V_{USB} = 5V, T_A = +25°C	V_{PEN1} = 0V, V_{PEN2} = 5V	450	475	500	mA
		V_{PEN1} = V_{PEN2} = 0V	80	95	100	
SYS Regulation Voltage	DC unconnected, V_{USB} = 6V, V_{PEN2} = 5V, I_{SYS} = 1mA to 400mA, $V_{\overline{CEN}}$ = 5V		4.29	4.35	4.4	V
Input Limiter Soft-Start Time	Input current ramp time			50		µs
Thermal-Limit Temperature	Die temperature at when the charging current and input current limits are reduced			100		°C
Thermal-Limit Gain	I_{SYS} reduction with die temperature (above +100°C)			5		%/°C
V_L Voltage	DC unconnected, V_{USB} = 5V, I_{VL} = 0 to 5mA		3	3.3	3.6	V
LDO LINEAR REGULATOR						
LDO Output Voltage	DC unconnected, V_{USB} = 5V, I_{LDO} = 0mA		3.234	3.3	3.366	V
	V_{DC} = 5V, USB unconnected, I_{LDO} = 0mA		3.234	3.3	3.366	
	DC and USB unconnected, V_{BATT} = 4V, I_{LDO} = 0mA		3.234	3.3	3.366	
LDO Load Regulation	I_{LDO} = 0 to 30mA			0.003		%/mA
BATTERY CHARGER						
BATT-to-SYS On-Resistance	V_{DC} = 0V, V_{BATT} = 4.2V, I_{SYS} = 1A			0.04	0.08	Ω
BATT-to-SYS Reverse Regulation Voltage	V_{PEN1} = V_{PEN2} = 0V, I_{SYS} = 200mA		50	75	105	mV
BATT Regulation Voltage—Safety Region 2	I_{BATT} = 0mA	T_A = +25°C, V_{THM_T2} < V_{THM} < V_{THM_T3}	4.175	4.2	4.225	V
		T_A = 0°C to +85°C, V_{THM_T2} < V_{THM} < V_{THM_T3}	4.158	4.2	4.242	
		T_A = +25°C, V_{THM_T1} < V_{THM} < V_{THM_T2} or V_{THM_T3} < V_{THM} < V_{THM_T4}	4.05	4.075	4.1	
		T_A = 0°C to +85°C, V_{THM_T1} < V_{THM} < V_{THM_T2} or V_{THM_T3} < V_{THM} < V_{THM_T4}	4.034	4.075	4.1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DC} = V_{PEN1} = V_{PEN2} = 5V, $\overline{CEN}$ = USUS = THMEN = GND, V_{BATT} = 4V, V_{THM} = 1.65V, USB, THMSW, $\overline{CHG}$, $\overline{DONE}$, $\overline{OT}$, $\overline{DOK}$, $\overline{UOK}$, $\overline{FLT}$ are unconnected, C_{CT} = 0.068µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BATT Recharge Threshold—Safety Region 2	Change in V_{BATT} from DONE to fast-charge restart	$V_{THM_T2} < V_{THM} < V_{THM_T3}$	-145	-104	-65	mV
		$V_{THM_T1} < V_{THM} < V_{THM_T2}$ or $V_{THM_T3} < V_{THM} < V_{THM_T4}$	-120	-80	-40	
BATT Fast-Charge Current Range	R_{ISET} = 10kΩ to 2kΩ		0.3		1.5	A
BATT Charge Current Accuracy	V_{SYS} = 5.5V, $V_{THM_T1} < V_{THM} < V_{THM_T4}$ (safety region 2)	R_{ISET} = 2kΩ	1350	1500	1650	mA
		R_{ISET} = 4kΩ	675	750	825	
		R_{ISET} = 10kΩ	270	300	330	
		R_{ISET} = 2kΩ, V_{BATT} = 2.5V (prequal)	270	300	330	
		R_{ISET} = 4kΩ, V_{BATT} = 2.5V (prequal)	130	150	170	
		R_{ISET} = 10kΩ, V_{BATT} = 2.5V (prequal)		60		
ISET Output Voltage	R_{ISET} = 4kΩ, I_{BATT} = 500mA (V_{ISET} = 1.5V at full charge current) $V_{THM_T1} < V_{THM} < V_{THM_T4}$		0.9	1	1.1	V
Charger Soft-Start Time	Charge-current ramp time			1.5		ms
BATT Prequal Threshold	V_{BATT} rising, 180mV hysteresis		2.9	3	3.1	V
BATT Input Current	V_{BATT} = 4.2V, I_{LDO} = 0	No DC or USB power connected, THMEN = low, $V_{\overline{CEN}}$ = 5V		5	12	µA
		No DC or USB power connected, THMEN = high, $V_{\overline{CEN}}$ = 5V		12	25	
		DC or USB power connected, $V_{\overline{CEN}}$ = 5V		0.003	2	
DONE Threshold as a Percentage of Fast-Charge Current	I_{BATT} decreasing			20		%
Maximum Prequal Time	From $\overline{CEN}$ falling to end of prequal charge, V_{BATT} = 2.5V			180		min
Maximum Fast-Charge Time	From $\overline{CEN}$ falling to $\overline{FLT}$ falling			300		min
Maximum Top-Off Time				15		s
Timer Accuracy			-20		+20	%
Timer Extend Threshold	Percentage of fast-charge current below where the timer clock operates at half-speed			50		%
Timer Suspend Threshold	Percentage of fast-charge current below where timer clock pauses			20		%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DC} = V_{PEN1} = V_{PEN2} = 5V, $\overline{CEN}$ = USUS = THMEN = GND, V_{BATT} = 4V, V_{THM} = 1.65V, USB, THMSW, $\overline{CHG}$, $\overline{DONE}$, $\overline{OT}$, $\overline{DOK}$, $\overline{UOK}$, $\overline{FLT}$ are unconnected, C_{CT} = 0.068µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
THERMISTOR MONITOR (Beta = 3964) (Note 2)						
THM Cold No-Charge Threshold (T1)	I_{CHG} = 0A, when charging is suspended, 2°C hysteresis		-2.1	0	+2.4	°C
			76.4	77.2	77.9	% of THMSW
THM Cold Threshold (T2)	V_{BATT_REG}, reduced, 2°C hysteresis		8.2	10	12	°C
			66.2	67	67.6	% of THMSW
THM Hot Threshold (T3)	V_{BATT_REG} reduced, 2.5°C hysteresis		42.8	45	47.5	°C
			29.8	30	30.6	% of THMSW
THM Hot No-Charge Threshold (T4)	I_{CHG} = 0mA, when charging is suspended, 3°C hysteresis		57	60	63.5	°C
			19.5	19.8	20.1	% of THMSW
THM Hot Discharge Threshold ($T_{\overline{OT}}$)	$\overline{OT}$ asserts low, 5°C hysteresis		71	75	80	°C
			12.6	12.9	13.1	% of THMSW
THM Input leakage	THM = GND or LDO	T_A = +25°C	-1	+0.001	+1	µA
		T_A = +85°C		0.01		
THMSW Output Leakage	THMSW = GND	T_A = +25°C	-0.2	+0.001	+1	µA
		T_A = +85°C		0.01		
THMSW Output Voltage High	Sourcing 1mA		V_{LDO} - 0.05			V
LOGIC I/O: PEN1, PEN2, $\overline{CHG}$, $\overline{FLT}$, $\overline{DONE}$, $\overline{DOK}$, $\overline{UOK}$, USUS, THMEN)						
Logic-Input Thresholds	High level		1.3			V
	Low level				0.4	
	Hysteresis			50		mV
Logic-Input Leakage Current	V_{IN} = 0 to 5.5V	T_A = +25°C		0.001	1	µA
		T_A = +85°C		0.01		
Logic-Low Output Voltage	Sinking 1mA			25	100	mV
Logic-High Output Leakage Current	V_{OUT} = 5.5V	T_A = +25°C		0.001	1	µA
		T_A = +85°C		0.01		

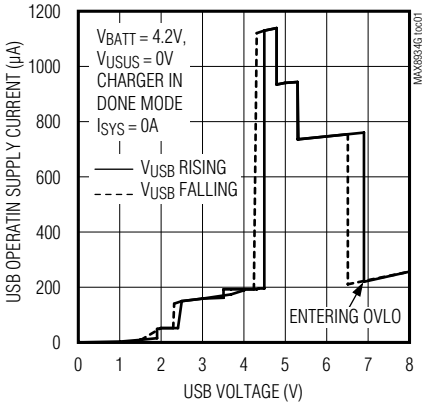
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: °C includes external NTC thermistor error. % of THMSW excludes thermistor beta error and external pullup error. NTC thermistor assumed to be 100kΩ ±1% nominal, part number Vishay NTHS0603N01N1003FF, external pullup resistor = 100kΩ ±1%.

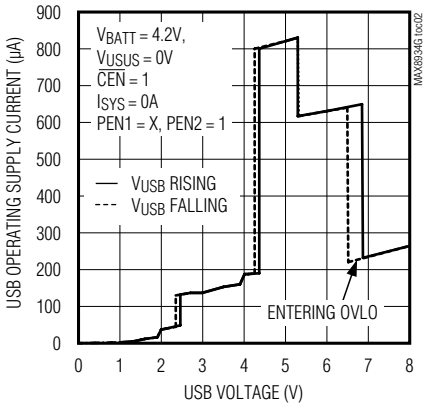
Typical Operating Characteristics

(T_A = +25°C, circuit of Figure 2, V_{DC} = 6V, V_{BATT} = 3.6V, thermistor Beta = 3964, unless otherwise noted. Negative battery current indicates charging.)

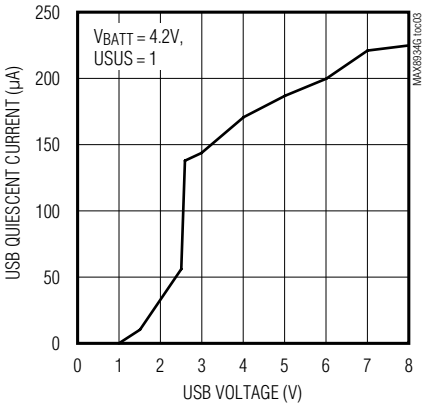
USB OPERATING SUPPLY CURRENT vs. USB VOLTAGE (CHARGER ENABLED)



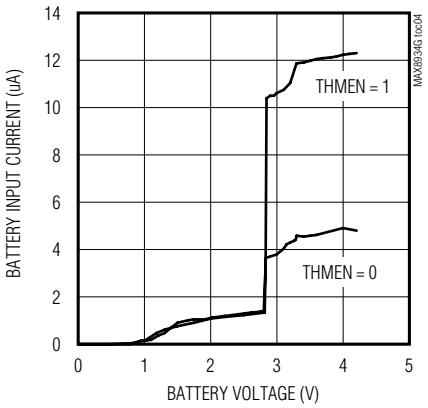
USB OPERATING SUPPLY CURRENT vs. USB VOLTAGE (CHARGER DISABLED)



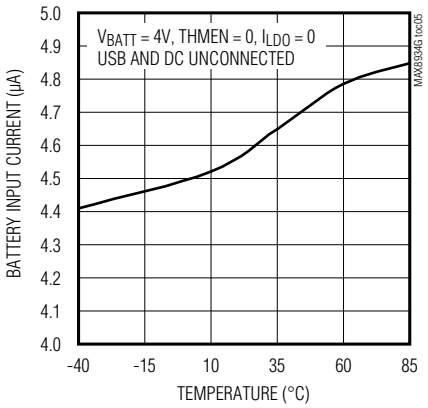
USB SUSPEND CURRENT vs. USB VOLTAGE



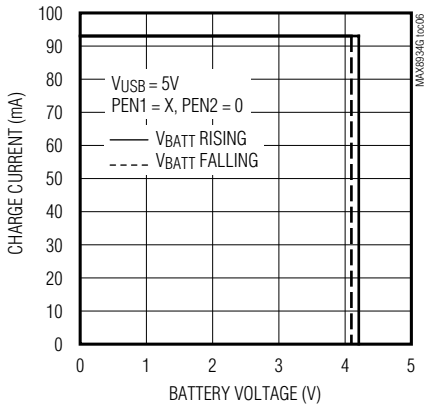
BATTERY INPUT CURRENT vs. BATTERY VOLTAGE (USB DISCONNECTED)



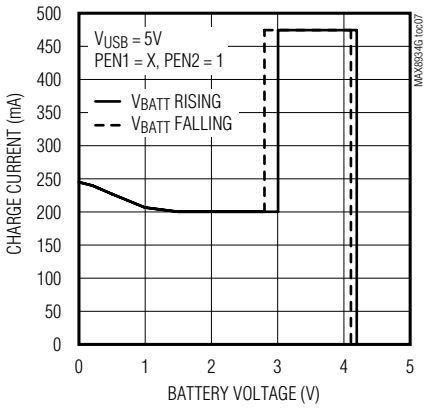
BATTERY INPUT CURRENT vs. TEMPERATURE



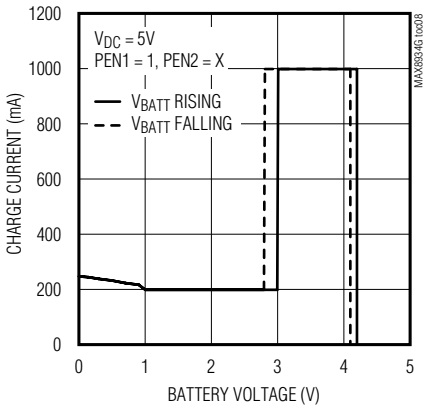
CHARGE CURRENT vs. BATTERY VOLTAGE (100mA USB)



CHARGE CURRENT vs. BATTERY VOLTAGE (500mA USB)



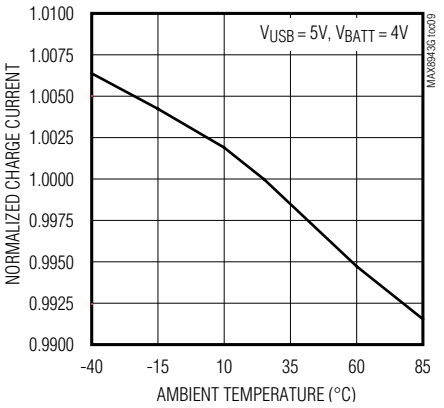
CHARGE CURRENT vs. BATTERY VOLTAGE (1A DC)



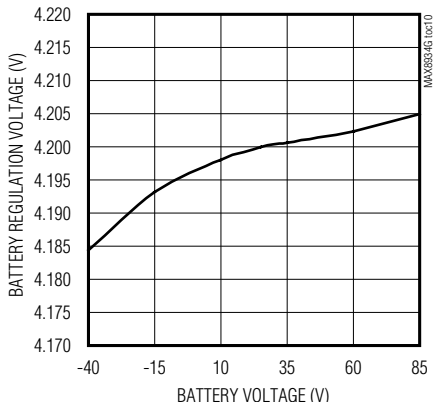
Typical Operating Characteristics (continued)

(T_A = +25°C, circuit of Figure 2, V_{DC} = 6V, V_{BATT} = 3.6V, thermistor Beta = 3964, unless otherwise noted. Negative battery current indicates charging.)

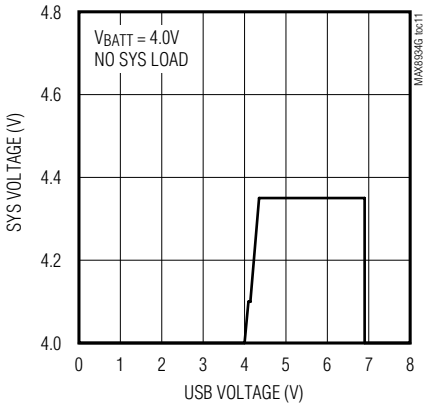
NORMALIZED CHARGE CURRENT vs. AMBIENT TEMPERATURE (LOW IC POWER DISSIPATION)



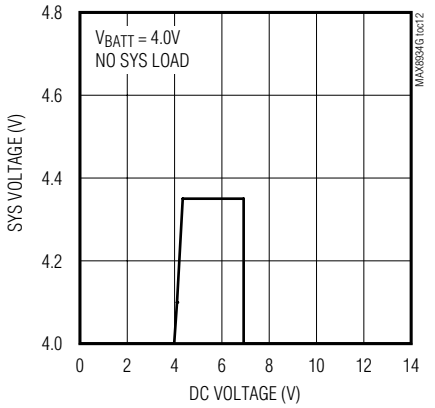
BATTERY REGULATION VOLTAGE vs. TEMPERATURE



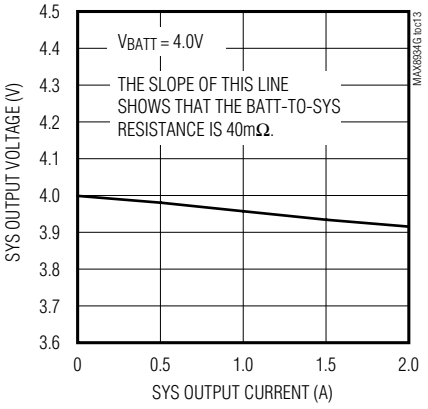
SYS OUTPUT VOLTAGE vs. USB VOLTAGE



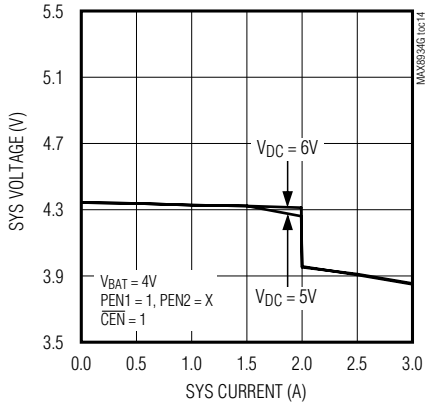
SYS OUTPUT VOLTAGE vs. DC VOLTAGE



SYS OUTPUT VOLTAGE vs. SYS OUTPUT CURRENT (USB AND DC DISCONNECTED)



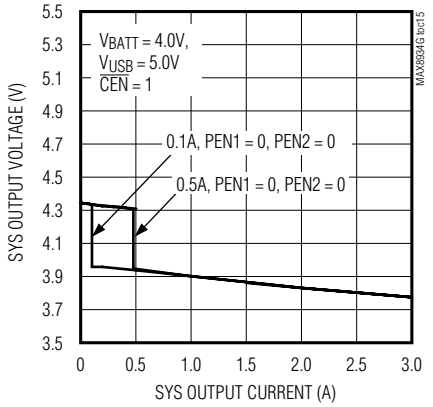
SYS OUTPUT VOLTAGE vs. SYS OUTPUT CURRENT (DC)



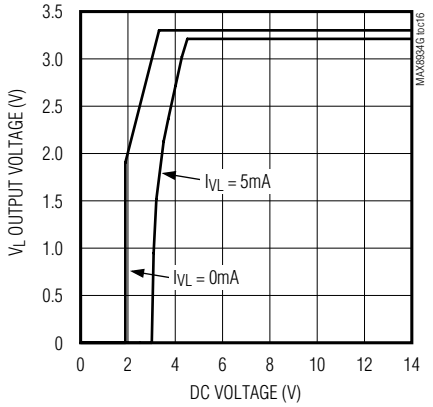
Typical Operating Characteristics (continued)

(T_A = +25°C, circuit of Figure 2, V_{DC} = 6V, V_{BATT} = 3.6V, thermistor Beta = 3964, unless otherwise noted. Negative battery current indicates charging.)

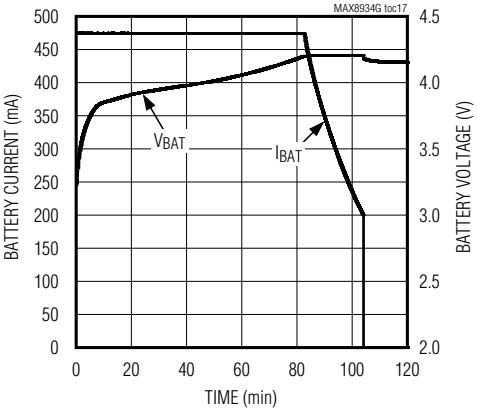
SYS OUTPUT VOLTAGE vs. SYS OUTPUT CURRENT (USB)



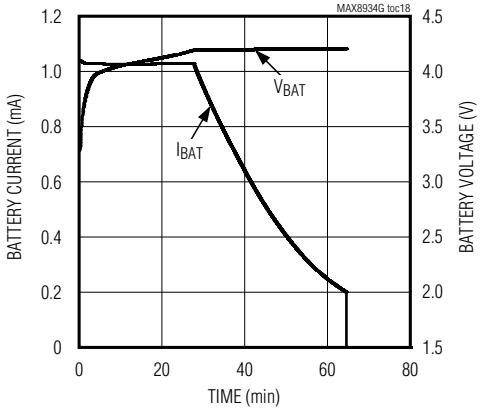
VL OUTPUT VOLTAGE vs. DC VOLTAGE



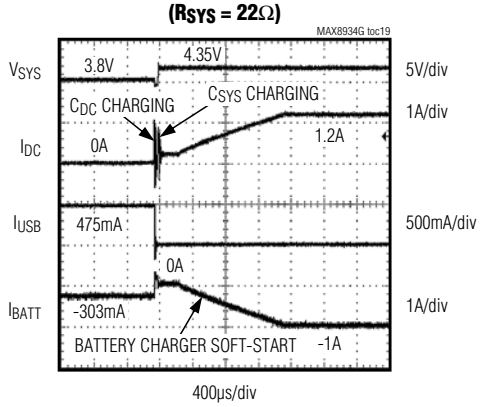
CHARGE PROFILE—820mAh BATTERY USB INPUT—500mA CHARGE



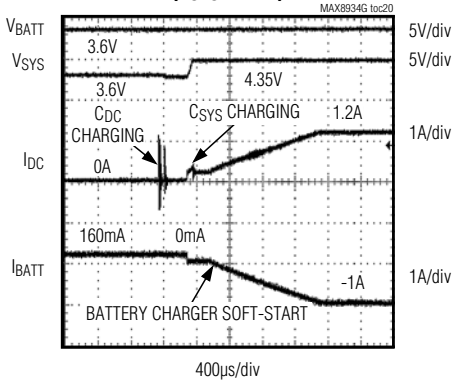
CHARGE PROFILE—820mAh BATTERY ADAPTER INPUT—1A CHARGE



DC CONNECT WITH USB CONNECTED (R_{SYS} = 22Ω)



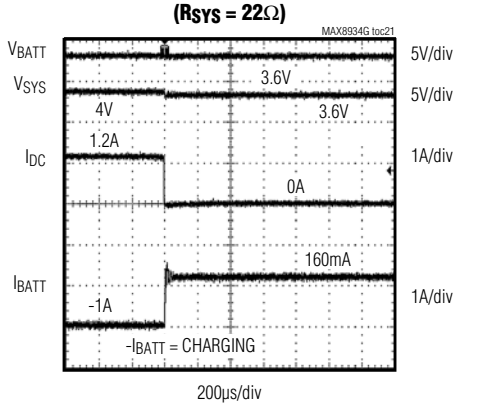
DC CONNECT WITH NO USB (R_{SYS} = 22Ω)



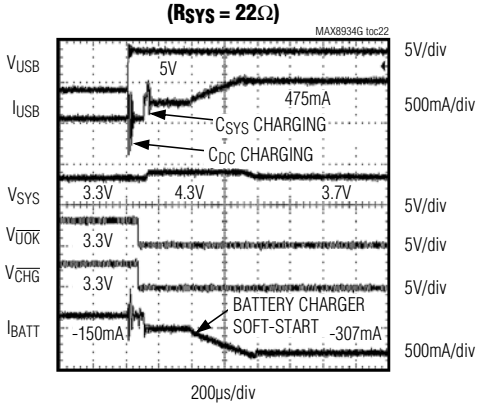
Typical Operating Characteristics (continued)

(T_A = +25°C, circuit of Figure 2, V_{DC} = 6V, V_{BATT} = 3.6V, thermistor Beta = 3964, unless otherwise noted. Negative battery current indicates charging.)

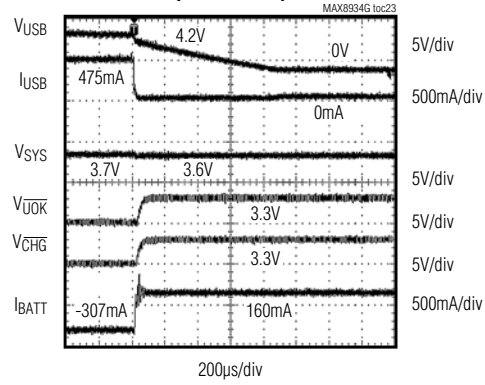
DC DISCONNECT WITH NO USB (R_{SYS} = 22Ω)



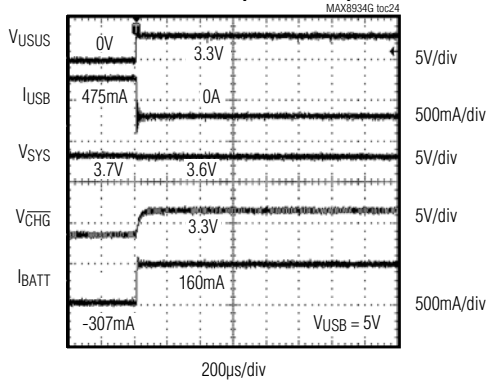
USB CONNECT WITH NO DC (R_{SYS} = 22Ω)



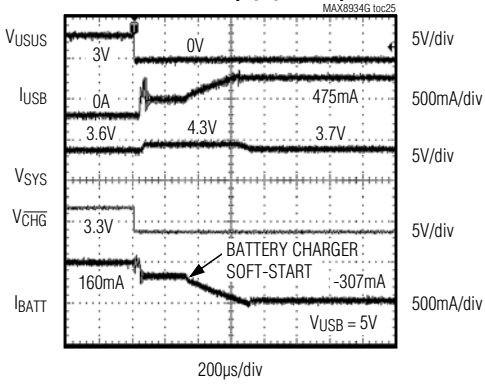
USB DISCONNECT WITH NO DC (R_{SYS} = 22Ω)



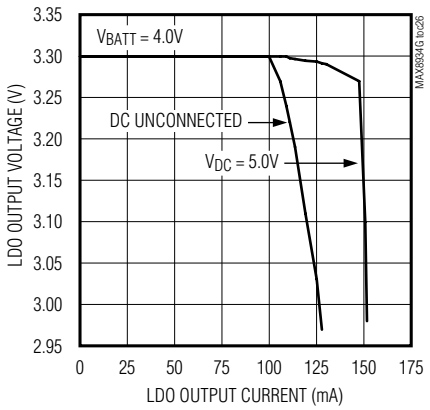
USB SUSPEND (R_{SYS} = 22Ω)



USB RESUME (R_{SYS} = 22Ω)



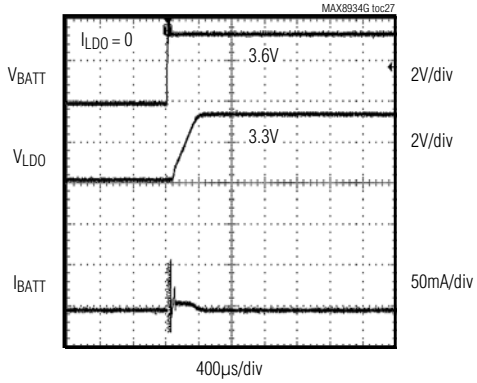
LDO OUTPUT VOLTAGE vs. LDO OUTPUT CURRENT (USB DISCONNECTED)



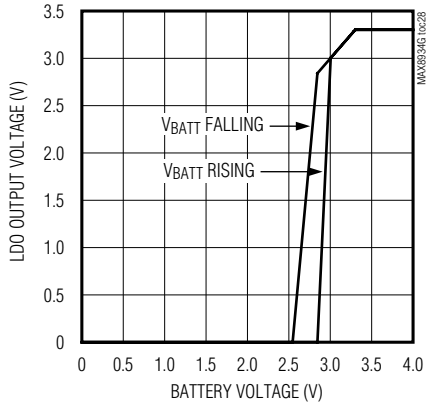
Typical Operating Characteristics (continued)

(T_A = +25°C, circuit of Figure 2, V_{DC} = 6V, V_{BATT} = 3.6V, thermistor Beta = 3964, unless otherwise noted. Negative battery current indicates charging.)

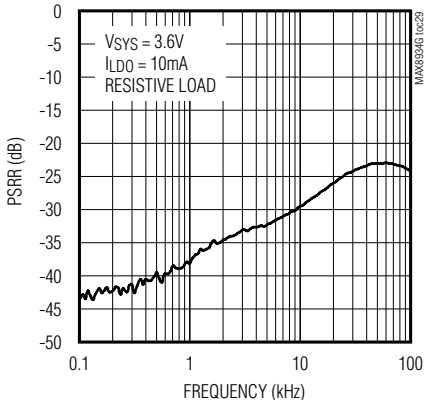
LDO STARTUP WAVEFORMS



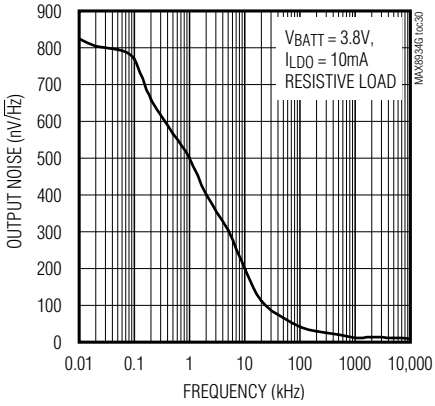
LDO OUTPUT VOLTAGE vs. BATTERY VOLTAGE



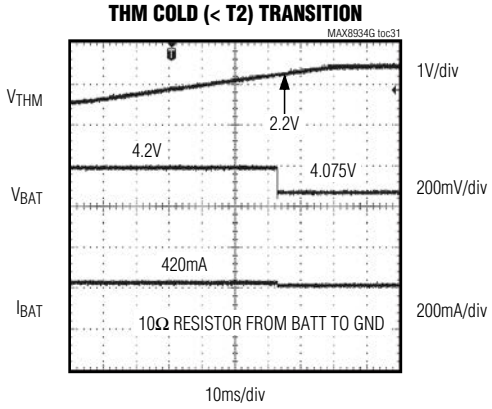
ALWAYS-ON LDO POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



LDO NOISE DENSITY vs. FREQUENCY



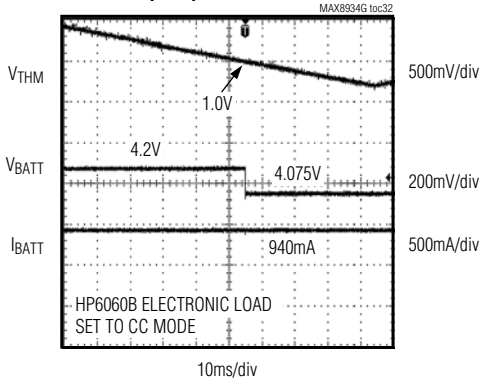
THM NORMAL TO THM COLD (< T2) TRANSITION



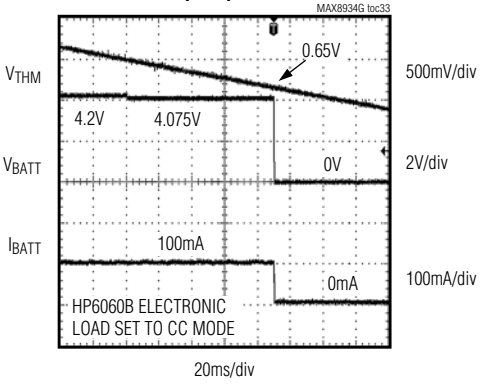
Typical Operating Characteristics (continued)

(T_A = +25°C, circuit of Figure 2, V_{DC} = 6V, V_{BATT} = 3.6V, thermistor Beta = 3964, unless otherwise noted. Negative battery current indicates charging.)

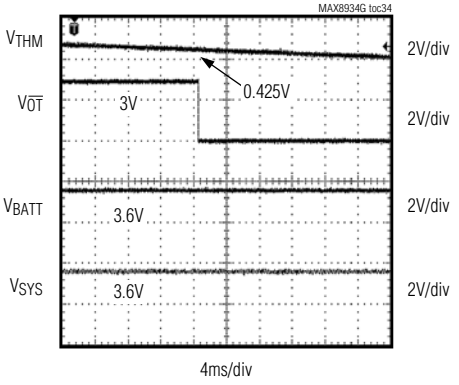
THM NORMAL TO THM HOT (> T3) TRANSITION



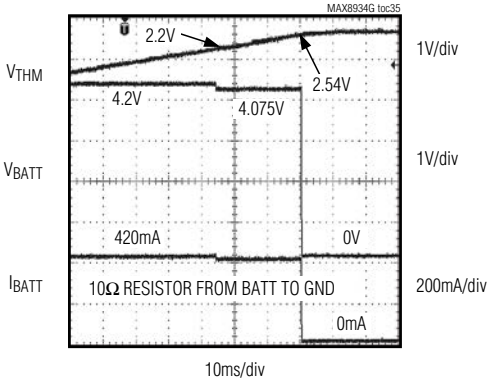
THM NORMAL TO THM HOT NO CHARGE (> T4) TRANSITION



THM NORMAL TO THM HOT THRESHOLD DISCHARGE $T_{\overline{OT}}$



THM NORMAL TO T2 TO T1 (COLD, NO CHARGE) TRANSITION



Pin Description

PIN	NAME	FUNCTION
1	$\overline{DONE}$	Charge Complete Output. The $\overline{DONE}$ active-low, open-drain output pulls low when the charger enters the DONE state. The charger current = 0mA when $\overline{DONE}$ is low. See Figure 7.
2, 3	DC	DC Power Input. DC is capable of delivering up to 2A to SYS. DC supports both AC adapter and USB inputs. The DC current limit is set with PEN1, PEN2, and R_{PSET}. See Table 2. Both DC pins must be connected together externally. Connect a 10µF ceramic capacitor from DC to GND. The DC inputs should be grounded if not used.
4	$\overline{CEN}$	Active-Low Charger Enable Input. Connect $\overline{CEN}$ to GND or drive low with a logic signal to enable battery charging when a valid source is connected at DC or USB. Drive high with a logic signal to disable battery charging.
5	PEN1	Input Limit Control 1. See Table 2 for complete information.
6	PEN2	Input Limit Control 2. See Table 2 for complete information.
7	PSET	DC Input Current-Limit Setting. Connect a resistor from PSET to GND to program the DC current limit up to 2A (3000V/R_{PSET}).
8	V_L	Internal Logic LDO Output Bypass Pin. Provides 3.3V when DC or USB is present. Connect a 0.1µF ceramic capacitor from V_L to GND. V_L powers the internal circuitry and provides up to 5mA to an external load.
9, 13	GND	Ground. Both GND pins must be connected together externally.
10	CT	Charge Timer Program Input. A capacitor from CT to GND sets the maximum prequal and fast-charge timers. Connect CT to GND to disable the timer.
11	ISET	Charge Current-Limit Setting. A resistor (R_{ISET}) from ISET to GND programs the fast-charge charge current up to 1.5A (3000V/R_{ISET}). The prequal charge current is 20% of the set fast-charge charge current.
12	USUS	USB Suspend Digital Input. As shown in Table 2, driving USUS high suspends the DC or USB inputs if they are configured as a USB power input.
14	THM	Thermistor Input. Connect a negative temperature coefficient (NTC) thermistor with good thermal contact with the battery from THM to GND. Use a thermistor with Beta = 3964. Connect a resistor of equal resistance to the thermistor resistance at +25°C from THM to THMSW so that the battery temperature can be monitored, and the fast-charge current and/or the charge termination voltage is automatically adjusted, in accordance with safety region 2 of the JEITA specification.
15	THMEN	Thermistor Enable Input. THMEN controls THMSW by connecting the external thermistor pullup resistor and the thermistor monitoring circuit to LDO. Drive THMEN high to enable the thermistor circuit in discharge mode and to connect the external thermistor pullup resistor. Drive THMEN low to disconnect the external thermistor pullup resistor and to disable the thermistor monitoring circuit to conserve battery energy when not charging.
16	THMSW	Thermistor Pullup Supply Switch. Drive THMEN high to enable the THMSW, shorting the THMSW output to LDO. Drive THMEN low to open the THMSW switch. THMSW is always on when a valid input source is present and the battery is being charged. When no input source is present, THMSW is controlled by THMEN. THMSW is also active when the battery is being discharged, so that the battery temperature can be monitored for an overtemperature condition.

Pin Description (continued)

PIN	NAME	FUNCTION
17	LDO	Always-On Linear Regulator Output. LDO is the output of an internal always-on 3.3V LDO that provides power to external circuitry. The LDO output provides up to 30mA of current for indicator LEDs or other loads. LDO remains active even when only a battery is present, so that the thermistor monitor circuitry can be activated when the battery is being discharged, and other circuitry can remain powered. Connect a 1µF ceramic capacitor from LDO to GND.
18, 19	USB	USB Power Input. USB is capable of delivering up to 0.5A to SYS. The USB current limit is set with PEN2 and USUS. See Table 2. Both USB pins must be connected together externally. Connect a 4.7µF ceramic capacitor from USB to GND.
20, 21	BATT	Battery Connection. Connect the positive terminal of a single-cell Li+ battery to BATT. The battery charges from SYS when a valid source is present at DC or USB. BATT powers SYS when neither DC nor USB power is present, or when the SYS load exceeds the input current limit. Both BATT pins must be connected together externally.
22	$\overline{CHG}$	Charger Status Output. The $\overline{CHG}$ active-low, open-drain output pulls low when the battery is in fast charge or prequal. Otherwise, $\overline{CHG}$ is high impedance.
23, 24	SYS	System Supply Output. SYS is connected to BATT through an internal 40mΩ system load switch when DC or USB are invalid, or when the SYS load is greater than the input current limit. When a valid voltage is present at DC or USB, SYS is limited to or 4.35V. When the system load (I_{SYS}) exceeds the DC or USB current limit, SYS is regulated to 75mV below V_{BATT} and both the input and the battery service the SYS load. Bypass SYS to GND with a 10µF ceramic capacitor. Both SYS pins must be connected together externally.
25	$\overline{OT}$	Battery Overtemperature Flag. The $\overline{OT}$ active-low, open-drain output pulls low when THMEN is high and the battery temperature is ≥ +75°C.
26	$\overline{DOK}$	DC Power-OK Output. The $\overline{DOK}$ active-low, open-drain output pulls low when a valid input is detected at DC.
27	$\overline{UOK}$	USB Power-OK Output. The $\overline{UOK}$ active-low, open-drain output pulls low when a valid input is detected at USB.
28	$\overline{FLT}$	Fault Output. The $\overline{FLT}$ active-low, open-drain output pulls low when the battery timer expires before prequal or fast charge complete.
—	EP	Exposed Pad. Connect the exposed pad to GND. Connecting the exposed pad does not remove the requirement for proper ground connections to the appropriate pins.

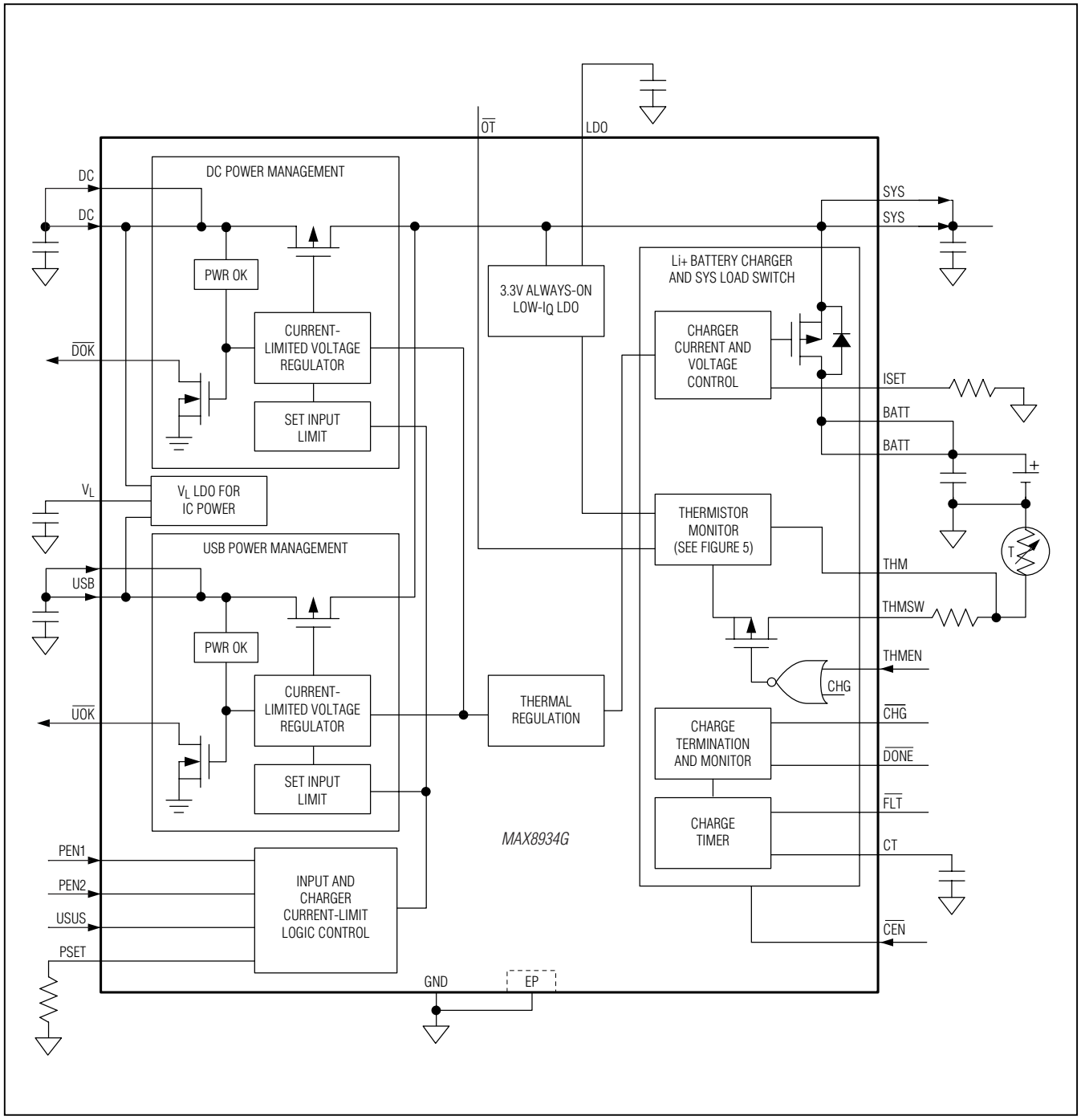


Figure 1. Block Diagram

Dual-Input Linear Charger, Smart Power Selector with Advanced Battery Temperature Monitoring

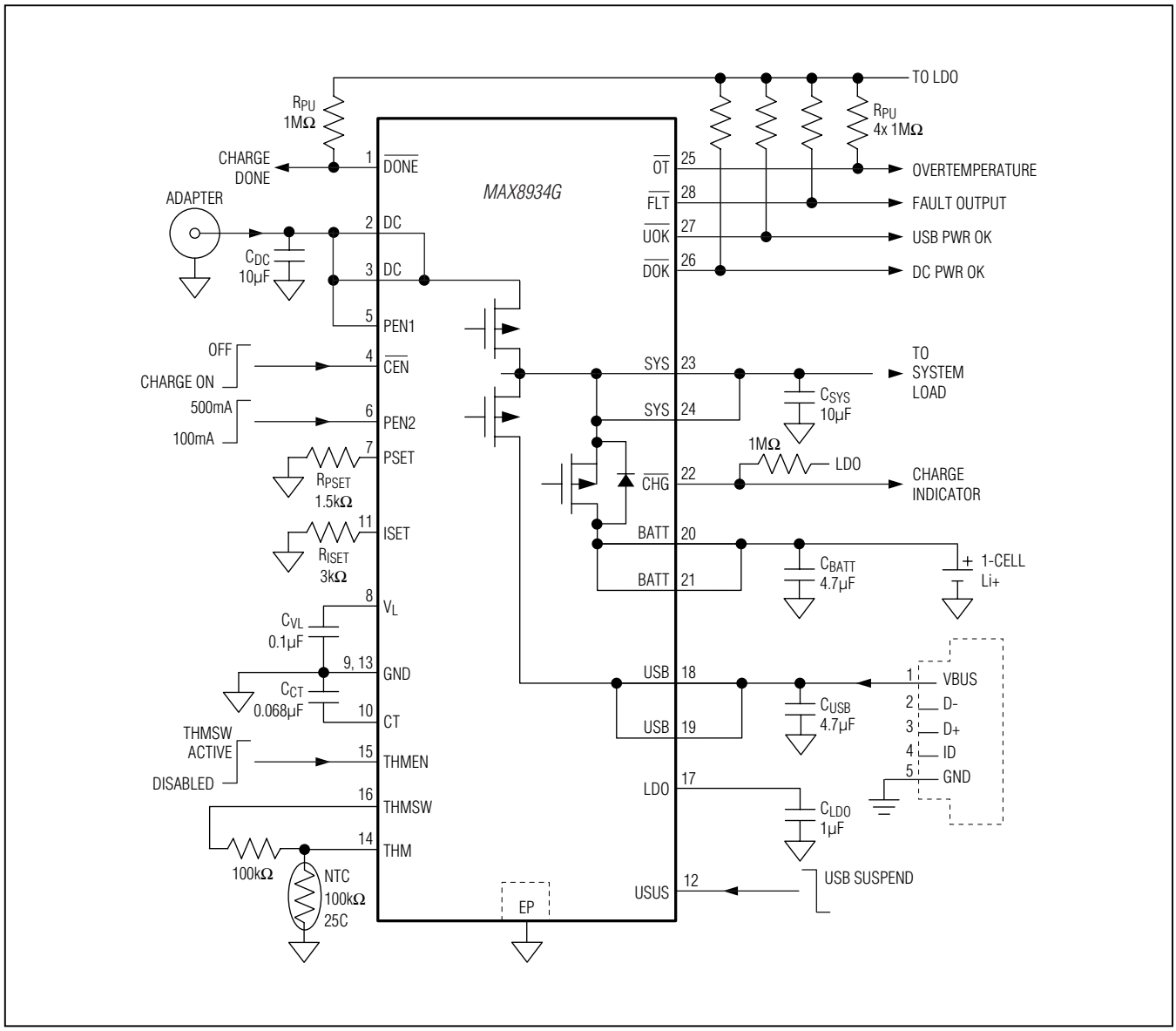


Figure 2. Typical Application Circuit Using Separate DC and USB Connector

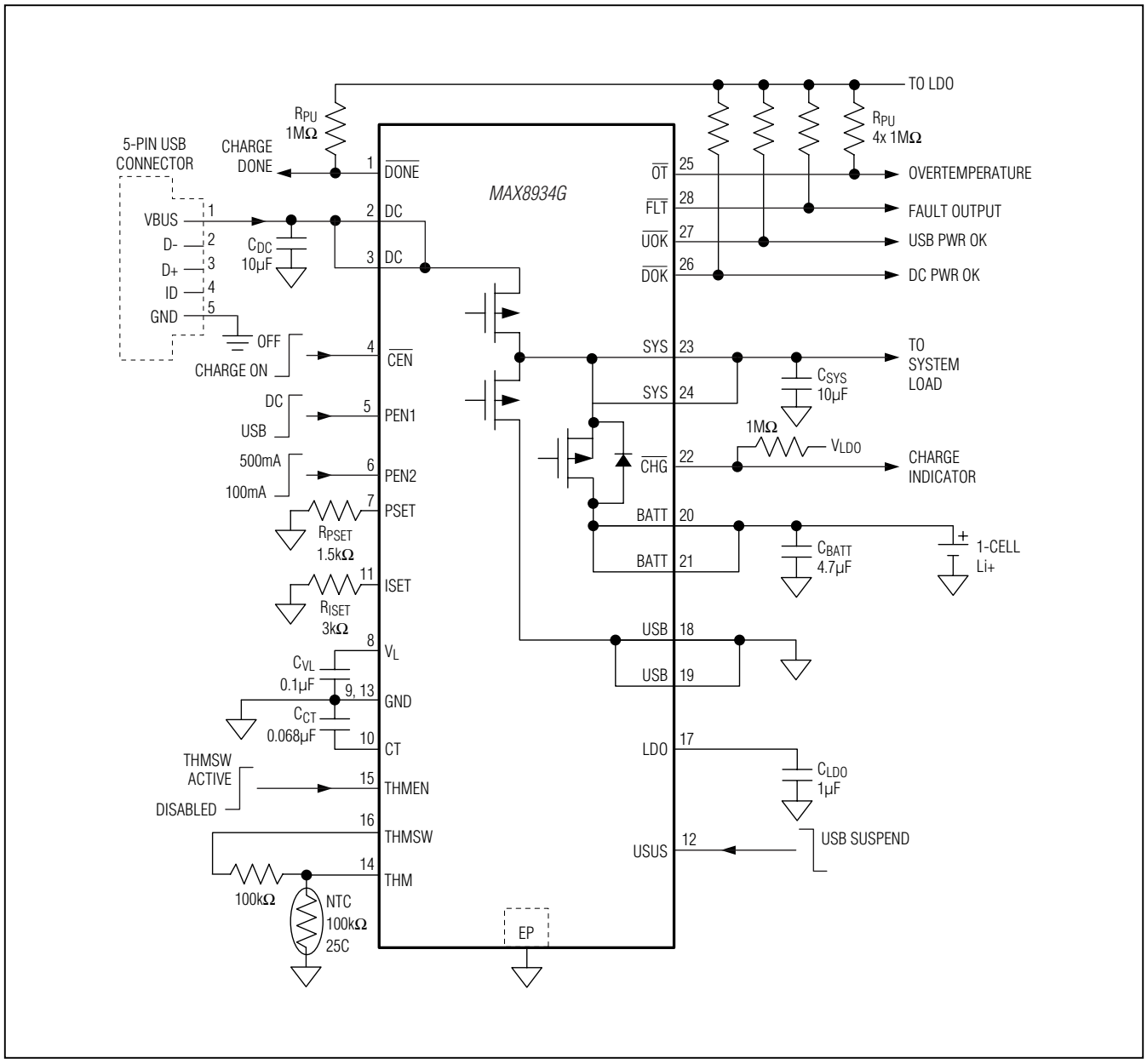


Figure 3. Typical Application Circuit Using a 5-Pin USB Connector or Other DC/USB Common Connector

Table 1. External Components List for Figures 2 and 3

COMPONENT (Figures 2 and 3)	FUNCTION	PART NUMBER
C_{DC}	DC filter capacitor	10µF ±10%, 16V X5R ceramic capacitor (0805) Taiyo Yuden EMK212BJ106KG
C_{USB}	USB filter capacitor	4.7µF ±10%, 10V X5R ceramic capacitor (0805) Taiyo Yuden LMK212BJ475KD
C_{VL}	V_L filter capacitor	0.1µF ±10%, 10V X5R ceramic capacitor (0402) Taiyo Yuden LMK105BJ104KV
C_{SYS}	SYS output bypass capacitors	10µF ±10%, 6.3V X5R ceramic capacitor (0805) Taiyo Yuden JMK212BJ106KD
C_{BATT}	Battery bypass capacitor	4.7µF ±10%, 6.3V X5R ceramic capacitor (0805) Taiyo Yuden JMK212BJ475KD
C_{CT}	Charger timing capacitor	0.068µF ±10%, 16V X5R ceramic capacitor (0402) Taiyo Yuden EMK105BJ683KV
C_{LDO}	LDO output capacitor	1µF ±10%, 6.3V X5R ceramic capacitor (0402) Taiyo Yuden JMK105BJ105KV
R_{PU} (x5)	Logic-output pullup resistors	1MΩ ±5% resistor
THM	Negative TC thermistor	Vishay NTC Thermistor P/N NTHS0603N01N1003FF
R_{THMSW}	THM pullup resistor	100kΩ
R_{PSET}	DC input current-limit programming resistor	1.5kΩ ±1% for 2A limit
R_{ISET}	Fast-charge current programming resistor	3kΩ ±1% for 1A charging

Detailed Description

The MAX8934G is a dual-input linear charger with Smart Power Selector that safely charges a single Li+/Li-Poly cell in accordance with JEITA specifications. The MAX8934G integrates power MOSFETs and control circuitry to manage power flow in portable devices. See Figure 1. The charger has two power inputs, DC and USB. These can be separately connected to an AC adapter output and a USB port, or the DC input could be a single power input that connects to either an adapter or USB. Logic inputs, PEN1 and PEN2, select the correct current limits for two-input or single-input operation. Figure 2 is the typical application circuit using separate DC and USB connectors. Figure 3 is the typical application circuit using a 5-pin USB connector or another DC/USB common connector.

In addition to charging the battery, the MAX8934G also supplies power to the system through the SYS output. The charging current is also provided from SYS so that the set input current limit controls the total SYS current, where total SYS current is the sum of the system load current and the battery-charging current. SYS is powered from either the DC input pin or the USB input pin. If both the DC and USB sources are connected, DC takes precedence.

In some instances, there may not be enough adapter current or USB current to supply peak system loads. The MAX8934G Smart Power Selector circuitry offers flexible power distribution from an AC adapter or USB source to the battery and system load. The battery is charged with any available power not used by the system load. If a system load peak exceeds the input current limit, supplemental current is taken from the battery. Thermal limiting prevents overheating by reducing power drawn from the input source.

The MAX8934G features an overvoltage limiter at SYS. If the DC or USB input voltage exceeds the SYS regulation voltage, V_{SYS} does not follow V_{DC} or V_{USB}, but remains at its regulation voltage. The MAX8934G has numerous other charging and power-management features that are detailed in the following sections.

A 3.3V ultra-low quiescent current, always-on LDO provides up to 30mA for indicator LEDs and for backup power to the system. This LDO powers the thermistor monitor circuitry and provides bias to the external pullup resistor for the thermistor.

Smart Power Selector

The MAX8934G Smart Power Selector seamlessly distributes power among the external inputs, the battery, and the system load (see the *Typical Operating Circuit*). The basic functions performed are:

- With both an external power supply (USB or adapter) and battery connected:
  - When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
  - When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no external power input, the system is powered from the battery.
- When an external power input is connected and there is no battery, the system is powered from the external power input.

System Load Switch

An internal 40mΩ MOSFET connects SYS to BATT (Q3 in the *Typical Operating Circuit*) when no voltage source is available at DC or USB. When an external source is detected at DC or USB, this switch is opened and SYS is powered from the valid input source through the input limiter.

The SYS-BATT switch also holds up SYS when the system load exceeds the input current limit. If that should happen, the SYS-BATT switch turns on so that the battery supplies additional SYS load current. If the system load continuously exceeds the input current limit, the battery does not charge, even though external power is connected. This is not expected to occur in most cases, since high loads usually occur only in short peaks. During these peaks, battery energy is used, but at all other times the battery charges.

Input Limiter

The input voltage limiter is essentially an LDO regulator. While in dropout, the regulator dissipates a small I^2R loss through the 0.2Ω MOSFET (Q1 in the *Typical Operating Circuit*) between DC and SYS. With an AC adapter or USB source connected, the input limiter distributes power from the external power source to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system and charger loads at SYS, it performs several additional functions to optimize use of available power.

Input Voltage Limiting

If an input voltage is above the overvoltage threshold (6.9V typ), the MAX8934G enters overvoltage lockout (OVLO). OVLO protects the MAX8934G and downstream circuitry from high-voltage stress up to 14V at DC and 8V at USB. In OVLO, V_L remains on, the input switch that sees overvoltage (Q1, Q2, *Typical Operating Circuit*) opens, the appropriate power-monitor output ($\overline{DOK}$, $\overline{UOK}$) is high impedance, and $\overline{CHG}$ is high impedance. If both DC and USB see overvoltage, both input switches (Q1 and Q2, *Typical Operating Circuit*) open and the charger turns off. The BATT-to-SYS switch (Q3, *Typical Operating Circuit*) closes, allowing the battery to power SYS. An input is also invalid if it is less than BATT, or less than the DC undervoltage threshold of 3.5V (falling). With an invalid input voltage, SYS connects to BATT through a 40mΩ switch (Q3, *Typical Operating Circuit*).

Input Overcurrent Protection

The current at DC and USB is limited to prevent input overload. This current limit can be selected to match the capabilities of the source, whether it is a 100mA or 500mA USB source, or an AC adapter. When the load exceeds the input current limit, SYS drops to 75mV below BATT and the battery supplies supplemental load current.

Thermal Limiting

The MAX8934G reduces input limiter current by 5%/°C when its die temperature exceeds +100°C. The system load (SYS) has priority over the charger current, so lowering the charge current first reduces the input current. If the junction temperature still reaches +120°C in spite of charge current reduction, no input (DC or USB) current is drawn, the battery supplies the entire system load, and SYS is regulated at 75mV below BATT. Note that this on-chip thermal-limiting circuitry is not related to and operates independently from the thermistor input.

Adaptive Battery Charging

While the system is powered from DC, the charger draws power from SYS to charge the battery. If the charger load plus system load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent the SYS voltage from collapsing. Maintaining a higher SYS voltage improves efficiency and reduces power dissipation in the input limiter. The total current through the switch (Q1 or Q2 in the *Typical Operating Circuit*) is the sum of the load current at SYS and the battery charging current. The MAX8934G limiter clamps at 4.35V, so input voltages greater than 4.35V can increase power dissipation in the limiter. The MAX8934G input

limiter power loss is (V_{DC} – V_{SYS}) x I_{DC}, where V_{SYS} may be as high as 4.35V. The input limiter power loss is not less than 0.2Ω x I_{DC}^2. Also note that the MAX8934G turns off when any input exceeds 6.9V (typ).

DC and USB Connections and Current-Limit Options

Input Current Limit

The input and charger current limits are set as shown in Table 2. It is often preferable to change the input current limit as the input power source is changed. The MAX8934G facilitates this by allowing different input current limits for DC and USB as shown in Table 2.

When the input current limit is reached, the first action taken by the MAX8934G is to reduce the battery charge current. This allows the regulator to stay in dropout during heavy loads, thus reducing power dissipation. If, after the charge current is reduced to 0mA, the load at SYS still exceeds the input current limit, SYS voltage begins to fall. When the SYS voltage drops to BATT, the SYS-to-BATT switch turns on, using battery power to support the system load during the load peak. The MAX8934G features flexible input connections (at the DC and USB input pins) and current-limit settings (set by PEN1, PEN2, PSET, and ISET) to accommodate nearly any input power configuration. However, it is expected that most systems use one of two external power schemes: separate connections for USB and an AC adapter, or a single connector that accepts either USB or AC adapter output. Input and charger current limit are controlled by PEN1, PEN2, R_{PSET}, and R_{ISET}, as shown in Table 2.

Separate Adapter and USB Connectors

When the AC adapter and USB have separate connectors, the adapter output connects to DC and the USB source connects to USB. PEN1 is permanently connected high (to DC or V_L). The DC current limit is set by R_{PSET}, while the USB current limit is set by PEN2 and USUS.

Single Common Connector for USB or Adapter

When a single common connector is used for both AC adapter and USB sources, the DC input is used for both input sources. The unused USB inputs should be grounded when an AC adapter is connected at DC, PEN1 should be pulled high to select the current limit set by R_{PSET}. When a USB source is connected, PEN1 should be low to select 500mA, 100mA, or USB suspend (further selected by PEN2 and USUS). PEN1 can be pulled up by the AC adapter power to implement hardware adapter/USB selection.

USB Suspend

Driving USUS high when PEN1 is low turns off the charger and reduces input current to 190µA to accommodate USB suspend mode. The input limiter is disabled and SYS is supported by BATT.

Power Monitor Outputs ($\overline{UOK}$, $\overline{DOK}$)

$\overline{DOK}$ is an open-drain output that pulls low when the DC input has valid power. $\overline{UOK}$ is an open-drain output that pulls low when the USB input has valid power. A valid input for DC or USB is between 4.1V and 6.6V. If a single power-OK output is preferred, $\overline{DOK}$ and $\overline{UOK}$ can be wire-ORed together. The combined output then pulls low if either USB or DC is valid.

Table 2. Input Limiter Control Logic

POWER SOURCE	$\overline{DOK}$	$\overline{UOK}$	PEN1	PEN2	USUS	DC INPUT CURRENT LIMIT	USB INPUT CURRENT LIMIT	MAXIMUM CHARGE CURRENT*
AC adapter at DC input	L	X	H	X	X	3000V/R_{PSET}	USB input off; DC input has priority	3000V/R_{ISET}
USB power at DC input	L	X	L	H	L	475mA		475mA
	L	X	L	L	L	95mA		95mA
	L	X	L	X	H	USB suspend		0
USB power at USB input; DC unconnected	H	L	X	H	L	No DC input	475mA	3000V/R_{ISET}
	H	L	X	L	L		95mA	
	H	L	X	X	H		USB suspend	0
DC and USB unconnected	H	H	X	X	X		No USB input	0

**Charge current cannot exceed the input current limit. Actual charge current may be less than the maximum charge current if the total SYS load exceeds the input current limit.*

Soft-Start

To prevent input transients that can cause instability in the USB or AC adapter power source, the rate of change of input current and charge current is limited. When a valid DC or USB input is connected, the input current limit is ramped from zero to the set current-limit value (as shown in Table 2). If DC is connected with no USB power present, input current ramps in 1.5ms. If DC is connected with USB already present, input current ramps in 50µs. When USB is connected with no DC present, input current also ramps in 50µs. If USB is connected with DC already present, the USB input is ignored.

If an adapter is plugged into DC while USB is already powered, the input current limit reramps from zero back up to the DC current limit so that the AC adapter does not see a load step. During this transition, if the input current limit is below the SYS load current, the battery supplies the additional current needed to support the load. Additionally, capacitance can be added to SYS to support the load during input power transitions. When the charger is turned on, charge current ramps from zero to the ISET current value in 1.5ms. Charge current also ramps when transitioning to fast-charge from prequal and when changing the USB charge current from 100mA to 500mA with PEN2. There is no dI/dt limiting, however, if ISET is changed suddenly using a switch at R_{ISET}.

Battery Charger

The battery charger state diagram is illustrated in Figure 7. With a valid DC or USB input, the battery charger initiates a charge cycle when the charger is enabled. It first detects the battery voltage. If the battery voltage is less than the BATT prequal threshold (3.0V), the charger enters prequal mode and charges the battery at 20% of the maximum fast-charge current. This reduced charge rate ensures that the maximum fast-charge current setting does not damage a deeply discharged battery. Once the battery voltage rises to 3.0V, the charger transitions to fast-charge mode and applies the maximum charge current. As charging continues, the battery voltage rises until it approaches the battery regulation voltage where charge current starts tapering down. When charge current decreases to 20% of the fast-charge current, the charger enters a brief 15s top-off state, then $\overline{DONE}$ pulls low and charging stops. If the battery voltage subsequently drops below the recharge threshold, charging restarts and the timers reset.

Charge Enable ($\overline{CEN}$)

When $\overline{CEN}$ is low, the charger is on. When $\overline{CEN}$ is high, the charger turns off. $\overline{CEN}$ does not affect the SYS output. In many systems, there is no need for the system controller (typically a microprocessor) to disable the charger, because the MAX8934G Smart Power Selector circuitry independently manages charging and adapter/battery power hand-off. In these situations, $\overline{CEN}$ can be connected to ground.

Setting the Charge Current

ISET adjusts charge current to match the capacity of the battery. A resistor from ISET to ground sets the maximum fast-charge current:

$$I_{CHGMAX} = 2000 \times 1.5V/R_{ISET} = 3000V/R_{ISET}$$

Determine the I_{CHGMAX} value by considering the characteristics of the battery. It is not necessary to limit the charge current based on the capabilities of the expected AC adapter/USB charging input, the system load, or thermal limitations of the PCB. The MAX8934G automatically adjusts the charging algorithm to accommodate these factors.

Monitoring the Charge Current

In addition to setting the charge current, ISET can also be used to monitor the actual current charging the battery. See Figure 4. The ISET output voltage is:

$$V_{ISET} = I_{CHG} \times 1.5V/I_{CHGMAX} = I_{CHG} \times R_{ISET}/2000$$

where I_{CHGMAX} is the set fast-charge current and I_{CHG} is the actual battery charge current. A 1.5V output indicates the battery is being charged at the maximum set fast charge current; 0V indicates no charging. This voltage is also used by the charger control circuitry to set and monitor the battery current. Avoid adding more than 10pF capacitance directly to the ISET pin. If filtering of the charge-current monitor is necessary, add a resistor of 100kΩ or more between ISET and the filter capacitor to preserve charger stability.

Note that the actual charge current can be less than the set fast-charge current when the charger enters voltage mode or when the input current limiter or thermal limiter reduces charge current. This prevents the charger from overloading the input source or overheating the system.

Charge Termination

When the charge current falls to the termination threshold and the charger is in voltage mode, charging is complete. Charging continues for a brief 15s top-off period and then enters the DONE state where charging stops. The DONE current threshold (I_{DONE}) is set to 20% of the

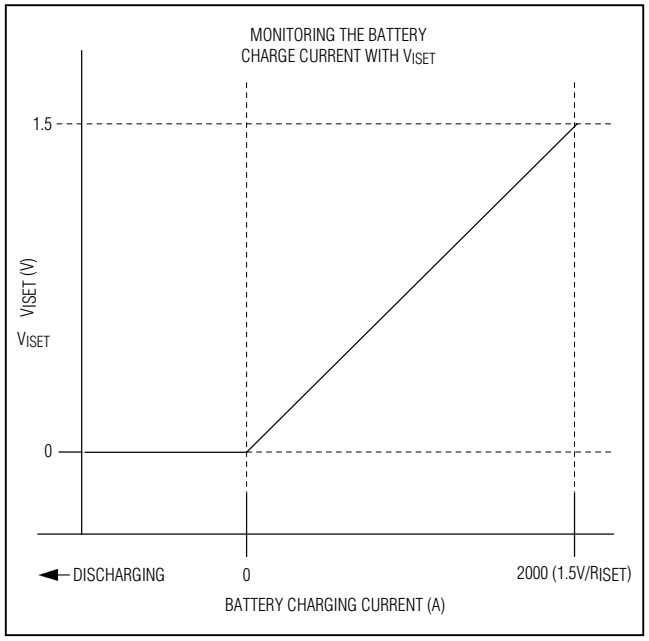


Figure 4. Monitoring the Battery Charge Current with VISET

fast-charge current setting. Note that if charge current falls to I_{DONE} as a result of the input or thermal limiter, the charger does not enter the DONE state. For the charger to enter the DONE state, the charge current must be less than I_{DONE}, the charger must be in voltage mode, and the input or thermal limiter must not be reducing the charge current. The charger exits the DONE state, and fast-charge resumes if the battery voltage subsequently drops 104mV or if $\overline{CEN}$ is cycled.

Charge Status Outputs

Charge Output ($\overline{CHG}$)

$\overline{CHG}$ is an open-drain, active-low output that is low during charging. $\overline{CHG}$ is low when the battery charger is in its prequalification and fast-charge states. When charge current falls to the charge termination threshold (I_{DONE}) and the charger is in voltage mode, $\overline{CHG}$ goes high impedance. $\overline{CHG}$ goes high impedance if the thermistor causes the charger to enter temperature suspend mode.

When the MAX8934G is used with a microprocessor (µP), connect a pullup resistor between $\overline{CHG}$ and the logic I/O voltage to indicate charge status to the µP. Alternatively, $\overline{CHG}$ can sink up to 20mA for an LED indicator.

Charge DONE Output ($\overline{DONE}$)

$\overline{DONE}$ is an open-drain, active-low output that goes low when charging is complete. The charger enters its DONE state 15s after the charge current falls to the charge-termination threshold (I_{DONE}) and the charger is in voltage mode. The charger exits the DONE state, and fast-charge resumes, if the battery voltage subsequently drops 104mV, or if input power or $\overline{CEN}$ is cycled. When the MAX8934G is used in conjunction with a µP, connect a pullup resistor between $\overline{DONE}$ and the logic I/O voltage to indicate charge status to the µP. Alternatively, $\overline{DONE}$ can sink up to 20mA for an LED indicator.

Fault Output ($\overline{FLT}$) and Charge Timer

$\overline{FLT}$ is an open-drain, active-low output that goes low during a battery fault. The fault state occurs when either the prequal or fast-charge timer expires. The prequal and fast-charge fault timers are set by C_{CT}:

$$\text{PREQUAL: } t_{PQ} = 180\text{min} \times \frac{C_{CT}}{0.068\mu F}$$

$$\text{FAST CHARGE: } t_{FC} = 300\text{min} \times \frac{C_{CT}}{0.068\mu F}$$

$$\text{TOP-OFF: } t_{TO} = 15\text{s}$$

While in fast-charge mode, a large system load or device self-heating can cause the MAX8934G to reduce charge current. Under these circumstances, the fast-charge timer adjusts to ensure that adequate charge time is still allowed. Consequently, the fast-charge timer is slowed by 2x if charge current is reduced below 50% of the programmed fast-charge level. If charge current is reduced to below 20% of the programmed level, the fast-charge timer is paused. The fast-charge timer is not adjusted if the charger is in voltage mode where charge current reduces due to current tapering under normal charging.

To exit a fault state, toggle $\overline{CEN}$ or remove and reconnect the input source(s). Note also that thermistor out of range or on-chip thermal-limit conditions are not considered faults. When the MAX8934G is used in conjunction with a µP, connect a pullup resistor between $\overline{FLT}$ and the logic I/O voltage to indicate fault status to the µP. Alternatively, $\overline{FLT}$ can sink up to 20mA for an LED indicator.

Thermistor Monitor

The MAX8934G thermistor monitor is configured to execute JEITA recommendations regarding Li+/Li-Poly battery charging by adjusting the fast charge current and/or the charge termination voltage accordingly (see Figure 6). Connect the THM input to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature. Since the thermistor monitoring circuit employs an external bias resistor from THM to THMSW, the thermistor is not limited only to 10kΩ (at

+25°C). Any thermistor resistance can be used as long as the value of R_{THMSW} is equivalent to the thermistor's +25°C resistance. The MAX8934G THM thresholds are optimized for a thermistor Beta of 3964. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} \times e^{\left\{\beta\left(\frac{1}{T+273°C} - \frac{1}{298°C}\right)\right\}}$$

where:

R_T = The resistance in ohms of the thermistor at temperature T in °C

R_{25} = The resistance in ohms of the thermistor at +25°C

ß = The material constant of the thermistor

T = The temperature of the thermistor in °C

Charging is suspended when the thermistor temperature is out of range ($V_{THM_T1} < V_{THM}$ or $V_{THM} < V_{THM_T4}$). The charge timers are also suspended and hold their state but no fault is indicated. When the thermistor comes back into range, charging resumes and the charge timer continues from where it left off.

The THMEN input controls THMSW and the thermistor monitor circuitry when the battery charger is disabled, providing the user with the means to minimize the battery current drain caused by the thermistor monitor. The THMEN input is ignored while the battery is charging, since the thermistor must be monitored at all times.

While charging, the thermistor monitor is used to automatically adjust the charge termination voltage and/or the fast-charge current, depending on the sensed battery temperature. If the battery temperature exceeds the THM hot overtemperature threshold and THMEN is high, the $\overline{OT}$ flag pulls low. Typical systems connect $\overline{OT}$ to a µP input so that the system can safely shut down.

Always-On LDO

The ultra-low quiescent current LDO is always on and is preset to an output voltage of 3.3V. The LDO provides up to 30mA output current. When DC and USB are invalid and the battery is discharging, the LDO output voltage tracks V_{SYS} as it drops below 3.3V. A 1µF ceramic capacitor connected from LDO to GND is recommended for most applications.

Power Dissipation

PCB Layout and Routing

Good design minimizes ground bounce and voltage gradients in the ground plane. GND should connect to the power-ground plane at only one point to minimize the effects of power-ground currents. Battery ground should connect directly to the power-ground plane. Connect GND to the exposed pad directly under the IC. Use multiple tightly spaced vias to the ground plane under the exposed pad to help cool the IC. Position input capacitors from DC, SYS, BATT, and USB to the power-ground plane as close as possible to the IC. Keep high current traces such as those to DC, SYS, and BATT as short and wide as possible. Refer to the MAX8934A Evaluation Kit for a suitable PCB layout example.

Table 3. Package Thermal Characteristics

	28-PIN 4mm x 4mm THIN QFN	
	SINGLE-LAYER PCB	**MULTILAYER PCB**
Continuous Power Dissipation	1666.7mW (derate 20.8mW/°C above +70°C)	2285.7mW (derate 28.6mW/°C above +70°C)
θ_{JA}	48°C/W	35°C/W
θ_{JC}	3°C/W	3°C/W

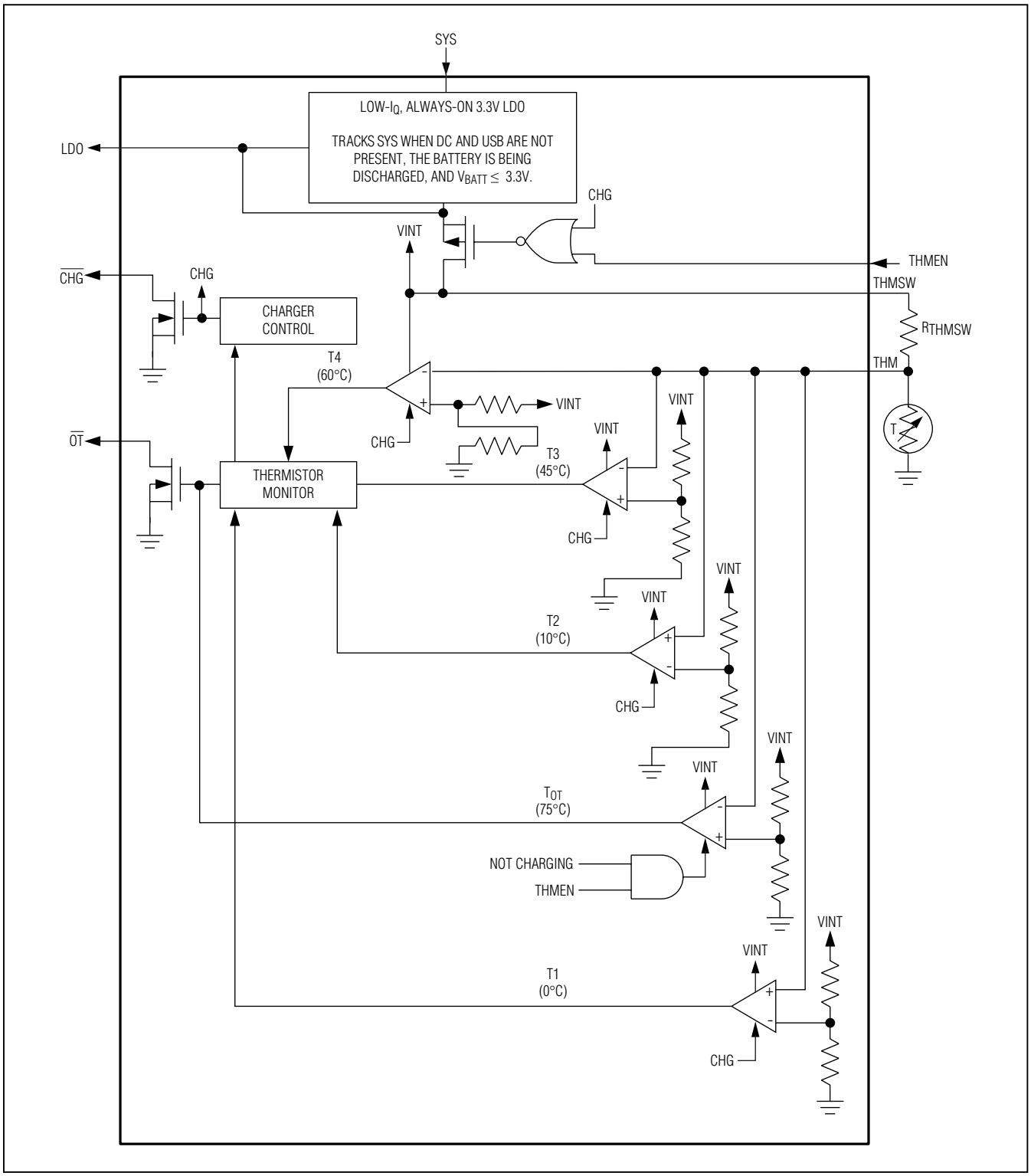


Figure 5. Thermistor Monitor Details

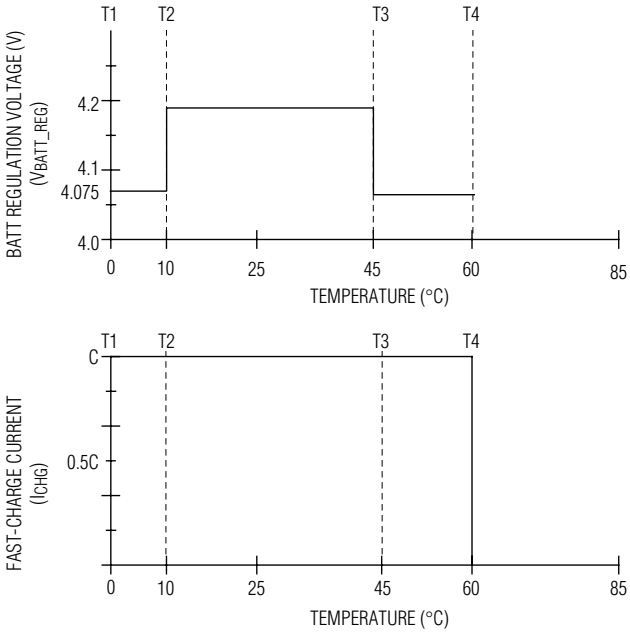


Figure 6. Safety Region 2: Fast-Charge Currents and Charge Termination Voltages

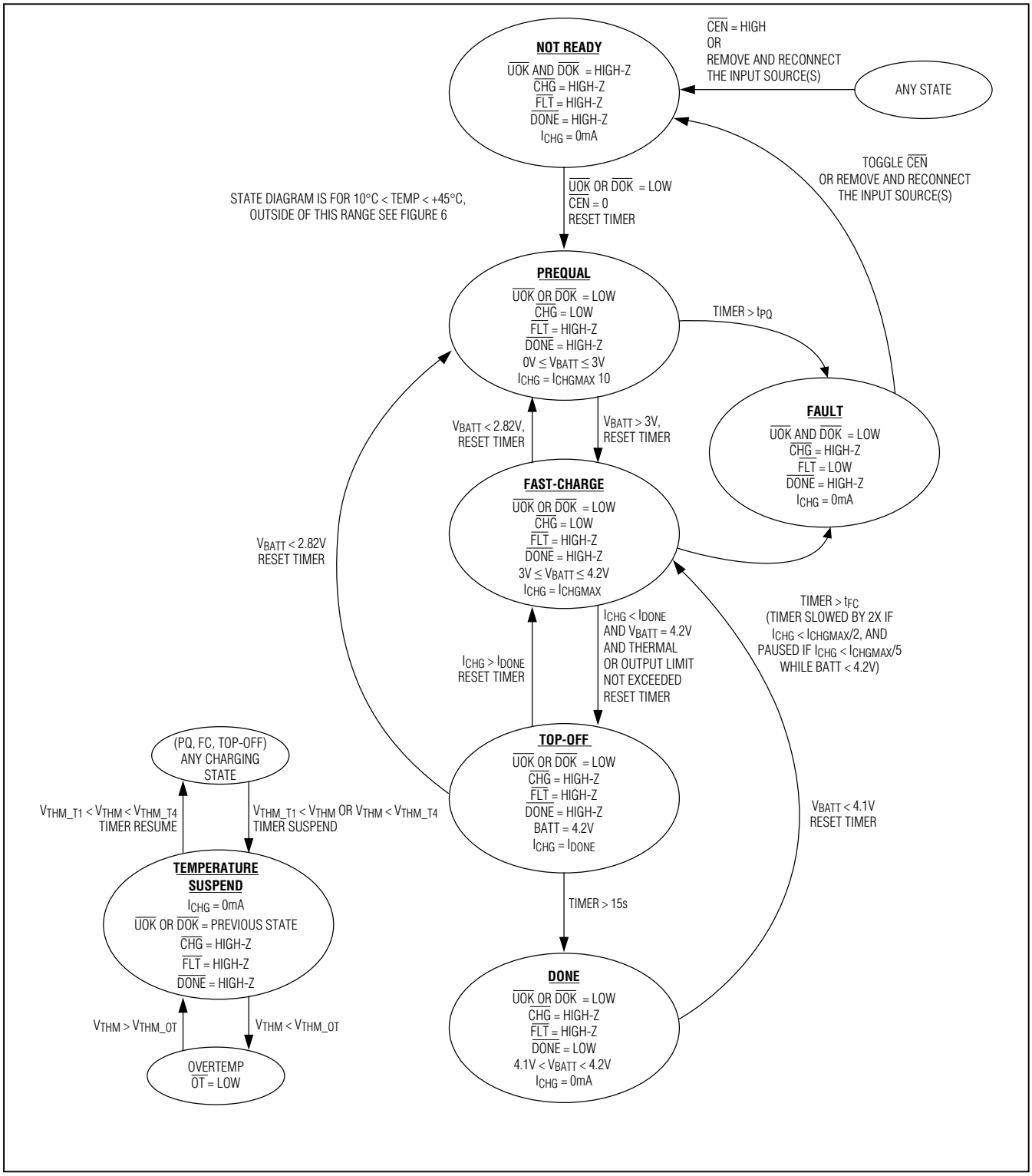


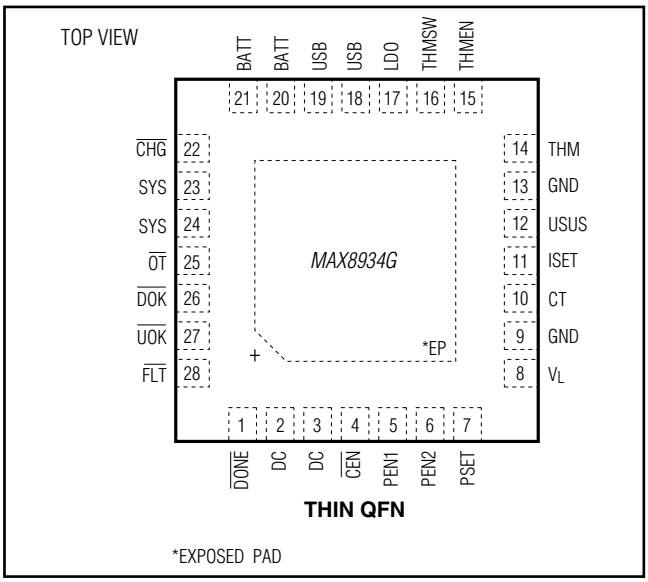
Figure 7. Charger State Diagram

Dual-Input Linear Charger, Smart Power Selector with Advanced Battery Temperature Monitoring

Chip Information

PROCESS: BiCMOS

Pin Configuration

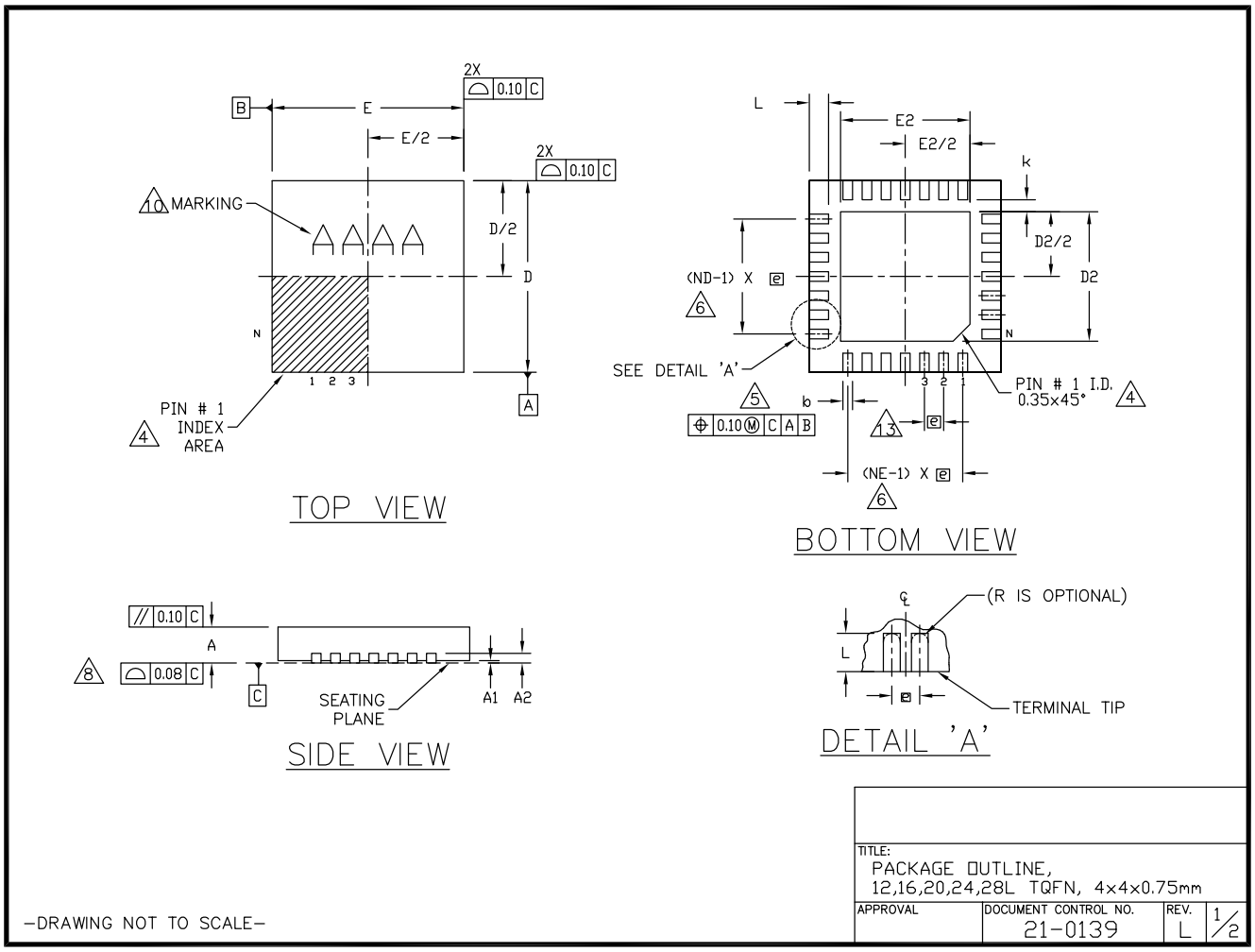


Dual-Input Linear Charger, Smart Power Selector with Advanced Battery Temperature Monitoring

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 TQFN-EP	T2844+1	21-0139	90-0068



Package Information (continued)

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444N-4	2.45	2.60	2.63	2.45	2.60	2.63
T2444M-1	2.45	2.60	2.63	2.45	2.60	2.63
T2444MK-1	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70
T2844N-1	2.65	2.70	2.75	2.65	2.70	2.75

DIMENSION VARIATIONS

PKG. CODE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T2044-4	2.85	2.90	2.95	2.85	2.90	2.95	0.25	0.30	0.35

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
16. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, 12,16,20,24,28L TQFN, 4x4x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0139	L	2/2

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION DATE	PAGES CHANGED
0	6/10	Initial release	—

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