

IRFP4321PbF

Applications

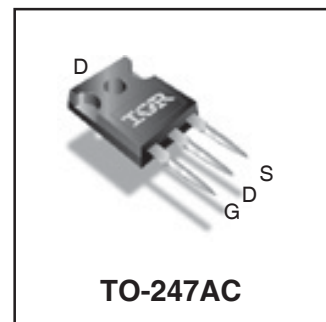
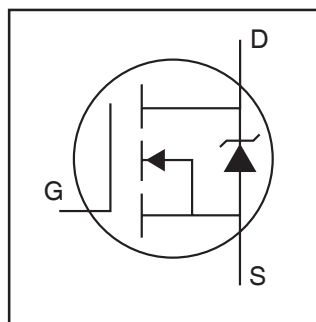
- Motion Control Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- Hard Switched and High Frequency Circuits

Benefits

- Low $R_{DS(on)}$ Reduces Losses
- Low Gate Charge Improves the Switching Performance
- Improved Diode Recovery Improves Switching & EMI Performance
- 30V Gate Voltage Rating Improves Robustness
- Fully Characterized Avalanche SOA

HEXFET® Power MOSFET

V_{DSS}	150V
$R_{DS(on)}$ typ. max.	12mΩ
	15.5mΩ
I_D	78A



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	78 ①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	55	
I _{DM}	Pulsed Drain Current ②	330	
P _D @T _C = 25°C	Maximum Power Dissipation	310	W
	Linear Derating Factor	2.0	W/°C
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS} (Thermally limited)	Single Pulse Avalanche Energy ③	210	mJ
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑤	—	0.49	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	40	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V$, $I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	150	—	mV/°C	Reference to 25°C , $I_D = 1mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	12	15.5	mΩ	$V_{GS} = 10V$, $I_D = 33A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}$, $I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V$, $V_{GS} = 0V$
		—	—	1.0	mA	$V_{DS} = 150V$, $V_{GS} = 0V$, $T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20V$
$R_{G(int)}$	Internal Gate Resistance	—	0.8	—	Ω	

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	130	—	—	S	$V_{DS} = 25V$, $I_D = 50A$
Q_g	Total Gate Charge	—	71	110	nC	$I_D = 50A$
Q_{gs}	Gate-to-Source Charge	—	24	—	nC	$V_{DS} = 75V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	21	—	nC	$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 75V$
t_r	Rise Time	—	60	—	ns	$I_D = 50A$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—	ns	$R_G = 2.5\Omega$
t_f	Fall Time	—	35	—	ns	$V_{GS} = 10V$ ④
C_{iss}	Input Capacitance	—	4460	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	390	—	pF	$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	82	—	pF	$f = 1.0MHz$

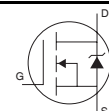
Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	78①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②	—	—	330	A	
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 50A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	89	130	ns	$I_D = 50A$
Q_{rr}	Reverse Recovery Charge	—	300	450	nC	$V_R = 128V$,
I_{RRM}	Reverse Recovery Current	—	6.5	—	A	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.17mH$
 $R_G = 25\Omega$, $I_{AS} = 50A$, $V_{GS} = 10V$. Part not recommended for use above this value.

- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ R_θ is measured at T_J approximately 90°C



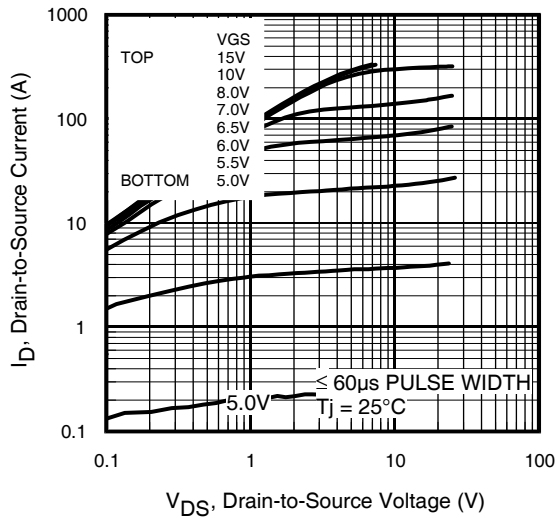


Fig 1. Typical Output Characteristics

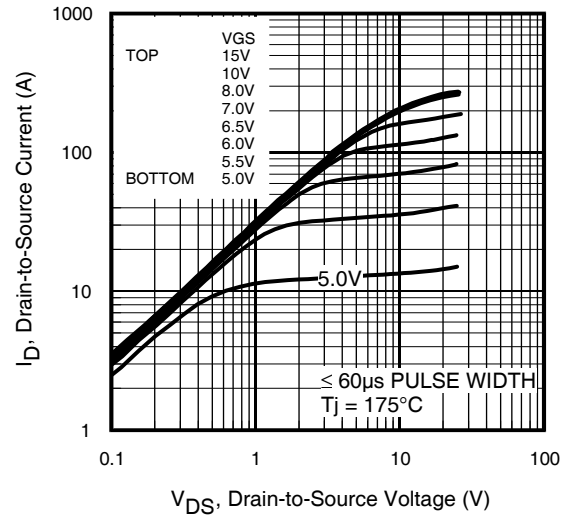


Fig 2. Typical Output Characteristics

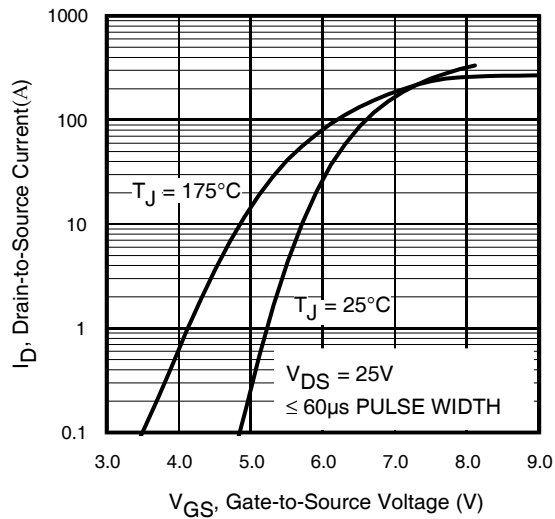


Fig 3. Typical Transfer Characteristics

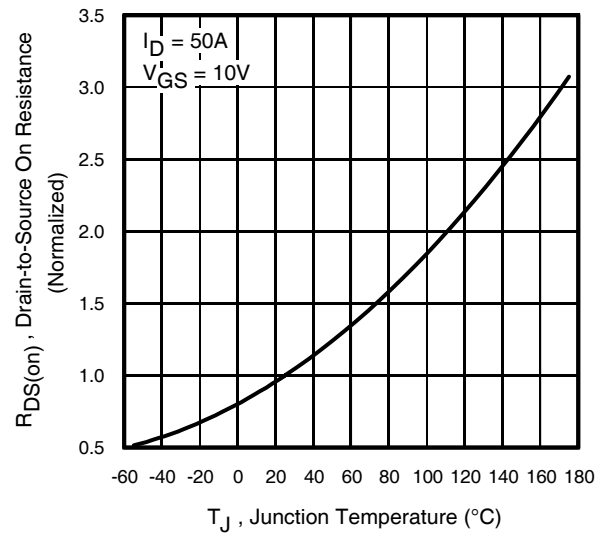


Fig 4. Normalized On-Resistance vs. Temperature

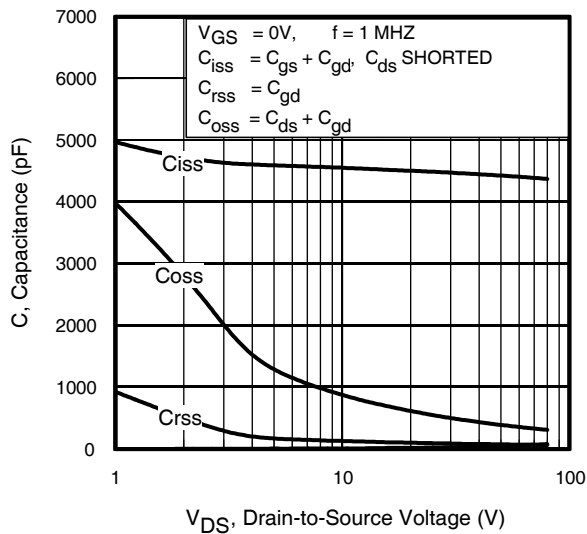


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

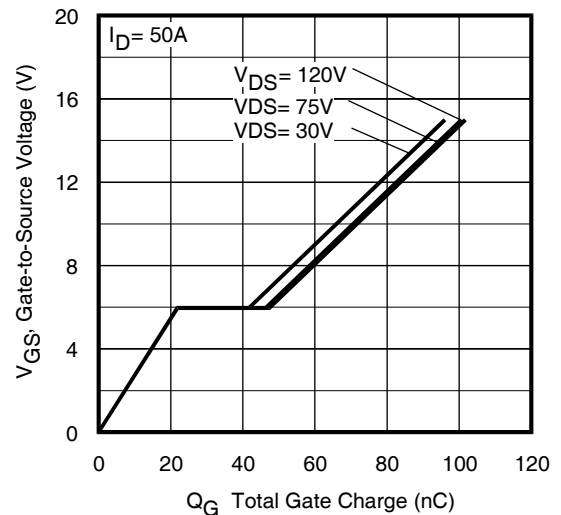


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

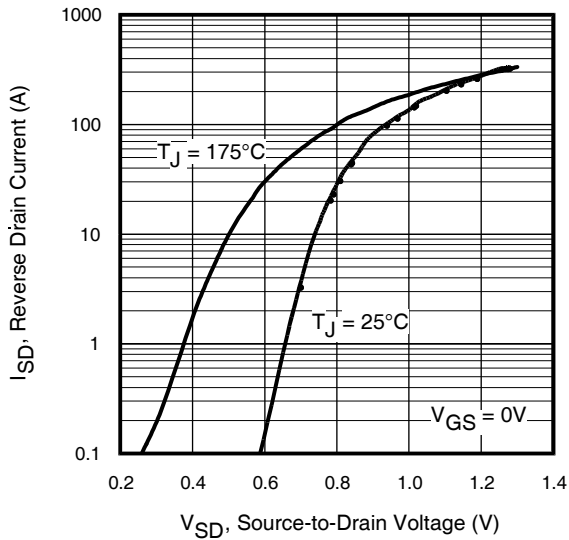


Fig 7. Typical Source-Drain Diode Forward Voltage

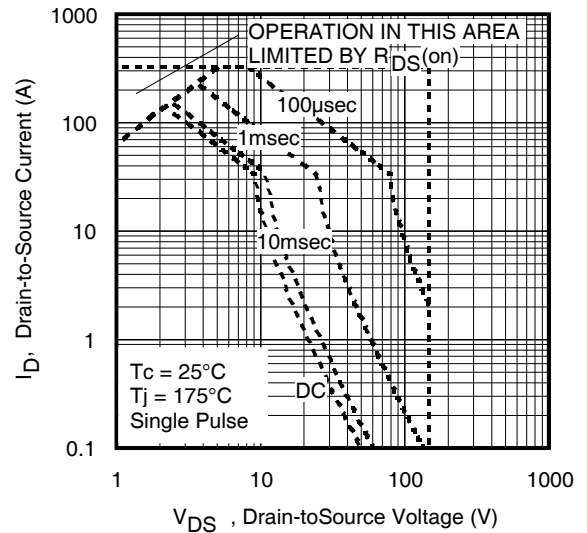


Fig 8. Maximum Safe Operating Area

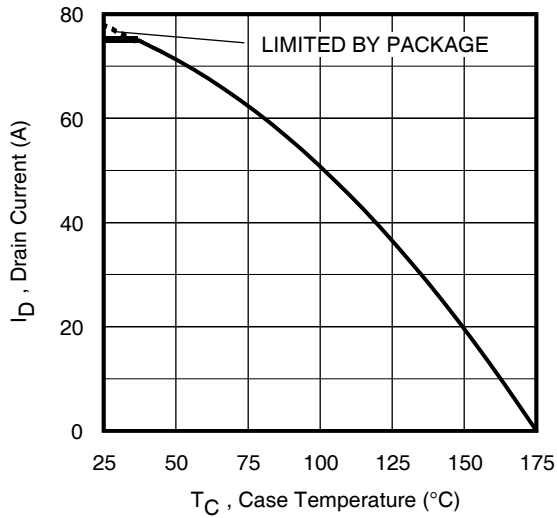


Fig 9. Maximum Drain Current vs. Case Temperature

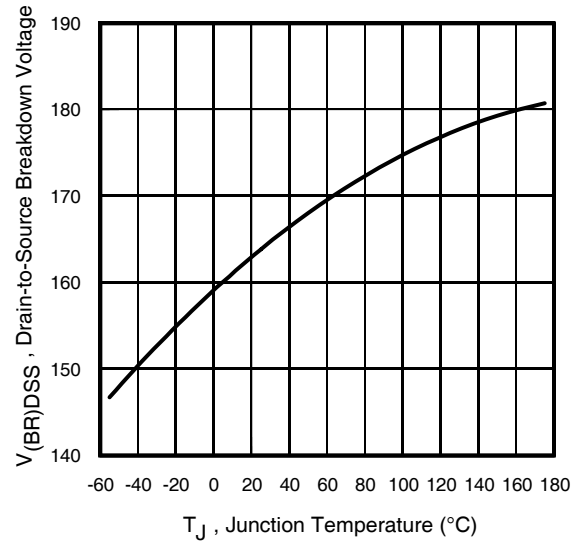


Fig 10. Drain-to-Source Breakdown Voltage

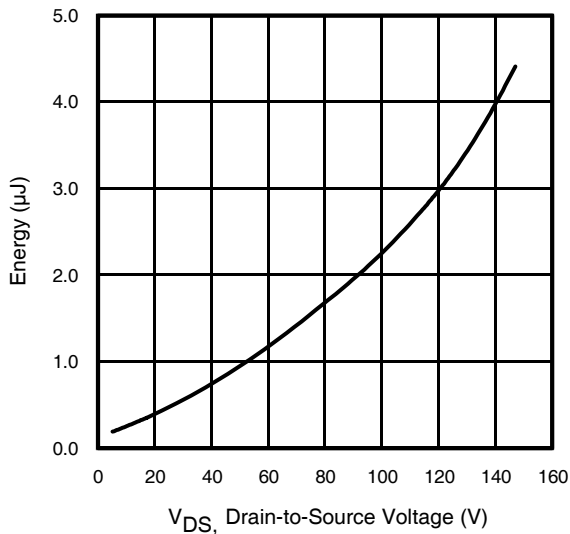


Fig 11. Typical C_{OSS} Stored Energy

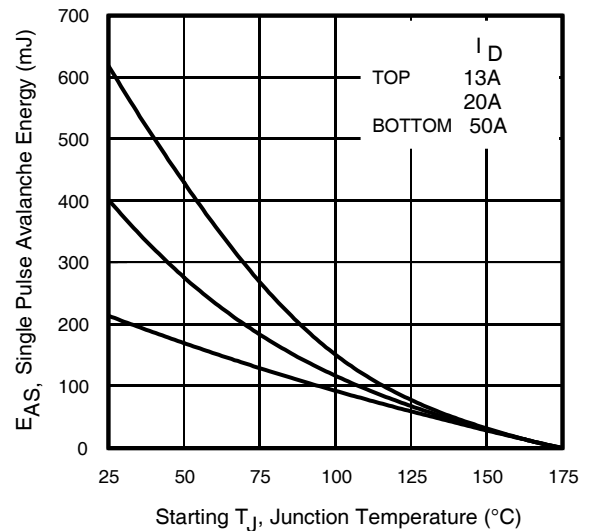


Fig 12. Maximum Avalanche Energy Vs. Drain Current
www.irf.com

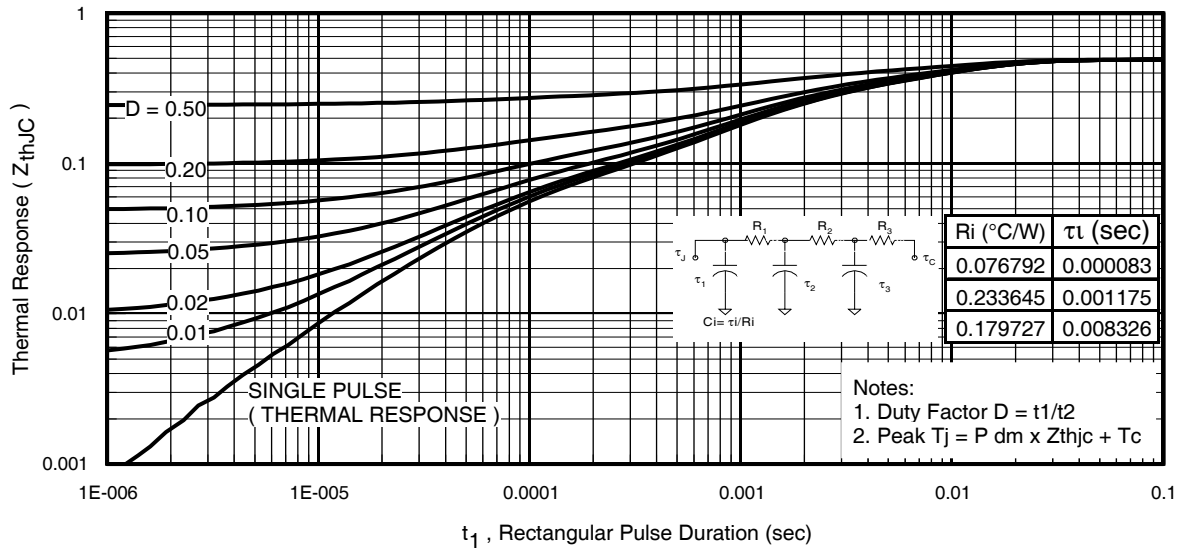


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

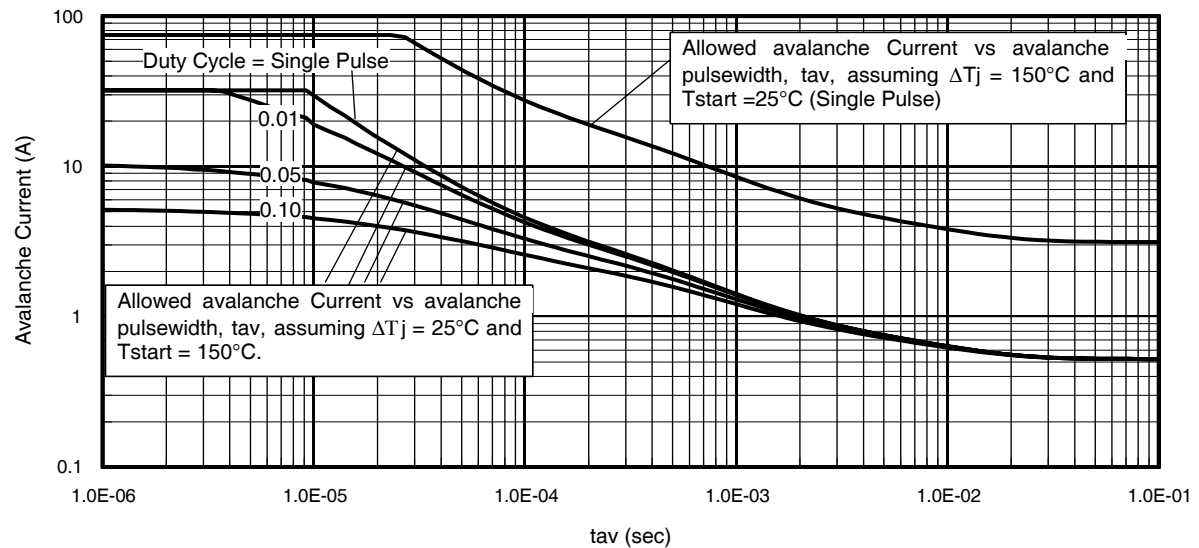


Fig 14. Typical Avalanche Current vs. Pulsewidth

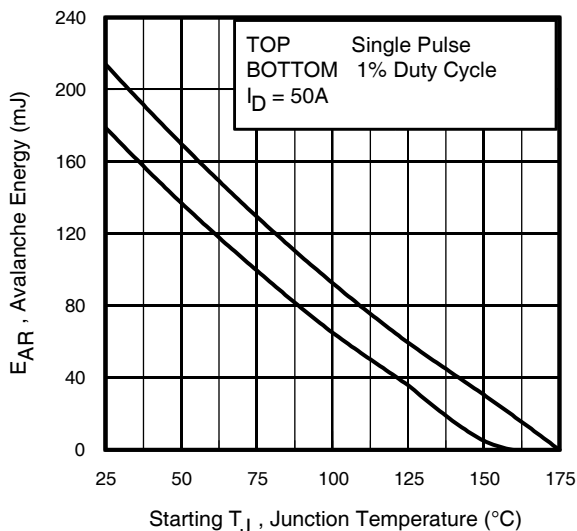


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

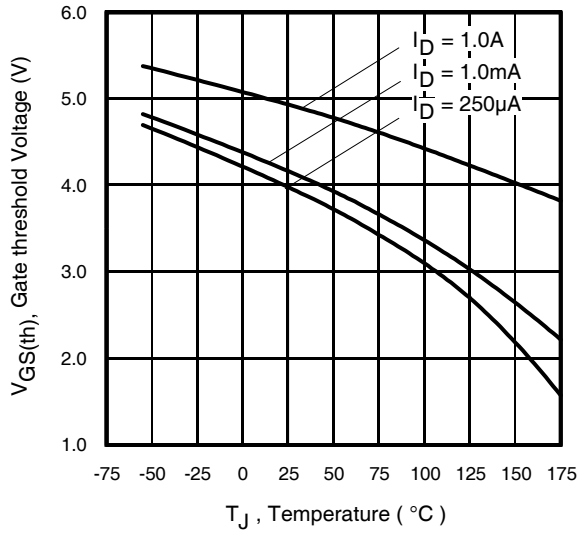


Fig 16. Threshold Voltage Vs. Temperature

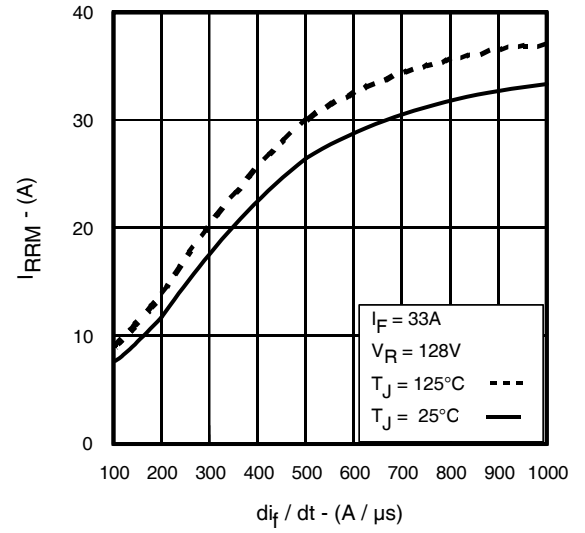


Fig. 17 - Typical Recovery Current vs. di_f/dt

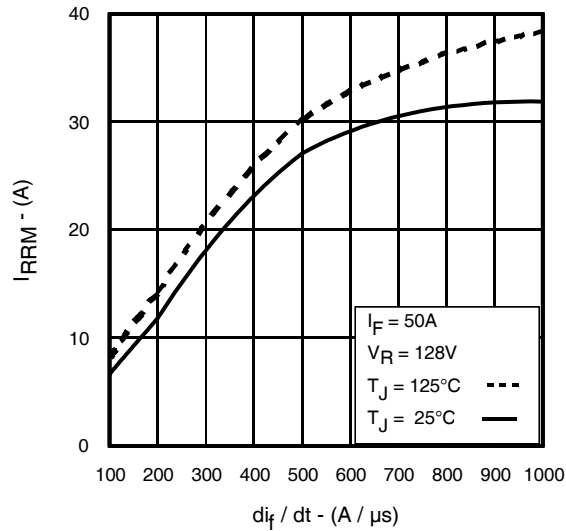


Fig. 18 - Typical Recovery Current vs. di_f/dt

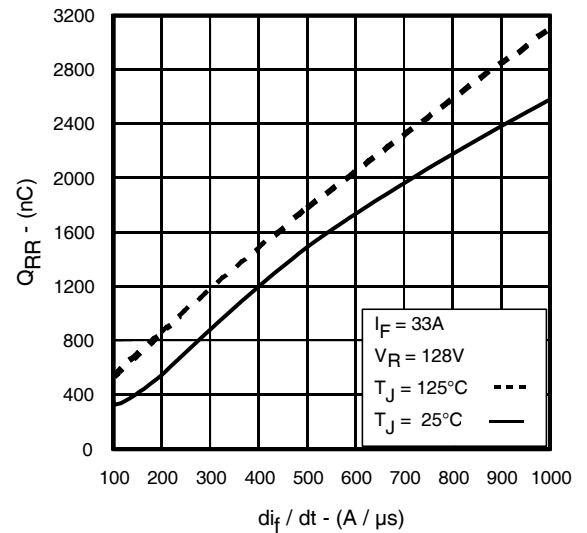


Fig. 19 - Typical Stored Charge vs. di_f/dt

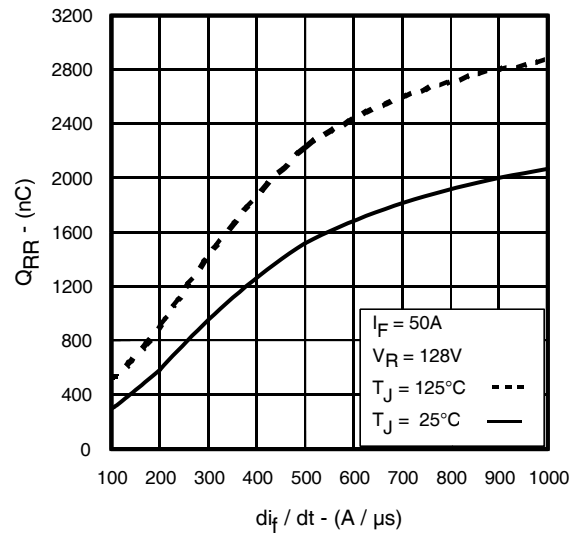
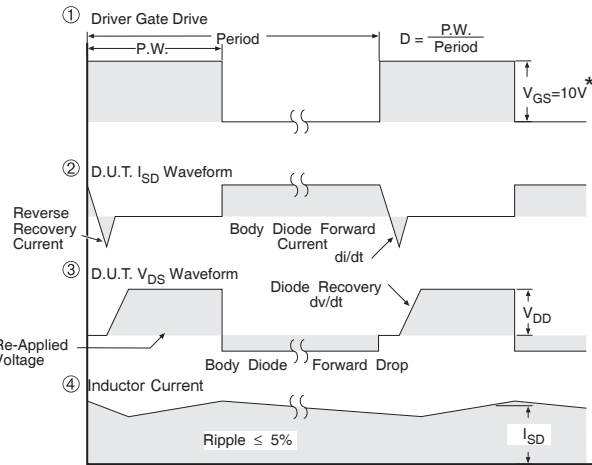
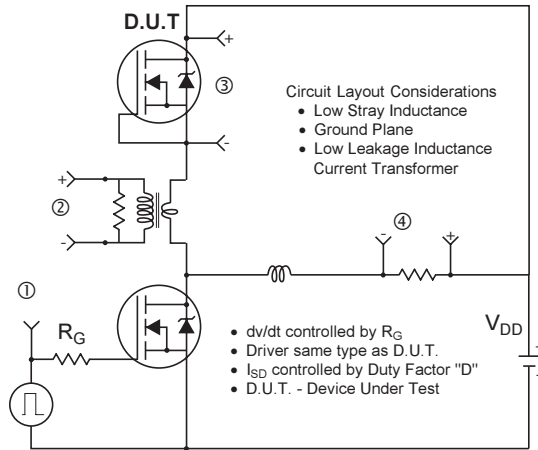


Fig. 20 - Typical Stored Charge vs. di_f/dt



* $V_{GS} = 5V$ for Logic Level Devices

Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

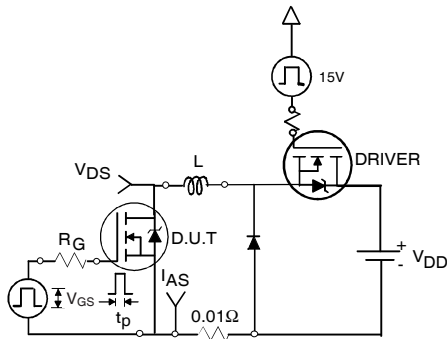


Fig 22a. Unclamped Inductive Test Circuit

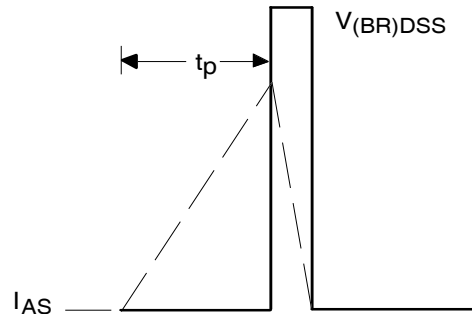


Fig 22b. Unclamped Inductive Waveforms

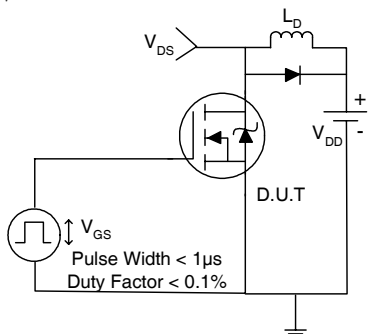


Fig 23a. Switching Time Test Circuit

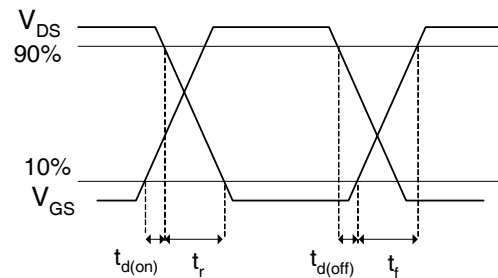


Fig 23b. Switching Time Waveforms

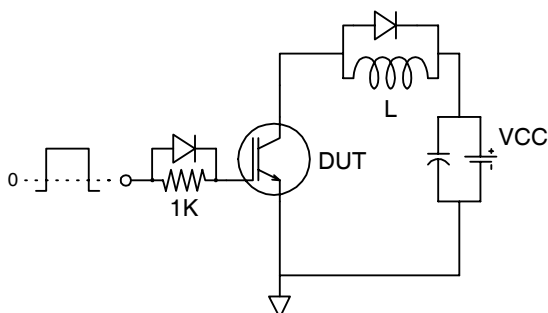


Fig 24a. Gate Charge Test Circuit

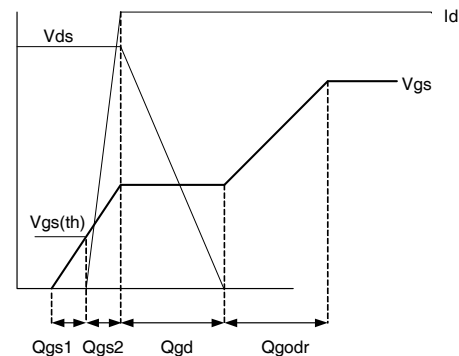


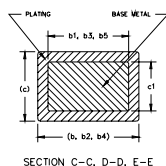
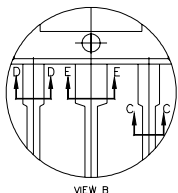
Fig 24b. Gate Charge Waveform

The figure consists of three main views of the probe assembly:

- Top View:** Shows the circular base with three probes labeled 1, 2, and 3. Dimensions include E (total width), A (probe diameter), Q (height from base to probe tip), L1 (height from base to probe body), L (total height), D (diameter of the central hole), and various mounting dimensions like 2x b2, b4, 2x b, and 3x b. A feature control frame indicates surface texture: $\sqrt{0.10} \text{ Ra}$. Section lines A-A are shown.
- Side View:** Shows the profile of the probe assembly with dimensions A (width), A2 (top flange width), B (height of the main body), and C (height of the base).
- Cross-sectional View (A-A):** Shows the internal structure of the probe assembly, including the LEAD TIP, THERMAL PAD, and various layers. Dimensions include S1 (thickness of the thermal pad), S2 (thickness of the lead tip), D1 (inner diameter), D2 (outer diameter), and E1 (base thickness). A feature control frame indicates surface texture: $\sqrt{0.10} \text{ Ra}$.

- | SYMBOL | DIMENSIONS | | | | NOTES |
|--------|------------|------|-------------|-------|-------|
| | INCHES | | MILLIMETERS | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | .183 | .209 | 4.65 | 5.31 | |
| A1 | .087 | .102 | 2.21 | 2.59 | |
| A2 | .059 | .098 | 1.50 | 2.49 | |
| b | .039 | .055 | 0.99 | 1.40 | |
| b1 | .039 | .053 | 0.99 | 1.35 | |
| b2 | .065 | .094 | 1.65 | 2.39 | |
| b3 | .065 | .092 | 1.65 | 2.34 | |
| b4 | .102 | .135 | 2.59 | 3.43 | |
| b5 | .102 | .133 | 2.59 | 3.38 | |
| c | .015 | .035 | 0.38 | 0.89 | |
| c1 | .015 | .033 | 0.38 | 0.84 | |
| D | .776 | .815 | 19.71 | 20.70 | 4 |
| D1 | .515 | — | 13.08 | — | 5 |
| D2 | .020 | .053 | 0.51 | 1.35 | |
| E | .602 | .625 | 15.29 | 15.87 | 4 |
| E1 | .530 | — | 13.46 | — | |
| E2 | .178 | .216 | 4.52 | 5.49 | |
| e | .215 BSC | | 5.46 BSC | | |
| øk | .010 | | 0.25 | | |
| L | .559 | .634 | 14.20 | 16.10 | |
| L1 | .146 | .169 | 3.71 | 4.29 | |
| øP | .140 | .144 | 3.56 | 3.66 | |
| øP1 | — | .291 | — | 7.39 | |
| Q | .209 | .224 | 5.31 | 5.69 | |
| S | .217 BSC | | 5.51 BSC | | |

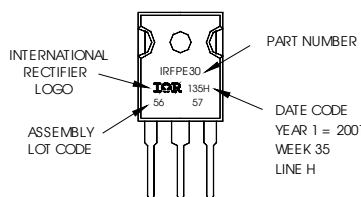
- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE



TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105

TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information. 06/06

www.irf.com

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>