MachXO Mini Development Kit

Easy-to-Use Low-Cost Platform for Designing With MachXO PLDs

The MachXO™ Mini Development Kit is an easy-to-use, low-cost platform for evaluating and designing with MachXO PLDs. The kit is based on a small form factor evaluation board that features the MachXO LCMXO2280 device.

Speed Time-to-Market with Mini SoC Design

To get started quickly, the board comes with the MachXO PLD pre-programmed with a miniature system-on-chip (Mini SoC) design that integrates multiple Lattice reference designs including the LatticeMico8™ (LM8) microcontroller, WISHBONE interconnect, and peripheral controllers for on-board SPI, SRAM, and I²C. The board can be controlled with switches and a menu-driven interface via a Windows or Linux terminal program over an RS-232/USB link.

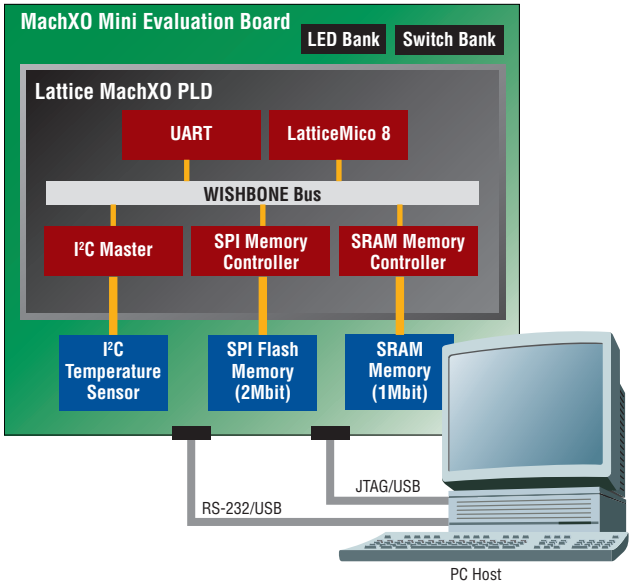
After running the Mini SoC demo on the board, you can easily access the reference design source code including the HDL, firmware, and design tools required to quickly modify it for your own application. For more information, go to www.latticesemi.com/ip

I²C and SPI Protocol Interface Support

An on-board I²C bus connects the MachXO PLD to an I²C temperature sensor. The Mini SoC demo uses the LM8 to sample the sensor over time, log the results to the on-board SRAM, and display the results on the LED array or terminal interface running on a PC via a RS-232/USB link.

An on-board SPI bus is also provided that connects the MachXO PLD to a 2Mbit non-volatile SPI Flash memory. The Mini SoC demo uses the LM8 to control transactions between the SRAM and SPI Flash memories.

MachXO Mini Eval Board Block Diagram



Key Features

- MachXO Device (LCMXO2280C-4TN144C)
- 2Mbit SPI Flash Memory
- 1Mbit SRAM
- I²C Temperature Sensor
- Programmed via Standard USB Cable
- RS-232/USB Interface
- JTAG/USB Interface
- 2x16 Expansion Header
- Push-buttons for Sleep Mode and Reset
- 4-bit DIP Switch
- Delta-Sigma ADC/DAC Circuits
- 8 Status LEDs
- QuickSTART Guide
- Marked for CE, China RoHS Environment-Friendly Use Period (EFUP) and Waste Electrical and Electronic Equipment (WEEE) Directives

Ordering Information

Product	Description	Ordering Part #
MachXO Mini Development Kit	MachXO Mini Evaluation Board with LCMXO2280C-4T144C device, USB cables, QuickSTART Guide, and demonstration design	LCMXO2280C-M-EVN

Flexible I/O Evaluation

Measure the drive strength, speed, and switching characteristics of the MachXO PLD I/Os, configured to the specification you program. The top and right banks of the I/O ring are available at the on-board header.

Low-Power Sleep Mode

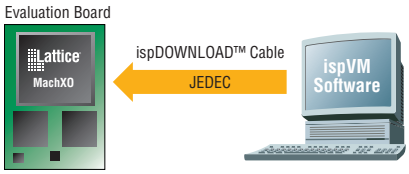
The MachXO PLD sleep mode feature allows standby current to be reduced dramatically during periods of system inactivity. A simple "self-wake" circuit of the evaluation board demonstrates how the sleep mode pin (SLEEPN) can be managed.

Transparent Field Reconfiguration (TransFR™)

Lattice's TransFR technology feature enables the MachXO PLD to be re-programmed without significant system interruption.

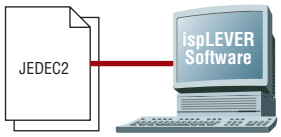
STEP 1

Program the MachXO PLD on the evaluation board with the sample program (JEDEC file) using the ispVM™ System software and the USB cable.



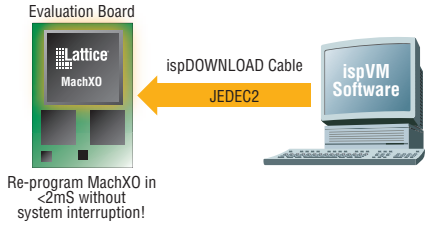
STEP 2

Use the free ispLEVER® Starter tools to modify the sample program (e.g. reverse the counter), and generate a second, modified JEDEC programming file (JEDEC2).



STEP 3

With the USB cable still attached, use ispVM System software to perform a TransFR operation to the MachXO PLD, programming the Flash Block on the MachXO PLD with the modified JEDEC file, while the PLD operates. The new program can then be loaded to the SRAM with convenient, for seamless function changeover.



Additional Information

Documentation including reference design source, sub-system descriptions, and schematics are available at www.latticesemi.com/machxo-mini.

ispLEVER Starter Development Tools FREE

Lattice's free ispLEVER development tools offer a comprehensive design environment for the MachXO architecture. The ispLEVER tools include everything you need for design entry, synthesis, map, place & route, I/O planning, simulation, project management, device programming and more. Synthesis and simulation tools from industry leaders Aldec® and Synopsys® are included with ispLEVER.

Download ispLEVER Starter at: www.latticesemi.com/products/designsoftware/isplever/ispleverstarter.

Reference Design Portfolio

Lattice offers an expanding portfolio of IP cores and reference designs targeted for low-density applications. Optimized for the MachXO architecture, available reference designs include popular protocol and connectivity standards such as I^2C, SPI, UART and PCI. The reference designs, source codes and documentation can be downloaded for free from the Lattice website. For more information, go to www.latticesemi.com/ip.

Applications Support
1-800-LATTICE (528-8423)
(503) 268-8001
techsupport@latticesemi.com

www.latticesemi.com

Copyright © 2009 Lattice Semiconductor Corporation. Lattice Semiconductor, L (stylized) Lattice Semiconductor Corp., and Lattice (design), ispDOWNLOAD, ispLEVER, ispVM, LatticeMico8, MachXO, and TransFR are either registered trademarks or trademarks of Lattice Semiconductor Corporation in the United States and/or other countries. Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

February 2009
Order #: I0199