

LTC6820

isoSPI 2-Wire Serial Interface

DESCRIPTION

Demonstration circuit 1941 is an isoSPI™ transceiver board, based on Linear Technology's LTC®6820. The LTC6820 provides a method of interconnecting standard serial peripheral interface (SPI) devices using a single twisted pair connection. This proprietary 2-wire interface is called isoSPI. The LTC6820 encodes SPI signals, up to 1Mbps, into a differential isoSPI signal which is transmitted via a simple pulse transformer through a twisted pair. At the other end of the twisted pair, the isoSPI signal can be translated back to SPI (using another LTC6820).

Another option would be for the isoSPI to connect to a Linear Technology device with a built-in isoSPI interface, such as the LTC6804.

Typically, the LTC6820 will be used in one of two ways: See Figures 1 and 2.

Design files for this circuit board are available at <http://www.linear.com/demo/DC1941D>

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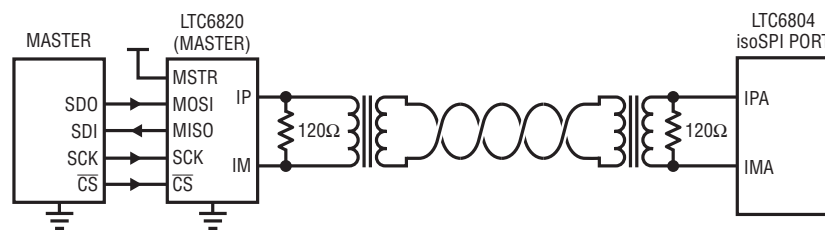


Figure 1. A Single LTC6820 Used to Translate an isoSPI Signal into SPI*

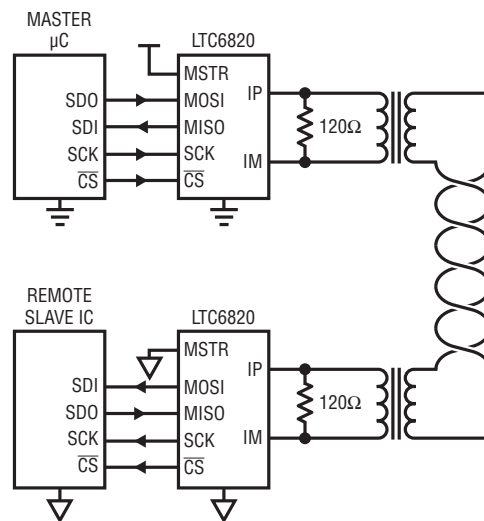


Figure 2. Two LTC6820 Devices Used to Translate SPI into isoSPI for Long Distance, Isolated Communications

* The isoSPI interface is built into numerous Linear Technology products.

OVERVIEW

The DC1941 enables isoSPI connection using the LTC6820. As a reference circuit, its combination of galvanic isolation, common mode filtering, and jumper options enables prototyping of typical applications that employ the LTC6820. This board provides the foundation for translation between SPI and isoSPI signals. The SPI Bus is a synchronous serial data link that uses four single-ended signals to transmit information over short distances (typically on a single PCB). SPI devices communicate in master/slave mode, where the master device initiates the data frame and multiple slave devices are allowed. Because the LTC6820 includes a Master and a Slave mode, LTC6820-based conversion between SPI and isoSPI can occur at the beginning, or upstream in an isoSPI connection.

Figure 1 shows a typical example with a LTC6820 connected in Master mode. In this example, a DC1941 connects the SPI port of a microcontroller to an isoSPI-based slave device (such as Linear Technology's LTC6804). In Figure 2, two DC1941s can be used to translate an end-to-end bidirectional SPI interface into an isoSPI interface. One DC1941 uses Master mode; the other, Slave mode. This configuration allows the outermost SPI devices to be galvanically isolated, and enables long distance, noise immune communication.

The 2-wire isoSPI interface is accessible using standard RJ45 connectors (J1 on the DC1941). Standard RJ45 connectors allow the use of simple CAT5 cable¹ to interconnect isoSPI ports. Other Linear Technology demo

boards with isoSPI also use RJ45 connectors for simple interconnection. The LTC6820's four SPI signals are accessible via J2 (14-pin ribbon connector) or JP1 (6-pin header connector).

The SPI signal can be also translated to a USB signal for a connection to a PC using Linear Technology's DC2026 (Linduino Interface). The Linduino is connected to the DC1941 through J2.

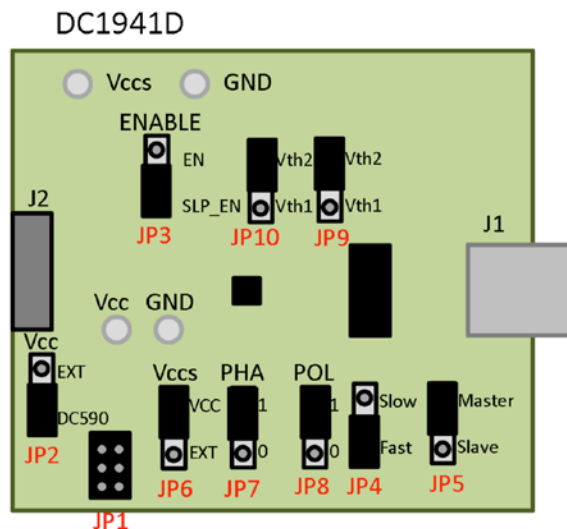
Power to the DC1941 can be supplied via the SPI connection (J2, JP1) or the turrets on the board. Typically, the most convenient method to provide power is to connect J2, through a 14 pin ribbon cable, to a DC2026 Linduino board. The Linduino DC2026 sends power on pin 2 of this connector; it can be 2.5, 3.3, or 5V depending on a jumper on the DC2026. Whichever voltage is chosen on the DC2026 will be available at pin 2 of J2, assuming ribbon cable connection.

That said, the DC1941 board, with its LTC6820, does not require connection to a DC2026. Power can be provided directly to the DC1941 at turrets from an external source. In addition, because the VCC and VCCS pins of the LTC6820 do not need to be coupled, one can bring in two distinct supplies to the DC1941 board. Such a configuration might be needed if the I/O voltage of the SPI signals differs from the nominal supply voltage of the LTC6820.

¹ A single twisted pair inside the CAT5 is used for the isoSPI interconnection.

JUMPERS

Jumper settings are provided on the DC1941 to configure the SPI mode, speed and master/slave operation. Jumpers are also provided to configure the isoSPI shutdown and output power level, as well as power supply options.



dc1941dfb

JUMPERS

JP2 – VCC to EXT/DC590:

EXT: Set to EXT if the DC1941 is powered from an external supply. In such a case, power is provided typically at the turrets on the board.

DC590B (DEFAULT): Set to DC590 if the DC1941 is powered through the 14-pin ribbon cable connector (J2 on the DC1941). The DC2026 connects to the DC1941 through this 14-pin ribbon cable.

JP3 – EN/SLP_EN:

EN: Set to have the LTC6820 always enabled.

SLP_EN (DEFAULT): When selected, the LTC6820 will enter shutdown after 4ms of inactivity and will require a wake up pulse.

JP4 – SLOW/FAST:

SLOW: Set for SPI clock frequencies of 100kHz or less.

FAST (DEFAULT): Set for SPI clock frequencies greater than 100kHz.

JP5 – MASTER/SLAVE:

The LTC6820 can sit at the start of an SPI connection when in Master mode. It can alternatively sit at the end of an isoSPI connection and talk to a slave SPI device when it is in Slave mode.

MASTER(DEFAULT): Configures the SPI for master mode; the LTC6820 will operate as the isoSPI master. When this jumper is set to 'master', the J2 connector should be connected to a SPI master.

SLAVE: Configures the SPI for slave mode; the LTC6820 will operate as an isoSPI slave. The DC1941 should be connected to a SPI slave device.

JP6 – VCCS to VCC/EXT:

VCC (DEFAULT): Sets the LTC6820 SPI input/output supply voltage (V_{CCS}) to V_{CC} , which sets the SPI logic levels to V_{CC} .

EXT: Allows the SPI input/output supply (V_{CCS}) to be connected to a separate voltage from V_{CC} , which allows the logic levels to be set to a different voltage. An external supply can be connected on the turret labeled V_{CCS} .

JP7,8 – PHA/POL:

POL indicates whether SCK idles high (1) or low (0). PHA indicates latching on the first edge (0) or the second edge (1).

These jumpers set the SPI mode per the following table.

Table 1

MODE	POL	PHA
0	0	0
1	0	1
2	1	0
3 (Default)	1	1

Set to mode 3 for use with LTC6804.

If POL = 0, SCK idles low. Data is latched on the rising (first) clock edge if PHA = 0 and on the falling (second) clock edge if PHA = 1.

If POL = 1, SCK idles high. Data is latched on the falling (first) clock edge if PHA = 0 and on the rising (second) clock edge if PHA = 1.

The two most common configurations are mode 0 (PHA = 0 and POL = 0) and mode 3 (PHA = 1 and POL = 1) because these modes latch data on a rising clock edge. For example, in the Default case of mode 3, SCK normally idles high; the first latching edge is the first rise after the reset to 0 out of idle.

JP9,10 – VTH1/VTH2:

VTH1: Sets the LTC6820 output drive to 1V, and the receiver input threshold to 500mV.

VTH2 (DEFAULT): Sets the LTC6820 output drive to 1V, and the receiver input threshold to 600mV. The VTH2 settings are compatible with other Linear Technology isoSPI-based demo boards.

SETUP: DC1941 TO isoSPI-BASED DEMO BOARD

A single Master mode DC1941 converts SPI to isoSPI.

1. Connect a USB port to DC2026.
2. Connect DC2026 14-pin connector to DC1941 14-pin connector (J2) with 14-wire ribbon.
3. The DC1941 must be in Master mode (JP5 = Master). It can take power from the DC2026 (JP2 = DC590).
4. Connect J1 of DC1941 to isoSPI-based demo board Port A using an Ethernet Patch Cable.
5. Check jumpers on all boards and adjust if necessary.
6. Refer to the Linduino demo manual for software instructions.

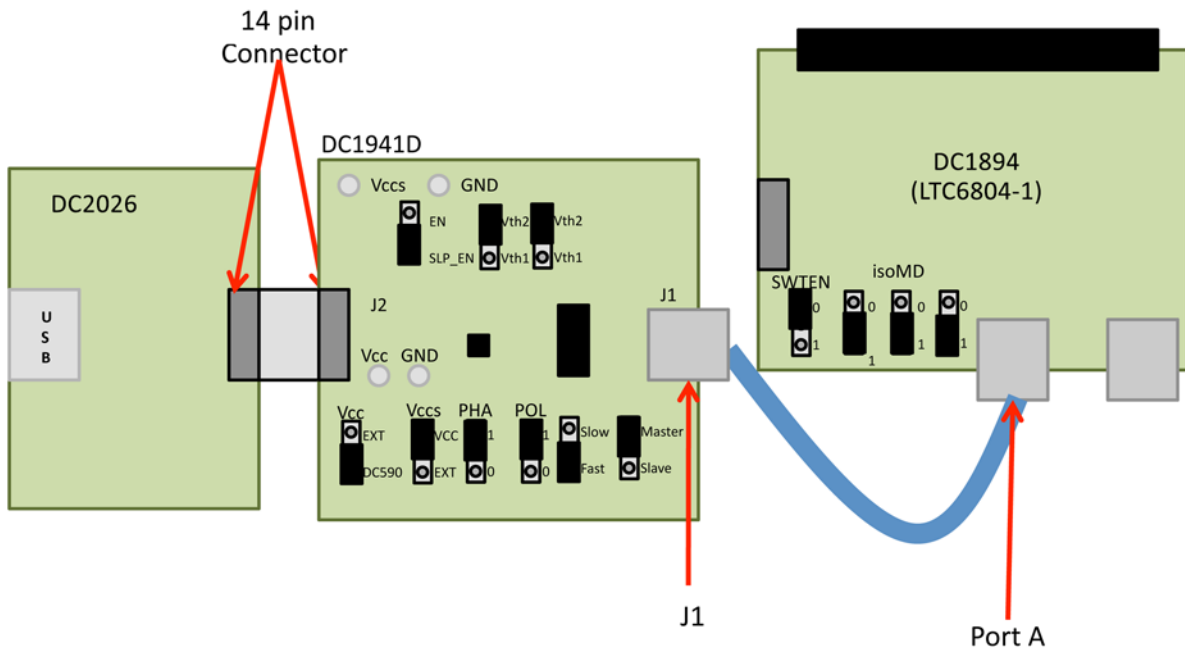


Figure 3. Hardware and Jumper Settings to an isoSPI-based Demo Board (Illustrated with the DC1894, LTC6804-1 Demo Board)

LTC6820 TO LTC6804 SETUP

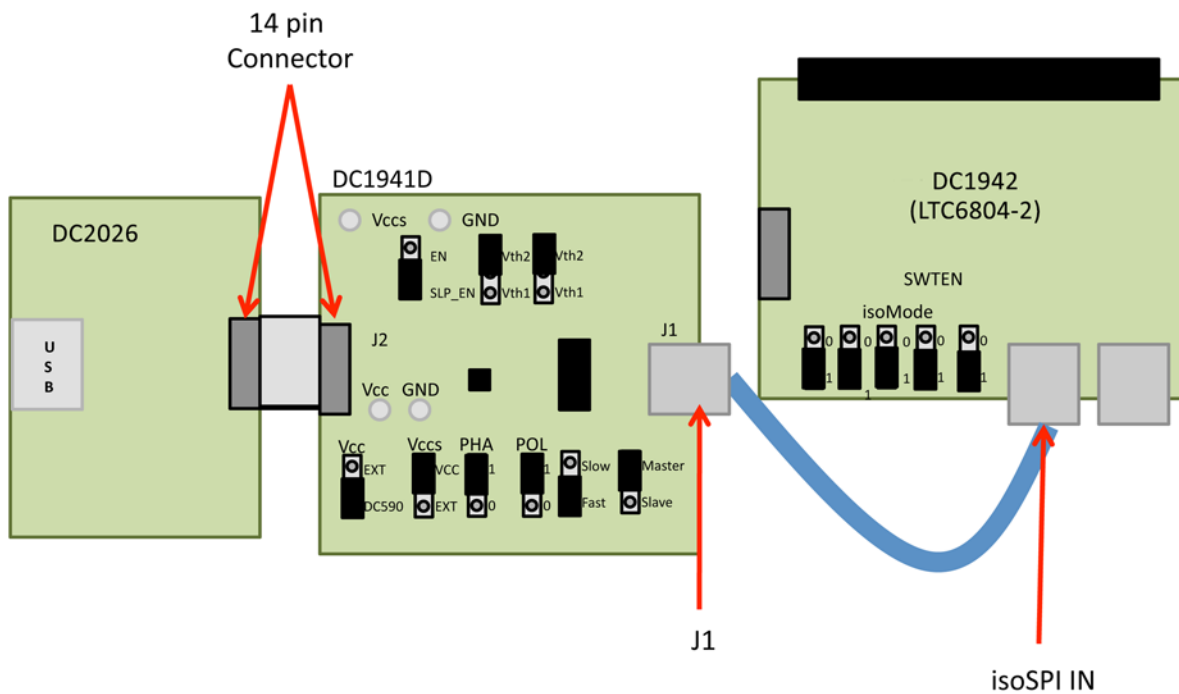


Figure 4. Hardware and Jumper Settings to an isoSPI-based Demo Board (Illustrated with the DC1942, LTC6804-2 Demo Board)

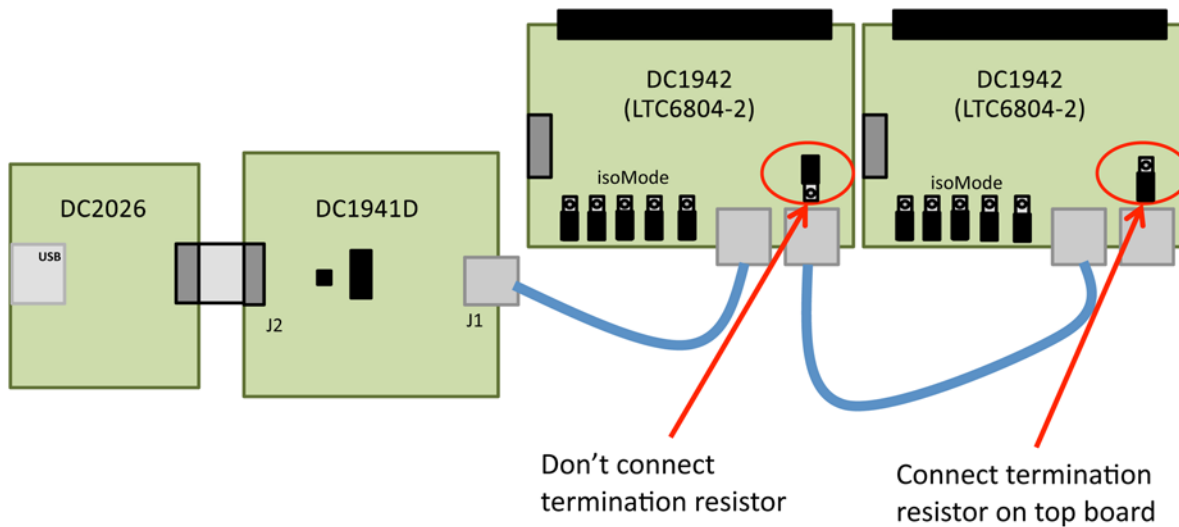


Figure 5. (Illustrated with Multiple DC1942, LTC6804-2 Demo Boards) Multidrop Example

SETUP: DC1941 TO DC1941 FOR SPI TO SPI WITH ISOLATION

The combination of one Master mode DC1941 and one Slave mode DC1941 enables SPI with isolation using isoSPI.

1. Connect a USB port to DC2026.
2. Connect DC2026 14-pin connector to DC1941 14-pin connector (J2) with 14-wire ribbon.
3. The DC1941 must be in Master mode (JP5 = Master). It can take power from the DC2026 (JP2 = DC590).
4. Connect J1 of DC1941 to J1 of a second DC1941 using an Ethernet Patch Cable.
5. This second DC1941 must be in Slave mode (JP5 = Slave). It can take power from an external supply (JP2 = EXT).
6. Connect the SPI of the second DC1941 board to a SPI slave device.

7. Check jumpers on all boards and adjust if necessary.
8. Refer to the Linduino Demo Manual for software instructions.

If the SPI-based slave board is a Linear Technology demo board, then it may have the same 14-pin connector. In this case, this demo board can connect to J2 of the second DC1941 board. Often engineers will use QuikEval™ software from Linear Technology when evaluating an SPI-based demo board. This paradigm remains unchanged when there is an isoSPI bridge between the DC2026 SPI port and the SPI-based demo board. QuikEval will operate normally; a host PC that interfaces with the DC2026 will not know anything about the isoSPI intermediary physical layer.

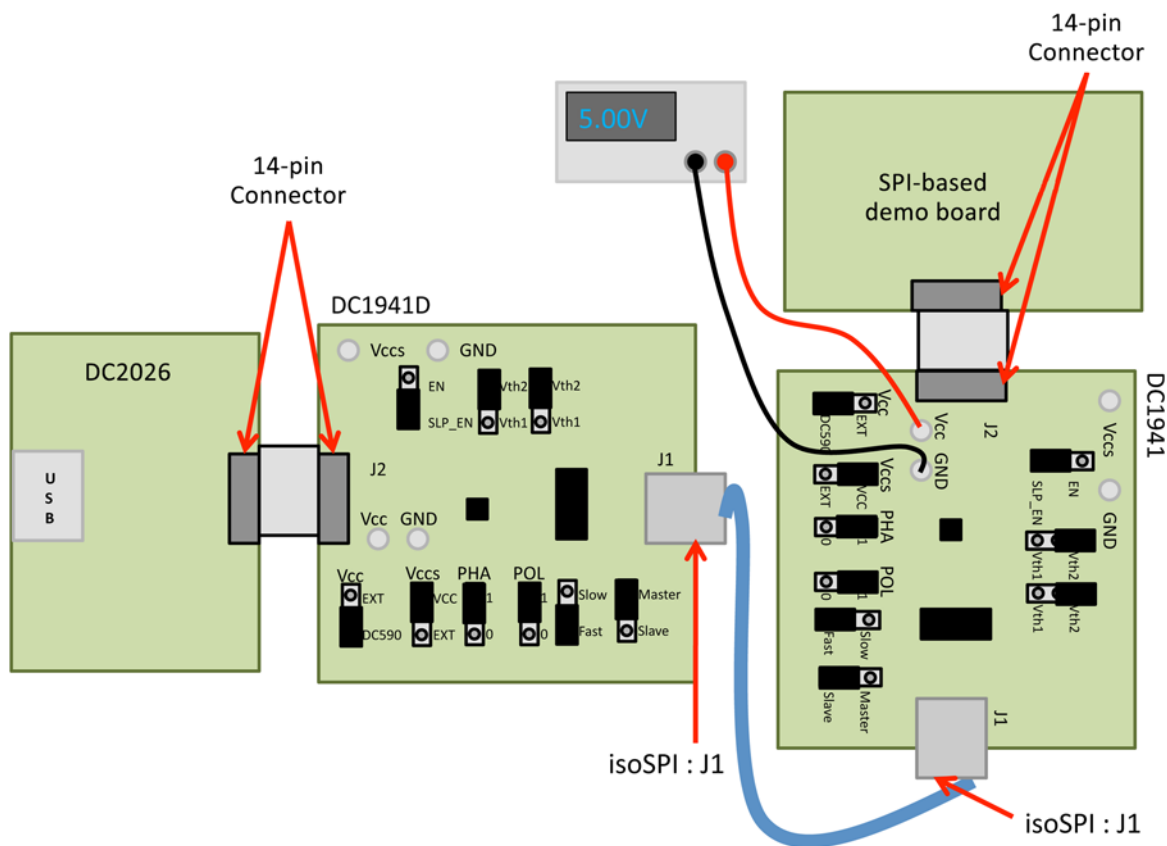
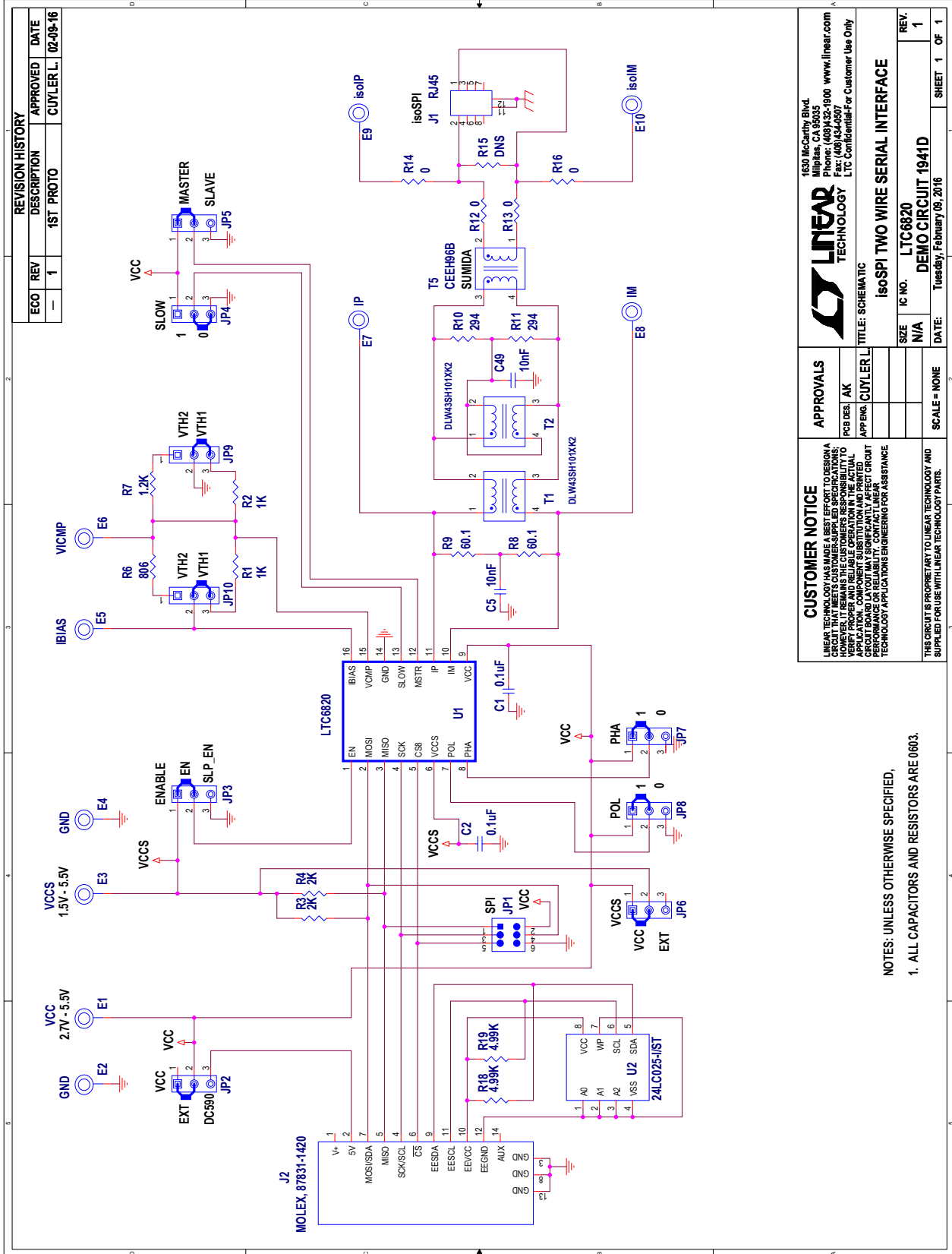


Figure 6. Hardware and Jumper Settings to Connect Two DC1941s and Add isoSPI Capability to a Standard SPI Slave

SCHEMATIC DIAGRAM



REVISION HISTORY		
ECO	REV	DESCRIPTION
—	1	1ST PROTO
		APPROVED DATE
		CUYLER L. 02-09-16

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TITLE: SCHEMATIC

IC NO. LTC6820

SIZE N/A

SCALE = NONE

ISO-SPI TWO WIRE SERIAL INTERFACE

REV. 1

DATE: Tuesday, February 09, 2016

SHEET 1 OF 1

NOTES: UNLESS OTHERWISE SPECIFIED,
1. ALL CAPACITORS AND RESISTORS ARE 0603.

DEMO MANUAL DC1941D

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