Short Form Data Sheet
June 2012

MAX24405, MAX24410
5 or 10 Output Any-Rate Clock Multipliers

General Description

The MAX24405 and MAX24410 are flexible, high-performance clock multiplier/synthesizer ICs with two independent APLLs. Each APLL performs any-to-any frequency conversion. From any input clock frequency 9.72MHz to 750MHz these devices can produce frequency-locked APLL output frequencies up to 750MHz and as many as 10 differential output clock signals that are integer divisors of the APLL frequencies. Output jitter is typically 0.35 to 0.5ps RMS (12kHz to 20MHz) on all outputs and can be as low as 0.24ps RMS. Each device can configure itself from an external EEPROM so that clock signals are available immediately after power-up or reset.

Applications

Frequency Conversion and Synthesis Applications in a Wide Variety of Equipment Types

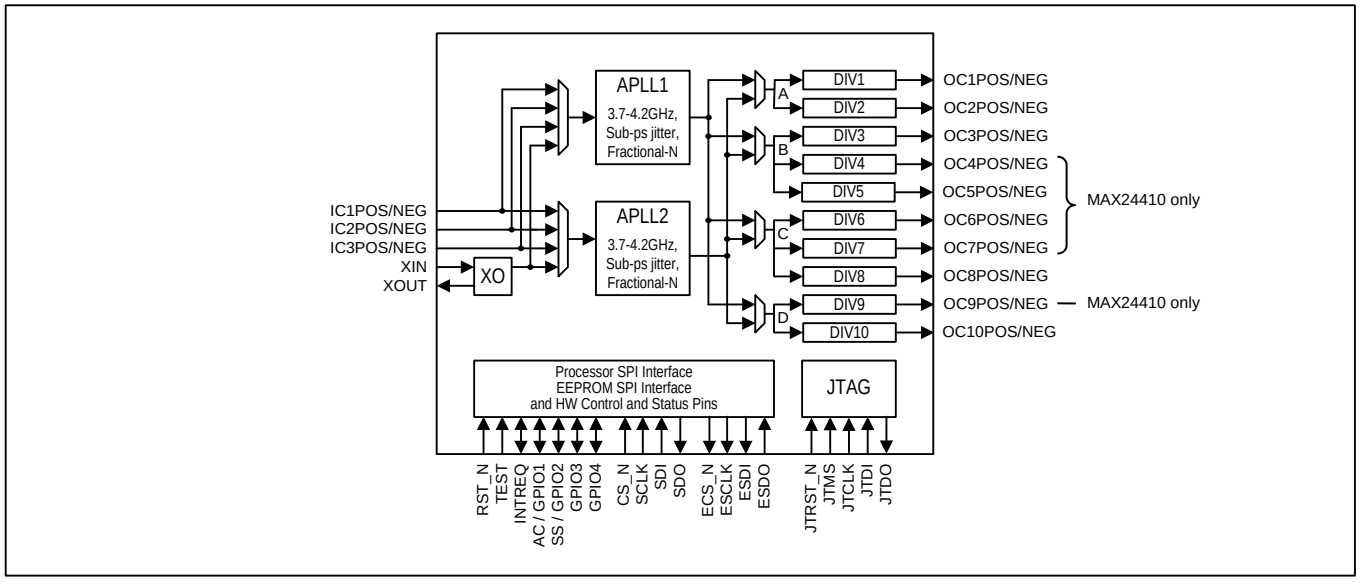
Ordering Information

PART	OUTPUTS	PIN-PACKAGE
MAX24405EXG+	5	81-CSBGA (10mm)^2
MAX24410EXG+	10	81-CSBGA (10mm)^2

Features

- **Input Clocks**
  - One Crystal or CMOS Input
  - Three Differential or CMOS Inputs
  - Differential to 750MHz, CMOS to 125MHz
  - Clock Selection By Pin or Register Control
- **Two APLLs Plus 5 or 10 Output Clocks**
  - APLLs Perform High Resolution Fractional-N Clock Multiplication
  - Any Output Frequency from <1Hz to 750MHz
  - Each Output Has an Independent Divider
  - Output Jitter 0.35 to 0.5ps RMS Typical on All Outputs, Can Be As Low As 0.24ps RMS
  - Outputs are CML or 2xCMOS, Can Interface to LVDS, LVPECL, HSTL, SSTL and HCSL
  - CMOS Output Voltage from 1.5V to 3.3V
- **General Features**
  - Automatic Self-Configuration at Power-Up from External EEPROM Memory
  - SPI™ Processor Interface
  - 1.8V + 3.3V Operation (5V Tolerant)
  - -40 to +85°C Operating Temp. Range

Block Diagram



1. Application Examples

Figure 1-1. Asynchronous Ethernet Clocks

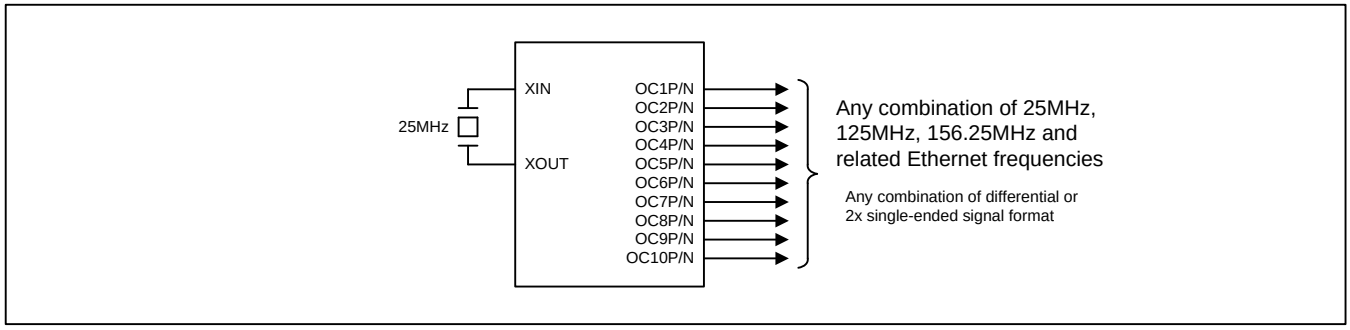
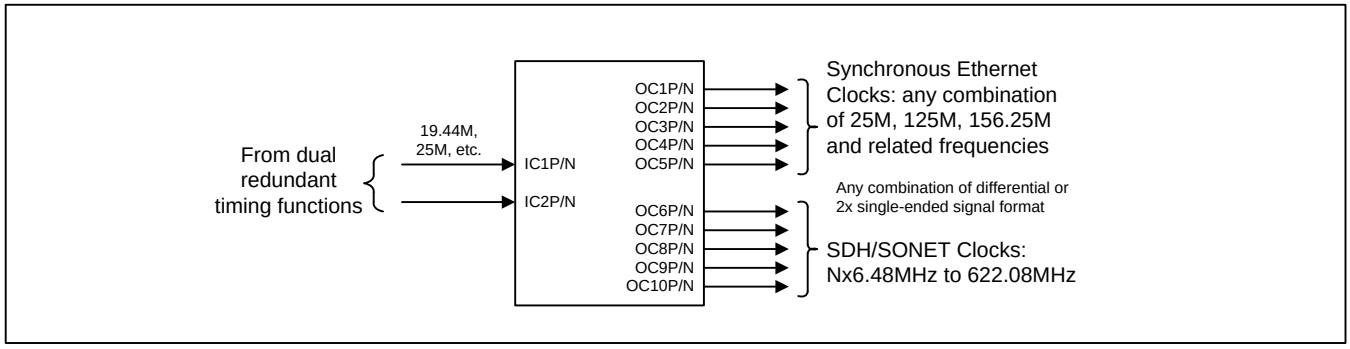


Figure 1-2. Synchronous Ethernet and SDH/SONET Line Card



2. Detailed Features

2.1 APLL Features

- Two independent APLLs
- Very high-resolution fractional scaling (i.e. non-integer multiplication)
- Output jitter is typically 0.35 to 0.5ps RMS and can be as low as 0.24ps RMS (12kHz to 20MHz)
- Telecom output frequencies include 622.08MHz for SONET/SDH and 625MHz for Synchronous Ethernet
- Bypass mode for each APLL supports system testing and allows the devices to be used in fanout applications

2.2 Output Clock Features

- Up to five (MAX24405) or ten (MAX24410) low-jitter output clocks
- Each output can be one differential output or two CMOS/TTL outputs
- Outputs easily interface with CML, LVDS, LVPECL, HSTL, SSTL, HCSL components
- Each output can be any integer divisor of an APLL output clock
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can also produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Per-output delay adjustment
- Per-output enable/disable

2.3 General Features

- SPI serial microprocessor interface
- Optional automatic self-configuration at power-up from external EEPROM memory
- Four general-purpose I/O pins
- Register set can be write-protected
- Internal compensation for local oscillator frequency error

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