11-/14-Bit, 2.5 GSPS, RF Digital-to-Analog Converters

Data Sheet **AD9737A/AD9739A**

FEATURES

- Direct RF synthesis at 2.5 GSPS update rate
  - DC to 1.25 GHz in baseband mode
  - 1.25 GHz to 3.0 GHz in mix-mode
- Industry leading single/multicarrier IF or RF synthesis
- Dual-port LVDS data interface
  - Up to 1.25 GSPS operation
  - Source synchronous DDR clocking
- Pin compatible with the AD9739
- Programmable output current: 8.7 mA to 31.7 mA
- Low power: 1.1 W at 2.5 GSPS

APPLICATIONS

- Broadband communications systems
  - DOCSIS CMTS systems
- Military jammers
- Instrumentation, automatic test equipment
- Radar, avionics

FUNCTIONAL BLOCK DIAGRAM

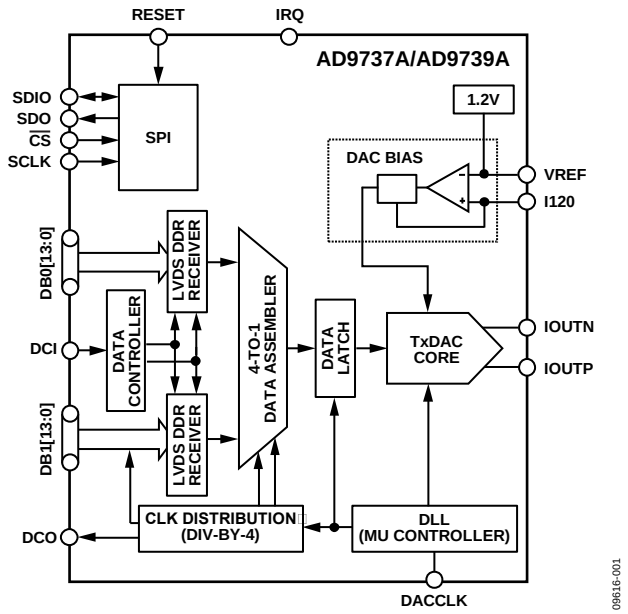

Figure 1.

GENERAL DESCRIPTION

The AD9737A/AD9739A are 11-bit and 14-bit, 2.5 GSPS high performance RF DACs that are capable of synthesizing wideband signals from dc up to 3 GHz. The AD9737A/AD9739A are pin and functionally compatible with the AD9739 with the exception that the AD9737A/AD9739A do not support synchronization or RZ mode, and are specified to operate between 1.6 GSPS and 2.5 GSPS.

By elimination of the synchronization circuitry, some nonideal artifacts such as images and discrete clock spurs remain stationary on the AD9737A/AD9739A between power-up cycles, thus allowing for possible system calibration. AC linearity and noise performance remain the same between the AD9739 and the AD9737A/AD9739A.

The inclusion of on-chip controllers simplifies system integration. A dual-port, source synchronous, LVDS interface simplifies the digital interface with existing FGPA/ASIC technology. On-chip controllers are used to manage external and internal clock domain variations over temperature to ensure reliable data transfer from the host to the DAC core. A serial peripheral interface (SPI) is used for device configuration as well as readback of status registers.

The AD9737A/AD9739A are manufactured on a 0.18 µm CMOS process and operate from 1.8 V and 3.3 V supplies. They are supplied in a 160-ball chip scale ball grid array for reduced package parasitics.

PRODUCT HIGHLIGHTS

1. Ability to synthesize high quality wideband signals with bandwidths of up to 1.25 GHz in the first or second Nyquist zone.
2. A proprietary quad-switch DAC architecture provides exceptional ac linearity performance while enabling mix-mode operation.
3. A dual-port, double data rate, LVDS interface supports the maximum conversion rate of 2500 MSPS.
4. On-chip controllers manage external and internal clock domain skews.
5. Programmable differential current output with an 8.66 mA to 31.66 mA range.

Rev. D
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REVISION HISTORY

6/2017—Rev. C to Rev. D

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Changes to Clock Input Considerations Section 56

2/2012—Rev. B to Rev. C

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2/2012—Rev. A to Rev. B

Added AD9737A ..... Universal
Reorganized Layout ..... Universal
Moved Revision History Section 3
Deleted ±6% from Table Summary Statement; Changes to Table 1 4
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Added Figure 5, Renumbered Sequentially 9
Added Figure 7 and Table 7, Renumbered Sequentially 10
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Added Static Linearity Section and Figure 78 to Figure 88 26
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Added SPI Port Configuration and Software Reset Section, Power-Down LVDS Interface and TxDAC Section, Controller Clock Disable Section, and Table 11 to Table 13 43
Added Interrupt Request (IRQ) Enable/Status Section, TxDAC Full-Scale Current Setting (I_{OUTFS}) and Sleep Section, TxDAC Quad-Switch Mode of Operation Section, DCI Phase Alignment Status Section, Data Receiver Controller Configuration Section, and Table 14 to Table 18 44
Added Data Receiver Controller_Data Sample Delay Value Section, Data Receiver Controller_DCI Delay Value/Window and Phase Rotation Section, Data Receiver Controller_Delay Line Status Section, Data Receiver Controller Lock/Tracking Status Section, and Table 19 to Table 22 45
Added CLK Input Common Mode Section, and Mu Controller Configuration and Status Section, and Table 23 and Table 24 46
Added Part ID Section, and Table 25 47
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Added Figure 167 and Table 27, Changes to Mu Controller Initialization Description Section 53
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7/2011—Rev. 0 to Rev. A

Changed Maximum Update Rate (DACCLK Input) Parameter to DAC Clock Rate Parameter in Table 4 6
Added Adjusted DAC Update Rate Parameter and Endnote 1 in Table 4 6
Updated Outline Dimensions 43

1/2011—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA.

Table 1.

	AD9737A			AD9739A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION		11			14		Bits
ACCURACY							
Integral Nonlinearity (INL)		±0.5			±2.5		LSB
Differential Nonlinearity (DNL)		±0.5			±2.0		LSB
ANALOG OUTPUTS							
Gain Error (with Internal Reference)		5.5			5.5		%
Full-Scale Output Current	8.66	20.2	31.66	8.66	20.2	31.66	mA
Output Compliance Range	−1.0		+1.0	−1.0		+1.0	V
Common-Mode Output Resistance		10			10		MΩ
Differential Output Resistance		70			70		Ω
Output Capacitance		1			1		pF
DAC CLOCK INPUT (DACCLK_P, DACCLK_N)							
Differential Peak-to-Peak Voltage	1.2	1.6	2.0	1.2	1.6	2.0	V
Common-Mode Voltage		900			900		mV
Clock Rate	1.6		2.5	1.6		2.5	GHz
TEMPERATURE DRIFT							
Gain		60			60		ppm/°C
Reference Voltage		20			20		ppm/°C
REFERENCE							
Internal Reference Voltage	1.15	1.2	1.25	1.15	1.2	1.25	V
Output Resistance		5			5		kΩ
ANALOG SUPPLY VOLTAGES							
VDDA	3.1	3.3	3.5	3.1	3.3	3.5	V
VDDC	1.70	1.8	1.90	1.70	1.8	1.90	V
DIGITAL SUPPLY VOLTAGES							
VDD33	3.10	3.3	3.5	3.10	3.3	3.5	V
VDD	1.70	1.8	1.90	1.70	1.8	1.90	V
SUPPLY CURRENTS AND POWER DISSIPATION, 2.0 GSPS							
I_{VDDA}		37	38		37	38	mA
I_{VDDC}		158	167		158	167	mA
I_{VDD33}		14.5	16		14.5	16	mA
I_{VDD}		173	183		173	183	mA
Power Dissipation		0.770			0.770		W
Sleep Mode, I_{VDDA}		2.5	2.75		2.5	2.75	mA
Power-Down Mode (All Power-Down Bits Set in Register 0x01 and Register 0x02)							
I_{VDDA}		0.02			0.02		mA
I_{VDDC}		6			6		mA
I_{VDD33}		0.6			0.6		mA
I_{VDD}		0.1			0.1		mA
SUPPLY CURRENTS AND POWER DISSIPATION, 2.5 GSPS							
I_{VDDC}		223			223		mA
I_{VDD33}		14.5			14.5		mA
I_{VDD}		215			215		mA
Power Dissipation		0.960			0.960		mW

LVDS DIGITAL SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA. LVDS drivers and receivers are compliant to the IEEE Standard 1596.3-1996 reduced range link, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
LVDS DATA INPUTS (DB0[13:0], DB1[13:0])[1]				
Input Common-Mode Voltage Range, V_{COM}	825		1575	mV
Logic High Differential Input Threshold, V_{IH_DTH}	175	400		mV
Logic Low Differential Input Threshold, V_{IL_DTH}	−175	−400		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
LVDS Input Rate	1250			MSPS
LVDS Minimum Data Valid Period (t_{MDE}) (See Figure 159)			344	ps
LVDS CLOCK INPUT (DCI)[2]				
Input Common-Mode Voltage Range, V_{COM}	825		1575	mV
Logic High Differential Input Threshold, V_{IH_DTH}	175	400		mV
Logic Low Differential Input Threshold, V_{IL_DTH}	−175	−400		mV
Receiver Differential Input Impedance, R_{IN}	80		120	Ω
Input Capacitance		1.2		pF
Maximum Clock Rate	625			MHz
LVDS CLOCK OUTPUT (DCO)[3]				
Output Voltage High (DCO_P or DCO_N)			1375	mV
Output Voltage Low (DCO_P or DCO_N)	1025			mV
Output Differential Voltage, $\|V_{OD}\|$	150	200	250	mV
Output Offset Voltage, V_{OS}	1150		1250	mV
Output Impedance, Single-Ended, R_O	80	100	120	Ω
R_O Single-Ended Mismatch			10	%
Maximum Clock Rate	625			MHz

[1] DB0[x]P, DB0[x]N, DB1[x]P, and DB1[x]N pins.
[2] DCI_P and DCI_N pins.
[3] DCO_P and DCO_N pins with 100 Ω differential termination.

SERIAL PORT SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V.

Table 3.

Parameter	Min	Typ	Max	Unit
WRITE OPERATION (See Figure 154)				
SCLK Clock Rate, f_{SCLK}, $1/t_{SCLK}$			20	MHz
SCLK Clock High, t_{HIGH}	18			ns
SCLK Clock Low, t_{LOW}	18			ns
SDIO to SCLK Setup Time, t_{DS}	2			ns
SCLK to SDIO Hold Time, t_{DH}	1			ns
$\overline{CS}$ to SCLK Setup Time, t_S	3			ns
SCLK to $\overline{CS}$ Hold Time, t_H	2			ns
READ OPERATION (See Figure 155 and Figure 156)				
SCLK Clock Rate, f_{SCLK}, $1/t_{SCLK}$			20	MHz
SCLK Clock High, t_{HIGH}	18			ns
SCLK Clock Low, t_{LOW}	18			ns
SDIO to SCLK Setup Time, t_{DS}	2			ns
SCLK to SDIO Hold Time, t_{DH}	1			ns
$\overline{CS}$ to SCLK Setup Time, t_S	3			ns
SCLK to SDIO (or SDO) Data Valid Time, t_{DV}			15	ns
$\overline{CS}$ to SDIO (or SDO) Output Valid to High-Z, t_{EZ}		2		ns
INPUTS (SDI, SDIO, SCLK, $\overline{CS}$)				
Voltage in High, V_{IH}	2.0	3.3		V
Voltage in Low, V_{IL}		0	0.8	V
Current in High, I_{IH}	−10		+10	µA
Current in Low, I_{IL}	−10		+10	µA
OUTPUT (SDIO)				
Voltage Out High, V_{OH}	2.4		3.5	V
Voltage Out Low, V_{OL}	0		0.4	V
Current Out High, I_{OH}		4		mA
Current Out Low, I_{OL}		4		mA

AC SPECIFICATIONS

VDDA = VDD33 = 3.3 V, VDDC = VDD = 1.8 V, I_{OUTFS} = 20 mA, f_{DAC} = 2400 MSPS, unless otherwise noted.

Table 4.

	AD9737A			AD9739A			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE							
DAC Clock Rate	1600		2500	1600		2500	MSPS
Adjusted DAC Update Rate[1]	1600		2500	1600		2500	MSPS
Output Settling Time to 0.1%		13			13		ns
SPURIOUS-FREE DYNAMIC RANGE (SFDR)							
f_{OUT} = 100 MHz		70			70		dBc
f_{OUT} = 350 MHz		65			65		dBc
f_{OUT} = 550 MHz		58			58		dBc
f_{OUT} = 950 MHz		55			55		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD), $f_{OUT2} = f_{OUT1} + 1.25$ MHz							
f_{OUT} = 100 MHz		94			94		dBc
f_{OUT} = 350 MHz		78			78		dBc
f_{OUT} = 550 MHz		72			72		dBc
f_{OUT} = 950 MHz		68			68		dBc
NOISE SPECTRAL DENSITY (NSD), 0 dBFS SINGLE TONE							
f_{OUT} = 100 MHz		−162			−167		dBm/Hz
f_{OUT} = 350 MHz		−162			−166		dBm/Hz
f_{OUT} = 550 MHz		−161			−164		dBm/Hz
f_{OUT} = 850 MHz		−161			−163		dBm/Hz
WCDMA ACLR (SINGLE CARRIER), ADJACENT/ALTERNATE ADJACENT CHANNEL							
f_{DAC} = 2457.6 MSPS, f_{OUT} = 350 MHz		80/81			80/80		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 950 MHz		75/75			78/79		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 1700 MHz (Mix-Mode)		69/71			74/74		dBc
f_{DAC} = 2457.6 MSPS, f_{OUT} = 2100 MHz (Mix-Mode)		66/67			69/72		dBc

[1] Adjusted DAC updated rate is calculated as f_{DAC} divided by the minimum required interpolation factor. For the AD9737A/AD9739A, the minimum interpolation factor is 1. Thus, with f_{DAC} = 2500 MSPS, f_{DAC}, adjusted, = 2500 MSPS.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VDDA to VSSA	−0.3 V to +3.6 V
VDD33 to VSS	−0.3 V to +3.6 V
VDD to VSS	−0.3 V to +1.98 V
VDDC to VSSC	−0.3 V to +1.98 V
VSSA to VSS	−0.3 V to +0.3 V
VSSA to VSSC	−0.3 V to +0.3 V
VSS to VSSC	−0.3 V to +0.3 V
DACCLK_P, DACCLK_N to VSSC	−0.3 V to VDDC + 0.18 V
DCI, DCO to VSS	−0.3 V to VDD33 + 0.3 V
LVDS Data Inputs to VSS	−0.3 V to VDD33 + 0.3 V
IOUTP, IOUTN to VSSA	−1.0 V to VDDA + 0.3 V
I120, VREF to VSSA	−0.3 V to VDDA + 0.3 V
IRQ, $\overline{CS}$, SCLK, SDO, SDIO, RESET to VSS	−0.3 V to VDD33 + 0.3 V
Junction Temperature	150°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
160-Ball CSP_BGA	31.2	7.0	°C/W[1]

[1] With no airflow movement.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

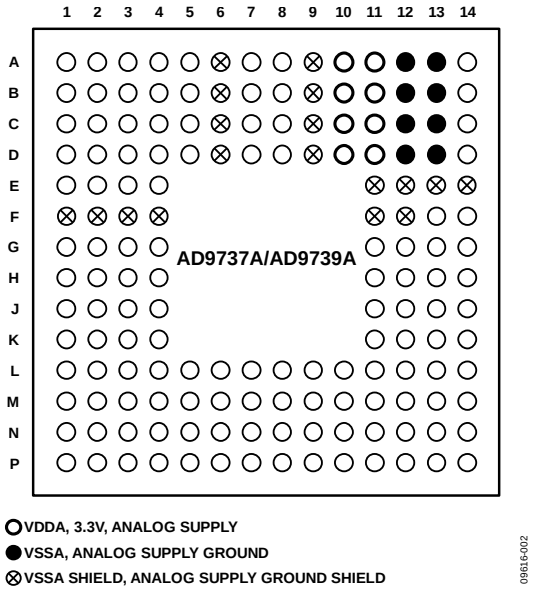


Figure 2. Analog Supply Pins (Top View)

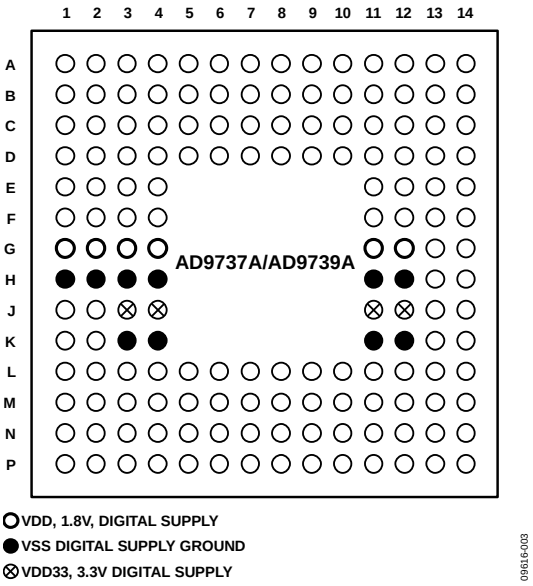


Figure 3. Digital Supply Pins (Top View)

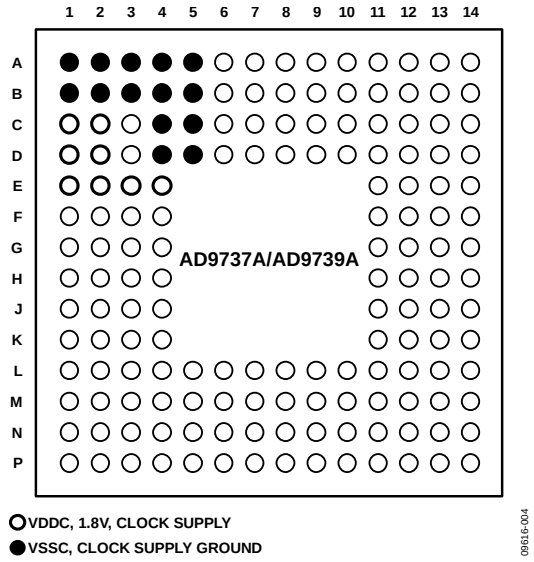


Figure 4. Digital LVDS Clock Supply Pins (Top View)

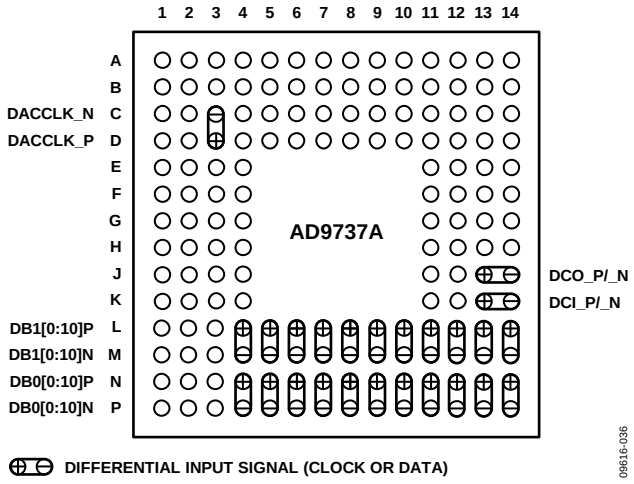


Figure 5. AD9737A Digital LVDS Input, Clock I/O (Top View)

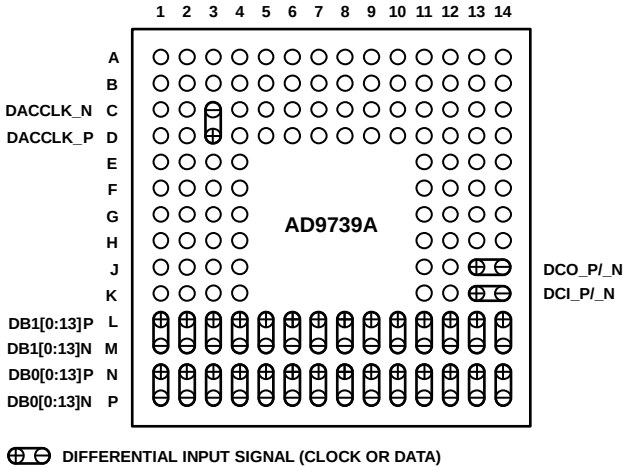


Figure 6. AD9739A Digital LVDS Input, Clock I/O (Top View)

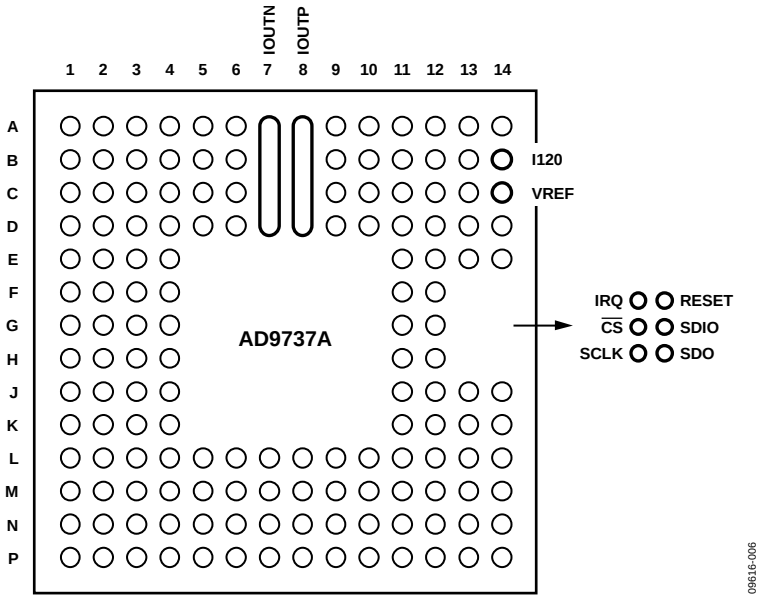


Figure 7. AD9737A Analog I/O and SPI Control Pins (Top View)

Table 7. AD9737A Pin Function Descriptions

Pin No.	Mnemonic	Description
C1, C2, D1, D2, E1, E2, E3, E4	VDDC	1.8 V Clock Supply Input.
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C4, C5, D4, D5	VSSC	Clock Supply Ground.
A10, A11, B10, B11, C10, C11, D10, D11	VDDA	3.3 V Analog Supply Input.
A12, A13, B12, B13, C12, C13, D12, D13,	VSSA	Analog Supply Ground.
A6, A9, B6, B9, C6, C9, D6, D9, E11, E12, E13, E14, F1, F2, F3, F4, F11, F12	VSSA Shield	Analog Supply Ground Shield. Tie to VSSA at the DAC.
A14	NC	Do not connect to this pin.
A7, B7, C7, D7	IOUTN	DAC Negative Current Output Source.
A8, B8, C8, D8	IOUTP	DAC Positive Current Output Source.
B14	I120	Nominal 1.2 V Reference. Tie to analog ground via a 10 kΩ resistor to generate a 120 µA reference current.
C14	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
D14	NC	Factory Test Pin. Do not connect to this pin.
C3, D3	DACCLK_N/DACCLK_P	Negative/Positive DAC Clock Input (DACCLK).
F13	IRQ	Interrupt Request Open Drain Output. Active high. Pull up to VDD33 with a 10 kΩ resistor.
F14	RESET	Reset Input. Active high. Tie to VSS if unused.
G13	$\overline{CS}$	Serial Port Enable Input.
G14	SDIO	Serial Port Data Input/Output.
H13	SCLK	Serial Port Clock Input.
H14	SDO	Serial Port Data Output.
J3, J4, J11, J12	VDD33	3.3 V Digital Supply Input.
G1, G2, G3, G4, G11, G12	VDD	1.8 V Digital Supply Input.
H1, H2, H3, H4, H11, H12, K3, K4, K11, K12	VSS	Digital Supply Ground.
J1, J2	NC	Differential resistor of 200 Ω exists between J1 and J2. Do not connect to this pin.
K1, K2	NC	Differential resistor of 100 Ω exists between K1 and K2. Do not connect to this pin.
J13, J14	DCO_P/DCO_N	Positive/Negative Data Clock Output (DCO).
K13, K14	DCI_P/DCI_N	Positive/Negative Data Clock Input (DCI).

Pin No.	Mnemonic	Description
L1, M1	NC, NC	Do not connect to this pin.
L2, M2	NC, NC	Do not connect to this pin.
L3, M3	NC, NC	Do not connect to this pin.
L4, M4	DB1[0]P/DB1[0]N	Port 1 Positive/Negative Data Input Bit 0.
L5, M5	DB1[1]P/DB1[1]N	Port 1 Positive/Negative Data Input Bit 1.
L6, M6	DB1[2]P/DB1[2]N	Port 1 Positive/Negative Data Input Bit 2.
L7, M7	DB1[3]P/DB1[3]N	Port 1 Positive/Negative Data Input Bit 3.
L8, M8	DB1[4]P/DB1[4]N	Port 1 Positive/Negative Data Input Bit 4.
L9, M9	DB1[5]P/DB1[5]N	Port 1 Positive/Negative Data Input Bit 5.
L10, M10	DB1[6]P/DB1[6]N	Port 1 Positive/Negative Data Input Bit 6.
L11, M11	DB1[7]P/DB1[7]N	Port 1 Positive/Negative Data Input Bit 7.
L12, M12	DB1[8]P/DB1[8]N	Port 1 Positive/Negative Data Input Bit 8.
L13, M13	DB1[9]P/DB1[9]N	Port 1 Positive/Negative Data Input Bit 9.
L14, M14	DB1[10]P/DB1[10]N	Port 1 Positive/Negative Data Input Bit 10.
N1, P1	NC, NC	Do not connect to this pin.
N2, P2	NC, NC	Do not connect to this pin.
N3, P3	NC, NC	Do not connect to this pin.
N4, P4	DB0[0]P/DB0[0]N	Port 0 Positive/Negative Data Input Bit 0.
N5, P5	DB0[1]P/DB0[1]N	Port 0 Positive/Negative Data Input Bit 1.
N6, P6	DB0[2]P/DB0[2]N	Port 0 Positive/Negative Data Input Bit 2.
N7, P7	DB0[3]P/DB0[3]N	Port 0 Positive/Negative Data Input Bit 3.
N8, P8	DB0[4]P/DB0[4]N	Port 0 Positive/Negative Data Input Bit 4.
N9, P9	DB0[5]P/DB0[5]N	Port 0 Positive/Negative Data Input Bit 5.
N10, P10	DB0[6]P/DB0[6]N	Port 0 Positive/Negative Data Input Bit 6.
N11, P11	DB0[7]P/DB0[7]N	Port 0 Positive/Negative Data Input Bit 7.
N12, P12	DB0[8]P/DB0[8]N	Port 0 Positive/Negative Data Input Bit 8.
N13, P13	DB0[9]P/DB0[9]N	Port 0 Positive/Negative Data Input Bit 9.
N14, P14	DB0[10]P/DB0[10]N	Port 0 Positive/Negative Data Input Bit 10.

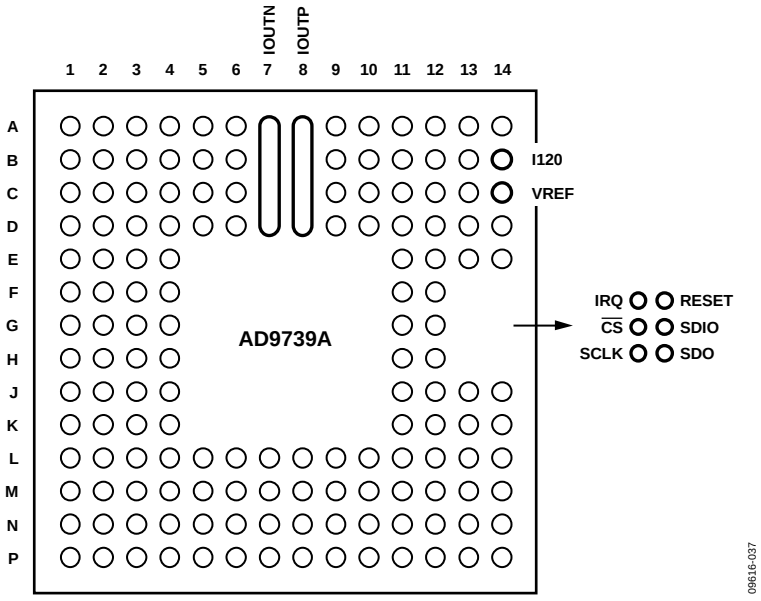


Figure 8. AD9739A Analog I/O and SPI Control Pins (Top View)

Table 8. AD9739A Pin Function Descriptions

Pin No.	Mnemonic	Description
C1, C2, D1, D2, E1, E2, E3, E4	VDDC	1.8 V Clock Supply Input.
A1, A2, A3, A4, A5, B1, B2, B3, B4, B5, C4, C5, D4, D5	VSSC	Clock Supply Ground.
A10, A11, B10, B11, C10, C11, D10, D11	VDDA	3.3 V Analog Supply Input.
A12, A13, B12, B13, C12, C13, D12, D13,	VSSA	Analog Supply Ground.
A6, A9, B6, B9, C6, C9, D6, D9, E11, E12, E13, E14, F1, F2, F3, F4, F11, F12	VSSA Shield	Analog Supply Ground Shield. Tie to VSSA at the DAC.
A14	NC	Do not connect to this pin.
A7, B7, C7, D7	IOUTN	DAC Negative Current Output Source.
A8, B8, C8, D8	IOUTP	DAC Positive Current Output Source.
B14	I120	Nominal 1.2 V Reference. Tie to analog ground via a 10 kΩ resistor to generate a 120 µA reference current.
C14	VREF	Voltage Reference Input/Output. Decouple to VSSA with a 1 nF capacitor.
D14	NC	Factory Test Pin. Do not connect to this pin.
C3, D3	DACCLK_N/DACCLK_P	Negative/Positive DAC Clock Input (DACCLK).
F13	IRQ	Interrupt Request Open Drain Output. Active high. Pull up to VDD33 with a 10 kΩ resistor.
F14	RESET	Reset Input. Active high. Tie to VSS if unused.
G13	$\overline{CS}$	Serial Port Enable Input.
G14	SDIO	Serial Port Data Input/Output.
H13	SCLK	Serial Port Clock Input.
H14	SDO	Serial Port Data Output.
J3, J4, J11, J12	VDD33	3.3 V Digital Supply Input.
G1, G2, G3, G4, G11, G12	VDD	1.8 V Digital Supply Input.
H1, H2, H3, H4, H11, H12, K3, K4, K11, K12	VSS	Digital Supply Ground.
J1, J2	NC	Differential resistor of 200 Ω exists between J1 and J2. Do not connect to this pin.
K1, K2	NC	Differential resistor of 100 Ω exists between K1 and K2. Do not connect to this pin.
J13, J14	DCO_P/DCO_N	Positive/Negative Data Clock Output (DCO).
K13, K14	DCI_P/DCI_N	Positive/Negative Data Clock Input (DCI).

Pin No.	Mnemonic	Description
L1, M1	DB1[0]P/DB1[0]N	Port 1 Positive/Negative Data Input Bit 0.
L2, M2	DB1[1]P/DB1[1]N	Port 1 Positive/Negative Data Input Bit 1.
L3, M3	DB1[2]P/DB1[2]N	Port 1 Positive/Negative Data Input Bit 2.
L4, M4	DB1[3]P/DB1[3]N	Port 1 Positive/Negative Data Input Bit 3.
L5, M5	DB1[4]P/DB1[4]N	Port 1 Positive/Negative Data Input Bit 4.
L6, M6	DB1[5]P/DB1[5]N	Port 1 Positive/Negative Data Input Bit 5.
L7, M7	DB1[6]P/DB1[6]N	Port 1 Positive/Negative Data Input Bit 6.
L8, M8	DB1[7]P/DB1[7]N	Port 1 Positive/Negative Data Input Bit 7.
L9, M9	DB1[8]P/DB1[8]N	Port 1 Positive/Negative Data Input Bit 8.
L10, M10	DB1[9]P/DB1[9]N	Port 1 Positive/Negative Data Input Bit 9.
L11, M11	DB1[10]P/DB1[10]N	Port 1 Positive/Negative Data Input Bit 10.
L12, M12	DB1[11]P/DB1[11]N	Port 1 Positive/Negative Data Input Bit 11.
L13, M13	DB1[12]P/DB1[12]N	Port 1 Positive/Negative Data Input Bit 12.
L14, M14	DB1[13]P/DB1[13]N	Port 1 Positive/Negative Data Input Bit 13.
N1, P1	DB0[0]P/DB0[0]N	Port 0 Positive/Negative Data Input Bit 0.
N2, P2	DB0[1]P/DB0[1]N	Port 0 Positive/Negative Data Input Bit 1.
N3, P3	DB0[2]P/DB0[2]N	Port 0 Positive/Negative Data Input Bit 2.
N4, P4	DB0[3]P/DB0[3]N	Port 0 Positive/Negative Data Input Bit 3.
N5, P5	DB0[4]P/DB0[4]N	Port 0 Positive/Negative Data Input Bit 4.
N6, P6	DB0[5]P/DB0[5]N	Port 0 Positive/Negative Data Input Bit 5.
N7, P7	DB0[6]P/DB0[6]N	Port 0 Positive/Negative Data Input Bit 6.
N8, P8	DB0[7]P/DB0[7]N	Port 0 Positive/Negative Data Input Bit 7.
N9, P9	DB0[8]P/DB0[8]N	Port 0 Positive/Negative Data Input Bit 8.
N10, P10	DB0[9]P/DB0[9]N	Port 0 Positive/Negative Data Input Bit 9.
N11, P11	DB0[10]P/DB0[10]N	Port 0 Positive/Negative Data Input Bit 10.
N12, P12	DB0[11]P/DB0[11]N	Port 0 Positive/Negative Data Input Bit 11.
N13, P13	DB0[12]P/DB0[12]N	Port 0 Positive/Negative Data Input Bit 12.
N14, P14	DB0[13]P/DB0[13]N	Port 0 Positive/Negative Data Input Bit 13.

TYPICAL PERFORMANCE CHARACTERISTICS—AD9737A

STATIC LINEARITY

I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

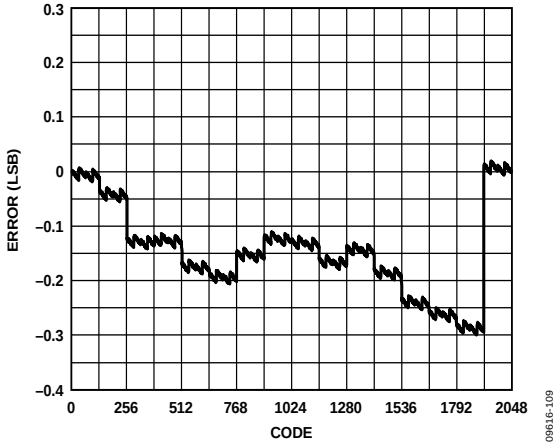


Figure 9. Typical INL, 20 mA at 25°C

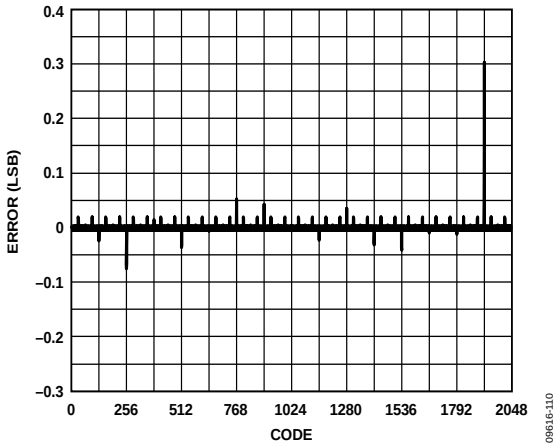


Figure 10. Typical DNL, 20 mA at 25°C

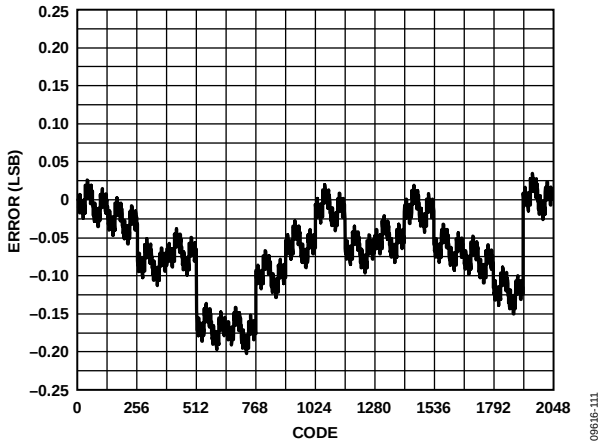


Figure 11. Typical INL, 10 mA at 25°C

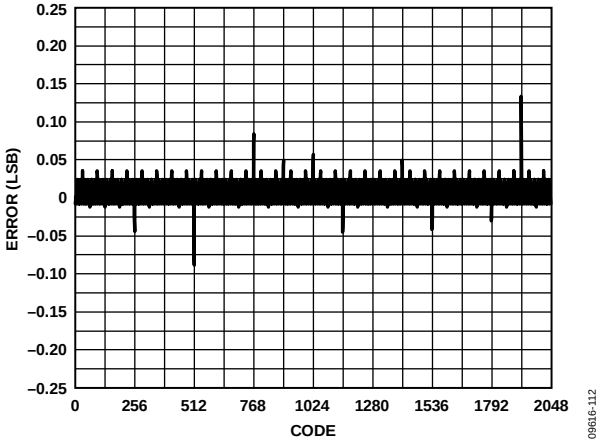


Figure 12. Typical DNL, 10 mA at 25°C

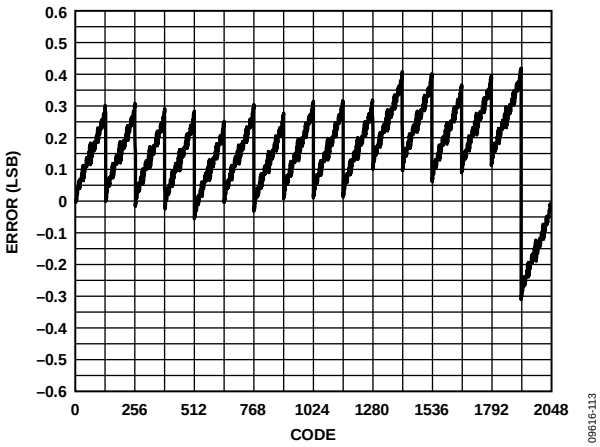


Figure 13. Typical INL, 30 mA at 25°C

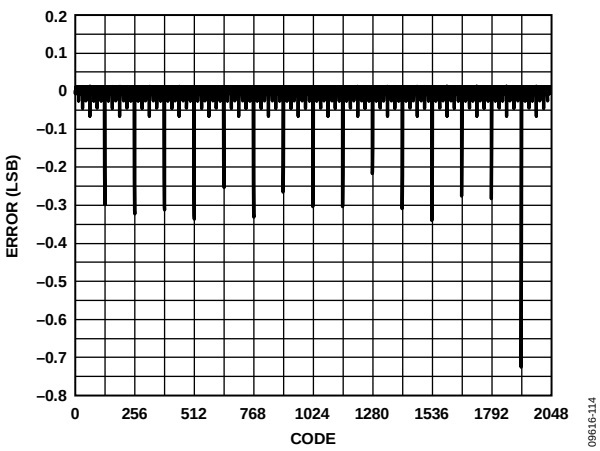


Figure 14. Typical DNL, 30 mA at 25°C

AC (NORMAL MODE)

I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

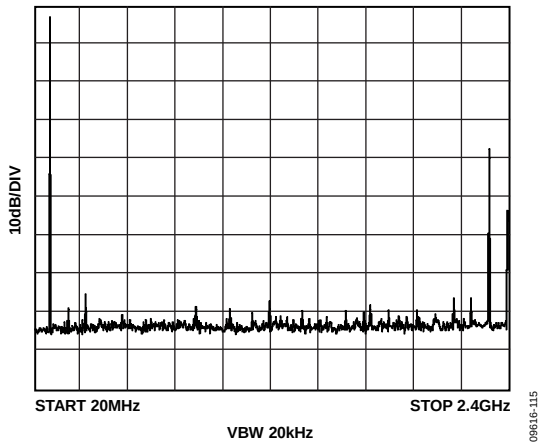


Figure 15. Single Tone Spectrum at f_{OUT} = 91 MHz, f_{DAC} = 2.4 GSPS

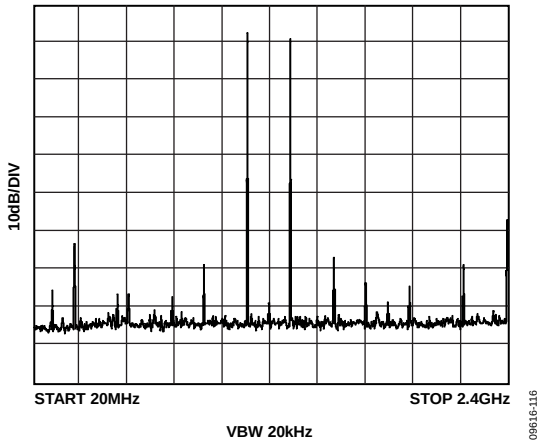


Figure 16. Single-Tone Spectrum at f_{OUT} = 1091 MHz, f_{DAC} = 2.4 GSPS

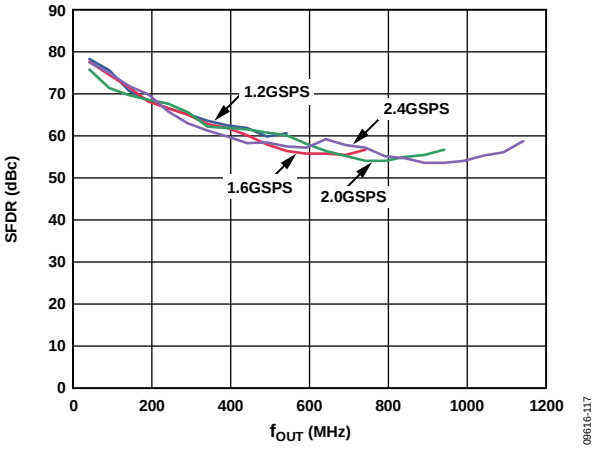


Figure 17. SFDR vs. f_{OUT} over f_{DAC}

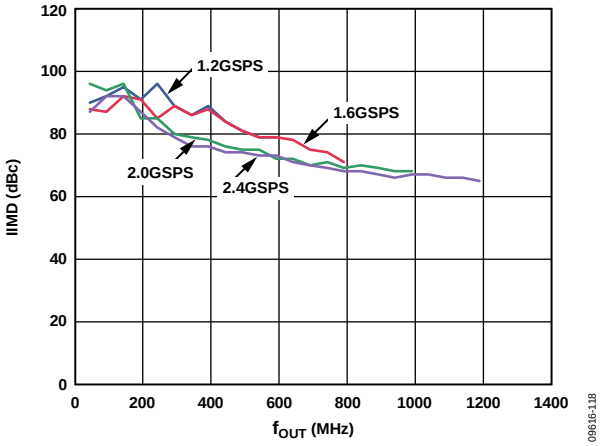


Figure 18. IMD vs. f_{OUT} over f_{DAC}

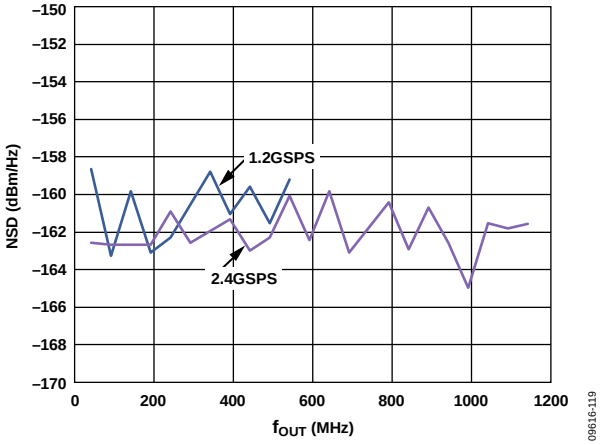


Figure 19. Single-Tone NSD over f_{OUT}

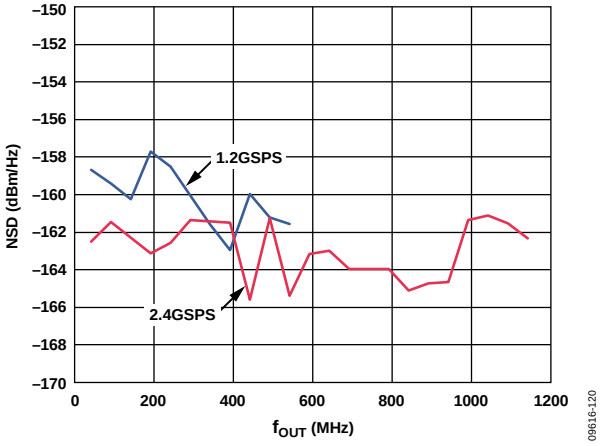


Figure 20. Eight-Tone NSD over f_{OUT}

f_{DAC} = 2 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

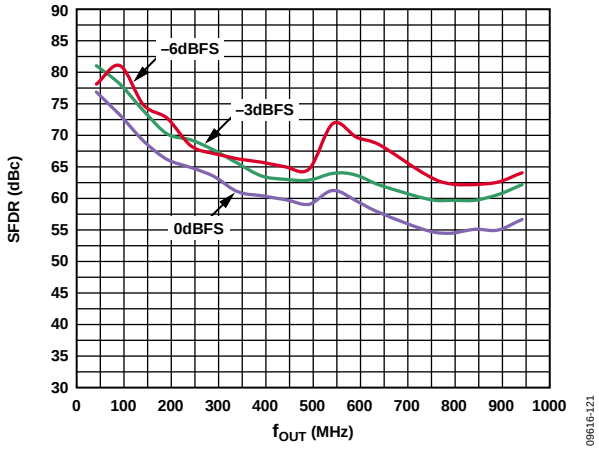


Figure 21. SFDR vs. f_{OUT} over Digital Full Scale

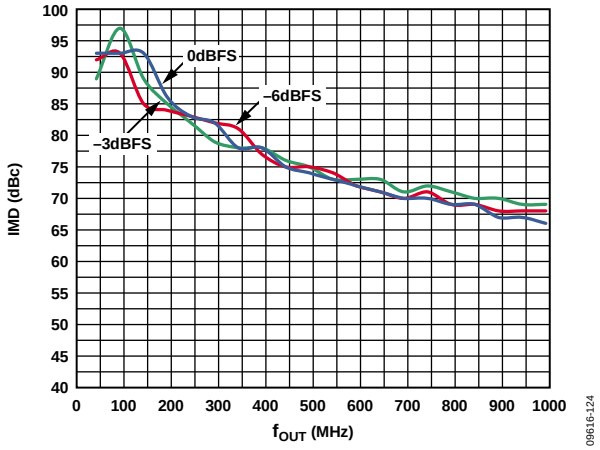


Figure 24. IMD vs. f_{OUT} over Digital Full Scale

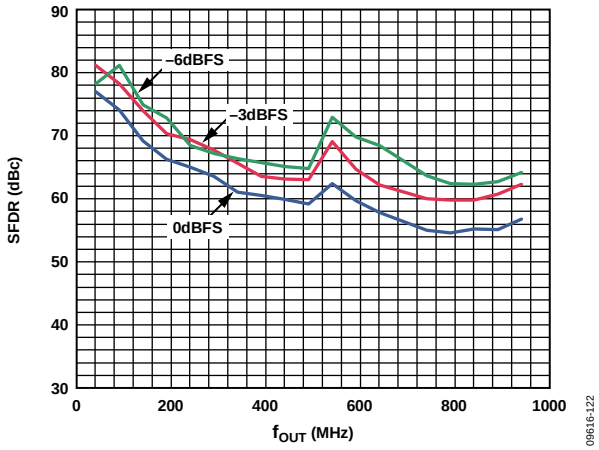


Figure 22. SFDR for Second Harmonic vs. f_{OUT} over Digital Full Scale

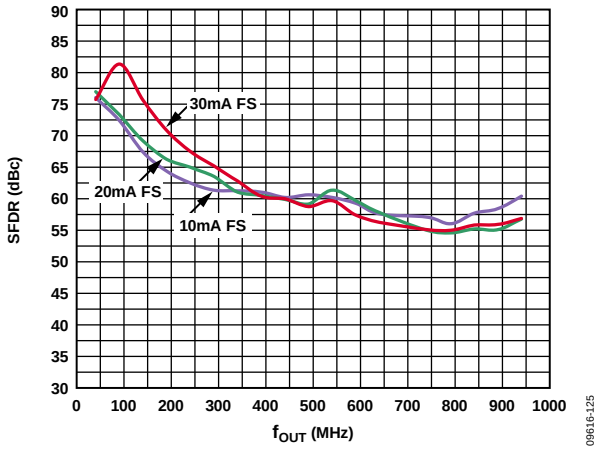


Figure 25. SFDR vs. f_{OUT} over DAC I_{OUTFS}

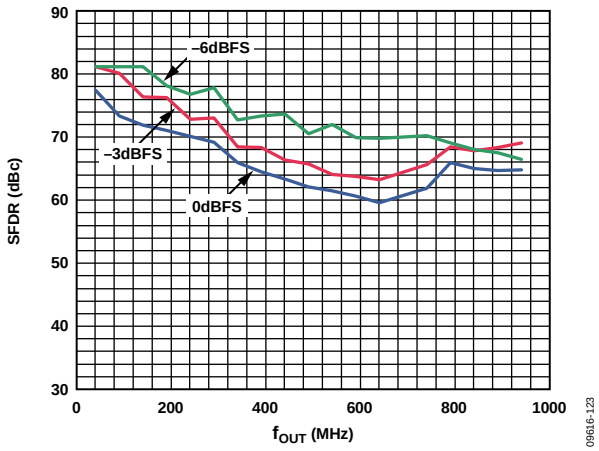


Figure 23. SFDR for Third Harmonic vs. f_{OUT} over Digital Full Scale

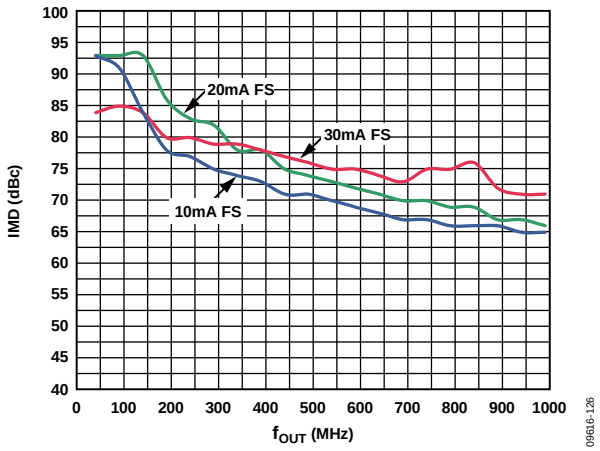


Figure 26. IMD vs. f_{OUT} over DAC I_{OUTFS}

AC (MIX-MODE)

f_{DAC} = 2.1 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

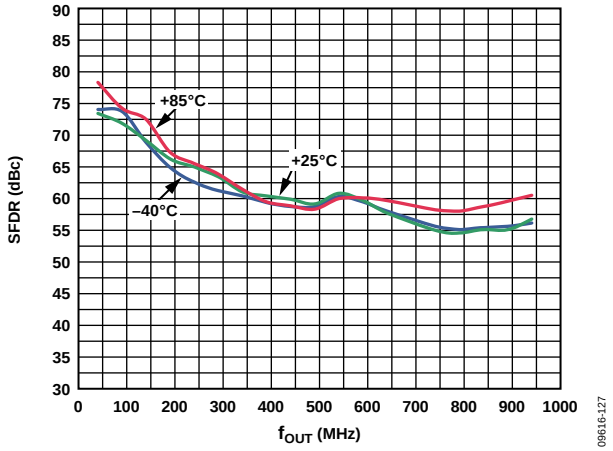


Figure 27. SFDR vs. f_{OUT} over Temperature

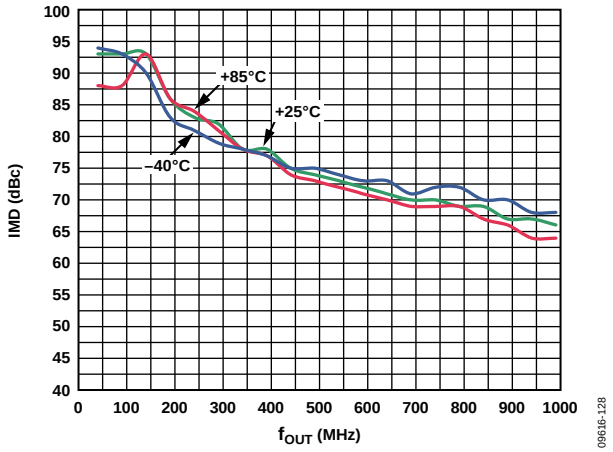


Figure 28. IMD vs. f_{OUT} over Temperature

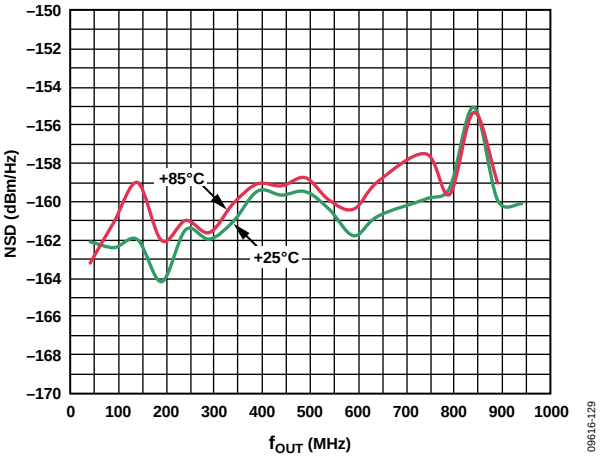


Figure 29. Single-Tone NSD vs. f_{OUT} over Temperature

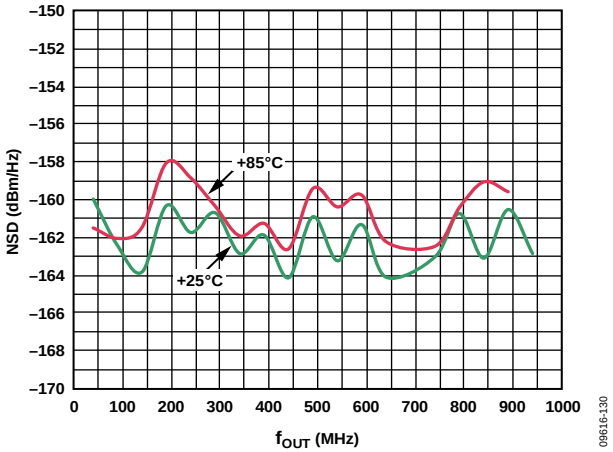


Figure 30. Eight-Tone NSD vs. f_{OUT} over Temperature

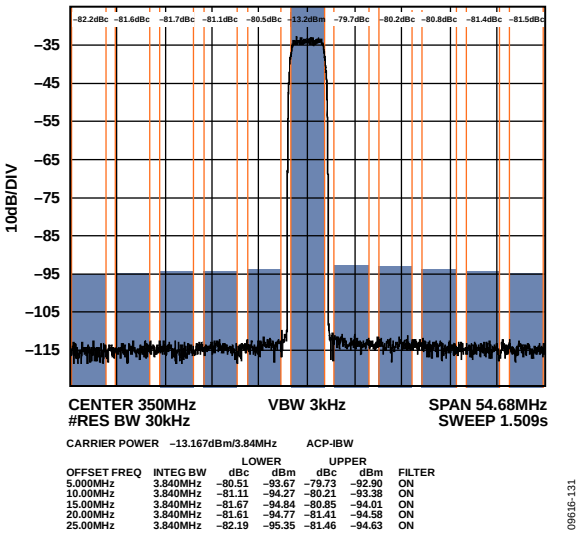


Figure 31. Single-Carrier WCDMA at 350 MHz, f_{DAC} = 2457.6 MSPS

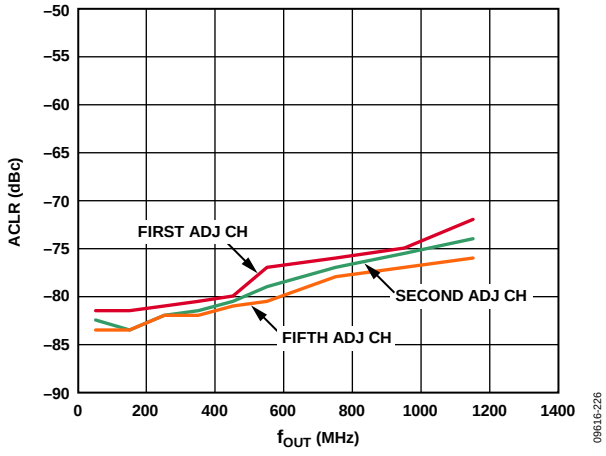


Figure 32. Single-Carrier WCDMA ACLR vs. f_{OUT} at 2457.6 MSPS

f_{DAC} = 2.1 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

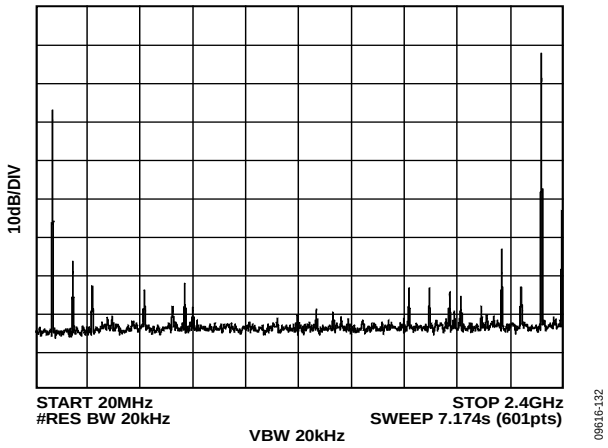


Figure 33. Single-Tone Spectrum at f_{OUT} = 2.31 GHz, f_{DAC} = 2.4 GSPS

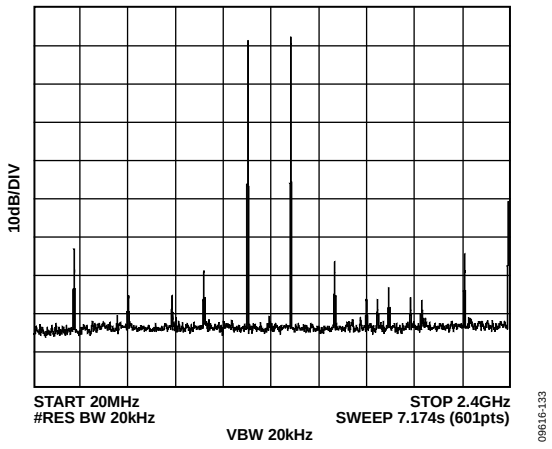


Figure 34. Single-Tone Spectrum at f_{OUT} = 1.31 GHz, f_{DAC} = 2.4 GSPS

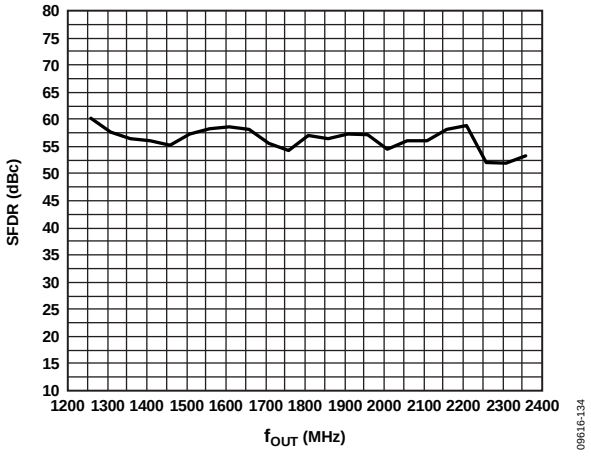


Figure 35. SFDR in Mix-mode vs. f_{OUT} at 2.4 GSPS

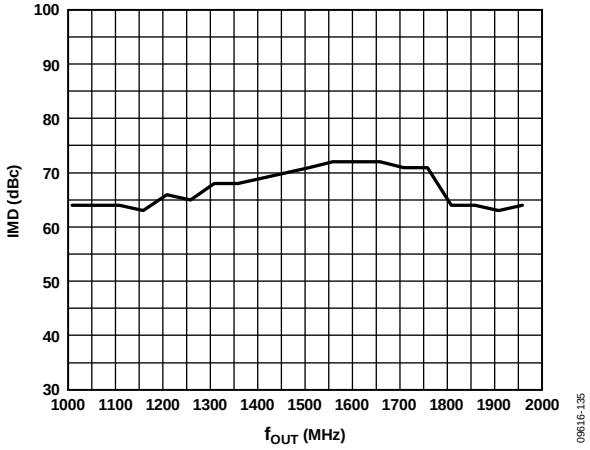


Figure 36. IMD in Mix-Mode vs. f_{OUT} at 2.4 GSPS

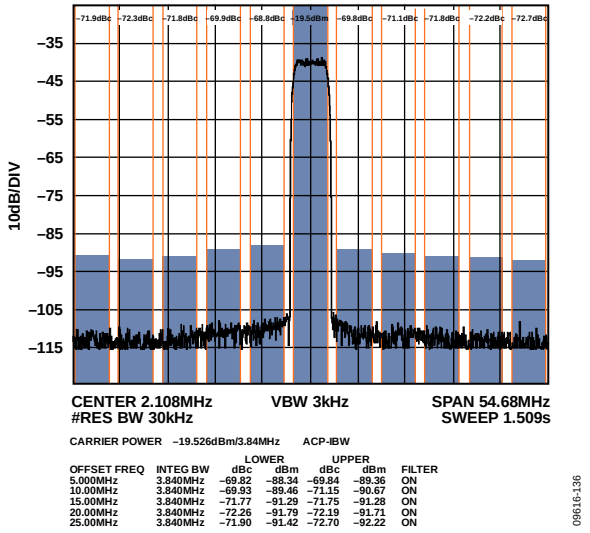


Figure 37. Typical Single-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)

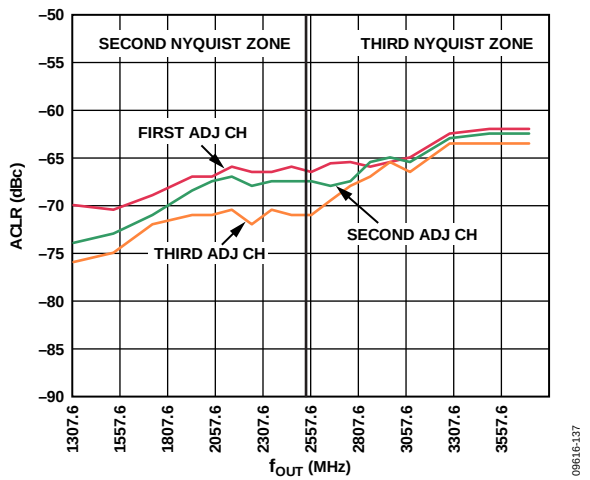


Figure 38. Single-Carrier WCDMA ACLR vs. f_{OUT}, f_{DAC} = 2457.6 MSPS

f_{DAC} = 2.1 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

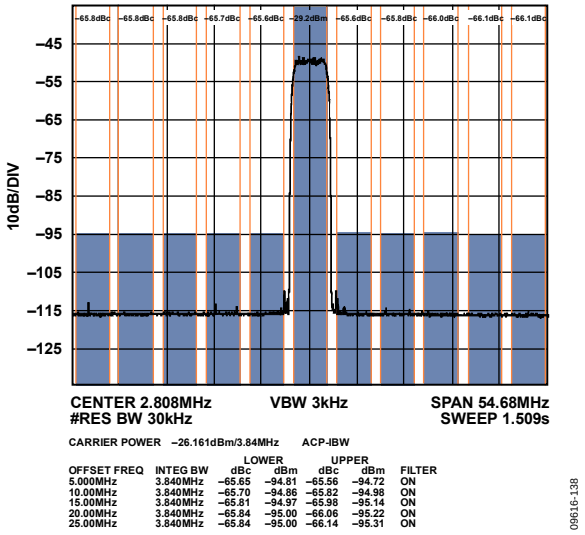


Figure 39. Typical Single-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)

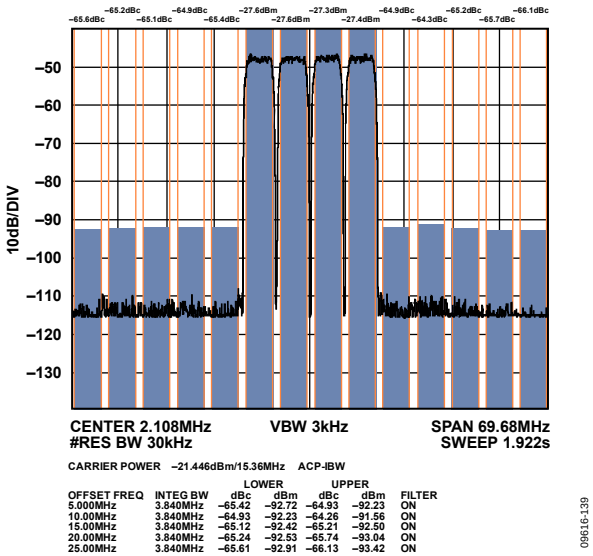


Figure 40. Typical Four-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)

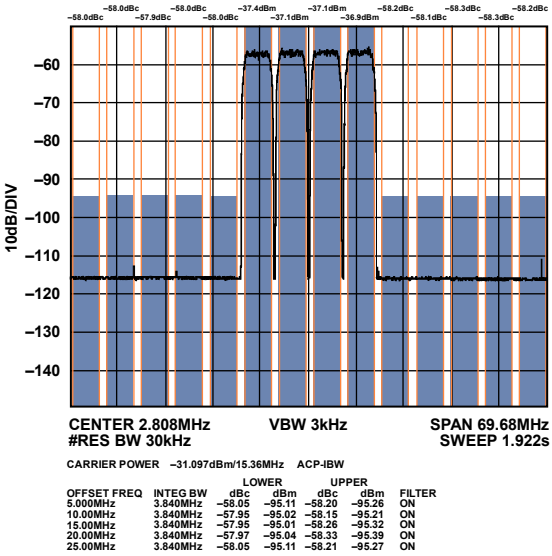


Figure 41. Typical Four-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)

ONE-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

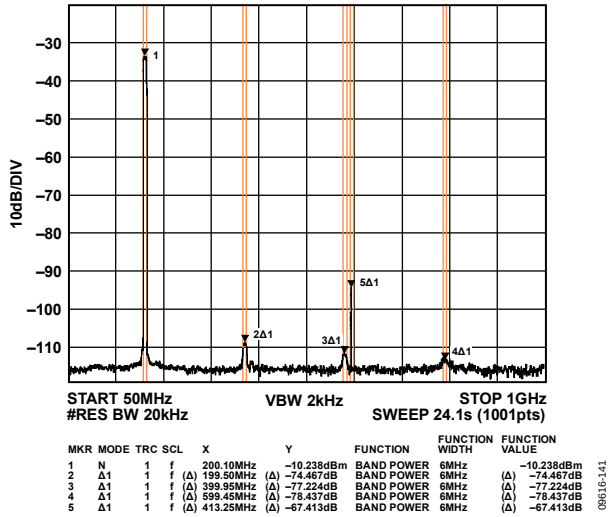


Figure 42. Low Band Wideband ACLR

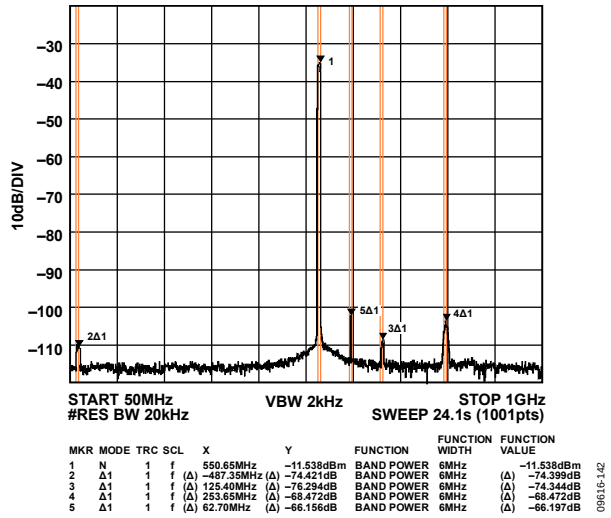


Figure 43. Mid Band Wideband ACLR

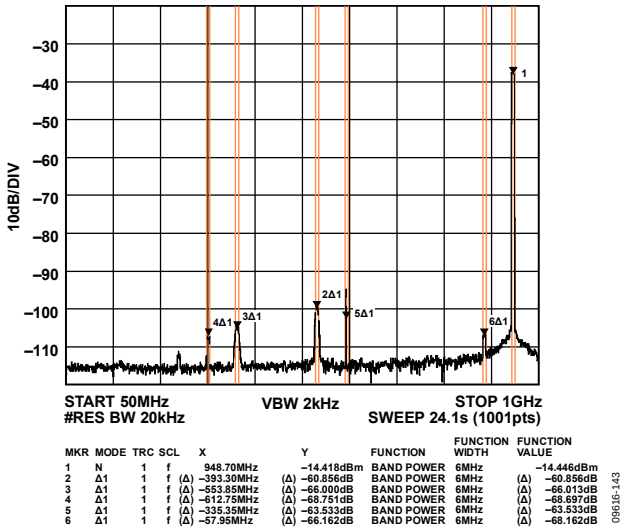


Figure 44. High Band Wideband ACLR

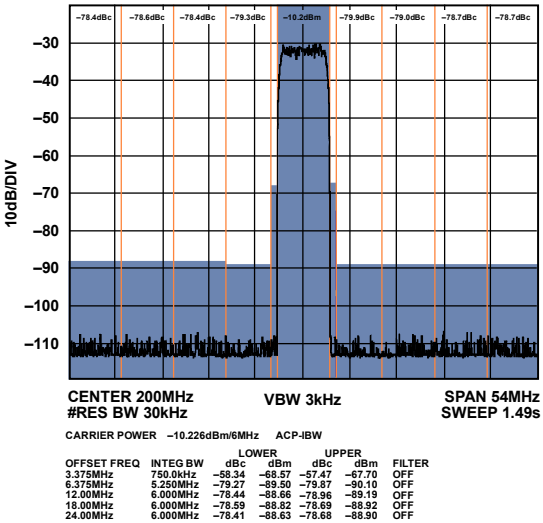


Figure 45. Low Band Narrow-Band ACLR

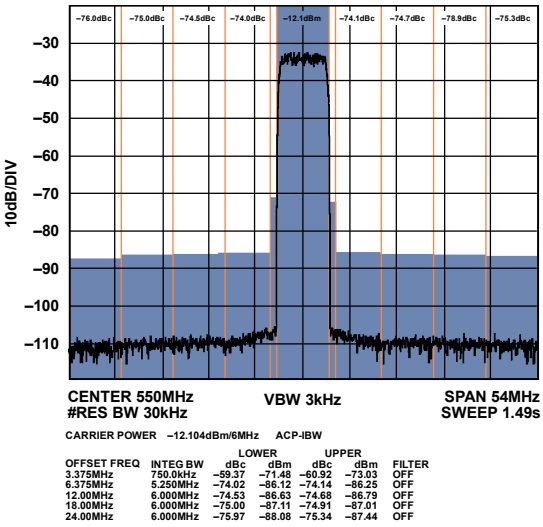


Figure 46. Mid Band Narrow-Band ACLR

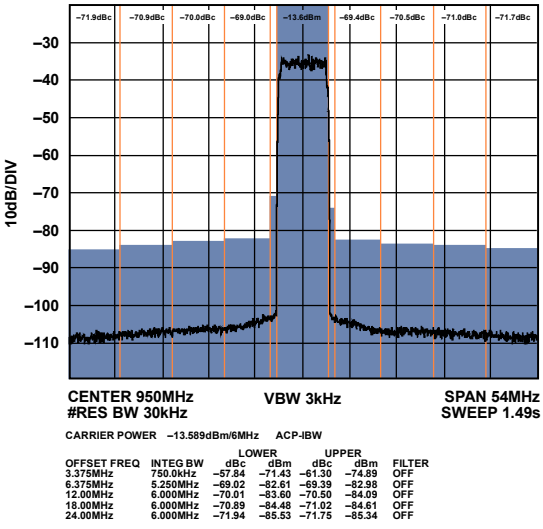


Figure 47. High Band Narrow-Band ACLR

FOUR-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

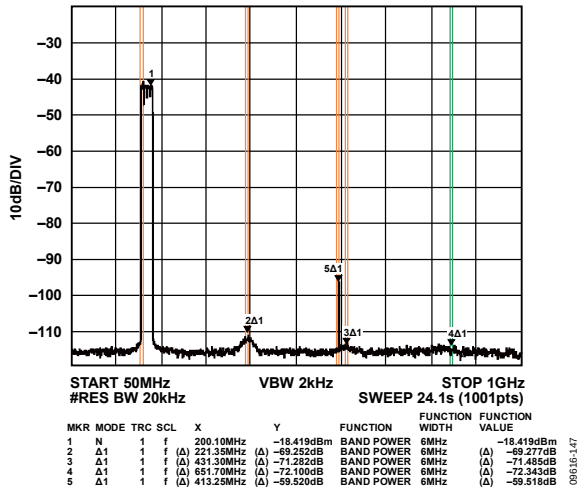


Figure 48. Low Band Wideband ACLR

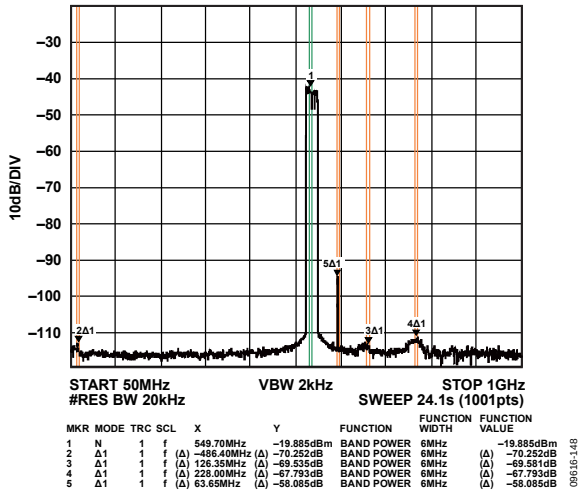


Figure 49. Mid Band Wideband ACLR

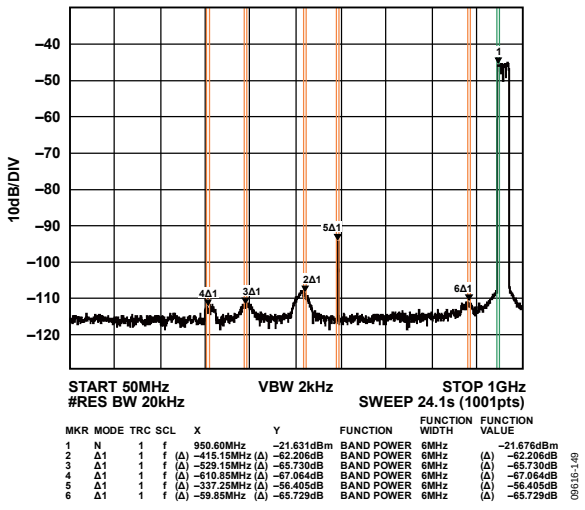


Figure 50. High Band Wideband ACLR

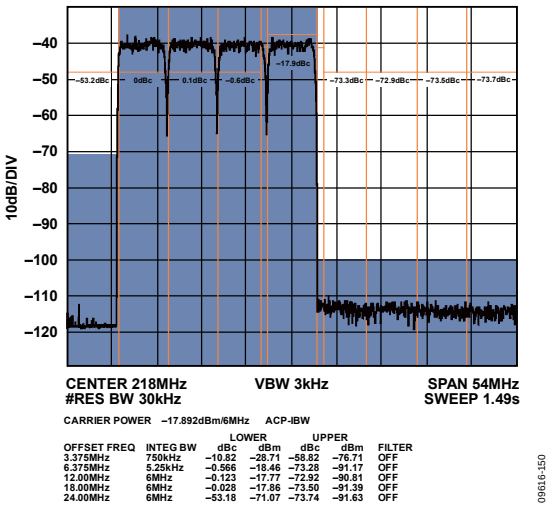


Figure 51. Low Band Narrow-Band ACLR (Worse Side)

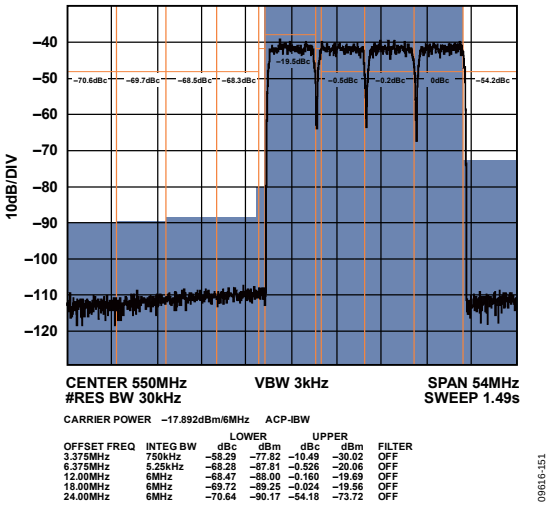


Figure 52. Mid Band Narrow-Band ACLR (Worse Side)

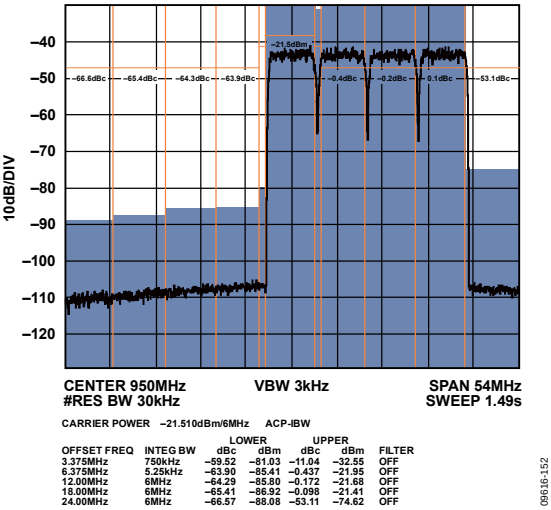


Figure 53. High Band Narrow-Band ACLR (Worse Side)

EIGHT-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

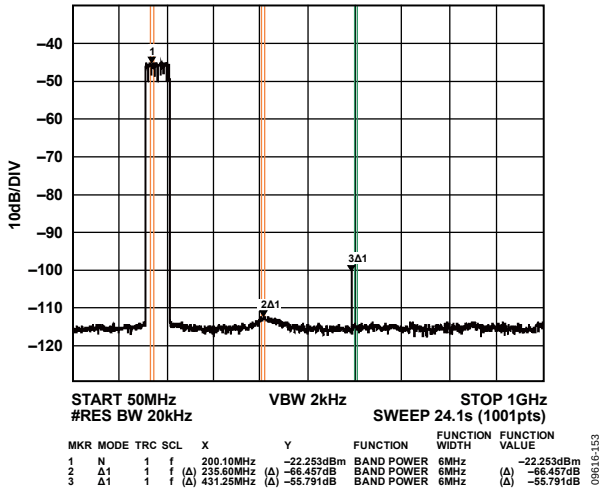


Figure 54. Low Band Wideband ACLR

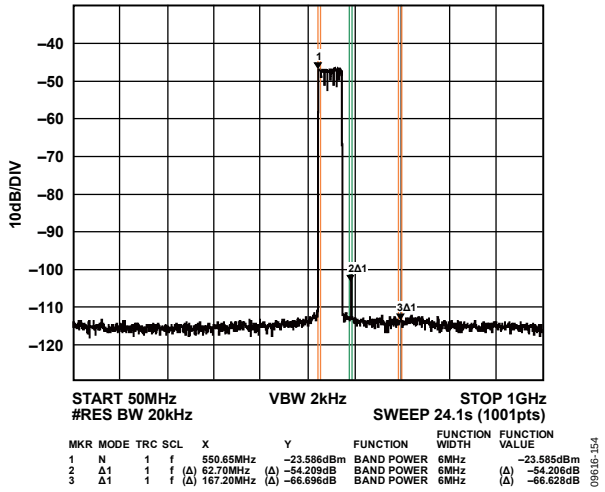


Figure 55. Mid Band Wideband ACLR

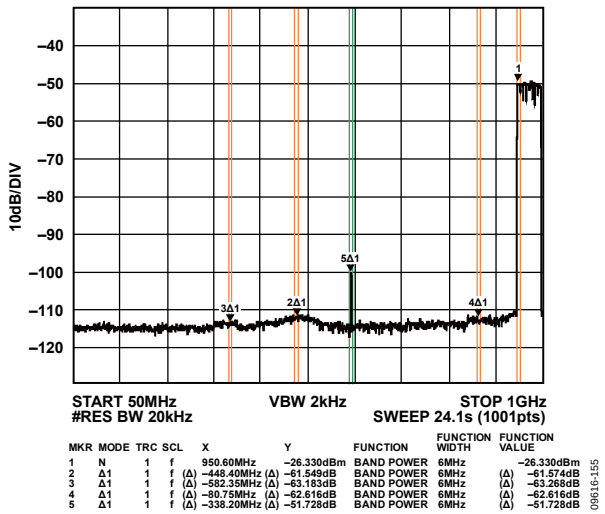


Figure 56. High Band Wideband ACLR

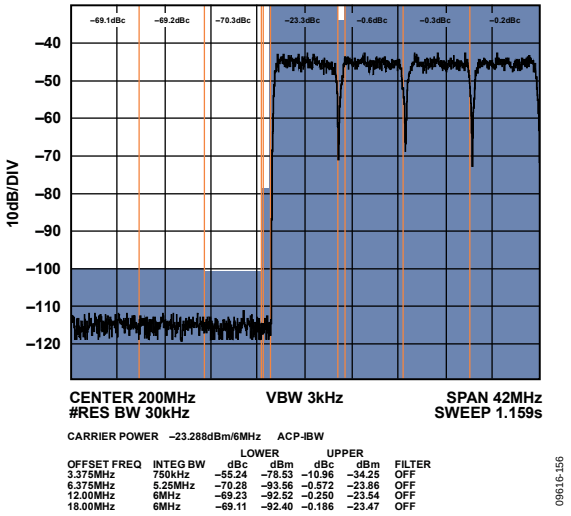


Figure 57. Low Band Narrow-Band ACLR (Worse Side)

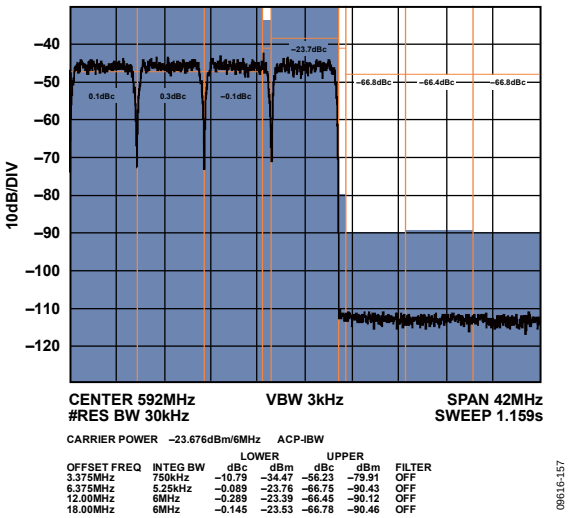


Figure 58. Mid Band Narrow-Band ACLR (Worse Side)

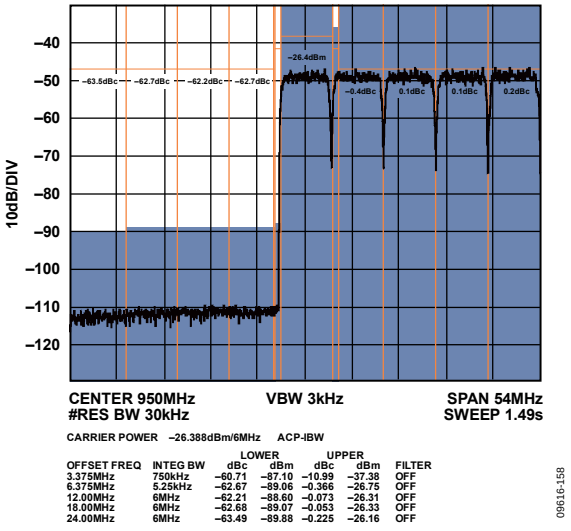


Figure 59. High Band Narrow-Band ACLR

16-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

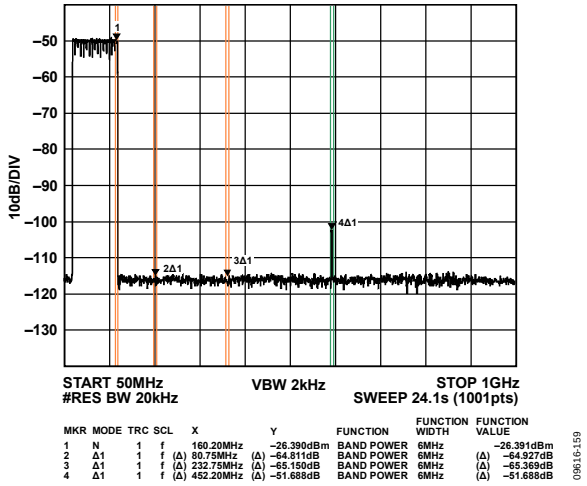


Figure 60. Low Band Wideband ACLR

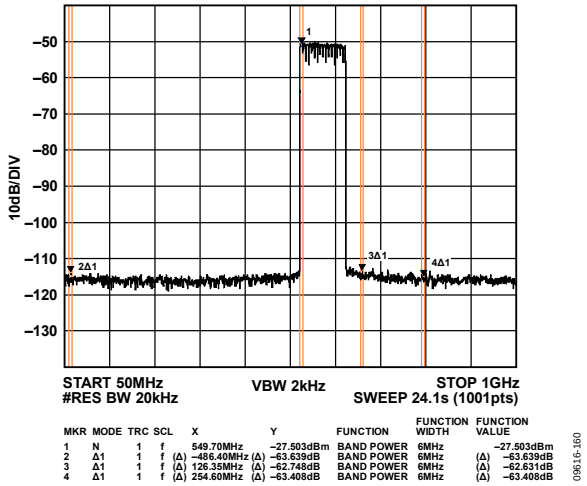


Figure 61. Mid Band Wideband ACLR

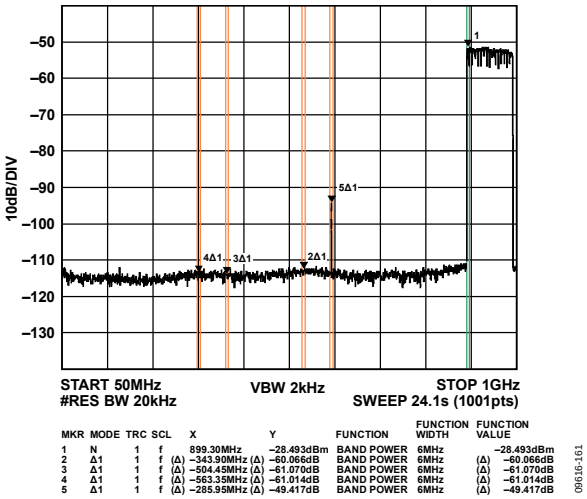


Figure 62. High Band Wideband ACLR

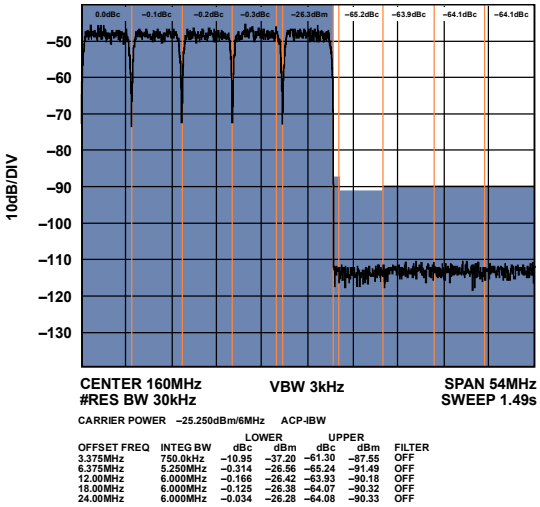


Figure 63. Low Band Narrow-Band ACLR

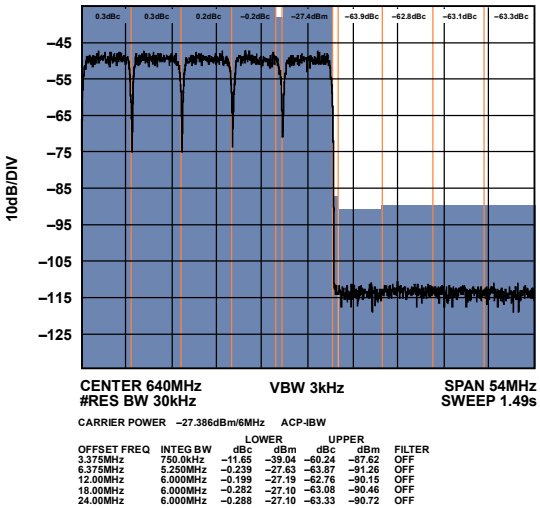


Figure 64. Mid Band Narrow-Band ACLR (Worse Side)

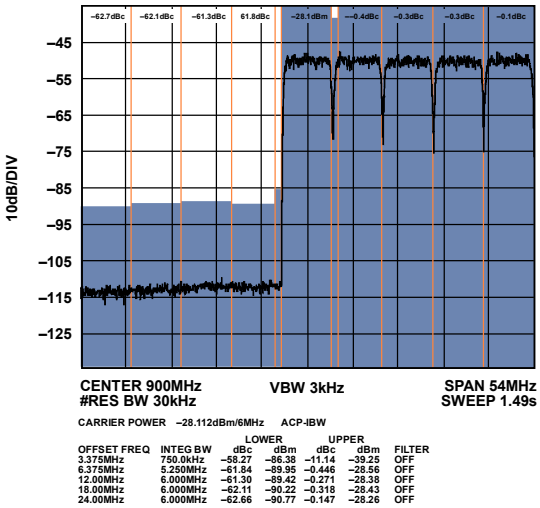


Figure 65. High Band Narrow-Band ACLR

32-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

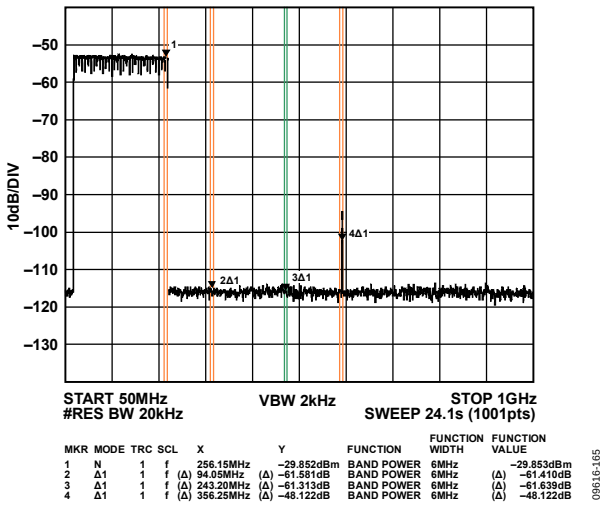


Figure 66. Low Band Wideband ACLR

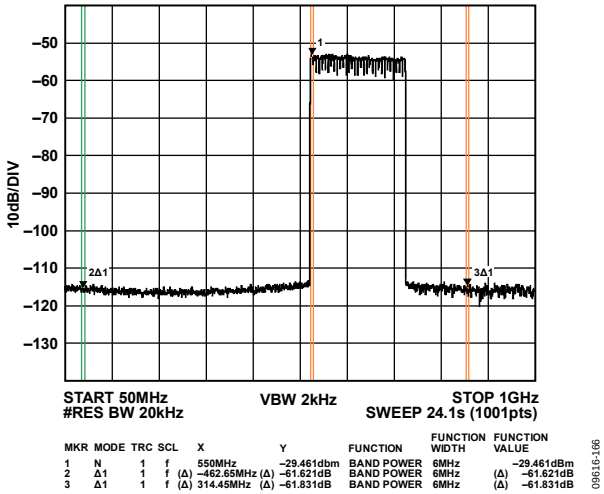


Figure 67. Mid Band Wideband ACLR

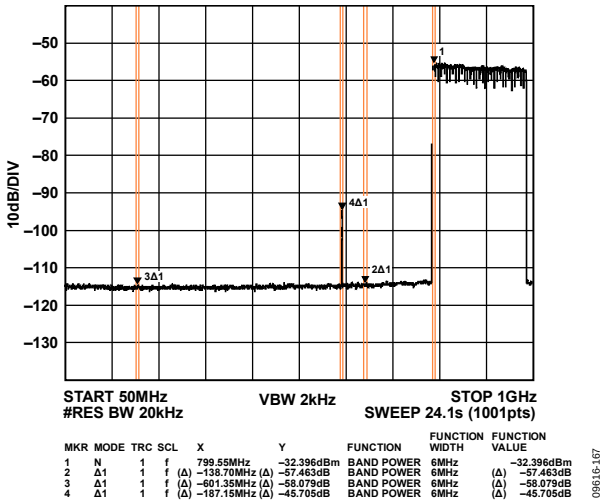


Figure 68. High Band Wideband ACLR

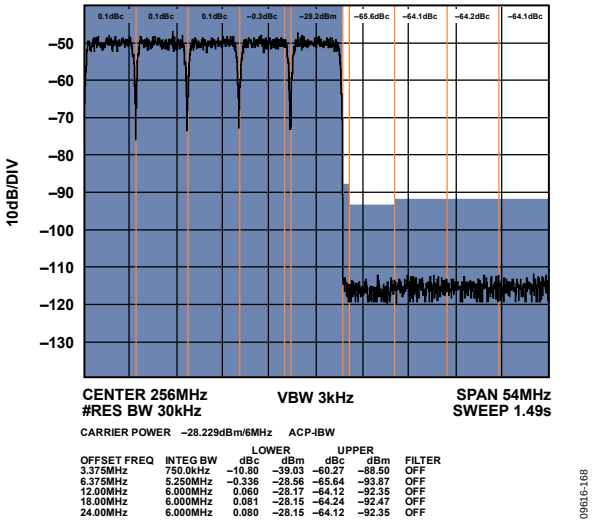


Figure 69. Low Band Narrow-Band ACLR

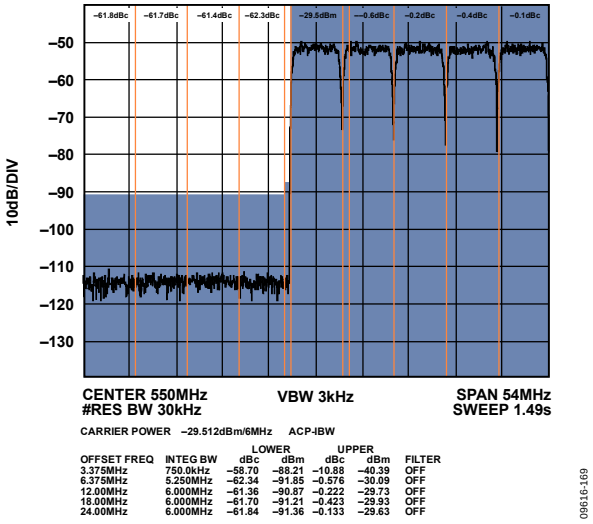


Figure 70. Mid Band Narrow-Band ACLR (Worse Side)

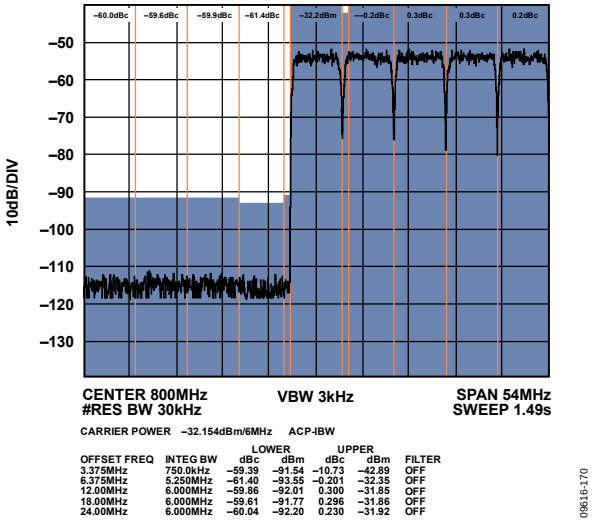


Figure 71. High Band Narrow-Band ACLR

64- AND 128-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

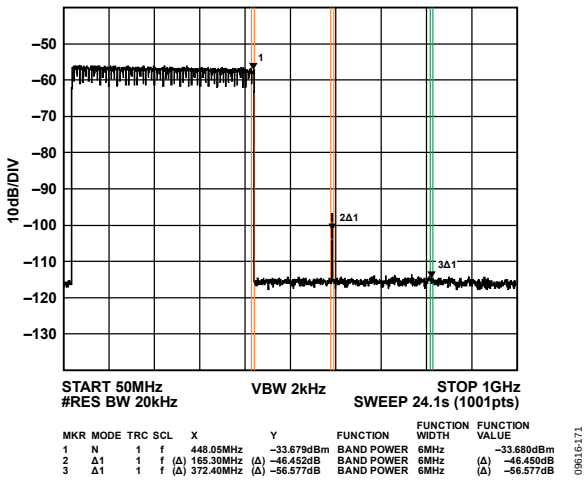


Figure 72. Low Band Wideband ACLR

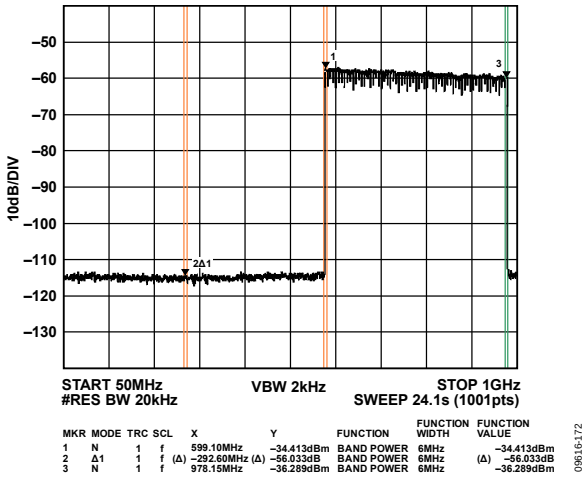


Figure 73. High Band Wideband ACLR

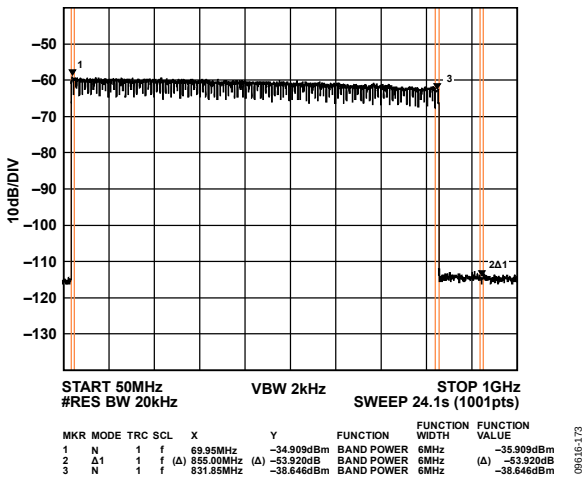


Figure 74. 128-Carrier Low Band Wideband ACLR

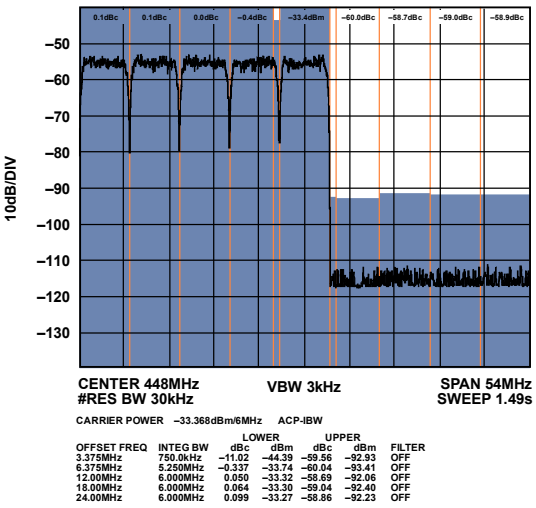


Figure 75. 64-Carrier Low Band Narrow-Band ACLR

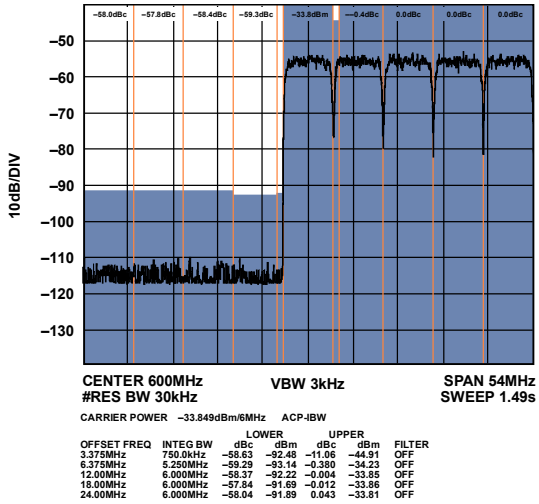


Figure 76. 64-Carrier High Band Narrow-Band ACLR

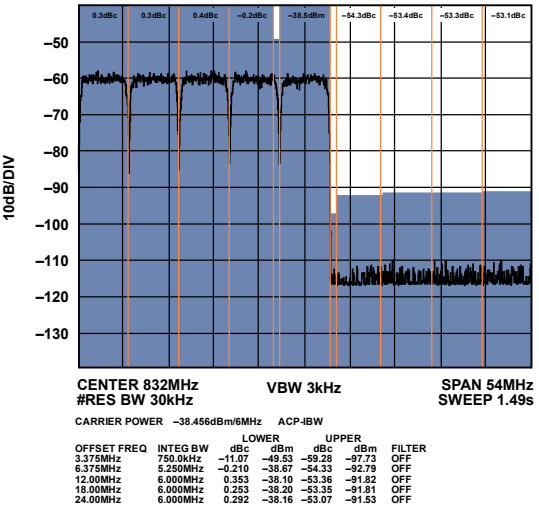


Figure 77. 128-Carrier Narrow-Band ACLR

TYPICAL PERFORMANCE CHARACTERISTICS—AD9739A

STATIC LINEARITY

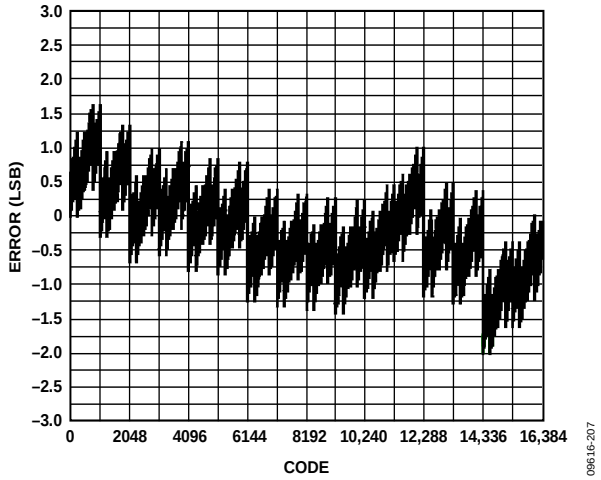


Figure 78. Typical INL, 20 mA at 25°C

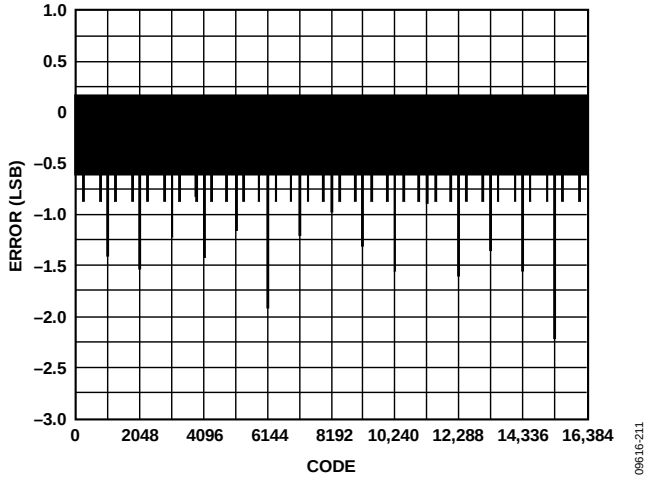


Figure 81. Typical DNL, 20 mA at –40°C

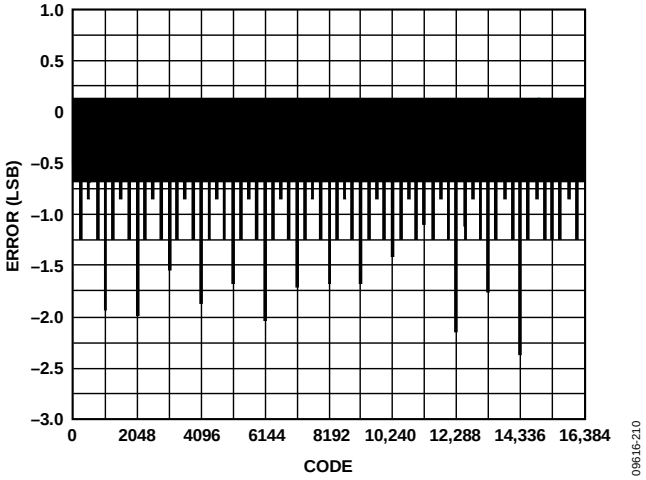


Figure 79. Typical DNL, 20 mA at 25°C

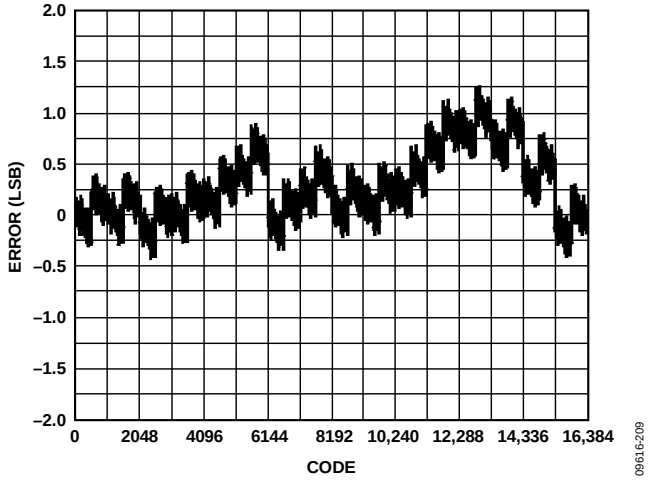


Figure 82. Typical INL, 20 mA at 85°C

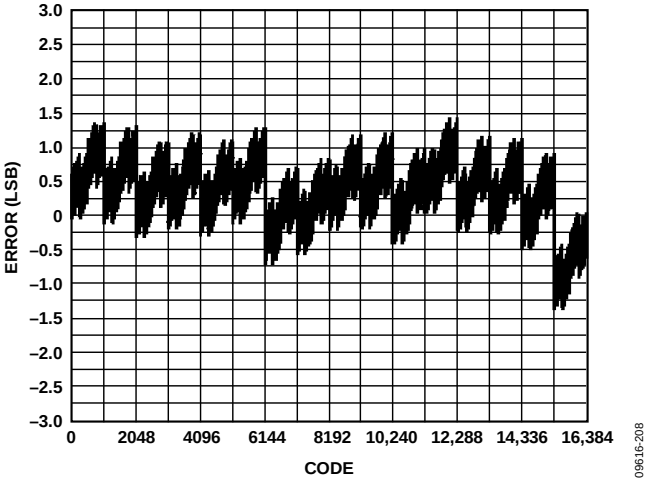


Figure 80. Typical INL, 20 mA at –40°C

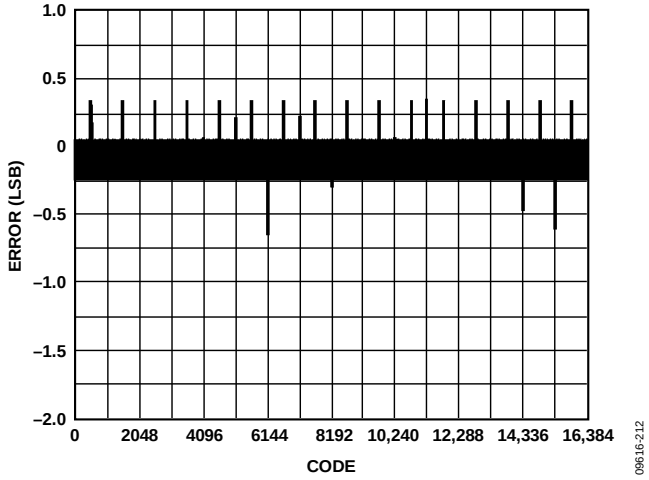


Figure 83. Typical DNL, 20 mA at 85°C

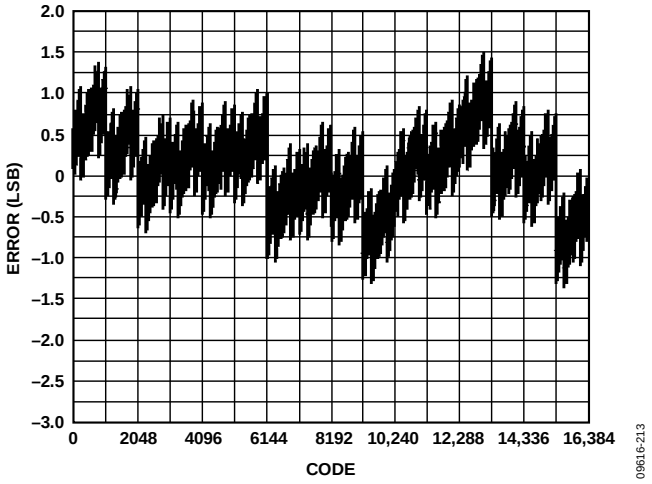


Figure 84. Typical INL, 10 mA at 25°C

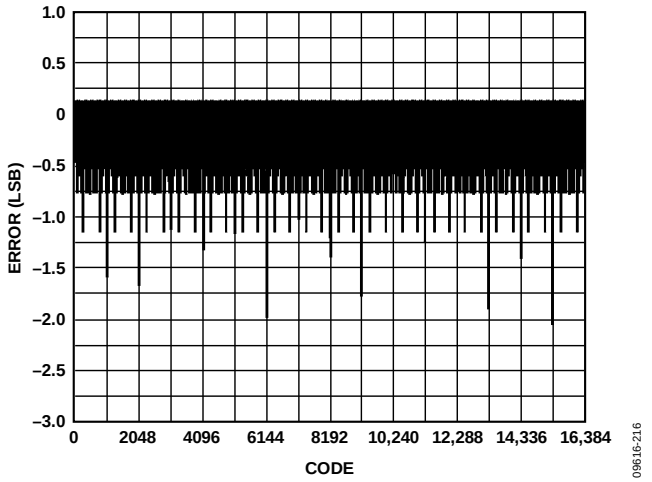


Figure 85. Typical DNL, 10 mA at 25°C

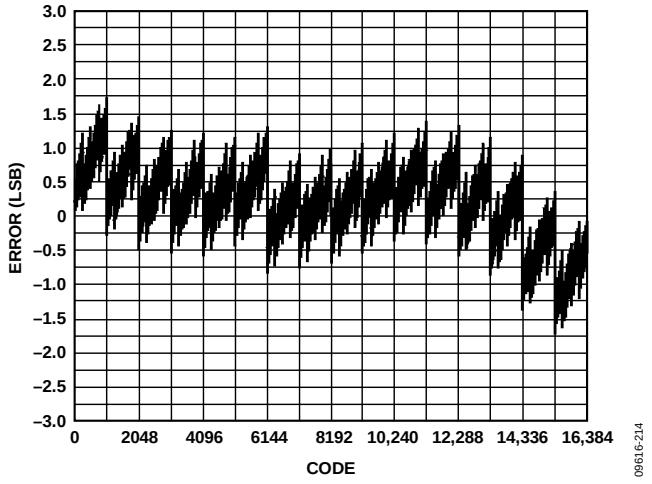


Figure 86. Typical INL, 30 mA at 25°C

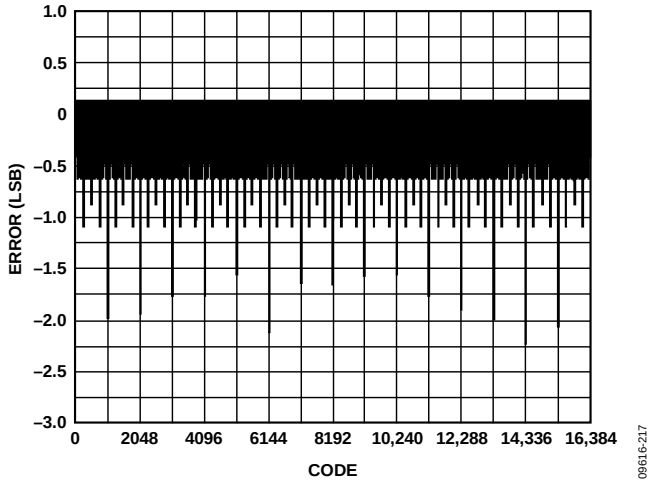


Figure 87. Typical DNL, 30 mA at 25°C

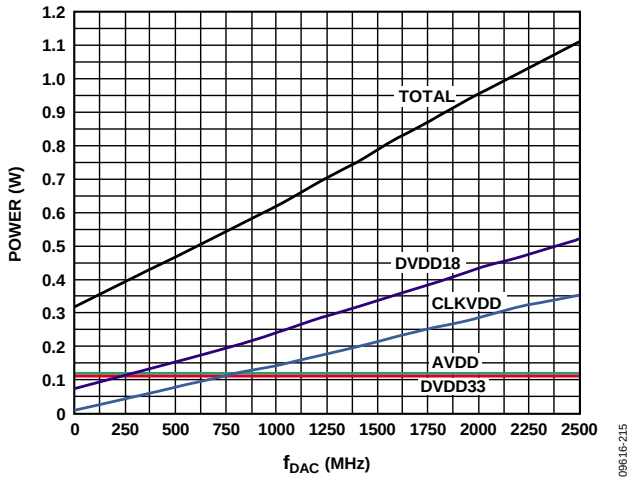


Figure 88. Power Consumption vs. f_{DAC} at 25°C

AC (NORMAL MODE)

I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

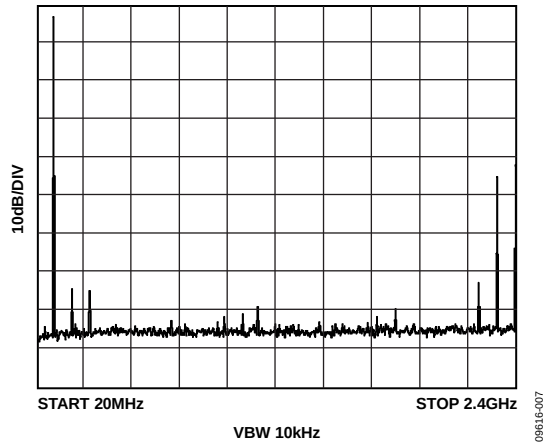


Figure 89. Single-Tone Spectrum at f_{OUT} = 91 MHz, f_{DAC} = 2.4 GSPS

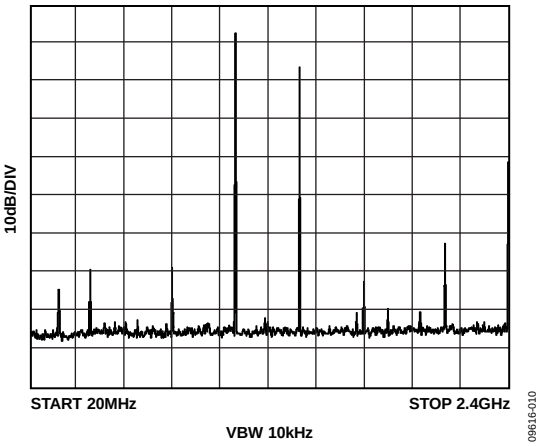


Figure 92. Single-Tone Spectrum at f_{OUT} = 1091 MHz, f_{DAC} = 2.4 GSPS

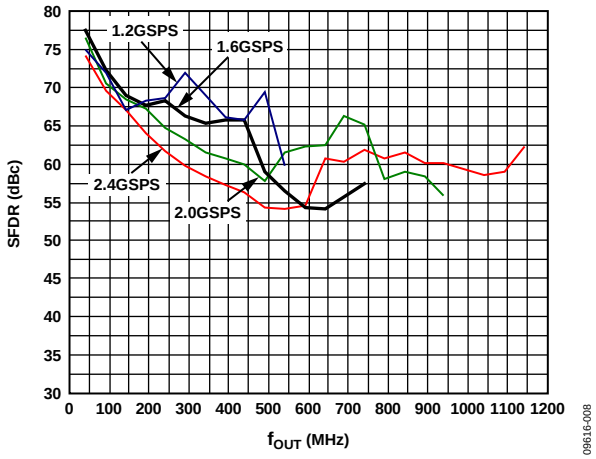


Figure 90. SFDR vs. f_{OUT} over f_{DAC}

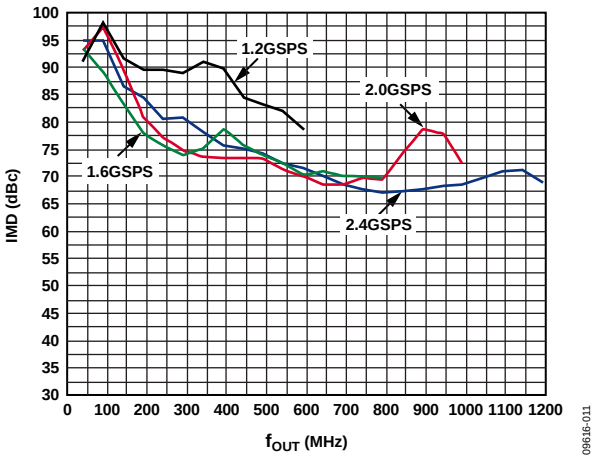


Figure 93. IMD vs. f_{OUT} over f_{DAC}

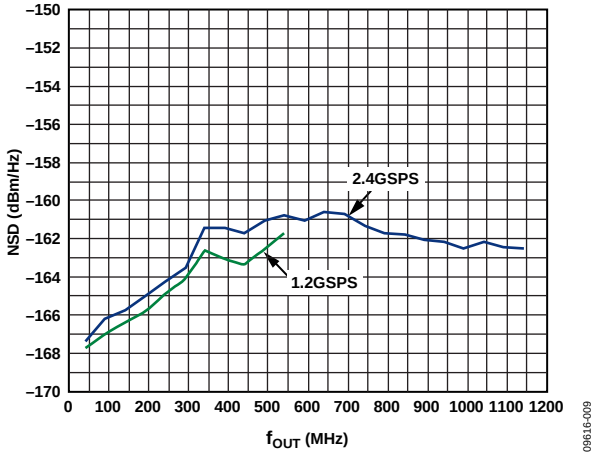


Figure 91. Single-Tone NSD vs. f_{OUT}

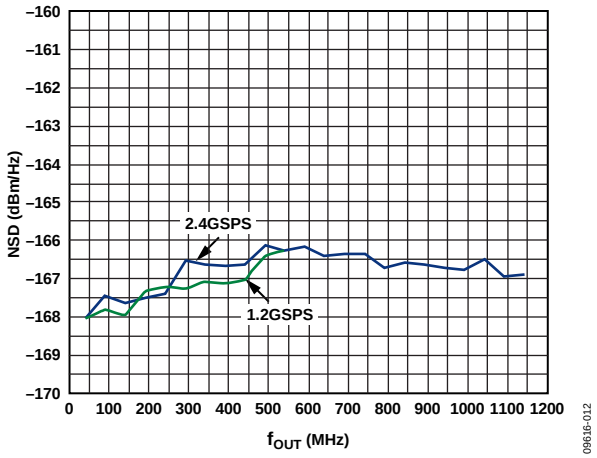


Figure 94. Eight-Tone NSD vs. f_{OUT}

f_{DAC} = 2 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

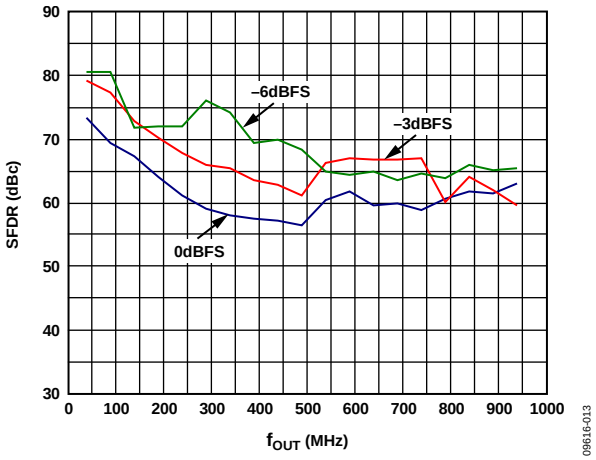


Figure 95. SFDR vs. f_{OUT} over Digital Full Scale

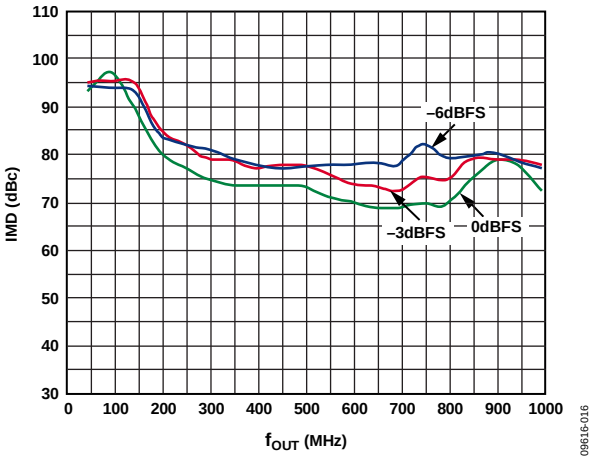


Figure 98. IMD vs. f_{OUT} over Digital Full Scale

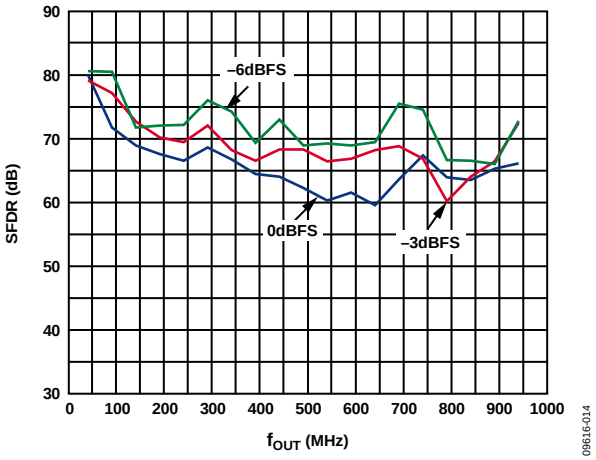


Figure 96. SFDR for Second Harmonic over f_{OUT} vs. Digital Full Scale

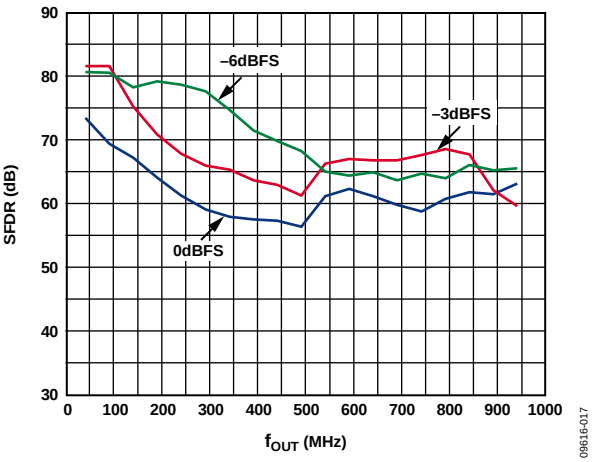


Figure 99. SFDR for Third Harmonic over f_{OUT} vs. Digital Full Scale

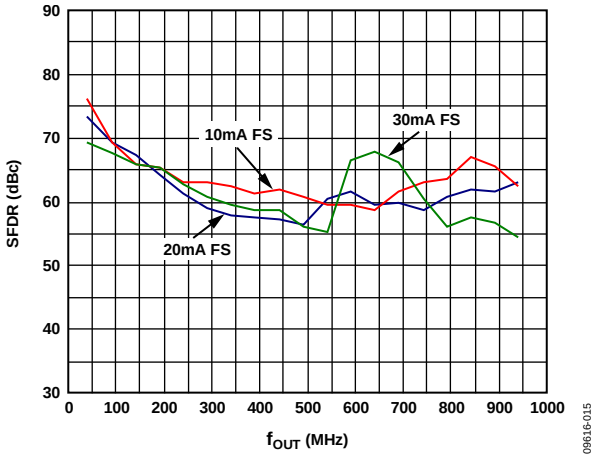


Figure 97. SFDR vs. f_{OUT} over DAC I_{OUTFS}

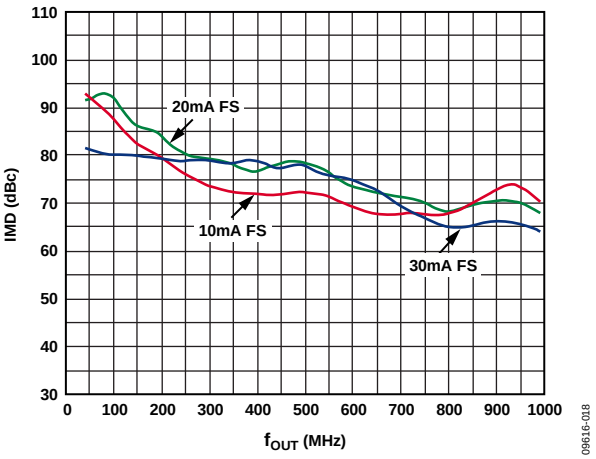


Figure 100. IMD vs. f_{OUT} over DAC I_{OUTFS}

f_{DAC} = 2 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

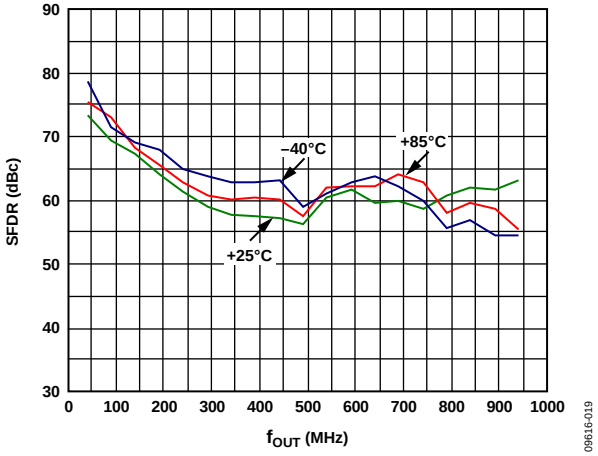


Figure 101. SFDR vs. f_{OUT} over Temperature

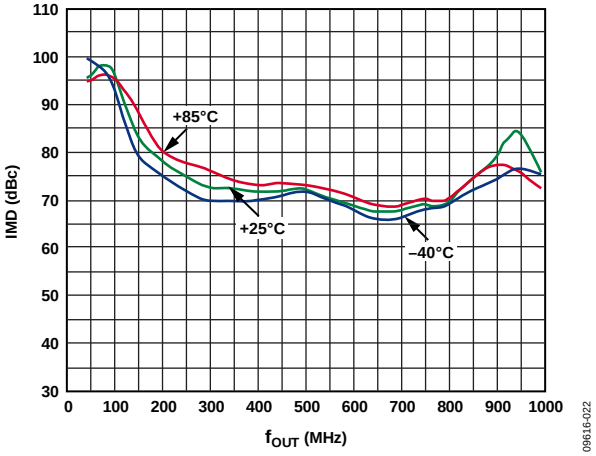


Figure 104. IMD vs. f_{OUT} over Temperature

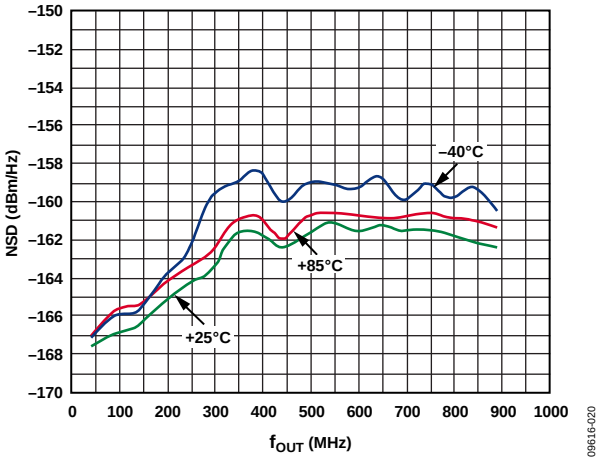


Figure 102. Single-Tone NSD vs. f_{OUT} over Temperature

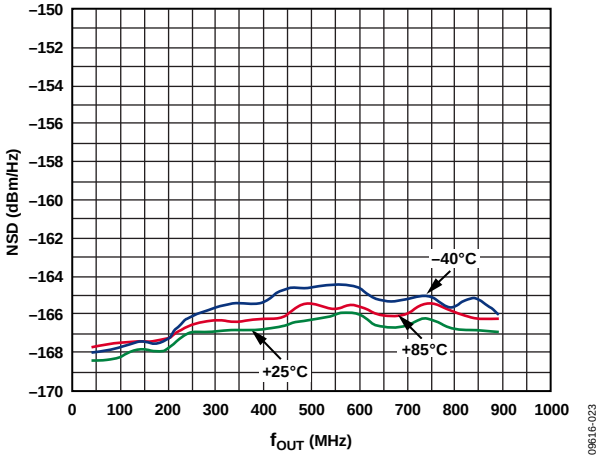
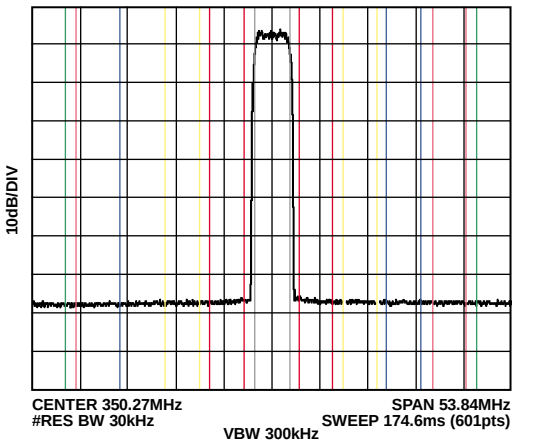


Figure 105. Eight-Tone NSD vs. f_{OUT} over Temperature



RMS RESULTS	FREQ OFFSET	REF BW	LOWER		UPPER	
CARRIER POWER	(MHz)	(MHz)	(dBc)	(dBm)	(dBc)	(dBm)
–14.54dBm/	5	3.84	–79.90	–94.44	–79.03	–93.57
3.84MHz	10	3.84	–80.60	–95.14	–79.36	–94.40
	15	3.84	–80.90	–95.45	–80.73	–95.27
	20	3.84	–80.62	–95.16	–80.97	–95.51
	25	3.84	–80.76	–95.30	–80.95	–95.49

Figure 103. Single-Carrier WCDMA at 350 MHz, f_{DAC} = 2457.6 MSPS

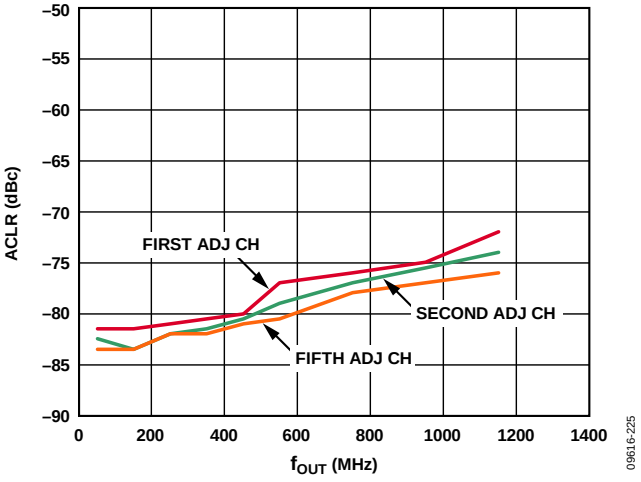


Figure 106. Single-Carrier WCDMA ACLR vs. f_{OUT} at 2457.6 MSPS

AC (MIX-MODE)

f_{DAC} = 2.4 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.

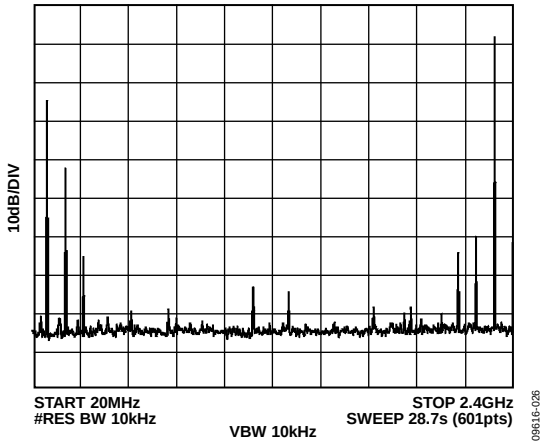


Figure 107. Single-Tone Spectrum at f_{OUT} = 2.31 GHz, f_{DAC} = 2.4 GSPS

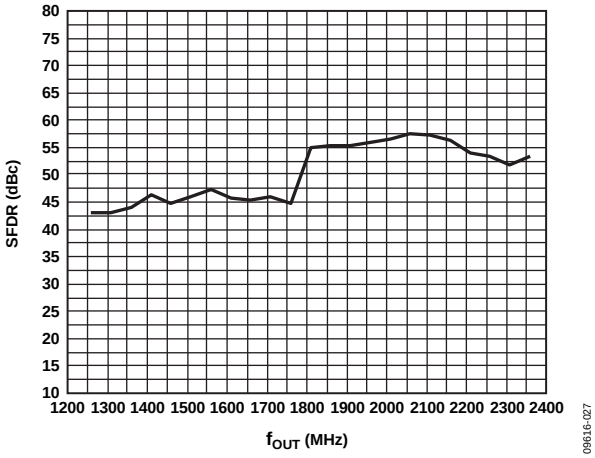


Figure 108. SFDR in Mix-Mode vs. f_{OUT} at 2.4 GSPS

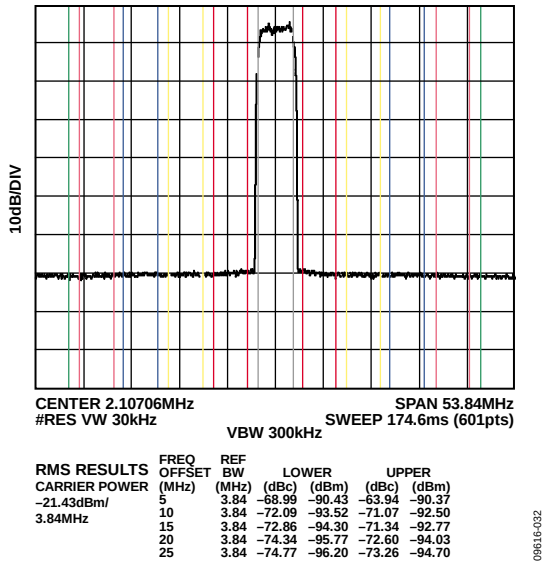


Figure 109. Typical Single-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)

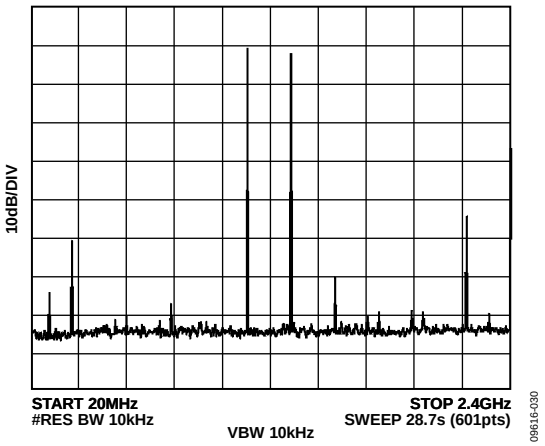


Figure 110. Single-Tone Spectrum in Mix-Mode at f_{OUT} = 1.31 GHz, f_{DAC} = 2.4 GSPS

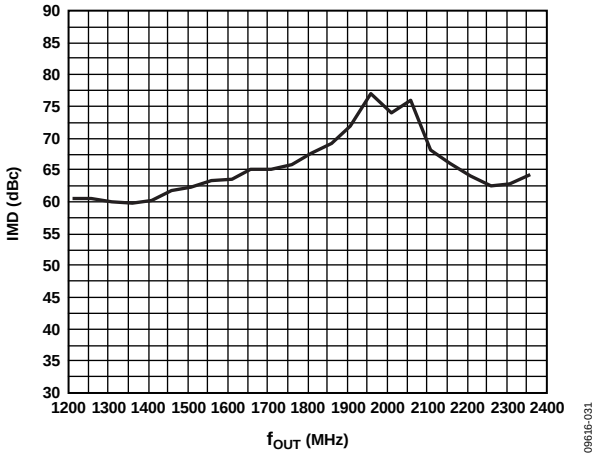


Figure 111. IMD in Mix-Mode vs. f_{OUT} at 2.4 GSPS

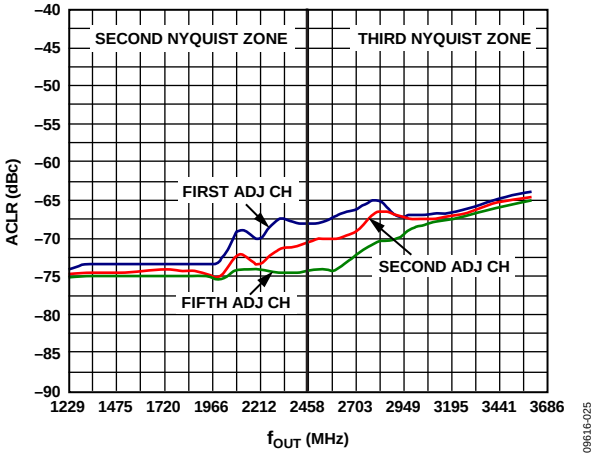
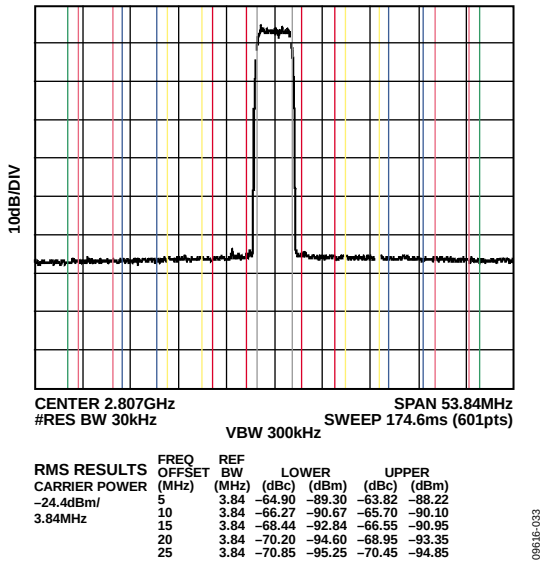


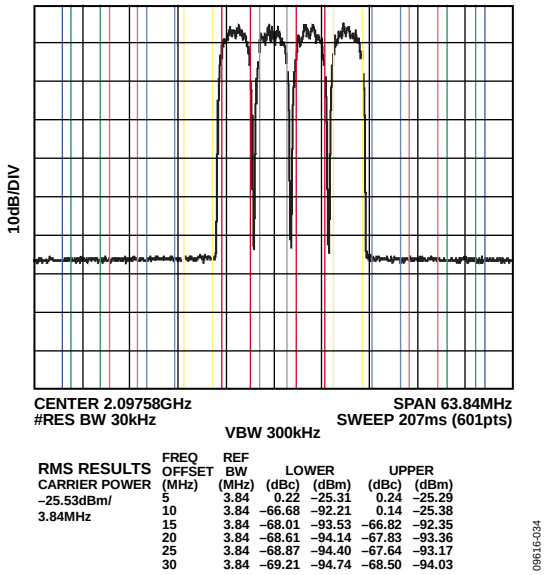
Figure 112. Single-Carrier WCDMA ACLR vs. f_{OUT} at 2457.6 MSPS

f_{DAC} = 2.4 GSPS, I_{OUTFS} = 20 mA, nominal supplies, T_A = 25°C, unless otherwise noted.



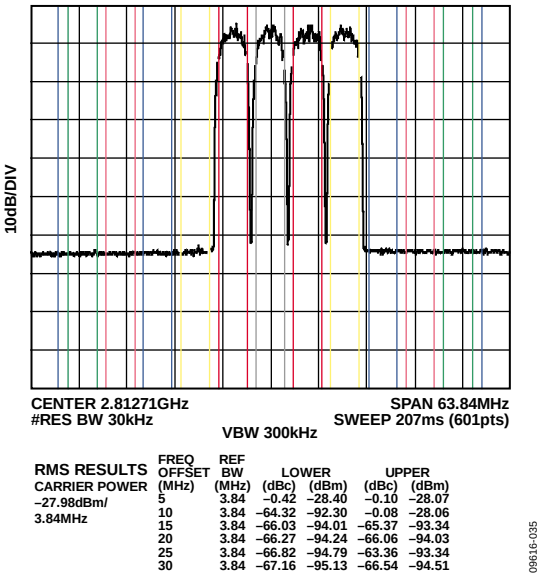
RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–24.4dBm/	5	3.84	–64.90	–89.30	–63.82	–88.22
3.84MHz	10	3.84	–66.27	–90.67	–65.70	–90.10
	15	3.84	–68.44	–92.84	–66.55	–90.95
	20	3.84	–70.20	–94.60	–68.95	–93.35
	25	3.84	–70.85	–95.25	–70.45	–94.85

Figure 113. Typical Single-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)



RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–25.53dBm/	5	3.84	0.22	–25.31	0.24	–25.29
3.84MHz	10	3.84	–66.68	–92.21	0.14	–25.38
	15	3.84	–68.01	–93.53	–66.82	–92.35
	20	3.84	–68.61	–94.14	–67.83	–93.36
	25	3.84	–68.87	–94.40	–67.64	–93.17
	30	3.84	–69.21	–94.74	–68.50	–94.03

Figure 114. Typical Four-Carrier WCDMA ACLR Performance at 2.1 GHz, f_{DAC} = 2457.6 MSPS (Second Nyquist Zone)

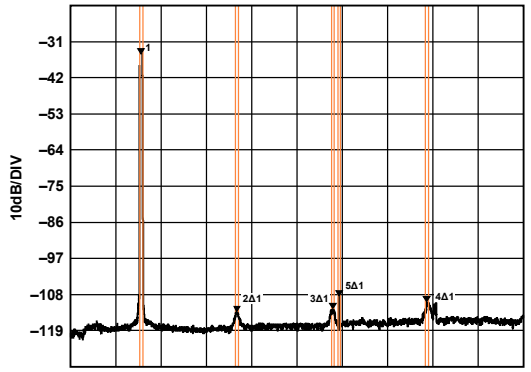


RMS RESULTS CARRIER POWER	FREQ OFFSET (MHz)	REF BW (MHz)	LOWER (dBc)	LOWER (dBm)	UPPER (dBc)	UPPER (dBm)
–27.98dBm/	5	3.84	–0.42	–28.40	–0.10	–28.07
3.84MHz	10	3.84	–64.32	–92.30	–0.08	–28.06
	15	3.84	–66.03	–94.01	–65.37	–93.34
	20	3.84	–66.27	–94.24	–66.06	–94.03
	25	3.84	–66.82	–94.79	–63.36	–93.34
	30	3.84	–67.16	–95.13	–66.54	–94.51

Figure 115. Typical Four-Carrier WCDMA ACLR Performance at 2.8 GHz, f_{DAC} = 2457.6 MSPS (Third Nyquist Zone)

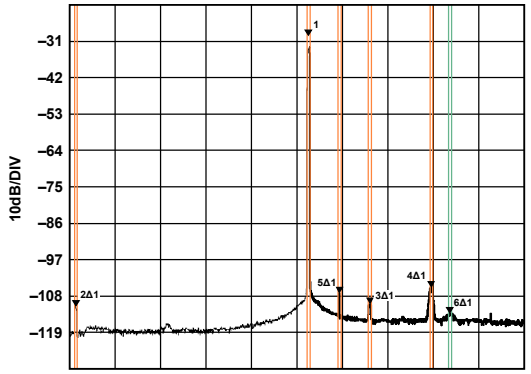
ONE-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

f_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.



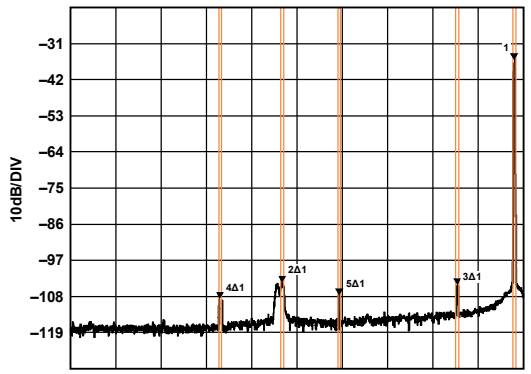
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	200.00MHz	−11.476dBm	BAND POWER	6MHz	−11.475dBm
2	Δ1	1	f	(Δ) 199.60MHz	(Δ) −77.042dB	BAND POWER	6MHz	(Δ) −77.042dB
3	Δ1	1	f	(Δ) 400.05MHz	(Δ) −76.238dB	BAND POWER	6MHz	(Δ) −76.238dB
4	Δ1	1	f	(Δ) 597.65MHz	(Δ) −74.526dB	BAND POWER	6MHz	(Δ) −74.526dB
5	Δ1	1	f	(Δ) 413.35MHz	(Δ) −75.919dB	BAND POWER	6MHz	(Δ) −75.919dB

Figure 116. Low Band Wideband ACLR



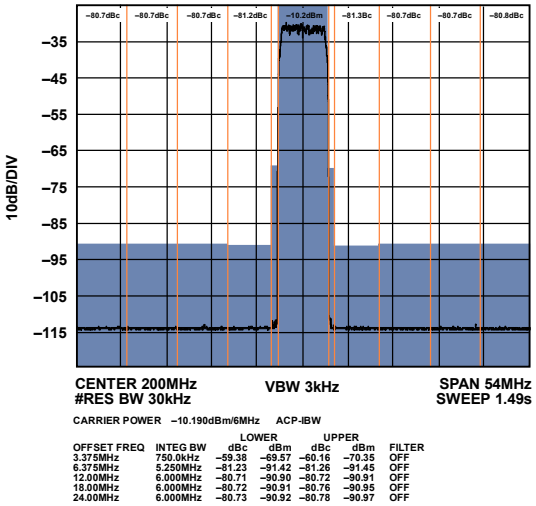
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	549.60MHz	−10.231dBm	BAND POWER	6MHz	−10.231dBm
2	Δ1	1	f	(Δ) −485.35MHz	(Δ) −76.444dB	BAND POWER	6MHz	(Δ) −76.425dB
3	Δ1	1	f	(Δ) 127.40MHz	(Δ) −75.649dB	BAND POWER	6MHz	(Δ) −75.626dB
4	Δ1	1	f	(Δ) 254.70MHz	(Δ) −70.658dB	BAND POWER	6MHz	(Δ) −70.658dB
5	Δ1	1	f	(Δ) 63.75MHz	(Δ) −75.836dB	BAND POWER	6MHz	(Δ) −75.824dB
6	Δ1	1	f	(Δ) 293.65MHz	(Δ) −78.054dB	BAND POWER	6MHz	(Δ) −78.118dB

Figure 117. Mid Band Wideband ACLR



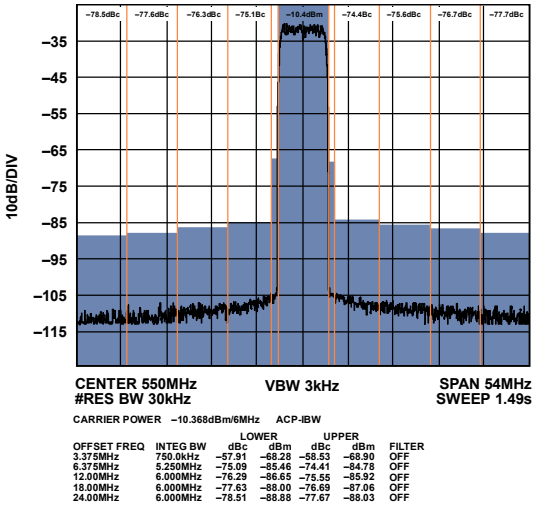
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	979.00MHz	−13.703dBm	BAND POWER	6MHz	−13.658dBm
2	Δ1	1	f	(Δ) −484.40MHz	(Δ) −65.548dB	BAND POWER	6MHz	(Δ) −66.548dB
3	Δ1	1	f	(Δ) −118.65MHz	(Δ) −66.990dB	BAND POWER	6MHz	(Δ) −66.990dB
4	Δ1	1	f	(Δ) −613.60MHz	(Δ) −69.044dB	BAND POWER	6MHz	(Δ) −69.049dB
5	Δ1	1	f	(Δ) −365.65MHz	(Δ) −72.789dB	BAND POWER	6MHz	(Δ) −72.789dB

Figure 118. High Band Wideband ACLR



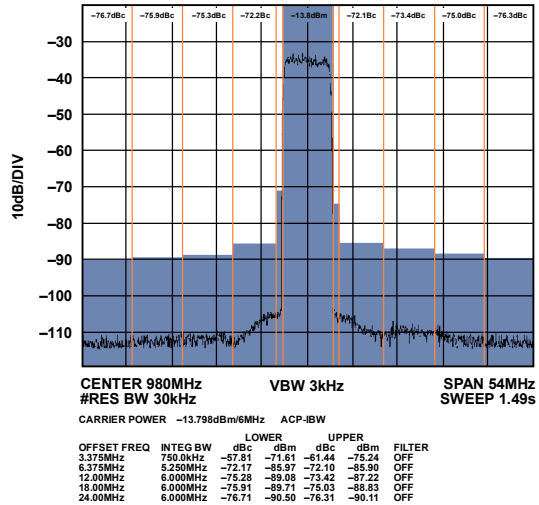
OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
3.375MHz	750.0kHz	−59.38	−69.57	−60.16	−70.35	OFF
6.375MHz	5.250MHz	−81.23	−91.42	−81.26	−91.45	OFF
12.00MHz	6.000MHz	−80.71	−90.90	−80.72	−90.91	OFF
18.00MHz	6.000MHz	−80.72	−90.91	−80.76	−90.95	OFF
24.00MHz	6.000MHz	−80.73	−90.92	−80.78	−90.97	OFF

Figure 119. Low Band Narrow-Band ACLR



OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
3.375MHz	750.0kHz	−57.91	−68.28	−58.53	−68.90	OFF
6.375MHz	5.250MHz	−75.09	−85.46	−74.41	−84.78	OFF
12.00MHz	6.000MHz	−76.29	−86.65	−75.55	−85.92	OFF
18.00MHz	6.000MHz	−77.63	−88.00	−76.69	−87.06	OFF
24.00MHz	6.000MHz	−78.51	−88.88	−77.67	−88.03	OFF

Figure 120. Mid Band Narrow-Band ACLR



OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
3.375MHz	750.0kHz	−57.81	−71.61	−61.44	−75.24	OFF
6.375MHz	5.250MHz	−72.17	−85.97	−72.10	−85.90	OFF
12.00MHz	6.000MHz	−75.28	−89.08	−73.42	−87.22	OFF
18.00MHz	6.000MHz	−75.91	−89.71	−75.03	−88.83	OFF
24.00MHz	6.000MHz	−76.71	−90.50	−76.31	−90.11	OFF

Figure 121. High Band Narrow-Band ACLR

FOUR-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

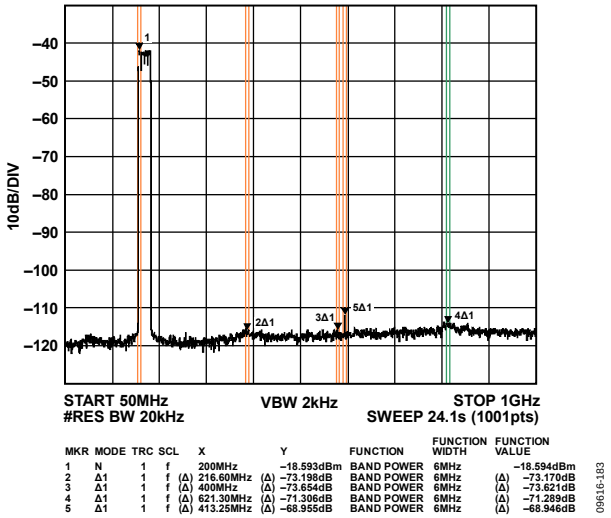


Figure 122. Low Band Wideband ACLR

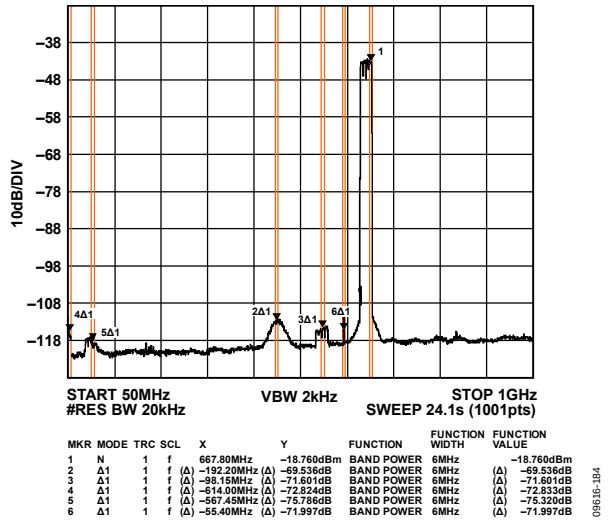


Figure 123. Mid Band Wideband ACLR

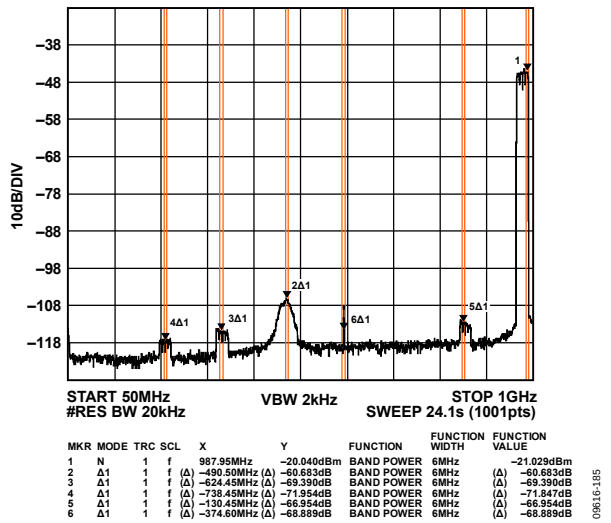


Figure 124. High Band Wideband ACLR

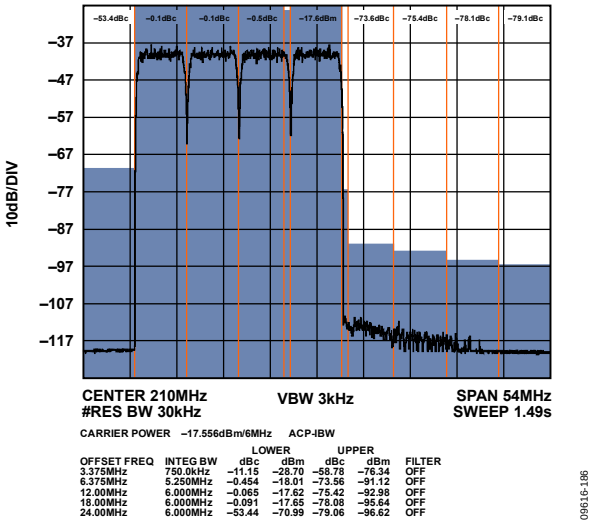


Figure 125. Low Band Narrow-Band ACLR (Worse Side)

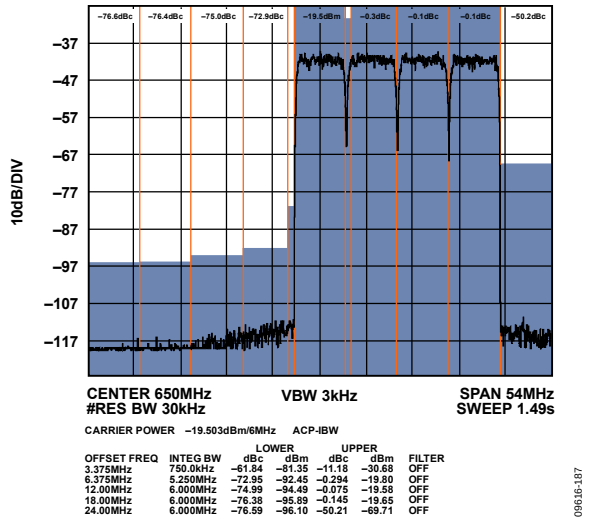


Figure 126. Mid Band Narrow-Band ACLR (Worse Side)

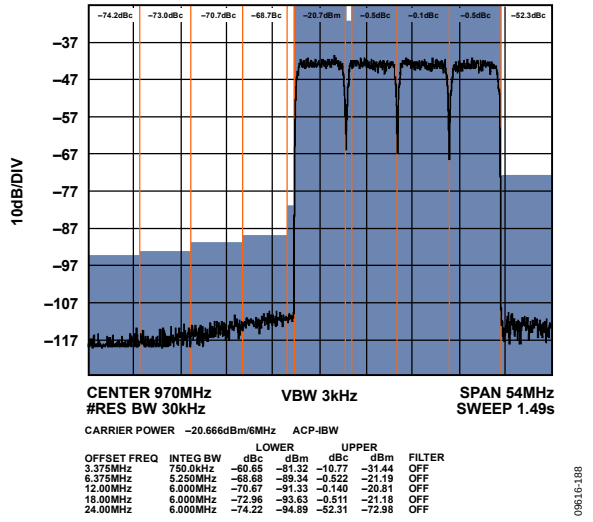


Figure 127. High Band Narrow-Band ACLR

EIGHT-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

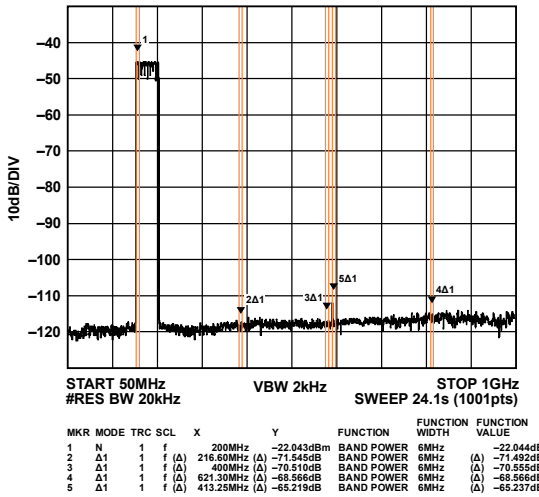


Figure 128. Low Band Wideband ACLR

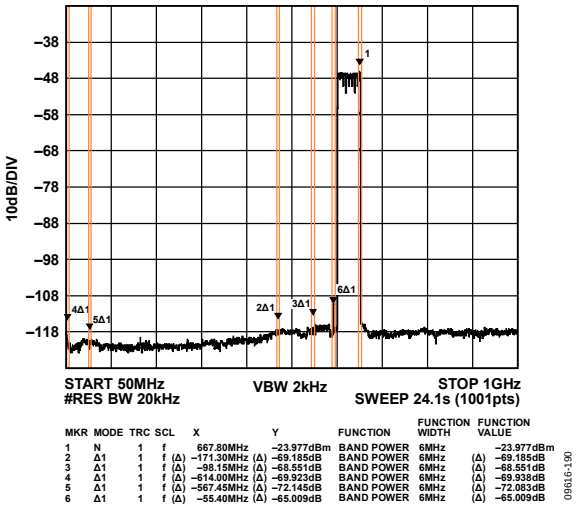


Figure 129. Mid Band Wideband ACLR

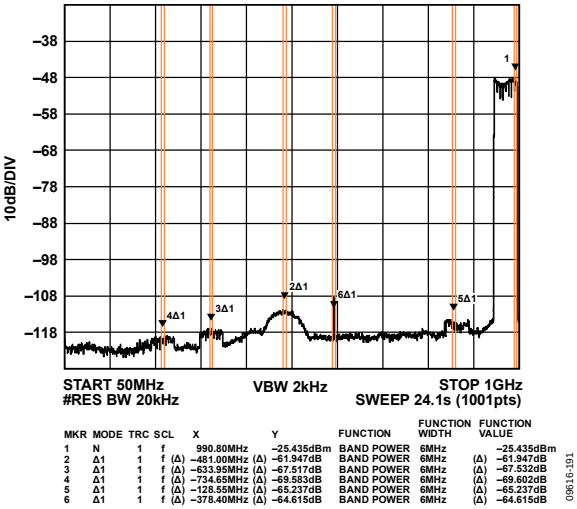


Figure 130. High Band Wideband ACLR

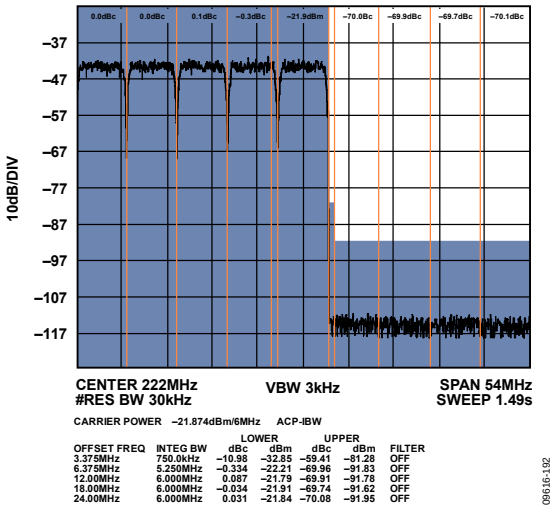


Figure 131. Low Band Narrow-Band ACLR (Worse Side)

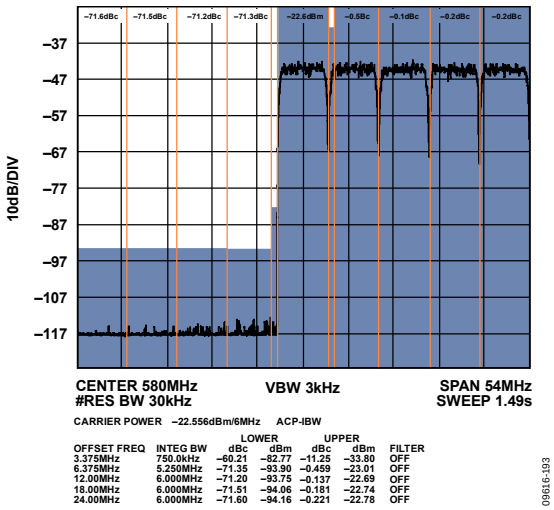


Figure 132. Mid Band Narrow-Band ACLR (Worse Side)

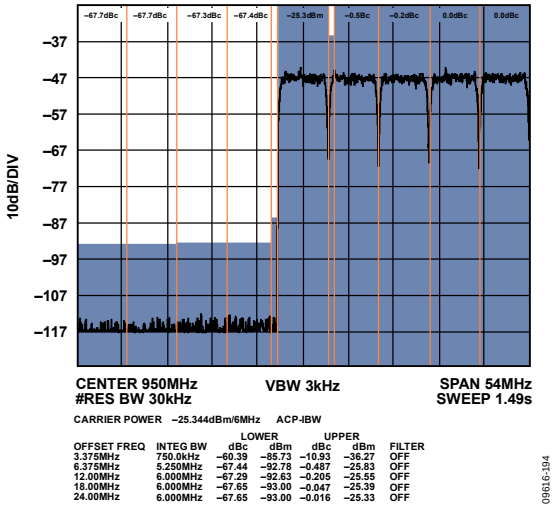
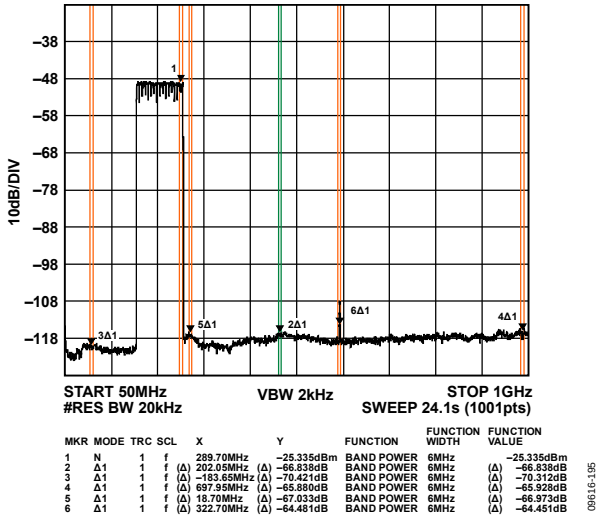


Figure 133. High Band Narrow-Band ACLR

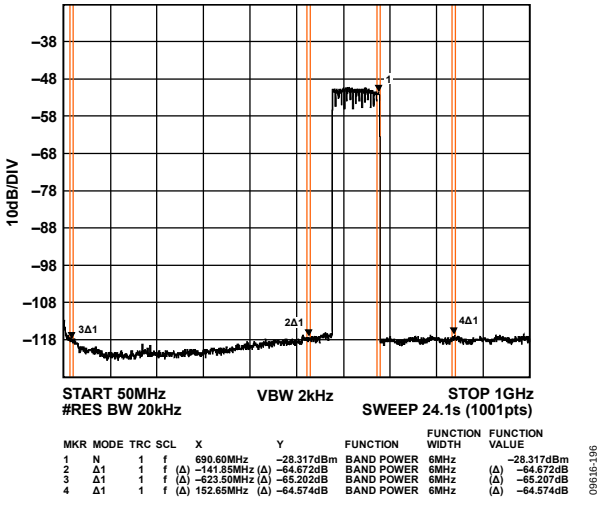
16-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.



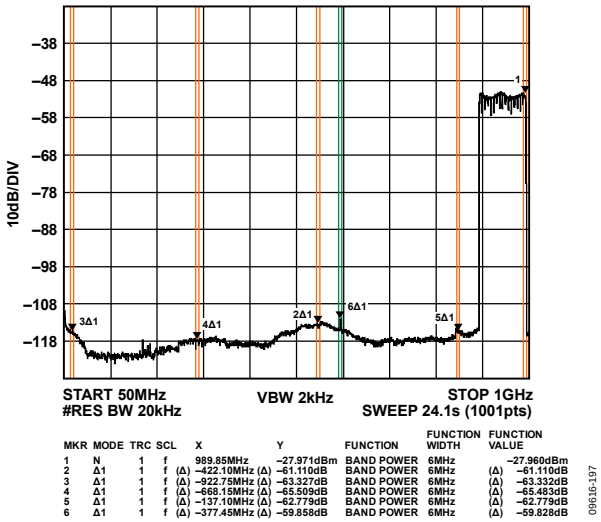
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	289.70MHz	−25.335dBm	BAND POWER	6MHz	−25.335dBm
2	Δ1	1	f	(Δ) 202.05MHz	(Δ) −66.838dB	BAND POWER	6MHz	(Δ) −66.838dB
3	Δ1	1	f	(Δ) −183.65MHz	(Δ) −70.421dB	BAND POWER	6MHz	(Δ) −70.312dB
4	Δ1	1	f	(Δ) 697.95MHz	(Δ) −65.880dB	BAND POWER	6MHz	(Δ) −65.928dB
5	Δ1	1	f	(Δ) 18.70MHz	(Δ) −67.033dB	BAND POWER	6MHz	(Δ) −66.973dB
6	Δ1	1	f	(Δ) 322.70MHz	(Δ) −64.481dB	BAND POWER	6MHz	(Δ) −64.451dB

Figure 134. Low Band Wideband ACLR



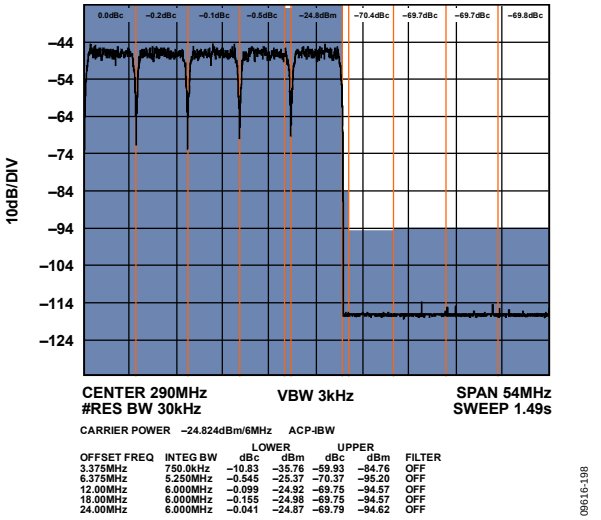
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	690.60MHz	−28.317dBm	BAND POWER	6MHz	−28.317dBm
2	Δ1	1	f	(Δ) −141.85MHz	(Δ) −64.672dB	BAND POWER	6MHz	(Δ) −64.672dB
3	Δ1	1	f	(Δ) −623.50MHz	(Δ) −65.202dB	BAND POWER	6MHz	(Δ) −65.207dB
4	Δ1	1	f	(Δ) 152.65MHz	(Δ) −64.574dB	BAND POWER	6MHz	(Δ) −64.574dB

Figure 135. Mid Band Wideband ACLR



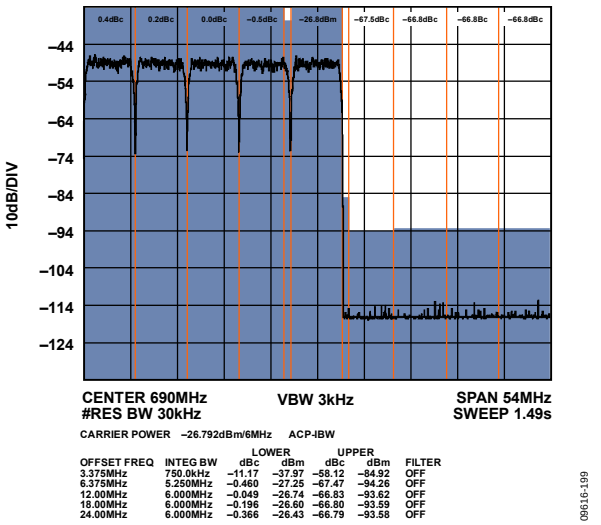
MKR	MODE	TRC	SCL	X	Y	FUNCTION	FUNCTION WIDTH	FUNCTION VALUE
1	N	1	f	989.85MHz	−27.971dBm	BAND POWER	6MHz	−27.960dBm
2	Δ1	1	f	(Δ) −422.10MHz	(Δ) −61.110dB	BAND POWER	6MHz	(Δ) −61.110dB
3	Δ1	1	f	(Δ) −922.75MHz	(Δ) −63.327dB	BAND POWER	6MHz	(Δ) −63.332dB
4	Δ1	1	f	(Δ) −668.15MHz	(Δ) −65.509dB	BAND POWER	6MHz	(Δ) −65.483dB
5	Δ1	1	f	(Δ) −137.10MHz	(Δ) −62.779dB	BAND POWER	6MHz	(Δ) −62.779dB
6	Δ1	1	f	(Δ) −377.45MHz	(Δ) −59.858dB	BAND POWER	6MHz	(Δ) −59.828dB

Figure 136. High Band Wideband ACLR



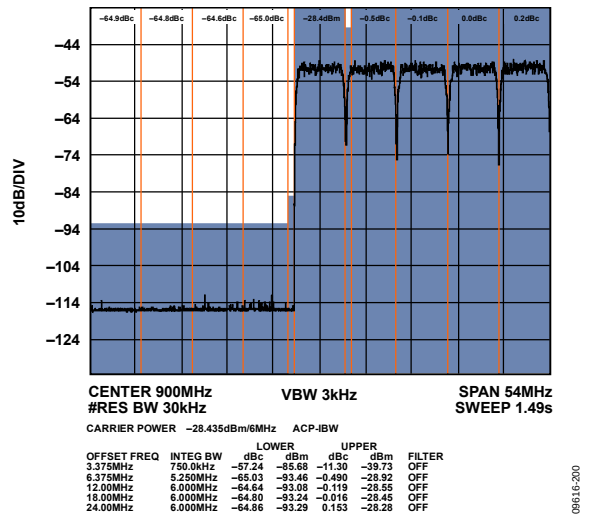
OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
3.375MHz	750.0kHz	−10.83	−35.76	−59.93	−84.76	OFF
6.375MHz	5.250MHz	−0.545	−25.37	−70.37	−95.20	OFF
12.00MHz	6.000MHz	−0.099	−24.92	−69.75	−94.57	OFF
18.00MHz	6.000MHz	−0.155	−24.98	−69.75	−94.57	OFF
24.00MHz	6.000MHz	−0.041	−24.87	−69.79	−94.62	OFF

Figure 137. Low Band Narrow-Band ACLR



OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
3.375MHz	750.0kHz	−11.17	−37.97	−58.12	−84.92	OFF
6.375MHz	5.250MHz	−0.460	−27.25	−67.47	−94.26	OFF
12.00MHz	6.000MHz	−0.049	−26.74	−66.83	−93.62	OFF
18.00MHz	6.000MHz	−0.196	−26.60	−66.80	−93.59	OFF
24.00MHz	6.000MHz	−0.366	−26.43	−66.79	−93.58	OFF

Figure 138. Mid Band Narrow-Band ACLR (Worse Side)



OFFSET FREQ	INTEG BW	LOWER dBc	LOWER dBm	UPPER dBc	UPPER dBm	FILTER
3.375MHz	750.0kHz	−57.24	−85.68	−11.30	−39.73	OFF
6.375MHz	5.250MHz	−65.03	−93.46	−0.490	−28.92	OFF
12.00MHz	6.000MHz	−64.64	−93.08	−0.119	−28.55	OFF
18.00MHz	6.000MHz	−64.80	−93.24	−0.016	−28.45	OFF
24.00MHz	6.000MHz	−64.86	−93.29	0.153	−28.28	OFF

Figure 139. High Band Narrow-Band ACLR

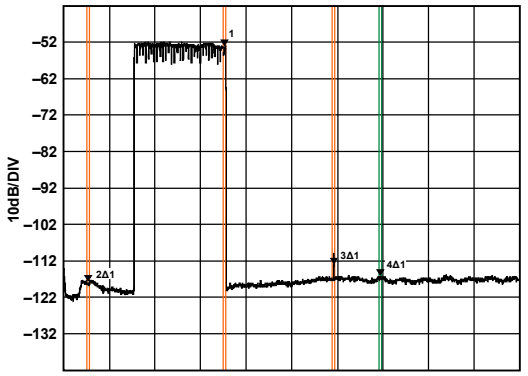


Figure 140. Low Band Wideband ACLR

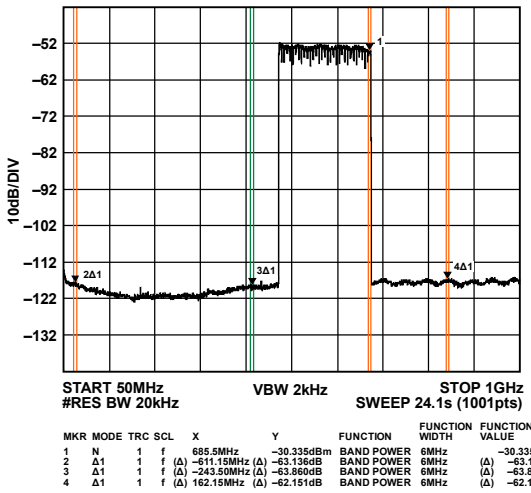


Figure 141. Mid Band Wideband ACLR

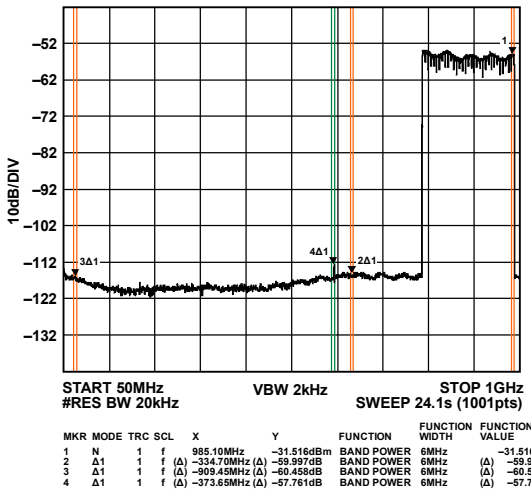


Figure 142. High Band Wideband ACLR

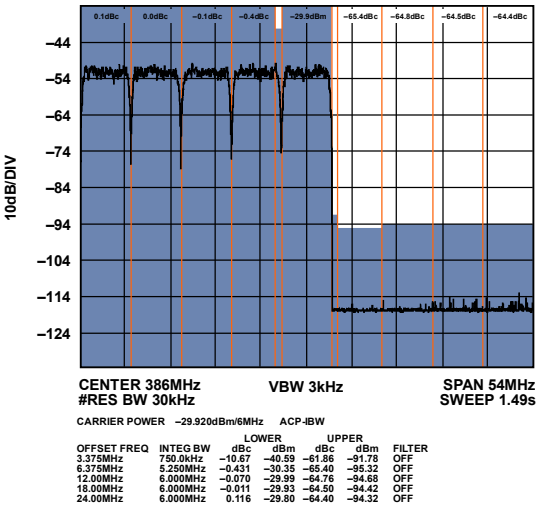


Figure 143. Low Band Narrow-Band ACLR

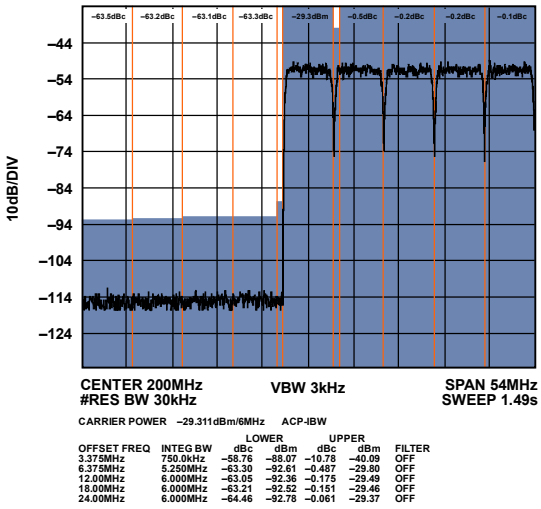


Figure 144. Mid Band Narrow-Band ACLR (Worse Side)

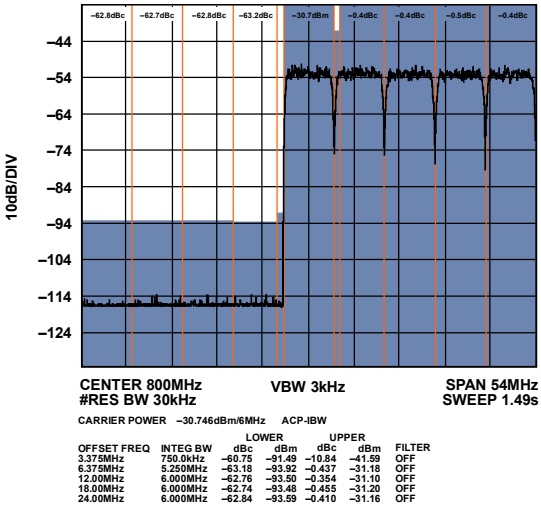


Figure 145. High Band Narrow-Band ACLR

64- AND 128-CARRIER DOCSIS PERFORMANCE (NORMAL MODE)

I_{OUTFS} = 20 mA, f_{DAC} = 2.4576 GSPS, nominal supplies, T_A = 25°C, unless otherwise noted.

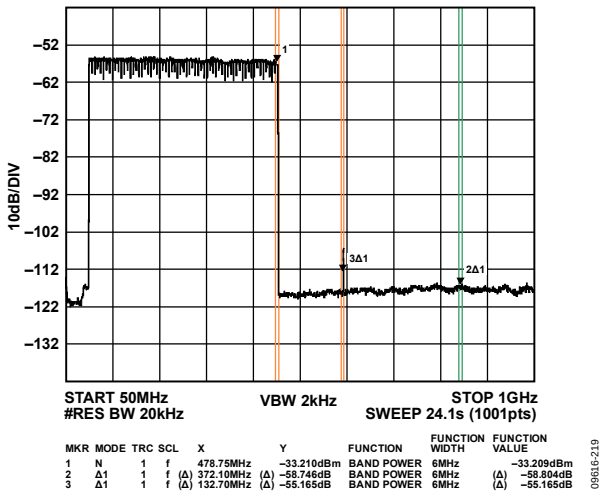


Figure 146. 64-Carrier Low Band Wideband ACLR

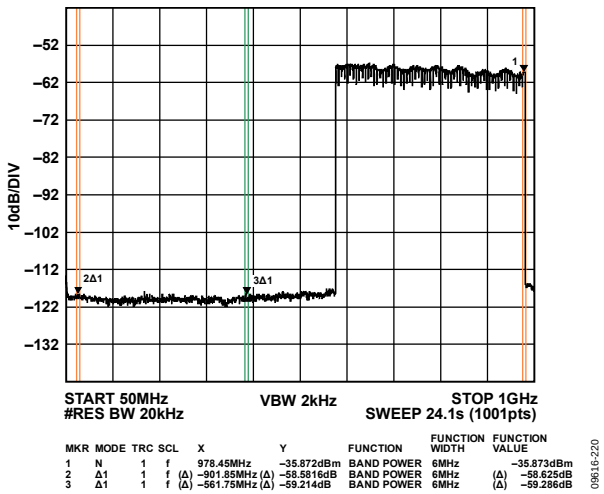


Figure 147. 64-Carrier High Band Wideband ACLR

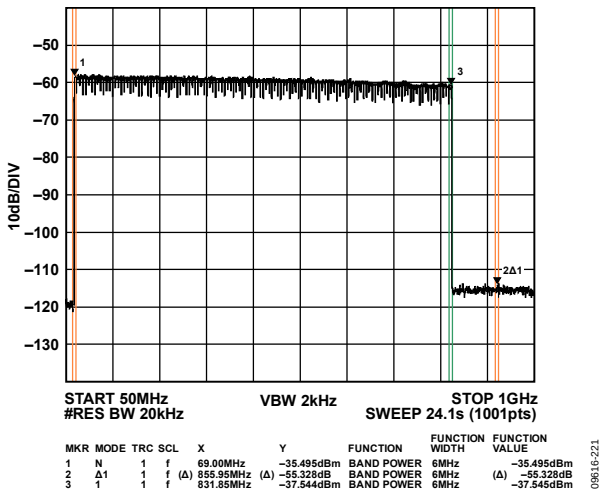


Figure 148. 128-Carrier Wideband ACLR

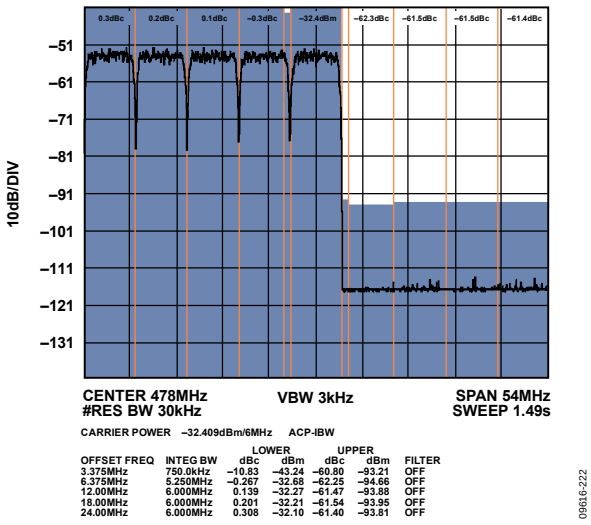


Figure 149. 64-Carrier Low Band Narrow-Band ACLR

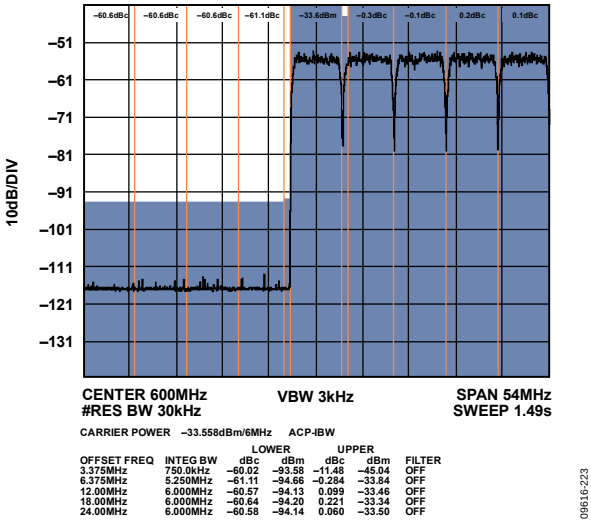


Figure 150. 64-Carrier High Band Narrow-Band ACLR

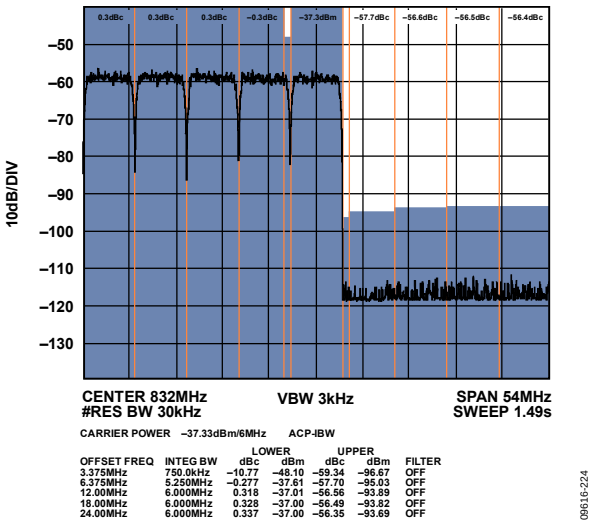


Figure 151. 128-Carrier Narrow-Band ACLR

TERMINOLOGY

Linearity Error (Integral Nonlinearity or INL)
The maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from 0 to full scale.

Differential Nonlinearity (DNL)
The measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A DAC is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of 0 is called the offset error. For IOUTP, 0 mA output is expected when the inputs are all 0s. For IOUTN, 0 mA output is expected when all inputs are set to 1.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1 minus the output when all inputs are set to 0.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown, resulting in nonlinear performance.

Temperature Drift
Specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Spurious-Free Dynamic Range
The difference, in decibels (dB), between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Noise Spectral Density (NSD)
NSD is the converter noise power per unit of bandwidth. This is usually specified in dBm/Hz in the presence of a 0 dBm full-scale signal.

Adjacent Channel Leakage Ratio (ACLR)
The adjacent channel leakage (power) ratio is a ratio, in dBc, of the measured power within a channel relative to its adjacent channels.

Modulation Error Ratio (MER)
Modulated signals create a discrete set of output values referred to as a constellation. Each symbol creates an output signal corresponding to one point on the constellation. MER is a measure of the discrepancy between the average output symbol magnitude and the rms error magnitude of the individual symbol.

Intermodulation Distortion (IMD)
IMD is the result of two or more signals at different frequencies mixing together. Many products are created according to the formula, aF1 ± bF2, where a and b are integer values.

SERIAL PORT INTERFACE (SPI) REGISTER

SPI REGISTER MAP DESCRIPTION

The AD9737A/AD9739A contain a set of programmable registers, described in Table 10, that are used to configure and monitor various internal parameters. Note the following points when programming the AD9737A/AD9739A SPI registers:

- Registers pertaining to similar functions are grouped together and assigned adjacent addresses.
- Bits that are undefined within a register should be assigned a 0 when writing to that register.
- Registers that are undefined should not be written to.
- A hardware or software reset is recommended on power-up to place SPI registers in a known state.
- A SPI initialization routine is required as part of the boot process. See Table 29 for an example procedure.

Reset

Issuing a hardware or software reset places the AD9737A/AD9739A SPI registers in a known state. All SPI registers (excluding 0x00) are set to their default states, as described in Table 10, upon issuing a reset. After issuing a reset, the SPI initialization process needs only to write to registers that are required for the boot process as well as any other register settings that must be modified, depending on the target application.

Although the AD9737A/AD9739A do feature an internal power-on reset (POR), it is still recommended that a software or hardware reset be implemented shortly after power-up. The internal reset signal is derived from a logical OR operation from the internal POR signal, the RESET pin, and the software reset state. A software reset can be issued via the reset bit (Register 0x00, Bit 5) by toggling the bit high, then low. Note that, because the MSB/LSB format may still be unknown upon initial power-up (that is, internal POR is unsuccessful), it is also recommended that the bit settings for Bits[7:5] be mirrored onto Bits[2:0] for the instruction cycle that issues a software reset. A hardware reset can be issued from a host or external supervisory IC by applying a high pulse with a minimum width of 40 ns to the RESET pin (that is, Pin F14). RESET should be tied to VSS if unused.

Table 9. SPI Registers Pertaining to SPI Options

Address (Hex)	Bit	Description
0x00	7	Enable 3-wire SPI
	6	Enable SPI LSB first
	5	Software reset

SPI OPERATION

The serial port of the AD9737A/AD9739A, shown in Figure 152, has a 3- or 4-wire SPI capability, allowing read/write access to all registers that configure the device's internal parameters. It provides a flexible, synchronous serial communications port, allowing easy interface to many industry-standard microcontrollers and microprocessors. The 3.3 V serial I/O is compatible with most synchronous transfer formats, including the Motorola® SPI and the Intel® SSR protocols.

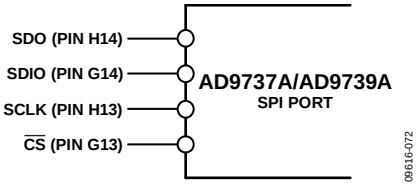


Figure 152. AD9737A/AD9739A SPI Port

The default 4-wire SPI interface consists of a clock (SCLK), serial port enable ($\overline{CS}$), serial data input (SDIO), and serial data output (SDO). The inputs to SCLK, $\overline{CS}$, and SDIO contain a Schmitt trigger with a nominal hysteresis of 0.4 V centered about VDD33/2. The maximum frequency for SCLK is 20 MHz. The SDO pin is active only during the transmission of data and remains three-stated at any other time.

A 3-wire SPI interface can be enabled by setting the SDIO_DIR bit (Register 0x00, Bit 7). This causes the SDIO pin to become bidirectional such that output data appears on only the SDIO pin during a read operation. The SDO pin remains three-stated in a 3-wire SPI interface.

Instruction Header Information

MSB							LSB
17	16	15	14	13	12	11	10
R/$\overline{W}$	A6	A5	A4	A3	A2	A1	A0

An 8-bit instruction header must accompany each read and write operation. The MSB is a R/$\overline{W}$ indicator bit with logic high indicating a read operation. The remaining seven bits specify the address bits to be accessed during the data transfer portion. The eight data bits immediately follow the instruction header for both read and write operations. For write operations, registers change immediately upon writing to the last bit of each transfer byte. $\overline{CS}$ can be raised after each sequence of eight bits (except the last byte) to stall the bus. The serial transfer resumes when $\overline{CS}$ is lowered. Stalling on nonbyte boundaries resets the SPI.

The AD9737A/AD9739A serial port can support both most significant bit (MSB) first and least significant bit (LSB) first data formats. Figure 153 illustrates how the serial port words are formed for the MSB first and LSB first modes. The bit order is controlled by the LSB/MSB bit (Register 0x00, Bit 6). The default value of Bit 6 is 0, MSB first. When the LSB/MSB bit is set high, the serial port interprets both instruction and data bytes LSB first.

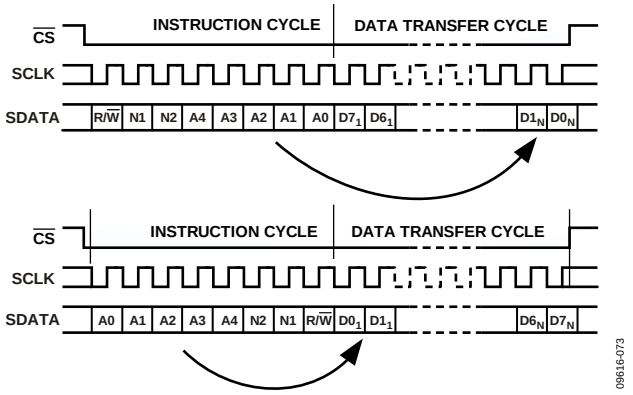


Figure 153. SPI Timing, MSB First (Upper) and LSB First (Lower)

Figure 154 illustrates the timing requirements for a write operation to the SPI port. After the serial port enable ($\overline{CS}$) signal goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of the clock (SCLK). To initiate a write operation, the read/not-write bit is set low. After the instruction header is read, the eight data bits pertaining to the specified register are shifted into the SDIO pin on the rising edge of the next eight clock cycles.

Figure 155 illustrates the timing for a 3-wire read operation to the SPI port. After $\overline{CS}$ goes low, data (SDIO) pertaining to the instruction header is read on the rising edges of SCLK. A read operation occurs if the read/not-write indicator is set high. After the address bits of the instruction header are read, the eight data bits pertaining to the specified register are shifted out of the SDIO pin on the falling edges of the next eight clock cycles.

Figure 156 illustrates the timing for a 4-wire read operation to the SPI port. The timing is similar to the 3-wire read operation with the exception that data appears at the SDO pin only, whereas the SDIO pin remains at high impedance throughout the operation. The SDO pin is an active output only during the data transfer phase and remains three-stated at all other times.

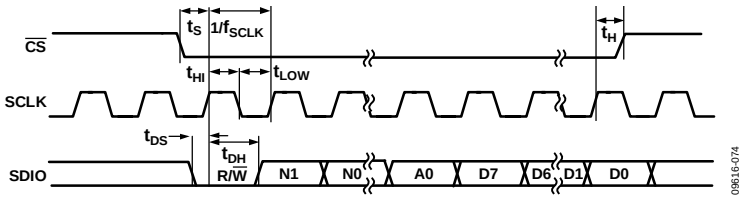


Figure 154. SPI Write Operation Timing

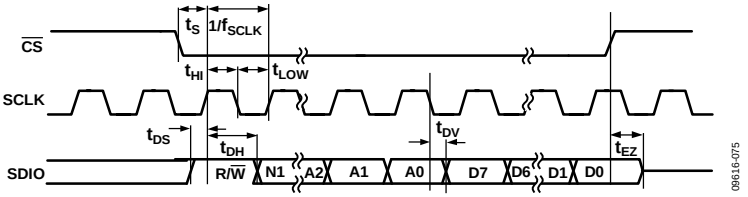


Figure 155. SPI 3-Wire Read Operation Timing

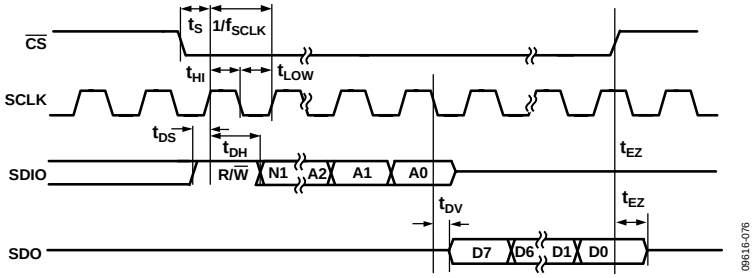


Figure 156. SPI 4-Wire Read Operation Timing

SPI REGISTER MAP

Table 10. Full Register Map (N/A = Not Applicable)

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Mode	0x00	SDIO_DIR	LSB/MSB	Reset	N/A	N/A	N/A	N/A	N/A	0x00
Power-Down	0x01	N/A	N/A	LVDS_ DRVR_PD	LVDS_ RCVR_PD	N/A	N/A	CLK_RCVR_ PD	DAC_BIAS_ PD	0x00
CNT_CLK_ DIS	0x02	N/A	N/A	N/A	N/A	CLKGEN_PD	N/A	REC_CNT_ CLK	MU_CNT_ CLK	0x03
IRQ_EN	0x03	N/A	N/A	N/A	N/A	MU_LST_EN	MU_LCK_EN	RCV_LST_EN	RCV_LCK_EN	0x00
IRQ_REQ	0x04	N/A	N/A	N/A	N/A	MU_LST_IRQ	MU_LCK_IRQ	RCV_LST_ IRQ	RCV_LCK_ IRQ	0x00
RSVD	0x05	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
FSC_1	0x06	FSC[7]	FSC[6]	FSC[5]	FSC[4]	FSC[3]	FSC[2]	FSC[1]	FSC[0]	0x00
FSC_2	0x07	Sleep	N/A	N/A	N/A	N/A	N/A	FSC[9]	FSC[8]	0x02
DEC_CNT	0x08	N/A	N/A	N/A	N/A	N/A	N/A	DAC_DEC[1]	DAC_DEC[0]	0x00
RSVD	0x09	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_CNT	0x0A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
DIG_STAT	0x0B	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	RNDM
LVDS_STAT1	0x0C	SUP/HLD_ Edge1	N/A	DCI_PHS3	DCI_PHS1	DCI_PRE_ PH2	DCI_PRE_ PH0	DCI_PST_ PH2	DCI_PST_ PH0	RNDM
LVDS_STAT2	0x0D	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	RNDM/0
RSVD	0x0E	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	0x0F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
LVDS_ REC_CNT1	0x10	N/A	N/A	N/A	N/A	N/A	RCVR_FLG_ RST	RCVR_ LOOP_ON	RCVR_CNT_ ENA	0x42
LVDS_ REC_CNT2	0x11	SMP_DEL[1]	SMP_DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	0xDD
LVDS_ REC_CNT3	0x12	SMP_DEL[9]	SMP_DEL[8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5]	SMP_DEL[4]	SMP_DEL[3]	SMP_DEL[2]	0x29
LVDS_ REC_CNT4	0x13	DCI_DEL[3]	DCI_DEL[2]	DCI_DEL[1]	DCI_DEL[0]	FINE_DEL_ SKW[3]	FINE_DEL_ SKW[2]	FINE_DEL_ SKW[1]	FINE_DEL_ SKW[0]	0x71
LVDS_ REC_CNT5	0x14	N/A	N/A	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7]	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]	0x0A
LVDS_ REC_CNT6	0x15	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x42
LVDS_ REC_CNT7	0x16	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_CNT8	0x17	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_CNT9	0x18	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_STAT1	0x19	SMP_DEL[1]	SMP_DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	0xC7
LVDS_ REC_STAT2	0x1A	SMP_DEL[9]	SMP_DEL[8]	SMP_DEL[7]	SMP_DEL[6]	SMP_DEL[5]	SMP_DEL[4]	SMP_DEL[3]	SMP_DEL[2]	0x29
LVDS_ REC_STAT3	0x1B	DCI_DEL[1]	DCI_DEL[0]	N/A	N/A	N/A	N/A	N/A	N/A	0xC0
LVDS_ REC_STAT4	0x1C	DCI_DEL[9]	DCI_DEL[8]	DCI_DEL[7]	DCI_DEL[6]	DCI_DEL[5]	DCI_DEL[4]	DCI_DEL[3]	DCI_DEL[2]	0x29
LVDS_ REC_STAT5	0x1D	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x86
LVDS_ REC_STAT6	0x1E	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_STAT7	0x1F	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_STAT8	0x20	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x00
LVDS_ REC_STAT9	0x21	N/A	N/A	N/A	N/A	RCVR_TRK_ ON	RCVR_FE_ ON	RCVR_LST	RCVR_LCK	0x00
CROSS_ CNT1	0x22	N/A	N/A	N/A	DIR_P	CLKP_ OFFSET[3]	CLKP_ OFFSET[2]	CLKP_ OFFSET[1]	CLKP_ OFFSET[0]	0x00

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
CROSS_ CNT2	0x23	N/A	N/A	N/A	DIR_N	CLKN_ OFFSET[3]	CLKN_ OFFSET[2]	CLKN_ OFFSET[1]	CLKN_ OFFSET[0]	0x00
PHS_DET	0x24	N/A	N/A	CMP_BST	PHS_DET AUTO_EN	N/A	N/A	N/A	N/A	0x00
MU_DUTY	0x25	MU_ DUTYAUTO_ EN	POS/NEG	ADJ[5]	ADJ[4]	N/A	N/A	N/A	N/A	0x00
MU_CNT1	0x26	N/A	Slope	Mode[1]	Mode[0]	Read	Gain[1]	Gain[0]	Enable	0x42
MU_CNT2	0x27	MUDEL[0]	SRCH_ MODE[1]	SRCH_ MODE[0]	SET_PHS[4]	SET_PHS[3]	SET_PHS[2]	SET_PHS[1]	SET_PHS[0]	0x40
MU_CNT3	0x28	MUDEL[8]	MUDEL[7]	MUDEL[6]	MUDEL[5]	MUDEL[4]	MUDEL[3]	MUDEL[2]	MUDEL[1]	0x00
MU_CNT4	0x29	SEARCH_TOL	Retry	CONTRST	Guard[4]	Guard[3]	Guard[2]	Guard[1]	Guard[0]	0x0B
MU_STAT1	0x2A	N/A	N/A	N/A	N/A	N/A	N/A	MU_LOST	MU_LKD	0x00
RSVD	0x2B	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
RSVD	0x2C	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
ANA_CNT1	0x32	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0xCA
ANA_CNT2	0x33	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	0x03
RSVD	0x34	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
PART_ID	0x35	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	0x40

SPI PORT CONFIGURATION AND SOFTWARE RESET

Table 11. SPI Port Configuration and Software Reset Register (Mode)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x00	SDIO_DIR	7	R/W	0x0	0 = 4-wire SPI, 1 = 3-wire SPI.
	LSB/MSB	6	R/W	0x0	0 = MSB first, 1 = LSB first.
	Reset	5	R/W	0x0	Software reset is recommended before modification of other SPI registers from the default setting. 0 = inactive state; allows the user to modify registers from the default setting. 1 = causes all registers (except 0x00) to be set to the default setting.

POWER-DOWN LVDS INTERFACE AND TxDAC®

Table 12. Power-Down LVDS Interface and TxDAC Register (Power-Down)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x01	LVDS_DRVR_PD	5	R/W	0x0	Power-down of the LVDS drivers/receivers and TxDAC. 0 = enable, 1 = disable.
	LVDS_RCVR_PD	4	R/W	0x0	
	CLK_RCVR_PD	1	R/W	0x0	
	DAC_BIAS_PD	0	R/W	0x0	

CONTROLLER CLOCK DISABLE

Table 13. Controller Clock Disable Register (CNT_CLK_DIS)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x02	CLKGEN_PD	3	R/W	0x0	Internal CLK distribution enable: 0 = enable, 1 = disable.
	REC_CNT_CLK	1	R/W	0x1	LVDS receiver and Mu controller clock disable. 0 = disable, 1 = enable.
	MU_CNT_CLK	0	R/W	0x1	

INTERRUPT REQUEST (IRQ) ENABLE/STATUS

Table 14. Interrupt Request (IRQ) Enable (IRQ_EN)/Status (IRQ_REQ) Register

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x03	MU_LST_EN	3	W	0x0	This register enables the Mu and LVDS Rx controllers to update their corresponding IRQ status bits in Register 0x04, which defines whether the controller is locked (LCK) or unlocked (LST). 0 = disable (resets the status bit), 1 = enable.
	MU_LCK_EN	2	W	0x0	
	RCV_LST_EN	1	W	0x0	
	RCV_LCK_EN	0	W	0x0	
0x04	MU_LST_IRQ	3	R	0x0	This register indicates the status of the controllers. For LCK_IRQ bits: 0 = lock lost, 1 = locked. For LST_IRQ bits: 0 = lock not lost, 1 = unlocked. Note that, if the controller IRQ is serviced, the relevant bits in Register 0x03 should be reset by writing 0, followed by another write of 1 to enable.
	MU_LCK_IRQ	2	R	0x0	
	RCV_LST_IRQ	1	R	0x0	
	RCV_LCK_IRQ	0	R	0x0	

TxDAC FULL-SCALE CURRENT SETTING (I_{OUTFS}) AND SLEEP

Table 15. TxDAC Full-Scale Current Setting (I_{OUTFS}) and Sleep Register (FSC_1 and FSC_2)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x06	FSC[7:0]	[7:0]	R/W	0x00	Sets the TxDAC I_{OUTFS} current between 8 mA and 31 mA (default = 20 mA).
0x07	FSC[9:8]	[1:0]	R/W	0x02	$I_{OUTFS} = 0.0226 \times FSC[9:0] + 8.58$, where FSC = 0 to 1023.
	Sleep	7	R/W		0 = enable DAC output, 1 = disable DAC output (sleep).

TxDAC QUAD-SWITCH MODE OF OPERATION

Table 16. TxDAC Quad-Switch Mode of Operation Register (DEC_CNT)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x08	DAC_DEC	[1:0]	R/W	0x00	0x00 = normal baseband mode. 0x02 = mix-mode.

DCI PHASE ALIGNMENT STATUS

Table 17. DCI Phase Alignment Status Register (LVDS_STAT1)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x0C	DCI_PRE_PH0	2	R	0x0	0 = DCI rising edge is after the PRE delayed version of the Phase 0 sampling edge. 1 = DCI rising edge is before the PRE delayed version of the Phase 0 sampling edge.
	DCI_PST_PH0	0	R	0x0	0 = DCI rising edge is after the POST delayed version of the Phase 0 sampling edge. 1 = DCI rising edge is before the POST delayed version of the Phase 0 sampling edge.

DATA RECEIVER CONTROLLER CONFIGURATION

Table 18. Data Receiver Controller Configuration Register (LVDS_REC_CNT1)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x10	RCVR_FLG_RST	2	W	0x0	Data receiver controller flag reset. Write 1 followed by 0 to reset flags.
	RCVR_LOOP_ON	1	R/W	0x1	0 = disable, 1 = enable. When this bit is enabled, the data receiver controller generates an IRQ; it falls out of lock and automatically begins a search/track routine.
	RCVR_CNT_ENA	0	R/W	0x0	Data receiver controller enable. 0 = disable, 1 = enable.

DATA RECEIVER CONTROLLER_DATA SAMPLE DELAY VALUE

Table 19. Data Receiver Controller_Data Sample Delay Value Register (LVDS_REC_CNT2 and LVDS_REC_CNT3)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x11	SMP_DEL[1:0]	[7:6]	R/W	0x11	Controller enabled: the 10-bit value (with a maximum of 384) represents the start value for the delay line used by the state machine to sample data. Leave at the default setting of 167, which is near the midpoint of the delay line. Controller disabled: the value sets the actual value of the delay line.
0x12	SMP_DEL[9:2]	[7:0]	R/W	0x25	

DATA RECEIVER CONTROLLER_DCI DELAY VALUE/WINDOW AND PHASE ROTATION

Table 20. Data Receiver Controller_DCI Delay Value (LVDS_REC_CNT4)/Window and Phase Rotation Register (LVDS_REC_CNT5)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x13	DCI_DEL[3:0]	[7:4]	R/W	0x0111	Refer to the DCI_DEL description in Register 0x14.
	FINE_DEL_ SKW[3:0]	[3:0]	R/W	0x0001	A 4-bit value sets the difference (that is, window) for the DCI PRE and POST sampling clocks. Leave at the default value of 1 for a narrow window.
0x14	DCI_DEL[9:4]	[5:0]	R/W	0x001010	Controller enabled: the 10-bit value (with a maximum of 384) represents the start value for the delay line used by the state machine to sample the DCI input. Leave at the default setting of 167, which is near the midpoint of the delay line. Controller disabled: the value sets the actual value of the delay line.

DATA RECEIVER CONTROLLER_DELAY LINE STATUS

Table 21. Data Receiver Controller_Delay Line Status Register (LVDS_REC_STAT[1:4])

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x19	SMP_DEL[1:0]	[7:6]	R	0x00	The actual value of the DCI and data delay lines are determined by the data receiver controller (when enabled) after the state machine completes its search and enters track mode. Note that these values should be equal.
0x1A	SMP_DEL[9:2]	[7:0]	R	0x00	
0x1B	DCI_DEL[1:0]	[7:6]	R	0x00	
0x1C	DCI_DEL[9:2]	[7:0]	R	0x00	

DATA RECEIVER CONTROLLER LOCK/TRACKING STATUS

Table 22. Data Receiver Controller Lock/Tracking Status Register (LVDS_REC_STAT9)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x21	RCVR_TRK_ON	3	R	0x0	0 = tracking not established, 1 = tracking established.
	RCVR_FE_ON	2	R	0x0	0 = find edge state machine is not active, 1 = find edge state machine is active.
	RCVR_LST	1	R	0x0	0 = controller has not lost lock, 1 = controller has lost lock.
	RCVR_LCK	0	R	0x0	0 = controller is not locked, 1 = controller is locked.

CLK INPUT COMMON MODE

Table 23. CLK Input Common Mode Register (CROSS_CNT1 and CROSS_CNT2)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x22	DIR_P	4	R/W	0x0	DIR_P and DIR_N. 0 = VCM at the DACCLK_P input decreases with the offset value. 1 = VCM at the DACCLK_P input increases with the offset value. CLKx_OFFSET sets the magnitude of the offset for the DACCLK_P and DACCLK_N inputs. For optimum performance, set to 1111.
	CLKP_OFFSET[3:0]	[3:0]	R/W	0x0000	
0x23	DIR_N	4	R/W	0x0	
	CLKN_OFFSET[3:0]	[3:0]	R/W	0x0000	

MU CONTROLLER CONFIGURATION AND STATUS

Table 24. Mu Controller Configuration and Status Register (PHS_DET, MU_DUTY, MU_CNT[1:4], and MU_STAT1)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x24	CMP_BST	5	R/W	0x0	Phase detector enable and boost bias bits. Note that both bits should always be set to 1 to enable these functions.
	PHS_DET AUTO_EN	4	R/W	0x0	
0x25	MU_ DUTYAUTO_EN	7	R/W	0x0	Mu controller duty cycle enable. Note that this bit should always be set to 1 to enable.
0x26	Slope	6	R/W	0x1	Mu controller phase slope lock. 0 = negative slope, 1 = positive slope. Note that a setting of 0 is recommended for best ac performance.
	Mode[1:0]	[5:4]	R/W	0x00	Sets the Mu controller mode of operation. 00 = search and track (recommended). 01 = search only. 10 = track.
	Read	3	R/W	0x0	Set to 1 to read the current value of the Mu delay line in.
	Gain[1:0]	[2:1]	R/W	0x01	Sets the Mu controller tracking gain. Recommended to leave at the default 01 setting.
	Enable	0	R/W	0x0	0 = disable the Mu controller. 1 = enable the Mu controller.
0x27	MUDEL[0]	7	R/W	0x0	The LSB of the 9-bit MUDEL setting.
	SRCH_MODE[1:0]	[6:5]	R/W	0x0	Sets the direction in which the Mu controller searches (from its initial MUDEL setting) for the optimum Mu delay line setting that corresponds to the desired phase/slope setting (that is, SET_PHS and slope). 00 = down. 01 = up. 10 = down/up (recommended).
	SET_PHS[4:0]	[4:0]	R/W	0x0	Sets the target phase that the Mu controller locks to with a maximum setting of 16. A setting of 4 (that is, 00100) is recommended for optimum ac performance.
0x28	MUDEL[8:1]	[7:0]	W	0x00	With enable (Bit 0, Register 0x26) set to 0, this 9-bit value represents the value that the Mu delay is set to. Note that the maximum value is 432. With enable set to 1, this value represents the Mu delay value at which the controller begins its search. Setting this value to the delay line midpoint of 216 is recommended.
			R	0x00	When read (Bit 3, Register 0x26) is set to 1, the value read back is equal to the value written into the register when enable = 0 or the value that the Mu controller locks to when enable = 1.

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x29	SEARCH_TOL	7	R/W	0x0	0 = not exact (can find a phase within two values of the desired phase). 1 = finds the exact phase that is targeted (optimal setting).
	Retry	6	R/W	0x0	0 = stop the search if the correct value is not found, 1 = retry the search if the correct value is not found.
	CONTRST	5	R/W	0x0	Controls whether the controller resets or continues when it does not find the desired phase. 0 = continue (optimal setting), 1 = reset.
	Guard[4:0]	[4:0]	R/W	0x01011	Sets a guard band from the beginning and end of the Mu delay line, which the Mu controller does not enter into unless it does not find a valid phase outside the guard band (optimal value is Decimal 11 or 0x0B).
0x2A	MU_LOST	1	R	0x0	0 = Mu controller has not lost lock. 1 = Mu controller has lost lock.
	MU_LKD	0	R	0x0	0 = Mu controller is not locked. 1= Mu controller is locked.

PART ID

Table 25. Part ID Register (PART_ID)

Address (Hex)	Bit Name	Bits	R/W	Default Setting	Description
0x35	ID[7:0]	[7:0]	R	0x24	0x24—AD9739A
				0x27	0x2C—AD9737A

THEORY OF OPERATION

The AD9739A and the AD9737A are 14- and 11-bit TxDACs with a specified update rate of 1.6 GSPS to 2.5 GSPS. Figure 157 shows a top-level functional diagram of the AD9737A/AD9739A. A high performance TxDAC core delivers a signal dependent, differential current (nominal ±10 mA) to a balanced load referenced to ground. The frequency of the clock signal appearing at the AD9737A/AD9739A differential clock receiver, DACCLK, sets the TxDAC's update rate. This clock signal, which serves as the master clock, is routed directly to the TxDAC as well as to a clock distribution block that generates all critical internal and external clocks.

The AD9737A/AD9739A include two LVDS data ports (DB0 and DB1) to reduce the data interface rate to ½ the TxDAC update rate. The host processor drives deinterleaved data with offset binary format onto the DB0 and DB1 ports, along with an embedded DCI clock that is synchronous with the data. Because the interface is double data rate (DDR), the DCI clock is essentially an alternating 0-1 bit pattern with a frequency that is equal to ¼ the TxDAC update rate (f_{DAC}). To simplify synchronization with the host processor, the AD9737A/AD9739A passes an LVDS clock output (DCO) that is also equal to the DCI frequency.

The AD9737A/AD9739A data receiver controller generates an internal sampling clock for the DDR receiver such that the data instance sampling is optimized. When enabled and configured properly for track mode, it ensures proper data recovery between the host and the AD9737A/AD9739A clock domains. The data receiver controller has the ability to track several hundreds of picoseconds of drift between these clock domains, typically caused by supply and temperature variation.

As mentioned, the host processor provides the AD9737A/AD9739A with a deinterleaved data stream such that the DB0 and DB1 data ports receive alternating samples (that is, odd/even data streams). The AD9737A/AD9739A data assembler is used to reassemble (that is, multiplex) the odd/even data streams into their original order before delivery into the TxDAC for signal reconstruction. The pipeline delay from a sample being latched into the data port to when it appears at the DAC output is on the order of 78 (±) 2DACCLK cycles.

The AD9737A/AD9739A includes a delay lock loop (DLL) circuit controlled via a Mu controller to optimize the timing hand-off between the AD9737A/AD9739A digital clock domain and TxDAC core. Besides ensuring proper data reconstruction, the TxDAC's ac performance is also dependent on this critical hand-off between these clock domains with speeds of up to 2.5 GSPS. Once properly initialized and configured for track mode, the DLL maintains optimum timing alignment over temperature, time, and power supply variation.

A SPI interface is used to configure the various functional blocks as well as monitor their status for debug purposes. Proper operation of the AD9737A/AD9739A requires that controller blocks be initialized upon power-up. A simple SPI initialization routine is used to configure the controller blocks (see Table 28). An IRQ output signal is available to alert the host should any of the controllers fall out of lock during normal operation.

The following sections discuss the various functional blocks in more detail as well as their implications when interfacing to external ICs and circuitry. Although a detailed description of the various controllers (and associated SPI registers used to configure and monitor) is also included for completeness, the recommended SPI boot procedure can be used to ensure reliable operation.

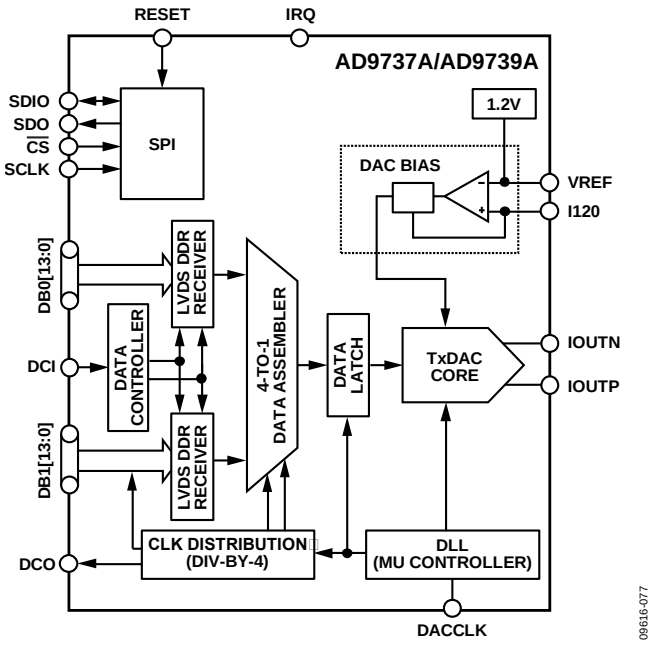


Figure 157. Functional Block Diagram of the AD9737A/AD9739A

LVDS DATA PORT INTERFACE

The AD9737A/AD9739A supports input data rates from 1.6 GSPS to 2.5 GSPS using dual LVDS data ports. The interface is source synchronous and double data rate (DDR) where the host provides an embedded data clock input (DCI) at $f_{DAC}/4$ with its rising and falling edges aligned with the data transitions. The data format is offset binary; however, twos complement format can be realized by reversing the polarity of the MSB differential trace. As shown in Figure 158, the host feeds the AD9737A/AD9739A with deinterleaved input data into two 11-bit LVDS data ports (DB0 and DB1) at ½ the DAC clock rate (that is, $f_{DAC}/2$). The AD9737A/AD9739A internal data receiver controller then generates a phase shifted version of DCI to register the input data on both the rising and falling edges.

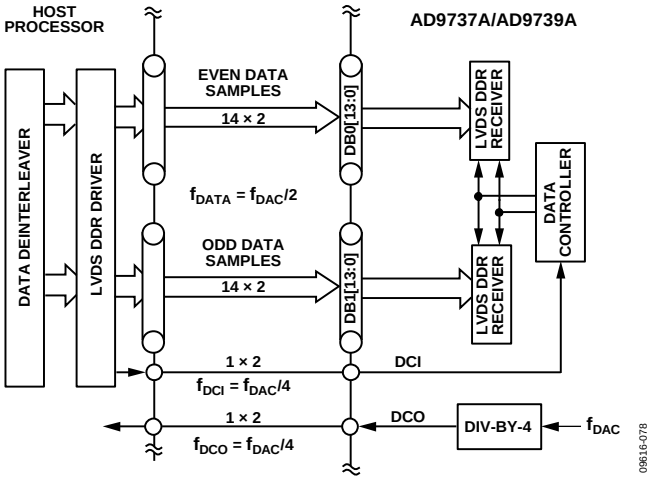


Figure 158. Recommended Digital Interface Between the AD9737A/AD9739A and Host Processor

As shown in Figure 159, the DCI clock edges must be coincident with the data bit transitions with minimum skew, jitter, and intersymbol interference. To ensure coincident transitions with the data bits, the DCI signal should be implemented as an additional data line with an alternating (010101…) bit sequence from the same output drivers used for the data. Maximizing the opening of the eye in both the DCI and data signals improves the reliability of the data port interface. Differential controlled impedance traces of equal length (that is, delay) should also be used between the host processor and AD9737A/AD9739A input to limit bit-to-bit skew.

The maximum allowable skew and jitter out of the host processor with respect to the DCI clock edge on each LVDS port is calculated as follows:

$$MaxSkew + Jitter = Period(\text{ps}) - ValidWindow(\text{ps}) - Guard$$
$$= 800\text{ ps} - 344\text{ ps} - 100\text{ ps}$$
$$= 356\text{ ps}$$

where *ValidWindow*(ps) is represented by t_{VALID} and *Guard* is represented by t_{GUARD} in Figure 159.

The minimum specified LVDS valid window is 344 ps, and a guard band of 100 ps is recommended. Therefore, at the maximum operating frequency of 2.5 GSPS, the maximum allowable FPGA and PCB bit skew plus jitter is equal to 356 ps.

For synchronous operation, the AD9737A/AD9739A provides a data clock output, DCO, to the host at the same rate as DCI (that is, $f_{DAC}/4$) to maintain the lowest skew variation between these clock domains. The host processor has a worst case skew between DCO and DCI that is both implementation and process dependent. This worst case skew can also vary an additional 30% over temperature and supply corners. The delay line within the data receiver controller can track a ±1.5 ns skew variation after initial lock. While it is possible for the host to have an internal PLL that generates a synchronous $f_{DAC}/4$ from which the DCI signal is derived, digital implementations that result in the shortest propagation delays result in the lowest skew variation.

The data receiver controller is used to ensure proper data handoff between the host and AD9737A/AD9739A internal digital clock domains. The circuit shown in Figure 160 functions as a delay lock loop in which a 90° phase shifted version of the DCI clock input is used to sample the input data into the DDR receiver registers. This ensures that the sampling instance occurs in the middle of the data pattern eyes (assuming matched DCI and DBx[13:0] delays). Note that, because the DCI delay and sample delay clocks are derived from the DIV-BY-4 circuitry, this 90° phase relationship holds as long as the delay settings (that is, DCI_DEL in Register 0x13 and Register 0x14, and SMP_DEL in Register 0x11 and Register 0x12) are also matched.

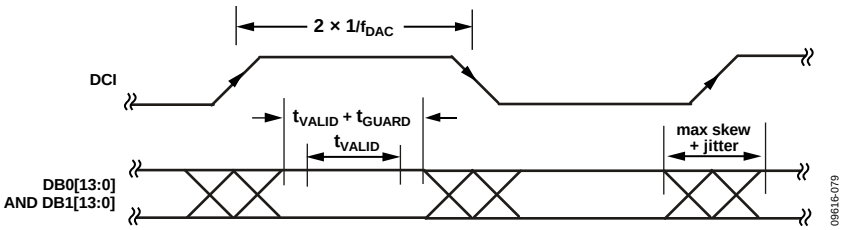


Figure 159. LVDS Data Port Timing Requirements

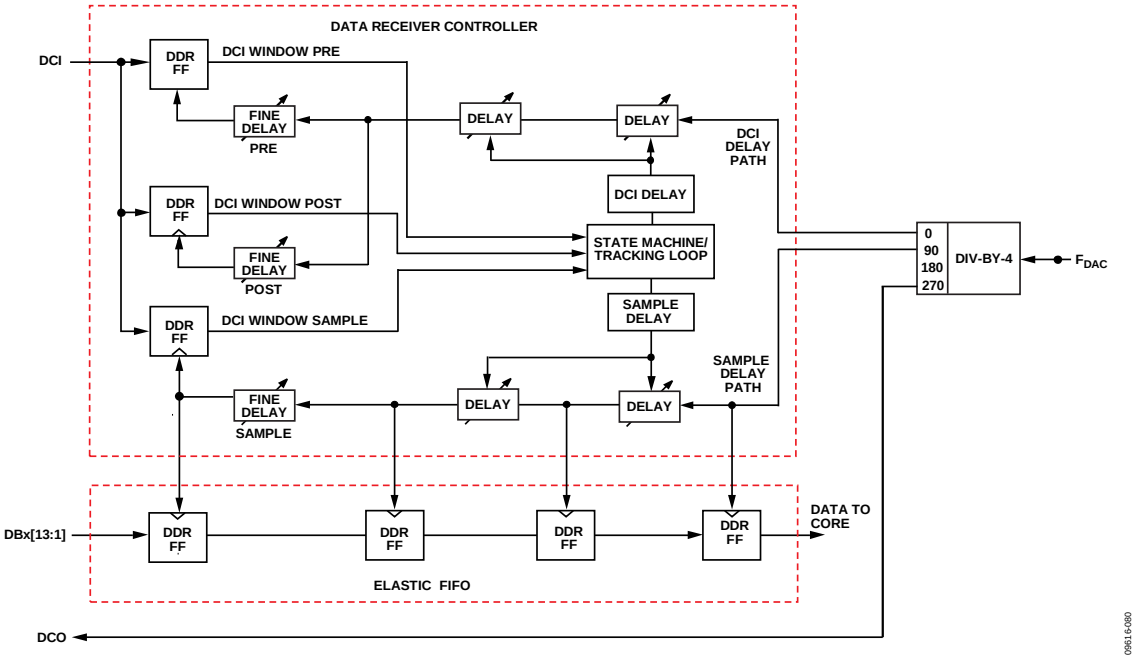


Figure 160. Top Level Diagram of the Data Receiver Controller

The DIV-BY-4 circuit generates four clock phases that serve as inputs to the data receiver controller. All DDR registers in the data and DCI paths operate on both clock edges; however, for clarity purposes, only the phases (that is, 0° and 90°) corresponding to the positive edge of each path are shown. One of the DIV-BY-4 phases is used to generate the DCO signal; therefore, the phase relationship between DCO and clocks fed into the controller remains fixed. Note that it is this attribute that allows possible factory calibration of images and clock spurs that are attributed to $f_{DAC}/4$ modulation of the critical DAC clock.

After this data has been successively sampled into the first set of registers, an elastic FIFO is used to transfer the data into the AD9737A/AD9739A clock domain. To track any phase variation continuously between the two clock domains, the data receiver controller should always be enabled and placed into track mode (Register 0x10, Bit 1 and Bit 0). Tracking mode operates continuously in the background to track delay variations between the host and AD9737A/AD9739A clock domains. It does so by ensuring that the DCI signal is sampled within a very narrow window defined by two internally generated clocks (that is, PRE and PST), as shown in Figure 161. Note that proper sampling of the DCI signal can also be confirmed by monitoring the status of DCI_PRE_PH0 (Register 0x0C, Bit 2) and DCI_PST_PH0 (Register 0x0C, Bit 0). If the delay settings are correct, the state of DCI_ PRE_PH0 should be 0, and the state of DCI_PST_PH0 should be 1.

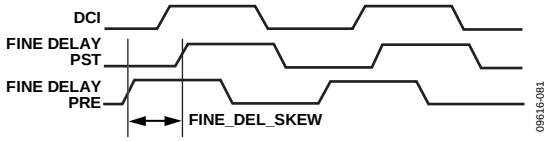


Figure 161. Pre- and Post-Delay Sampling Diagram

The skew or window width (FINE_DEL_SKEW) is set via Register 0x13, Bits[3:0], with a maximum skew of approximately 300 ps and resolution of 12 ps. It is recommended that the skew be set to 36 ps (that is, Register 0x13 = 0x72) during initialization. Note that the skew setting also affects the speed of the controller loop, with tighter skew settings corresponding to longer response time.

Data Receiver Controller Initialization Description

The data controller should be initialized and placed into track mode as the second step in the SPI boot sequence. The following steps are recommended for the initialization of the data receiver controller:

1. Set FINE_DEL_SKEW to 2 for a larger DCI sampling window (Register 0x13 = 0x72). Note that the default DCI_DEL and SMP_DEL settings of 167 are optimum.
2. Disable the controller before enabling (that is, Register 0x10 = 0x00).
3. Enable the Rx controller in two steps: Register 0x10 = 0x02 followed by Register 0x10 = 0x03.
4. Wait 135 k clock cycles.
5. Read back Register 0x21 and confirm that it is equal to 0x05 to ensure that the DLL loop is locked and tracking.
6. Read back the DCI_DEL value to determine whether the value falls within a user defined tracking guard band. If it does not, go back to Step 2.

After the controller is enabled during the initial SPI boot process (see Table 29), the controller enters a search mode where it seeks to find the closest rising edge of the DCI clock (relative to a delayed version of an internal $f_{DAC}/4$ clock) by simultaneously adjusting the delays in the clocks used to register the DCI and data inputs. A state machine searches above and below the initial DCI_DEL value. The state machine first searches for the first rising edge above the DCI_DEL and then searches for the first rising edge below the DCI_DEL value. The state machine selects the closest rising edge and then enters track mode. It is recommended that the default midpoint delay setting (that is, Decimal 167) for the DCI_DEL and SMP_DEL bits be kept to ensure that the selected edge remains closest to the delay line midpoint, thus providing the greatest range for tracking timing variations and preventing the controller from falling out of lock.

The adjustable delay span for these internal clocks (that is, DCI and sample delay) is nominally 4 ns. The 10-bit delay value is user programmable from the decimal equivalent code (0 to 384) with approximately 12 ps/LSB resolution via the DCI_DEL (Register 0x13 and Register 0x14)and SMP_DEL registers (Register 0x11 and Register 0x12). When the controller is enabled, it overwrites these registers with the delay value it converges upon. The minimum difference between this delay value and the minimum/maximum values (that is, 0 and 384) represents the guard band for tracking. Therefore, if the controller initially converges upon a DCI_DEL and SMP_DEL value between 80 and 3044, the controller has a guard band of at least 80 code (approximately 1 ns) to track phase variations between the clock domains.

On initialization of the AD9737A/AD9739A, a certain period of time is required for the data receiver controller to establish a lock of the DCI clock signal. Note that, due to its dependency on the Mu controller, the data receiver controller should be enabled only after the Mu controllers have been enabled and established lock. All of the internal controllers operate at a submultiple of the DAC update rate. The number of f_{DAC} clock cycles required to lock onto the DCI clock is typically 70 k clock cycles but can be up to 135 k clock cycles. During the SPI initialization process, the user has the option of polling Register 0x21 (Bit 0, Bit 1, and Bit 3) to determine if the data receiver controller is locked, has lost lock, or has entered into track mode before completing the boot sequence. Alternatively, the appropriate IRQ bit (Register 0x03 and Register 0x04) can be enabled such that an IRQ output signal is generated upon the controller establishing lock.

The data receiver controller can also be configured to generate an interrupt request (IRQ) upon losing lock. Losing lock can be caused by disruption of the main DAC clock input or loss of a power supply rail. To service the interrupt, the host can poll the RCVR_LCK bit (Bit 0, Recister 0x21) to determine the current state of the controller. If this bit is cleared, the search/track procedure can be restarted by setting the RCVR_LOOP_ON bit (Bit 1) in Register 0x10. After waiting the required lock time, the host can poll the RCVR_LCK bit to see if it has been set. Before leaving the interrupt routine, the RCVR_FLG_RST bit (Bit 2, Register 0x10) should be reset by writing a high followed by a low.

LVDS Driver and Receiver Input

The AD9737A/AD9739A feature an LVDS-compatible driver and receivers. The LVDS driver output used for the DCO signal includes an equivalent 200 Ω source resistor that limits its nominal output voltage swing to ±200 mV when driving a 100 Ω load. The DCO output driver can be powered down via Register 0x01, Bit 5. An equivalent circuit is shown in Figure 162.

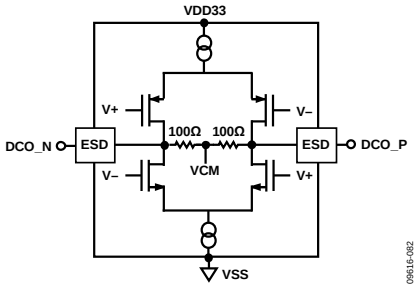


Figure 162. Equivalent LVDS Output

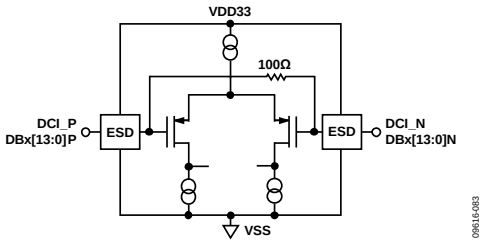


Figure 163. AD9739A Equivalent LVDS Input

The LVDS receivers include 100 Ω termination resistors, as shown in Figure 163. These receivers meet the IEEE-1596.3-1996 reduced swing specification (with the exception of input hysteresis, which cannot be guaranteed over all process corners). Figure 164 and Table 26 show an example of nominal LVDS voltage levels seen at the input of the differential receiver with resulting common-mode voltage and equivalent logic level. Note that the AD9737A/AD9739A LVDS inputs do not include fail-safe capability; hence, any unused input should be biased with an external circuit or static driver. The LVDS receivers can be powered-down via Register 0x01, Bit 4.

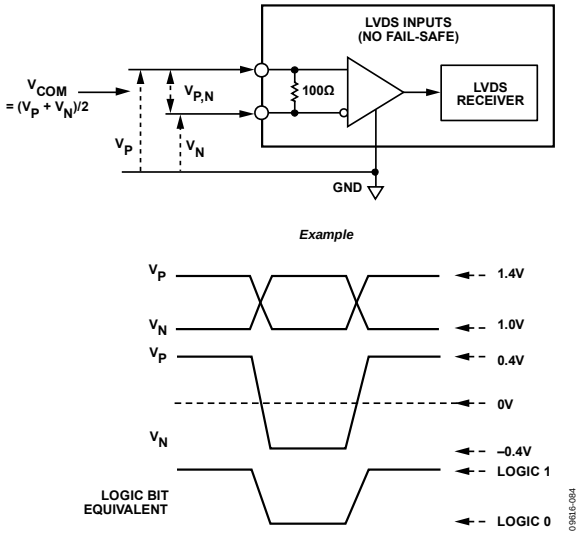


Figure 164. LVDS Data Input Levels

Table 26. Example of LVDS Input Levels

Applied Voltages		Resulting Differential Voltage	Resulting Common-Mode Voltage	Logic Bit Binary Equivalent
V_P	V_N	$V_{P,N}$	V_{COM}	
1.4 V	1.0 V	+0.4 V	1.2 V	1
1.0 V	1.4 V	−0.4 V	1.2 V	0
1.0 V	0.8 V	+200 mV	900 mV	1
0.8 V	1.0 V	−200 mV	900 mV	0

MU CONTROLLER

A delay lock loop (DLL) is used to optimize the timing between the internal digital and analog domains of the AD9737A/AD9739A such that data is successfully transferred into the TxDAC core at rates of up to 2.5 GSPS. As shown in Figure 165, the DAC clock is split into an analog and a digital path with the critical analog path leading to the DAC core (for minimum jitter degradation) and the digital path leading to a programmable delay line. Note that the output of this delay line serves as the master internal digital clock from which all other internal and external digital clocks are derived. The amount of delay added to this path is under the control of the Mu controller, which optimizes the timing between these two clock domains and continuously tracks any variation (once in track mode) to ensure proper data hand-off.

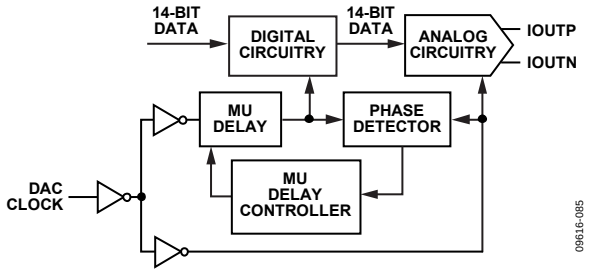


Figure 165. AD97339A Mu Delay Controller Block Diagram

The Mu controller adjusts the timing relationship between the digital and analog domains via a tapped digital delay line having a nominal total delay of 864 ps. The delay value is programmable to a 9-bit resolution (that is, 0 to 432 decimal) via the MUDEL bits (Register 0x27 and 0x28), resulting in a nominal resolution of 2 ps/LSB. Because a time delay maps to a phase offset for a fixed clock frequency, the control loop essentially compares the phase relationship between the two clock domains and adjusts the phase (that is, via a tapped delay line) of the digital clock such that it is at the desired fixed phase offset (SET_PHS) from the critical analog clock.

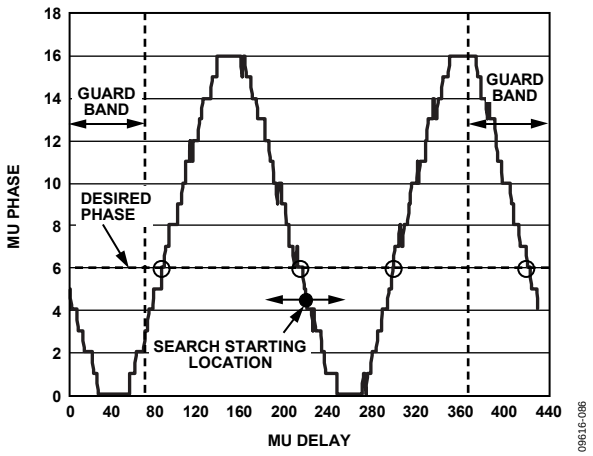


Figure 166. Typical Mu Phase Characteristic Plot at 2.4 GSPS

Figure 166 maps the typical Mu phase characteristic at 2.4 GSPS vs. the 9-bit digital delay setting (MUDEL). The Mu phase scaling is such that a value of 16 corresponds to 180 degrees. The critical keep-out window between the digital and analog domains occurs at a value of 0 (but can extend out to 2 depending on the clock rate). The target Mu phase (and slope) is selected to provide optimum ac performance while ensuring that the Mu controller for any device can establish and maintain lock. For example, although a slope and phase setting of −6 is considered optimum for operation between 1.6 GSPS and 2.5 GSPS, other values are required below 1.6 GSPS.

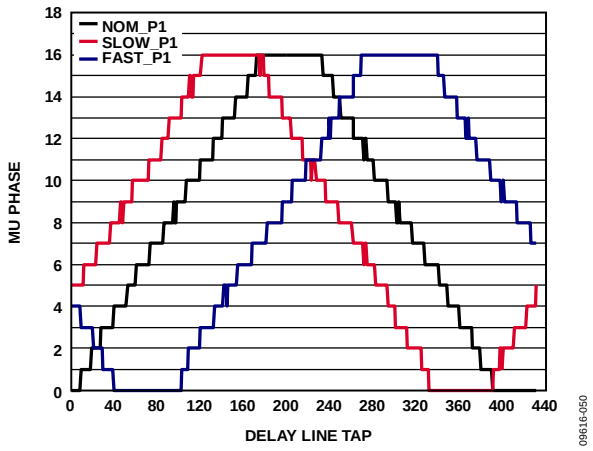


Figure 167. Mu Phase Characteristics of Three Devices from Different Process Lots at 1.2 GSPS

The Mu phase characteristics can vary significantly among devices due to g_m variations in the digital delay line that are sensitive to process skews, along with temperature and supply. As a result, careful selection of the target phase location is required such that the Mu controller can converge upon this phase location for all devices.

Figure 167 shows the Mu phase characteristics of three devices at 25°C from slow, nominal, and fast skew lots at 1.2 GSPS. Note that a −6 Mu phase setting does not map to any delay line tap setting for the fast process skew case; therefore, another target Mu phase is recommended at this clock rate.

Table 27 provides a list of recommended Mu phase/slope settings over the specified clock range of the AD9737A/AD9739A based on the considerations previously described. These values should be used to ensure robust operation of the Mu controller.

Table 27. Recommended Target Mu Phase Settings vs. Clock Rate

Clock Rate (GSPS)	Slope	Mu Phase
1.6 to 2.5	–	6

After the Mu controller completes its search and establishes lock on the target Mu phase, it attempts to maintain a constant timing relationship between the two clock domains over the specified temperature and supply range. If the Mu controller requests a Mu delay setting that exceeds the tapped delay line range (that is, <0 or >432), the Mu controller can lose lock, causing possible system disruption (that is, can generate an IRQ or restart the search). To avoid this scenario, symmetrical guard bands are recommended at each end of the Mu delay range. The guard band scaling is such that one LSB of Guard[4:0] (Register 0x29) corresponds to eight LSBs of MUDEL[8:0] (Register 0x28). The recommended guard band setting of 11 (that is, Register 0x29 = 0xCB) corresponds to 88 LSBs, thus providing sufficient margin.

Mu Controller Initialization Description

The Mu controller must be initialized and placed into track mode as a first step in the SPI boot sequence. The following steps are required for initialization of the Mu controller. Note that the AD9737A/AD9739A data sheet specifications and characterization data are based on the following Mu controller settings:

1. Turn on the phase detector with boost (Register 0x24 = 0x30).
2. Enable the Mu delay controller duty-cycle correction circuitry and specify the recommended slope for phase. (that is, Register 0x25 = 0x80 corresponds to a negative slope).
3. Specify search/track mode with a recommended target phase, SET_PHS, of 6 (for example) and an initial MUDEL[8:0] setting of 216 (Register 0x27 = 0x46 and Register 0x28 = 0x6C).
4. Set search tolerance to exact, and retry if the search fails its initial attempt. Also, set the guard band to the recommended setting of 11 (Register 0x29 = 0xCB).
5. Set the Mu controller tracking gain to the recommended setting and enable the Mu controller state machine (Register 0x26 = 0x03).

On completion of the last step, the Mu controller begins a search algorithm that starts with an initial delay setting specified by the MUDEL bits (that is, 216, which corresponds to the midpoint of the delay line). The initial search algorithm works by sweeping through different Mu delay values in an alternating manner until the desired phase (that is, a SET_PHS of 4) is exactly measured. When the desired phase is measured, the slope of the phase measurement is then calculated and compared against the specified slope (slope = negative).

If everything matches, the search algorithm is finished. If not, the search continues in both directions until an exact match is found or a programmable guard band is reached in one of the directions. When the guard band is reached, the search still continues but only in the opposite direction. If the desired phase is not found before the guard band is reached in the second direction, the search changes back to the alternating mode and continues looking within the guard band. The typical locking time for the Mu controller is approximately 180 k DAC cycles (at 2 GSPS ~ 75 µs).

The search fails if the Mu delay controller reaches the endpoints. The Mu controller can be configured to retry (Register 0x29, Bit 6) the search or stop. For applications that have a micro-controller, the preferred approach is to poll the MU_LKD status bit (Register 0x2A, Bit 0) after the typical locking time has expired. This method lets the system controller check the status of other system parameters (that is, power supplies and clock source) before reattempting the search (by writing 0x03 to Register 0x26).

For applications that do not have polling capabilities, the Mu controller state machine should be reconfigured to restart the search, such that lock can be re-attempted with system conditions that may have changed and be different, and thus may enable the controller to lock.

After the Mu delay value is found that exactly matches the desired Mu phase setting and slope (for example, 6 with a negative slope), the Mu controller goes into track mode. In this mode, the Mu controller makes slight adjustments to the delay value to track any variations between the two clock paths due to temperature, time, and supply variations. Two status bits, MU_LKD (Register 0x2A, Bit 0) and MU_LST (Register 0x2A, Bit 1) are available to the user to signal the existing status control loop. If the current phase is more than four steps away from the desired phase, the MU_LKD bit is cleared, and if the lock acquired was previously set, the MU_LST bit is set. Should the phase deviation return to within three steps, the MU_LKD bit is set again while the MU_LST is cleared. Note that this sort of event may occur if the main clock input (that is, DACCLK) is disrupted or the Mu controller exceeds the tapped delay line range (that is, <0 or >432).

If lock is lost, the Mu controller has the option of remaining in the tracking loop or resetting and starting the search again via the CONTRST bit (Register 0x29, Bit 5). Continued tracking is the preferred state because it is the least disruptive to a system in which the AD9737A/AD9739A temporarily loses lock. The user can poll the Mu delay and phase value by first setting the read bit high (Register 0x26, Bit 3). After the read bit is set, the MUDEL[8:0] bits and the SET_PHS[4:0] bits (Register 0x27 and Register 0x28) that the controller is currently using can be read.

INTERRUPT REQUESTS

The AD9737A/AD9739A can provide the host processor with an interrupt request output signal (IRQ) that indicates that one or more of the AD9737A/AD9739A internal controllers have achieved lock or lost lock. These controllers include the Mu, data receiver, and synchronization controllers. The host can then poll the IRQ status register (Register 0x04) to determine which controller has lost lock. The IRQ output signal is an active high output signal available on Pin F13. If used, its output should be connected via a 10 kΩ pull-up resistor to VDD33.

Each IRQ is enabled by setting the enable bits in Register 0x03, which purposely has the same bit mapping as the IRQ status bits in Register 0x04. Note that these IRQ status bits are set only when the controller transitions from a false to true state. Hence, it is possible for the x_LCK_IRQ and x_LST_IRQ status bits to be set when a controller temporarily loses lock but is able to reestablish lock before the IRQ is serviced by the host. In this case, the host should validate the present status of the suspect controller by reading back its current status bits, which are available in Register 0x21 and/or Register 0x2A. Based on the status of these bits, the host can take appropriate action, if required, to reestablish lock. To clear an IRQ after servicing, it is necessary to reset relevant bits in Register 0x03 by writing 0 followed by another write of 1 to reenable. A detailed diagram of the interrupt circuitry is shown in Figure 168.

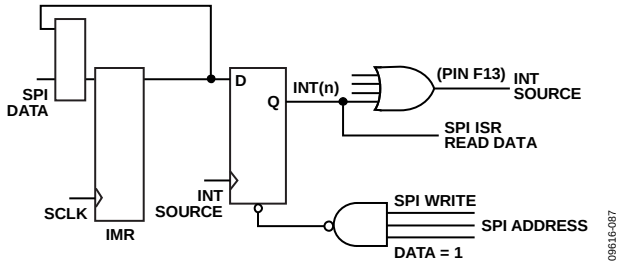


Figure 168. Interrupt Request Circuitry

It is also possible to use the IRQ during the AD9737A/AD9739A initialization phase after power-up to determine when the Mu and data receiver controllers have achieved lock. For example, before enabling the Mu controller, the MU_LCK_EN bit can be set and the IRQ output signal monitored to determine when lock has been established before continuing in a similar manner with the data receiver controllers. Note that the relevant LCK bit should be cleared before continuing to the next controller. After all controllers are locked, the lost lock enable bits (that is, x_LST_EN) should be set.

Table 28. Interrupt Request Registers

Address (Hex)	Bit	Description
0x03	3	MU_LST_EN
	2	MU_LCK_EN
	1	RCV_LST_EN
	0	RCV_LCK_EN
0x04	3	MU_LST_IRQ
	2	MU_LCK_IRQ
	1	RCV_LST_IRQ
	0	RCV_LCK_IRQ
0x21	3	RCVR_TRK_ON
	1	RCVR_LST
	0	RCVR_LCK
0x2A	1	MU_LST
	0	MU_LKD

ANALOG INTERFACE CONSIDERATIONS

ANALOG MODES OF OPERATION

The AD9737A/AD9739A use the quad-switch architecture shown in Figure 169. The quad-switch architecture masks the code-dependent glitches that occur in a conventional two-switch DAC. Figure 170 compares the waveforms for a conventional DAC and the quad-switch DAC. In the two-switch architecture, a code-dependent glitch occurs each time the DAC switches to a different state (that is, D1 to D2). This code-dependent glitching causes an increased amount of distortion in the DAC. In quad-switch architecture (no matter what the codes are), there are always two switches transitioning at each half clock cycle, thus eliminating the code-dependent glitches. However, a constant glitch occurs at 2 × DACCLK_x because half the internal switches change state on the rising DACCLK_x edge whereas the other half change state on the falling DACCLK_x edge.

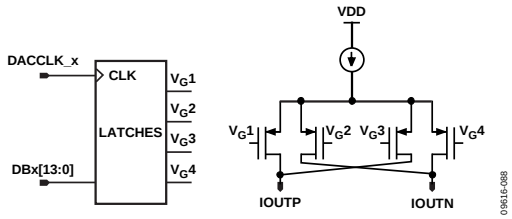


Figure 169. AD9739A Quad-Switch Architecture

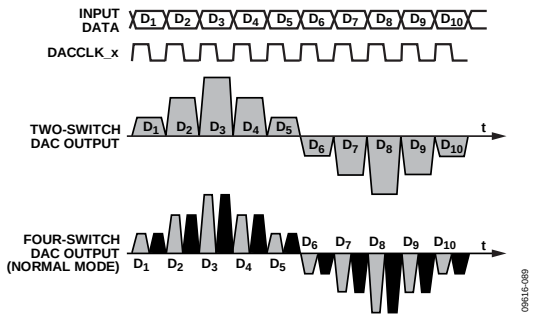


Figure 170. Two-Switch and Quad-Switch DAC Waveforms

Another attribute of the quad-switch architecture is that it also enables the DAC core to operate in one of the following two modes: normal mode and mix-mode. The mode is selected via SPI Register 0x08, Bits[1:0], with normal mode being the default value. In the mix-mode, the output is effectively chopped at the DAC sample rate. This has the effect of reducing the power of the fundamental signal while increasing the power of the images centered around the DAC sample rate, thus improving the output power of these images.

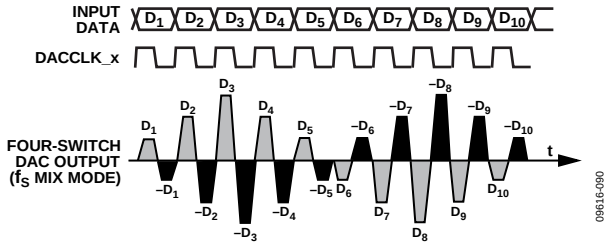


Figure 171. Mix-Mode DAC Waveforms

Figure 171 shows the DAC waveforms for mix-mode. This ability to change modes provides the user the flexibility to place a carrier anywhere in the first two Nyquist zones, depending on the operating mode selected. Switching between the analog modes reshapes the sinc roll-off that is inherent at the DAC output. The maximum amplitude in both Nyquist zones is impacted by this sinc roll-off, depending on where the carrier is placed (see Figure 172). As a practical matter, the usable bandwidth in the third Nyquist zone becomes limited at higher DAC clock rates (that is, >2 GSPS) when the output bandwidth of the DAC core and the interface network (that is, balun) contributes to additional roll-off.

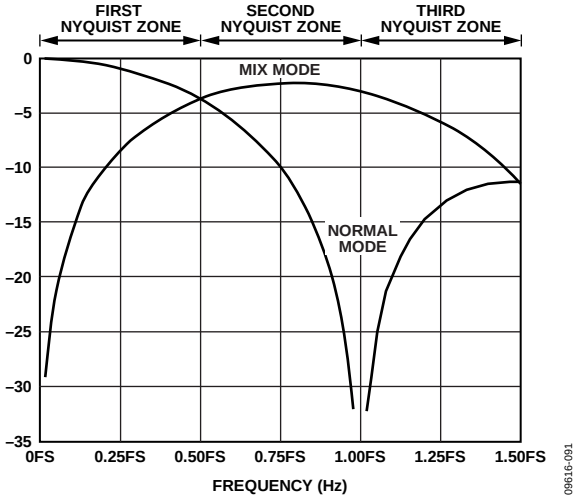


Figure 172. Sinc Roll-Off for Each Analog Operating Mode

CLOCK INPUT CONSIDERATIONS

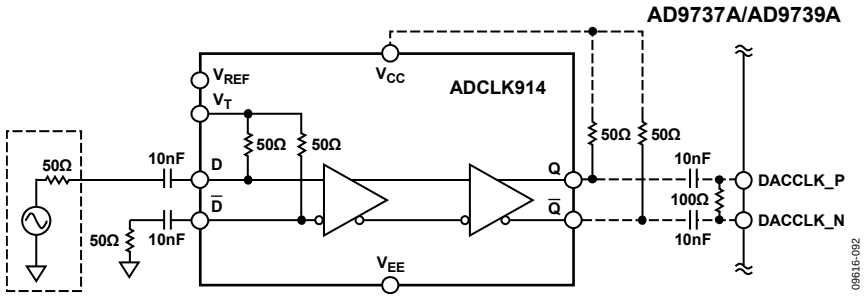


Figure 173. ADCLK914 Interface to the AD9737A/AD9739A CLK Input

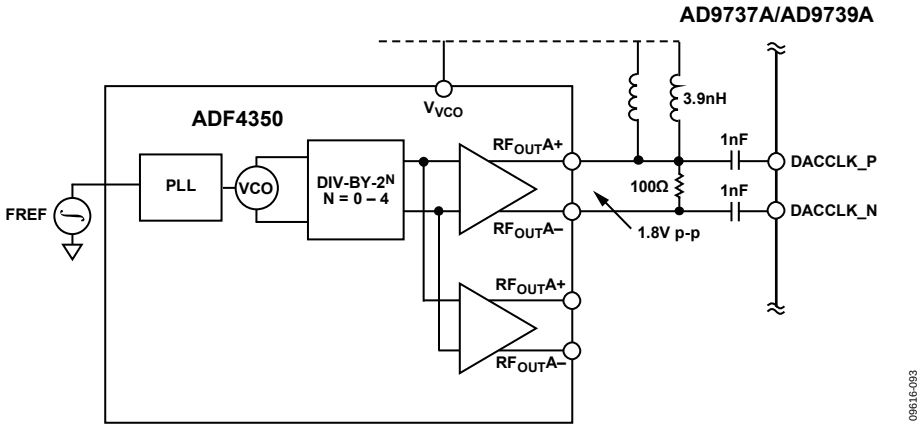


Figure 174. ADF4350 Interface to the AD9737A/AD9739A CLK Input

The quality of the clock source and its drive strength are important considerations in maintaining the specified ac performance. The phase noise and spur characteristics of the clock source should be selected to meet the target application requirements. For optimal ac performance of the AD9737A/AD9739A, the recommended minimum differential peak-to-peak voltage is approximately 1.4 VPP. Phase noise and spurs at a given frequency offset on the clock source are directly translated to the output signal. It can be shown that the phase noise characteristics of a reconstructed output sine wave are related to the clock source by 20 × log10(f_{OUT}/f_{CLK}) when the DAC clock path contribution, along with thermal and quantization effects, are negligible.

The AD9737A/AD9739A clock receiver provides optimum jitter performance when driven by a fast slew rate originating from the LVPECL or CML output drivers. For a low jitter sinusoidal clock source, the ADCLK914 can be used to square-up the signal and provide a CML input signal for the AD9737A/AD9739A clock receiver. Note that all specifications and characterization presented in the data sheet are with the ADCLK914 driven by a high quality RF signal generator with the clock receiver biased at an 800 mV level.

Figure 174 shows a clock source based on the ADF4350 low phase noise/jitter PLL. The ADF4350 can provide output frequencies from 140 MHz up to 4.4 GHz with jitter as low as 0.5 ps rms. Each single-ended output can provide a squared-up output level that can be varied from −4 dBm to +5 dBm, allowing for >2 V p-p output differential swings. The ADF4350 also includes an additional CML buffer that can be used to drive another AD9737A/AD9739A device.

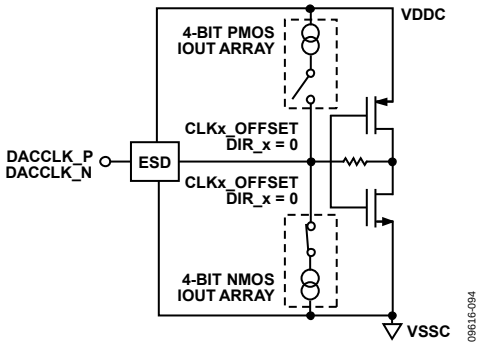


Figure 175. Clock Input and Common-Mode Control

The AD9737A/AD9739A clock receiver features the ability to independently adjust the common-mode level of its inputs over a span of ±100 mV centered about its mid-supply point (that is, VDDC/2), as well as an offset for hysteresis purposes. Figure 175 shows the equivalent input circuit of one of the inputs. ESD diodes are not shown for clarity purposes. It has been found through characterization that the optimum setting is for both inputs to be biased at approximately 0.8 V. This can be achieved by writing a 0x0F (corresponding to a −15) setting to both cross controller registers (that is, Register 0x22 and Register 0x23).

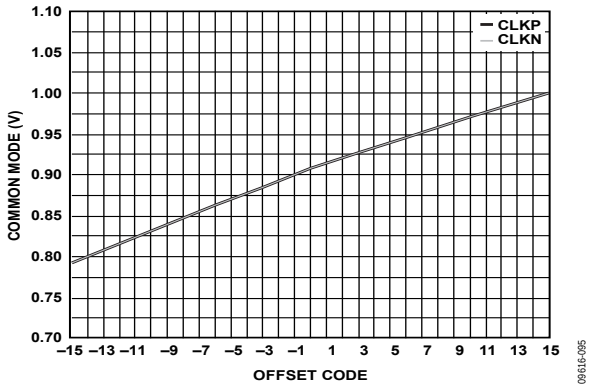


Figure 176. Common-Mode Voltage with Respect to CLKP_OFFSET/CLKN_OFFSET and DIR_P/DIR_N

VOLTAGE REFERENCE

The AD9737A/AD9739A output current is set by a combination of digital control bits and the I120 reference current, as shown in Figure 177.

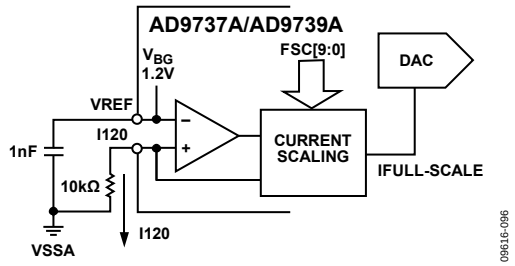


Figure 177. Voltage Reference Circuit

The reference current is obtained by forcing the band gap voltage across an external 10 kΩ resistor from I120 (Pin B14) to ground. The 1.2 V nominal band gap voltage (VREF) generates a 120 µA reference current in the 10 kΩ resistor. Note the following constraints when configuring the voltage reference circuit:

- Both the 10 kΩ resistor and 1 nF bypass capacitor are required for proper operation.
- Digitally adjust the DAC's output full-scale current, I_{OUTFS}, from its default setting of 20 mA.
- The AD9737A/AD9739A are not a multiplying DAC. Modulating the reference current, I120, with an ac signal is not supported.
- The band gap voltage appearing at the VREF pin (Pin C14) must be buffered for use with an external circuitry because its output impedance is approximately 5 kΩ.
- An external reference can be used to overdrive the internal reference by connecting it to the VREF pin.

I_{OUTFS} can be adjusted digitally over 8.7 mA to 31.7 mA by using FSC[9:0] (Register 0x06 and Register 0x07).

The following equation relates I_{OUTFS} to the FSC[9:0] bits, which can be set from 0 to 1023.

$$I_{OUTFS} = 22.6 \times FSC[9:0]/1000 + 8.7 \quad (1)$$

Note that a default value of 0x200 generates 20 mA full scale, which is used for most of the characterization presented in this data sheet (unless noted otherwise).

ANALOG OUTPUTS

Equivalent DAC Output and Transfer Function

The AD9737A/AD9739A provide complementary current outputs, IOUTP and IOUTN, that source current into an external ground reference load. Figure 178 shows an equivalent output circuit for the DAC. Note that, compared to most current output DACs of this type, the AD9737A/AD9739A outputs exhibit a slight offset current (that is, $I_{OUTFS}/16$), and the peak differential ac current is slightly below $I_{OUTFS}/2$ (that is, $15/32 \times I_{OUTFS}$).

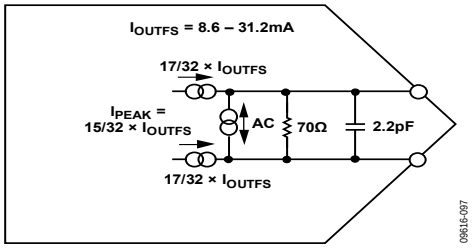


Figure 178. Equivalent DAC Output Circuit

As shown in Figure 178, the DAC output can be modeled as a pair of dc current sources that source a current of $17/32 \times I_{OUTFS}$ to each output. A differential ac current source, I_{PEAK}, is used to model the signal-dependent nature of the DAC output. The polarity and signal dependency of this ac current source are related to the digital code by the following equation:

$$F(Code) = (DACCODE - 8192)/8192 \quad (2)$$

$$-1 \leq F(Code) < 1 \quad (3)$$

where *DACCODE* = 0 to 16,383 (decimal).

Because I_{PEAK} can swing $\pm(15/32) \times I_{OUTFS}$, the output currents measured at IOUTP and IOUTN can span from $I_{OUTFS}/16$ to I_{OUTFS}. However, because the ac signal-dependent current component is complementary, the sum of the two outputs is always constant (that is, IOUTP + IOUTN = $(34/32) \times I_{OUTFS}$).

The code-dependent current measured at the IOUTP and IOUTN outputs is as follows:

$$IOUTP = 17/32 \times I_{OUTFS} + 15/32 \times I_{OUTFS} \times F(Code) \quad (4)$$

$$IOUTN = 17/32 \times I_{OUTFS} - 15/32 \times I_{OUTFS} \times F(Code) \quad (5)$$

Figure 179 shows the IOUTP vs. DACCODE transfer function when I_{OUTFS} is set to 19.65 mA.

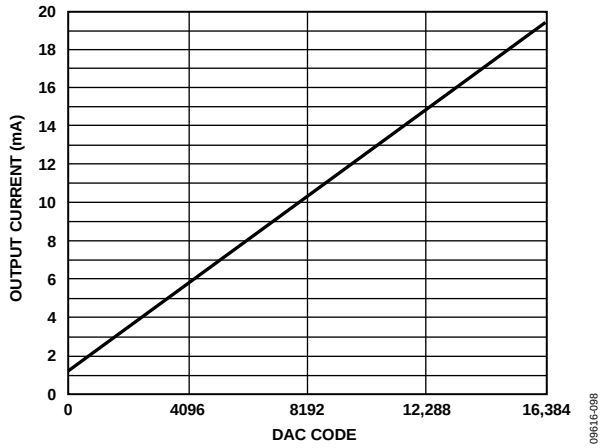


Figure 179. Gain Curve for FSC[9:0] = 512, DAC OFFSET = 1.228 mA

Peak DAC Output Power Capability

The maximum peak power capability of a differential current output DAC is dependent on its peak differential ac current, I_{PEAK}, and the equivalent load resistance it sees. Because the AD9737A/AD9739A include a differential 70 Ω resistance, it is best to use a doubly terminated external output network similar to what is shown in Figure 181. In this case, the equivalent load seen by the ac current source of the DAC is 25 Ω.

If the AD9737A/AD9739A are programmed for I_{OUTFS} = 20 mA, the peak ac current is 9.375 mA and the peak power delivered to the equivalent load is 2.2 mW (that is, $P = I^2R$). Because the source and load resistance seen by the 1:1 balun are equal, this power is shared equally; therefore, the output load receives 1.1 mW or 0.4 dBm.

To calculate the rms power delivered to the load, the following must be considered:

- Peak-to-rms of the digital waveform
- Any digital backoff from digital full scale
- The DAC's sinc response and nonideal losses in external network

For example, a reconstructed sine wave with no digital backoff ideally measures −2.6 dBm because it has a peak-to-rms ratio of 3 dB. If a typical balun loss of 0.4 dBm is included, −3 dBm of actual power can be expected in the region where the sinc response of the DAC has negligible influence. Increasing the output power is best accomplished by increasing I_{OUTFS}, although any degradation in linearity performance must be considered acceptable for the target application.

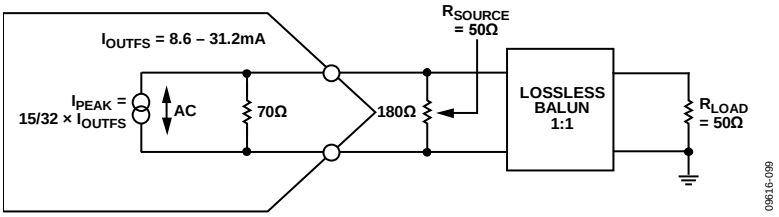


Figure 180. Equivalent Circuit for Determining Maximum Peak Power to a 50 Ω Load

OUTPUT STAGE CONFIGURATION

The AD9737A/AD9739A are intended to serve high dynamic range applications that require wide signal reconstruction bandwidth (that is, DOCSIS CMTS) and/or high IF/RF signal generation. Optimum ac performance can be realized only if the DAC output is configured for differential (that is, balanced) operation with its output common-mode voltage biased to analog ground. The output network used to interface to the DAC should provide a near 0 Ω dc bias path to analog ground. Any imbalance in the output impedance between the IOUTP and IOUTN pins results in asymmetrical signal swings that degrade the distortion performance (mostly even order) and noise performance. Component selection and layout are critical in realizing the performance potential of the AD9737A/AD9739A.

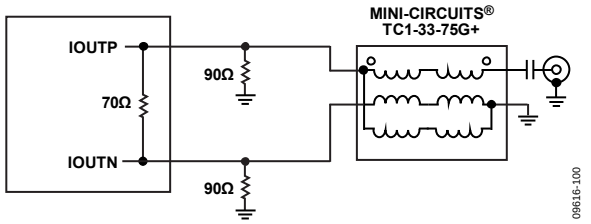


Figure 181. Recommended Balun for Wideband Applications with Upper Bandwidths of up to 2.2 GHz

Most applications requiring balanced-to-unbalanced conversion can take advantage of the Ruthroff 1:1 balun configuration shown in Figure 181. This configuration provides excellent amplitude/phase balance over a wide frequency range while providing a 0 Ω dc bias path to each DAC output. Also, its design provides exceptional bandwidth and can be considered for applications requiring signal reconstruction of up to 2.2 GHz. The characterization plots shown in this data sheet are based on the AD9737A/AD9739A evaluation board, which uses this configuration. Figure 182 compares the measured frequency response for normal and mix-mode using the AD9737A/AD9739A evaluation board vs. the ideal frequency response.

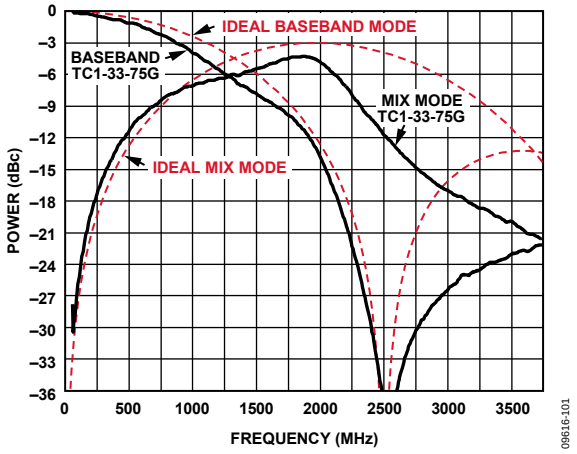


Figure 182. Measured vs. Ideal Frequency Response for Normal (Baseband) and Mix-Mode Operation Using a TC1-33-75G Transformer on the AD9737A/AD9739A EVB

Figure 183 shows an interface that can be considered when interfacing the DAC output to a self-biased differential gain block. The inductors shown serve as RF chokes (L) that provide the dc bias path to analog ground. The value of the inductor, along with the dc blocking capacitors (C), determines the lower cutoff frequency of the composite pass-band response. An RF balun should also be considered before the RF differential gain stage and any filtering to ensure symmetrical common-mode impedance seen by the DAC output while suppressing any common mode noise, harmonics, and clock spurs prior to amplification.

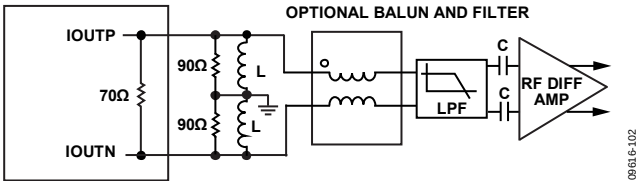


Figure 183. Interfacing the DAC Output to the Self-Biased Differential Gain Stage

For applications operating the AD9737A/AD9739A in mix-mode with output frequencies extending beyond 2.2 GHz, the circuits shown in Figure 184 should be considered. The circuit in Figure 184 uses a wideband balun with a configuration similar to the one shown in Figure 183 to provide a dc bias path for the DAC outputs. The circuit in Figure 185 takes advantage of ceramic chip baluns to provide a dc bias path for the DAC outputs while providing excellent amplitude/phase balance over a narrower RF band. These low cost, low insertion loss baluns are available for different popular RF bands and provide excellent amplitude/phase balance over their specified frequency range.

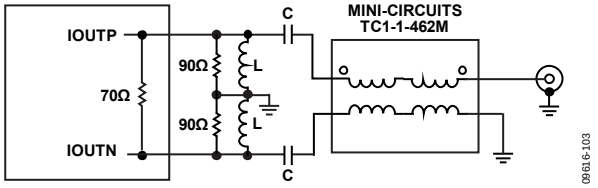


Figure 184. Recommended Mix-Mode Configuration Offering Extended RF Bandwidth Using a TC1-1-43A+ Balun

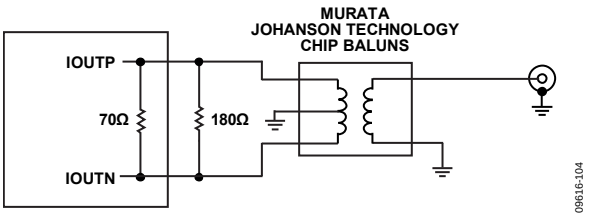


Figure 185. Lowest Cost and Size Configuration for Narrow RF Band Operation

NONIDEAL SPECTRAL ARTIFACTS

The AD9737A/AD9739A output spectrum contains spectral artifacts that are not part of the original digital input waveform. These nonideal artifacts include harmonics (including alias harmonics), images, and clock spurs. Figure 186 shows a spectral plot of the AD9737A/AD9739A within the first Nyquist zone (that is, dc to $f_{DAC}/2$) reconstructing a 650 MHz, 0 dBFS sine wave at 2.4 GSPS. Besides the desired fundamental tone at the −7.8 dBm level, the spectrum also reveals these nonideal artifacts that also appear as spurs above the measurement noise floor. Because these nonideal artifacts are also evident in the second and third Nyquist zones during mix-mode operation, the effects of these artifacts should also be considered when selecting the DAC clock rate for a target RF band.

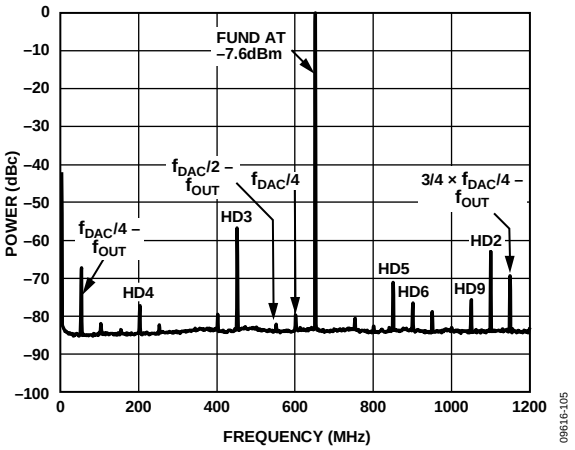


Figure 186. Spectral Plot

Note the following important observations pertaining to these nonideal spectral artifacts:

1. A full-scale sine wave (that is, single-tone) typically represents the worst case condition because it is has a peak-to-rms ratio of 3 dB and is unmodulated. Harmonics and aliased harmonics of a sine wave are easy to identify because they also appear as discrete spurs. Significant characterization of a high speed DAC is performed using single (or multitone) signals for this reason.
2. Modulated signals (that is, AM, PM, or FM) do not appear as spurs but rather as signals whose power spectral density is spread over a defined bandwidth determined by the modulation parameters of the signals. Any harmonics from the DAC spread over a wider bandwidth determined by the order of the harmonic and bandwidth of the modulated signal. For this reason, harmonics often appear as slight bumps in the measurement noise floor and can be difficult to discern.
3. Images appear as replicas of the original signal, hence, can be easier to identify. In the case of the AD9737A/AD9739A, internal modulation of the sampling clock at intervals related to $f_{DAC}/4$ generate image pairs at ¼ × f_{DAC}, ½ × f_{DAC}, and ¾ × f_{DAC}. Both upper and lower sideband images associated with ¼ × f_{DAC} fall within the first Nyquist zone, whereas only the lower image of ½ × f_{DAC} and ¾ × f_{DAC} fall back. Note that the lower images appear frequency inverted. The ratio between the fundamental and various images (that is, dBc) remains mostly signal independent because the mechanism causing these images is related to corruption of the sampling clock.
4. The magnitude of these images for a given device depends on several factors, including DAC clock rate, output frequency, and Mu controller phase setting. Because the image magnitude is repeatable between power-up cycles (assuming the same conditions), a one-time factory calibration procedure can be used to improve suppression. Calibration consists of additional dedicated DSP resources in the host that can generate a replica of the image with proper amplitude, phase, and frequency scaling to cancel the image from the DAC. Because the image magnitude can vary among devices, each device must be calibrated.
5. A clock spur appears at $f_{DAC}/4$ and integer multiples of it. Similar to images, the spur magnitude also depends on the same factors that cause variations in image levels. However, unlike images and harmonics, clock spurs always appear as discrete spurs, albeit their magnitude shows a slight dependency on the digital waveform and output frequency. The calibration method is similar to image calibration; however, only a digital tone of equal amplitude and opposite phase at $f_{DAC}/4$ need be generated.
6. A large clock spur also appears at 2 × f_{DAC} in either normal or mix-mode operation. This clock spur is due to the quad switch DAC architecture causing switching events to occur on both edges of f_{DAC}.

LAB EVALUATION OF THE AD9737A/AD9739A

Figure 187 shows a recommended lab setup that was used to characterize the performance of the AD9737A/AD9739A. The DPG2 is a dual port LVDS/CMOS data pattern generator that is available from Analog Devices, Inc., with an up to 1.25 GSPS data rate. The DPG2 directly interfaces to the AD9737A/AD9739A evaluation board via Tyco Z-PACK HM-Zd connectors. A low phase noise/jitter RF source such as an R&S SMA100A signal generator is used for the DAC clock. A +5 V power supply is used to power up the AD9737A/AD9739A evaluation board, and SMA cabling is used to interface to the supply, clock source, and spectrum analyzer. A USB 2.0 interface to a host PC is used to communicate to both the AD9737A/AD9739A evaluation board and the DPG2.

A high dynamic range spectrum analyzer is required to evaluate the ac performance of the AD9737A/AD9739A reconstructed waveform. This is especially the case when measuring ACLR performance for high dynamic range applications such as multicarrier DOCSIS CMTS applications. Harmonic, SFDR, and IMD measurements pertaining to unmodulated carriers can benefit by using a sufficiently high RF attenuation setting because these artifacts are easy to identify above the spectrum analyzer noise floor. However, reconstructed waveforms having modulated carrier(s) often benefit from the use of a high dynamic range RF amplifier and/or passive filters to measure close-in and wideband ACLR performance when using spectrum analyzers of limited dynamic range.

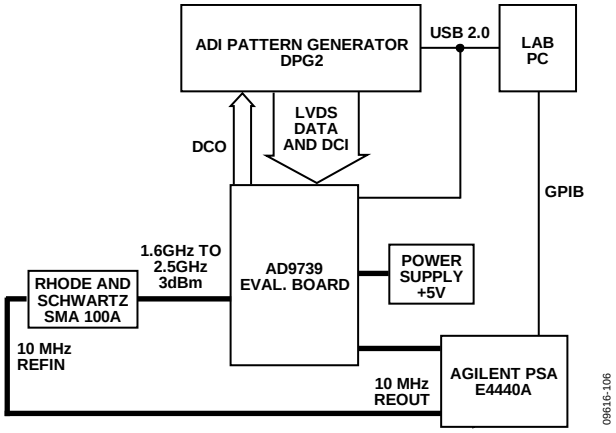


Figure 187. Lab Test Setup Used to Characterize the AD9737A/AD9739A

RECOMMENDED START-UP SEQUENCE

On power-up of the AD9737A/AD9739A, a host processor is required to initialize and configure the AD9737A/AD9739A via its SPI port. Figure 188 shows a flowchart of the sequential steps required. Table 29 provides more detail on the SPI register write/read operations required to implement the flowchart steps. Note the following:

- A software reset is optional because the AD9737A/AD9739A have both an internal POR circuit and a RESET pin.
- The Mu controller must be first enabled (and in track mode) before the data receiver controller is enabled because the DCO output signal is derived from this circuitry.
- A wait period is related to f_{DATA} periods.
- Limit the number of attempts to lock the controllers to three; locks typically occur on the first attempt.
- Hardware or software interrupts can be used to monitor the status of the controllers.

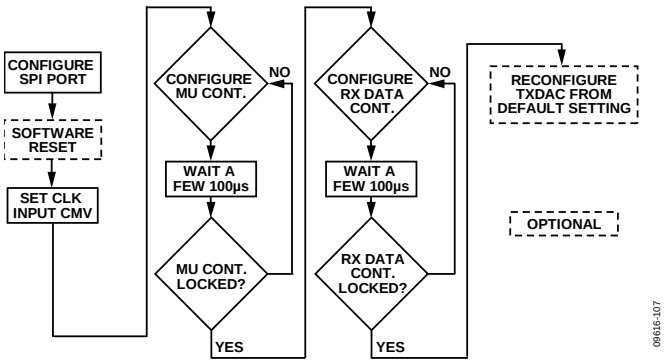
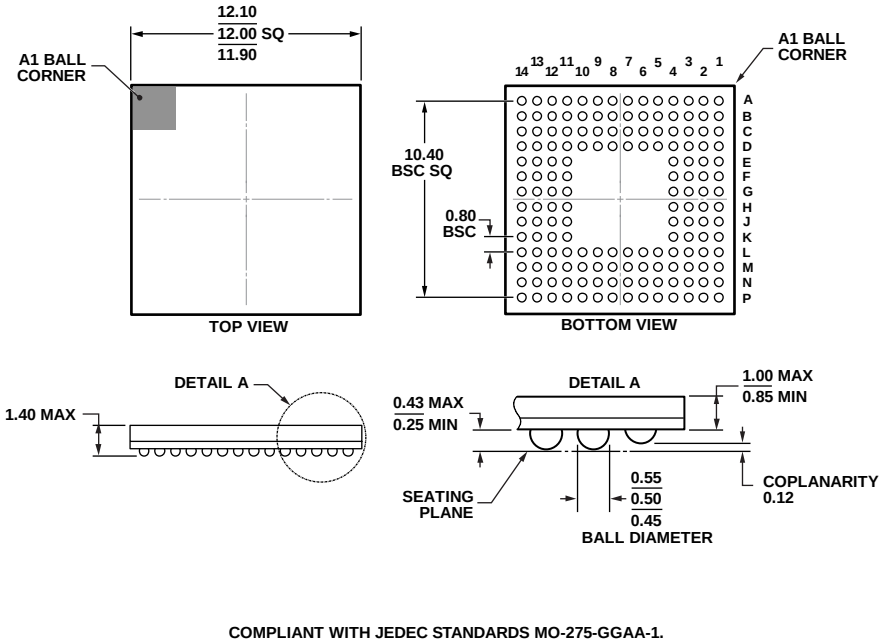


Figure 188. Flowchart for Initialization and Configuration of the AD9737A/AD9739A

Table 29. Recommended SPI Initialization

Step	Address (Hex)	Write Value	Comments
1	0x00	0x00	Configure for the 4-wire SPI mode with MSB. Note that Bits[7:5] must be mirrored onto Bits[2:0] because the MSB/LSB format can be unknown at power-up.
2	0x00	0x20	Software reset to default SPI values.
3	0x00	0x00	Clear the reset bit.
4	0x22	0x0F	Set the common-mode voltage of DACCLK_P and DACCLK_N inputs
5	0x23	0x0F	
6	0x24	0x30	Configure the Mu controller.
7	0x25	0x80	
8	0x27	0x44	
9	0x28	0x6C	
10	0x29	0xCB	
11	0x26	0x02	
12	0x26	0x03	Enable the Mu controller search and track mode.
13			Wait for 160 k × 1/f_{DATA} cycles.
14	0x2A		Read back Register 0x2A and confirm that it is equal to 0x01 to ensure that the DLL loop is locked. If it is not locked, return to Step 10 and repeat. Limit attempts to three before breaking out of the loop and reporting a Mu lock failure.
15			Ensure that the AD9737A/AD9739A are fed with DCI clock input from the data source.
16	0x13	0x72	Set FINE_DEL_SKEW to 2.
17	0x10	0x00	Disable the data Rx controller before enabling it.
18	0x10	0x02	Enable the data Rx controller for loop and IRQ.
19	0x10	0x03	Enable the data Rx controller for search and track mode.
20			Wait for 135 k × 1/f_{DATA} cycles.
21	0x21		Read back Register 0x21 and confirm that it is equal to 0x09 to ensure that the DLL loop is locked and tracking. If it is not locked and tracking, return to Step 16 and repeat. Limit attempts to three before breaking out of the loop and reporting an Rx data lock failure.
22	0x06 0x07	0x00 0x02	Optional: modify the TxDAC I_{OUTFS} setting (the default is 20 mA).
23	0x08	0x00	Optional: modify the TxDAC operation mode (the default is normal mode).

OUTLINE DIMENSIONS



COMPLIANT WITH JEDEC STANDARDS MO-275-GGAA-1.

Figure 189. 160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-160-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9737ABBCZ	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9737ABBCZRL	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9737A-EBZ		Evaluation Board for Normal, CMTS, and Mix-Mode Evaluation	
AD9739ABBCZ	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9739ABBCZRL	−40°C to +85°C	160-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-160-1
AD9739A-EBZ		Evaluation Board for Normal, CMTS, and Mix-Mode Evaluation	
AD9739A-FMC-EBZ		Evaluation Board with FMC Connector for Xilinx Based FPGA Development Platforms	

[1] Z = RoHS Compliant Part.

NOTES

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