Single-Ended 8-Channel/ Differential 4-Channel Analog Multiplexer with SMBus Interface

FEATURES

- Micropower Operation: Supply Current = 20µA Max
- 2-Wire SMBus Interface
- Single 2.7V to ±5V Supply Operation
- Expandable to 32 Single or 16 Differential Channels
- Guaranteed Break-Before-Make
- Low R_{ON}: 35Ω Single Ended/70Ω Differential
- Low Charge Injection: 20pC Max
- Low Leakage: ±5nA Max
- Available in 16-Lead SO and GN Packages

APPLICATIONS

- Data Acquisition Systems
- Process Control
- Laptop Computers
- Signal Multiplexing/Demultiplexing
- Analog-to-Digital Conversion Systems

DESCRIPTION

The LTC®1380/LTC1393 are CMOS analog multiplexers with SMBus® compatible digital interfaces. The LTC1380 is a single-ended 8-channel multiplexer, while the LTC1393 is a differential 4-channel multiplexer. The SMBus digital interface requires only two wires (SCL and SDA). Both the LTC1380 and the LTC1393 have four hard-wired SMBus addresses, selectable with two external address pins. This allows four devices, each with a unique SMBus address, to coexist on one system and for four devices to be synchronized with one stop bit.

The supply current is typically 10µA. Both digital interface pins are SMBus compatible over the full operating supply voltage range. The LTC1380 analog switches feature a typical R_{ON} of 35Ω (±5V supplies), typical switch leakage of 20pA and guaranteed break-before-make operation. Charge injection is ±1pC typical.

The LTC1380/LTC1393 are available in 16-lead SO and GN packages. Operation is fully specified over the commercial and industrial temperature ranges.

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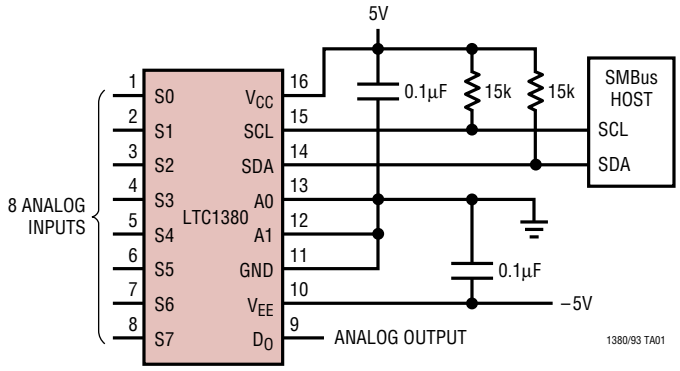
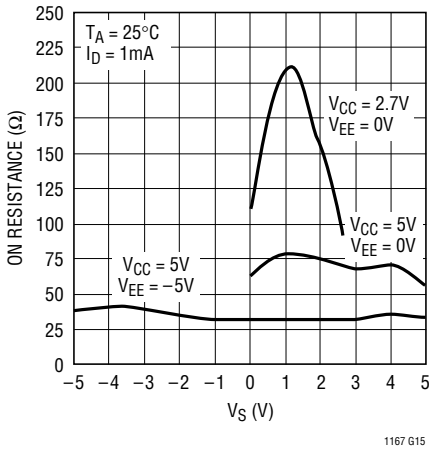
SMBus is a registered trademark of Intel Corporation.

TYPICAL APPLICATION

LTC1380 Single-Ended 8-Channel Multiplexer



On Resistance vs V_S



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage
- LTC1380 (V_{CC} to V_{EE}) 15V
- LTC1393 (V_{CC} to GND) 15V

Analog Input Voltage
- LTC1380 ..... V_{EE} – 0.3V to V_{CC} + 0.3V
- LTC1393 ..... – 0.3V to V_{CC} + 0.3V

Digital Inputs .....–0.3V to 15V
- LTC1380 (V_{CC} TO V_{EE}) .... (V_{EE} – 0.3V) to (V_{EE} + 15V)
- LTC1393 (V_{CC} to GND) .....–0.3V to 15V

Maximum Switch-On Current 65mA

Power Dissipation 500mW

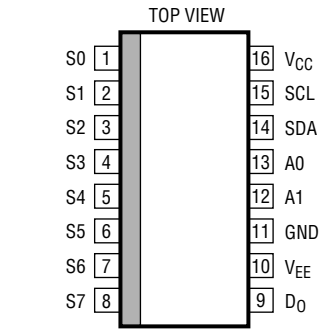
Operating Ambient Temperature Range
- LTC1380C/LTC1393C ..... 0°C ≤ T_A ≤ 70°C
- LTC1380I/LTC1393I ..... –40°C ≤ T_A ≤ 85°C

Junction Temperature ..... 125°C

Storage Temperature Range ..... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

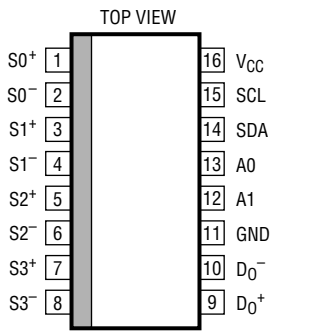


GN PACKAGE 16-LEAD PLASTIC SSOP
S PACKAGE 16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (GN)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER

LTC1380CGN
LTC1380CS
LTC1380IGN
LTC1380IS



GN PACKAGE 16-LEAD PLASTIC SSOP
S PACKAGE 16-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 130°C/W (GN)
T_{JMAX} = 125°C, θ_{JA} = 100°C/W (S)

ORDER PART NUMBER

LTC1393CGN
LTC1393CS
LTC1393IGN
LTC1393IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS (Notes 2, 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{ANALOG}	Analog Signal Range	LTC1380	●	V_{EE}		V_{CC}	V
		LTC1393	●	0		V_{CC}	V
R_{ON}	On Resistance	LT1380: V_{CC} = 5V, V_{EE} = –5V,			35	70	Ω
		$V_{EE} \le (V_S, V_D) \le V_{CC}$, I_D = ±1mA	●			120	Ω
		LT1393: V_{CC} = 5V,			70	140	Ω
		0V ≤ (V_S, V_D) ≤ V_{CC}, I_D = ±1mA	●			200	Ω
		LT1380/LTC1393: V_{CC} = 2.7V, V_{EE} = 0V,			210	400	Ω
		0V ≤ (V_S, V_D) ≤ V_{CC}, I_D = ±1mA	●			600	Ω
	ΔR_{ON} vs V_S	$V_{EE} \le (V_S, V_D) \le V_{CC}$, V_{CC} = 5V			20		%
	R_{ON} vs Temperature	V_{CC} = 5V			0.5		%/°C
I_{LEAK}	Off-Channel or On-Channel Switch Leakage	LTC1380: (V_{EE} + 0.5V) ≤ (V_S, V_D) ≤ (V_{CC} – 0.5V)			±0.05	±5	nA
		LTC1393: 0.5V ≤ (V_S, V_D) ≤ (V_{CC} – 0.5V)	●			±50	nA

ELECTRICAL CHARACTERISTICS (Notes 2, 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	SCL, SDA Input High Voltage		●	1.4			V
V_{IL}	SCL, SDA Input Low Voltage		●			0.6	V
V_{OL}	SDA Output Low Voltage	I_{SDA} = 3mA	●			0.4	V
V_{AH}	Address Input High Voltage	V_{CC} = 5V	●	2			V
V_{AL}	Address Input Low Voltage	V_{CC} = 5V	●			0.8	V
I_{IN}	SCL, SDA, Address Input Current	$0V \le V_{IN} \le V_{CC}$				±1	µA
I_{CC}	Positive Supply Current	V_{CC} = 5V, All Digital Inputs at 5V	●		10	20	µA
I_{EE}	Negative Supply Current	LTC1380: V_{CC} = 5V, V_{EE} = –5V, All Digital Inputs at 5V	●		–0.1	–5	µA
C_S	Input Off Capacitance	(Note 3)			3		pF
C_D	Output Off Capacitance	(Note 3) LTC1380 LTC1393			26 18		pF pF
t_{ON}	Switch Turn-On Time from Stop Condition	Figure 1 LTC1380: V_{CC} = 5V, V_{EE} = –5V LTC1393: V_{CC} = 5V LTC1380/LTC1393: V_{CC} = 2.7V, V_{EE} = 0V	● ● ●		850 850 1130	1500 1500 2000	ns ns ns
t_{OFF}	Switch Turn-Off Time from Stop Condition	Figure 1 LTC1380: V_{CC} = 5V, V_{EE} = –5V LTC1393: V_{CC} = 5V LTC1380/LTC1393: V_{CC} = 2.7V, V_{EE} = 0V	● ● ●		640 650 670	1200 1200 1200	ns ns ns
t_{OPEN}	Break-Before-Make Interval	$t_{ON} - t_{OFF}$	●	75	210		ns
OIRR	Off-Channel Isolation	Figure 2, V_S = 200mV_{P-P}, R_L = 1k, f = 100kHz (Note 3)			–65		dB
Q_{INJ}	Charge Injection	Figure 3, C_L = 1000pF (Note 3)	●		±1	±20	pC
SMBus Timing (Note 6)							
f_{SMB}	SMBus Operating Frequency		●			100	kHz
t_{BUF}	Bus Free Time Between Stop/Start		●	4.7			µs
$t_{HD:STA}$	Hold Time After (Repeated) Start		●	4.0			µs
$t_{SU:STA}$	Repeated Start Setup Time		●	4.7			µs
$t_{SU:STO}$	Stop Condition Setup Time		●	4.0			µs
$t_{HD:DAT}$	Data Hold Time		●	300			ns
$t_{SU:DAT}$	Data Setup Time		●	250			ns
t_{LOW}	Clock Low Period		●	4.7			µs
t_{HIGH}	Clock High Period		●	4.0			µs
t_f	SCL/SDA Fall Time	Time Interval Between $0.9V_{DD}$ and (V_{ILMAX} – 0.15)	●			300	ns
t_r	SCL/SDA Rise Time	Time Interval Between (V_{ILMAX} – 0.15) and (V_{IHMIN} + 0.15)	●			1000	ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All current into device pins is positive; all current out of device pins is negative. All voltages are referenced to ground unless otherwise specified. All typicals are given for T_A = 25°C, V_{CC} = 5V (for both LTC1380 and LTC1393) and V_{EE} = –5V (LTC1380).

Note 3: These typical parameters are based on bench measurements and are not production tested.

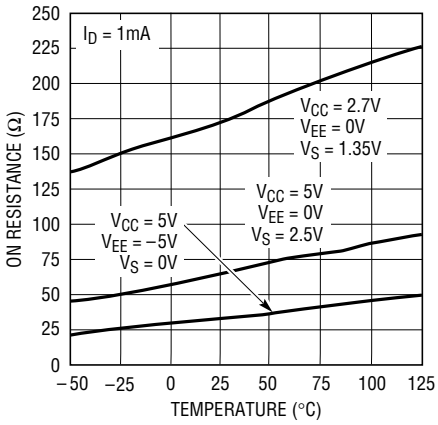
Note 4: Both SCL and SDA assume an external 15k pull-up resistor to a typical SMBus host power supply V_{DD} of 5V.

Note 5: Typical curves with V_{EE} = –5V apply to the LTC1380. Curves with V_{EE} = 0V apply to both the LTC1380 and the LTC1393.

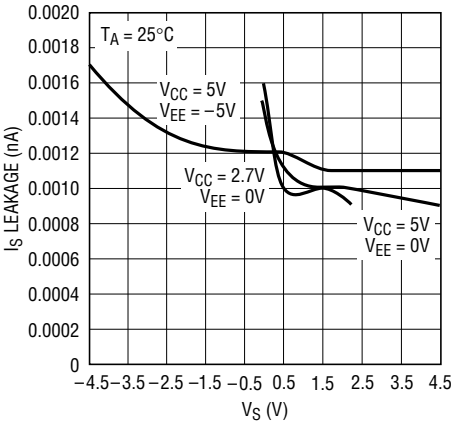
Note 6: These parameters are guaranteed by design and are not tested in production.

TYPICAL PERFORMANCE CHARACTERISTICS (Note 5)

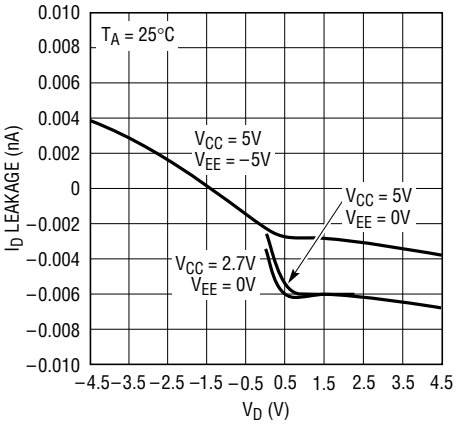
On Resistance vs Temperature



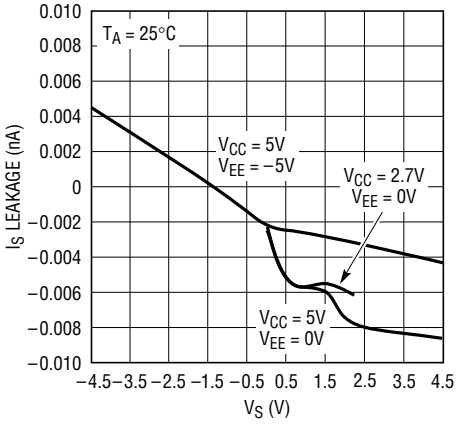
Off-Channel Input Leakage vs V_S



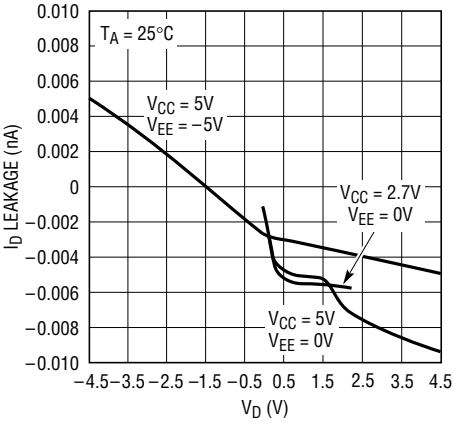
Off-Channel Output Leakage vs V_D



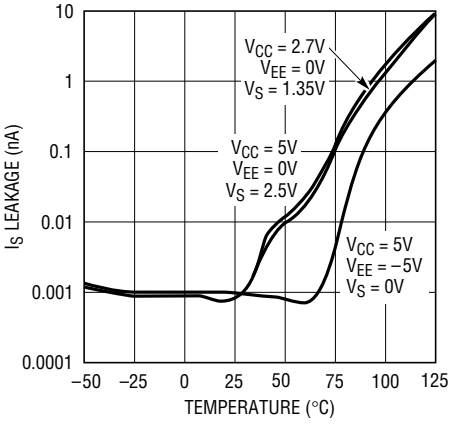
On-Channel Input Leakage vs V_S



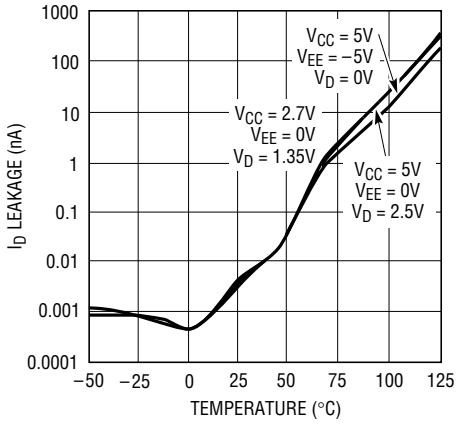
On-Channel Output Leakage vs V_D



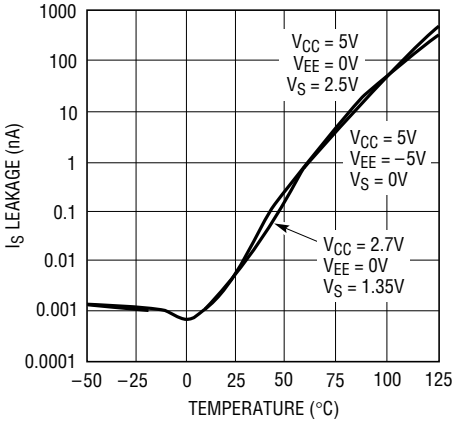
Off-Channel Input Leakage vs Temperature



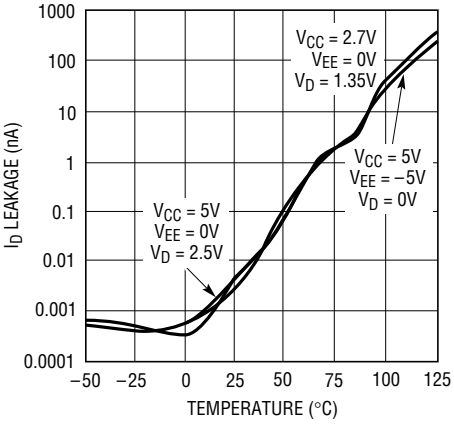
Off-Channel Output Leakage vs Temperature



On-Channel Input Leakage vs Temperature

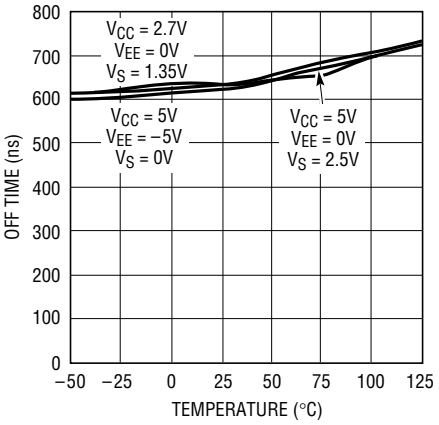


On-Channel Output Leakage vs Temperature

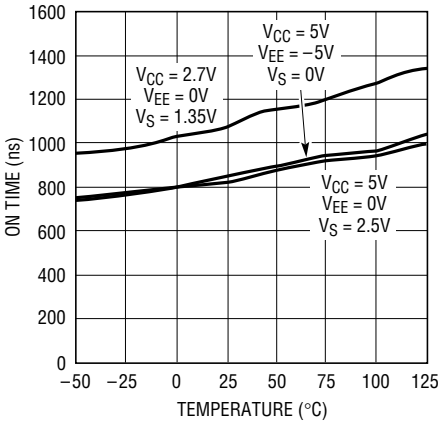


TYPICAL PERFORMANCE CHARACTERISTICS (Note 5)

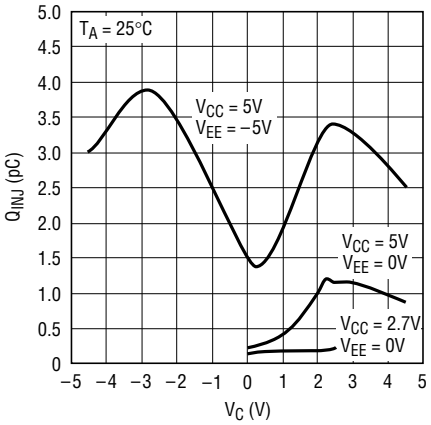
Off Time vs Temperature



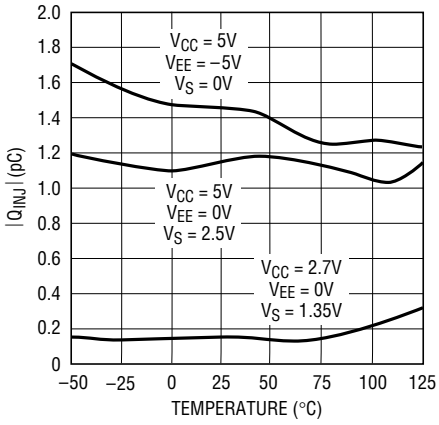
On Time vs Temperature



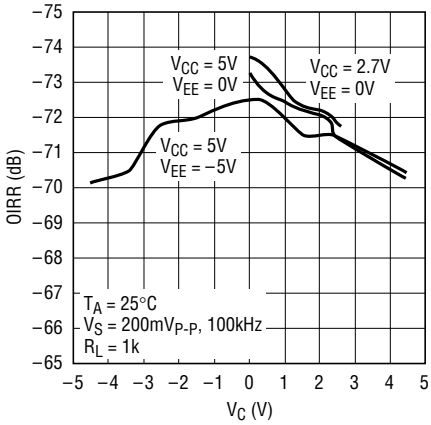
Q_{INJ} vs V_C (Figure 3)



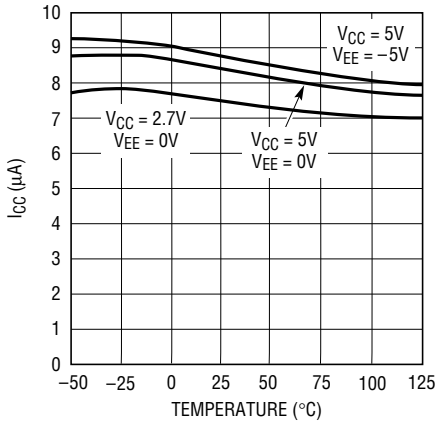
Q_{INJ} vs Temperature (Figure 3)



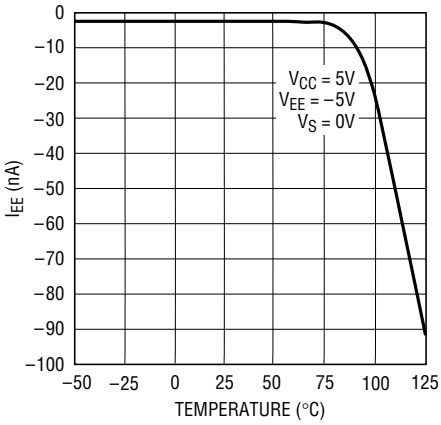
Off-Channel Isolation vs Input Common Mode Voltage (Figure 2)



I_{CC} vs Temperature



I_{EE} vs Temperature



PIN FUNCTIONS

S0 to S7/S0$^{\pm}$ to S3$^{\pm}$ (Pin 1 to Pin 8): Single-Ended Analog Multiplexer Inputs (S0 to S7) for the LTC1380. Differential Analog Multiplexer Inputs (S0$^{\pm}$ to S3$^{\pm}$) for the LTC1393.

D_O/D_O^+ (Pin 9): Analog Multiplexer Output for the LTC1380. Positive Differential Analog Multiplexer Output for the LTC1393.

V_{EE}/D_O^- (Pin 10): Negative Supply Pin for the LTC1380. Negative Differential Multiplexer Output for the LTC1393. For the LTC1380, V_{EE} should be bypassed to GND with a 0.1µF ceramic capacitor when operating from split supplies or connected to GND for single supply operation.

GND (Pin 11): Ground Pin.

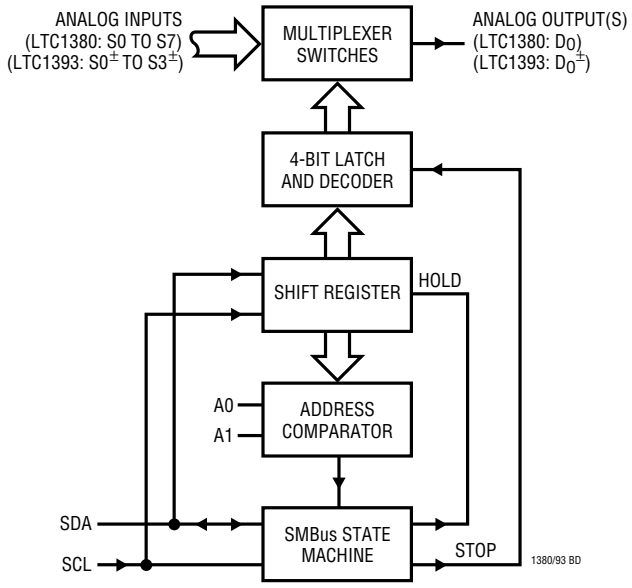
A1, A0 (Pin 12, Pin 13): Address Selection Pins. Tie these two pins to either V_{CC} or GND to select one of four possible addresses to which the LTC1380/LTC1393 will respond.

SDA (Pin 14): SMBus Bidirectional Digital Input/Output Pin. This pin has an open-drain output and requires a pull-up resistor or current source to the positive supply for normal operation. Data is shifted into and acknowledged by the LTC1380/LTC1393 using this pin.

SCL (Pin 15): SMBus Clock Input. SDA data is shifted in at rising edges of this clock during data transfer.

V_{CC} (Pin 16): Positive Supply Pin. This pin should be bypassed to GND with a 0.1µF ceramic capacitor.

BLOCK DIAGRAM



TEST CIRCUITS

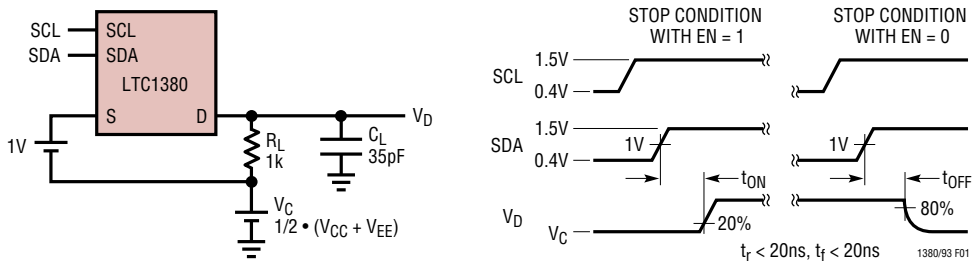


Figure 1. Switch t_{ON}/t_{OFF} Propagation Delay from SMBus STOP Condition

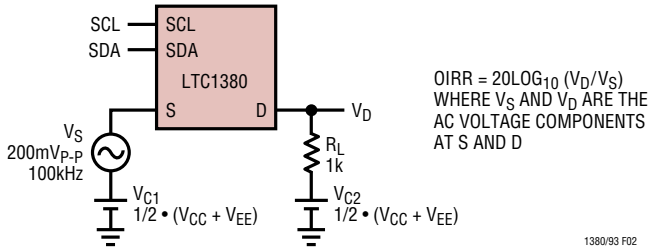


Figure 2. Off-Channel Isolation (OIRR) Test

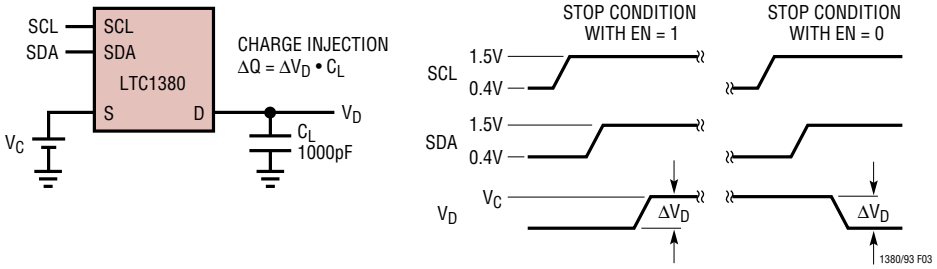
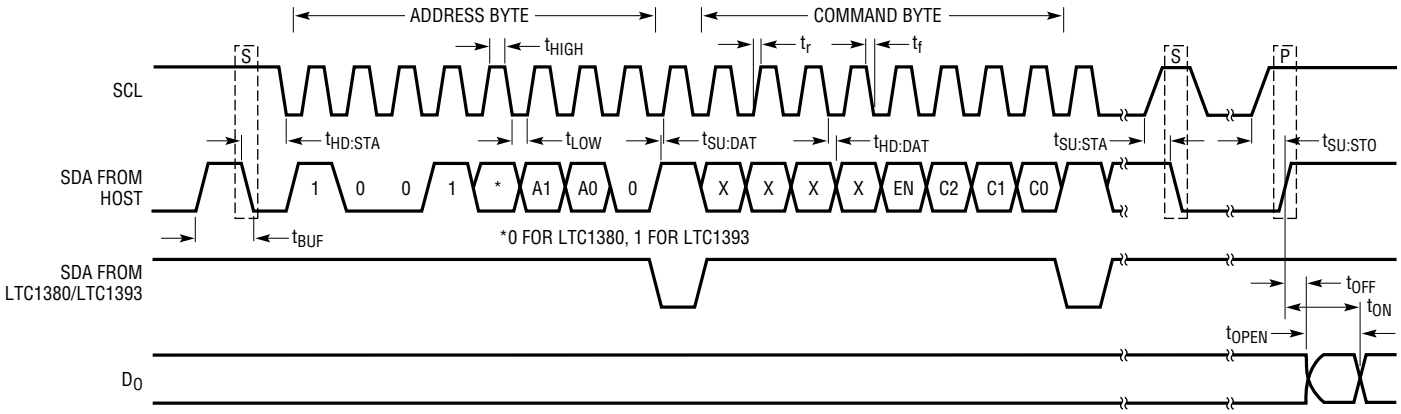


Figure 3. Charge Injection Test

TIMING DIAGRAM



APPLICATIONS INFORMATION

Theory of Operation

The LTC1380/LTC1393 are analog input multiplexers with an SMBus digital interface. The LTC1380 is a single-ended 8-to-1 multiplexer; the LTC1393 is a differential 4-to-1 mulitplexer. The LTC1380 operates on either bipolar or unipolar supplies, the LTC1393 operates on a single supply. The minimum V_{CC} supply for the LTC1380/LTC1393 is 2.7V. The maximum supply voltage (V_{CC} to V_{EE} for the LTC1380, V_{CC} for the LTC1393) should not exceed 14V. The multiplexer switches operate within the entire power supply range. The LTC1380 V_{CC} and V_{EE} supplies can be offset such as 2.7V/–11V and 11V/–3V.

Serial Interface

The LTC1380/LTC1393 serial interface supports SMBus send byte protocol as shown below with two interface signals, SCL and SDA.

LTC1380 Send Byte Protocol

S	1	0	0	1	0	A1	A0	$\overline{W}$	A	X	X	X	X	EN	C2	C1	C0	A	P

LTC1393 Send Byte Protocol

S	1	0	0	1	1	A1	A0	$\overline{W}$	A	X	X	X	X	EN	C2	C1	C0	A	P

ADDRESS BYTE → COMMAND BYTE →

S = SMBus START BIT
P = SMBus STOP BIT (THE FIRST STOP BIT AFTER A SUCCESSFUL COMMAND BYTE UPDATES THE MULTIPLEXER CONTROL LATCH)
A = ACKNOWLEDGE BIT FROM LTC1380/LTC1393
$\overline{W}$ = WRITE COMMAND BIT
A1, A0 = ADDRESS BITS
EN, C2, C1, C0 = MULTIPLEXER CONTROL BITS

A send byte protocol is initiated by the SMBus host with a start bit followed by a 7-bit address code and a write bit. Each slave compares the address code with its address. The send byte write bit is Low. The selected slaves then reply with an acknowledge bit by pulling the SDA line Low. Next, the host sends an 8-bit command byte. When the selected slave receives the whole command byte, it acknowledges and retains the command byte in the shift register. The host can terminate the serial transfer with a stop bit or communicate with another slave device with a repeat start. When a repeat start occurs but the slave is not selected, the command byte data is kept in the shift register but the multiplexer control is not updated. The multiplexer control latches the new command from the shift register on the first stop bit after a successful command byte transfer. This allows the host to synchronize several slave devices with a single stop bit. A1 and A0 select one of the four possible LTC1380/LTC1393 addresses as shown in Table 1. This allows up to four similar devices to share the same SMBus, expanding the multiplexer to 32 single-ended channels with the LTC1380; 16 differential channels with the LTC1393. The first stop bit after a successful send byte transfer will latch in the multiplexer control bits (EN, C2, C1 and C0) and initiate a break-before-make sequence.

APPLICATIONS INFORMATION

Table 1. LTC1380/LTC1393 Address Selection

A1	A0	LTC1380	LTC1393
0	0	90H	98H
0	1	92H	9AH
1	0	94H	9CH
1	1	96H	9EH

SCL is the synchronizing clock generated by the host. SDA is the bidirectional data transfer between the host and the slave. The host initiates a start bit by dropping the SDA line from High to Low while the SCL is High. The stop bit is initiated by changing the SDA line from Low to High while SCL is High. All address, command and acknowledge signals must be valid and should not change while SCL is High. The acknowledge bit signals to the host the acceptance of a correct address byte or the command byte.

At V_{CC} supply above 2.7V, the SCL and SDA input threshold is typically 1V with an input hysteresis of 100mV. The typical SCL and SDA lines have either a resistive or current source pull-up at the host. The LTC1380/LTC1393 have an open-drain NMOS transistor at the SDA pin to sink 3mA below 0.4V during the slave acknowledge sequence. The address selection input A1 and A0 are TTL compatible at V_{CC} = 5V.

Both the LTC1380 and LTC1393 are compatible with the Philips/Signetics I^2C Bus interface. This 1V threshold for SCA and SDA should not pose an operational problem with I^2C applications.

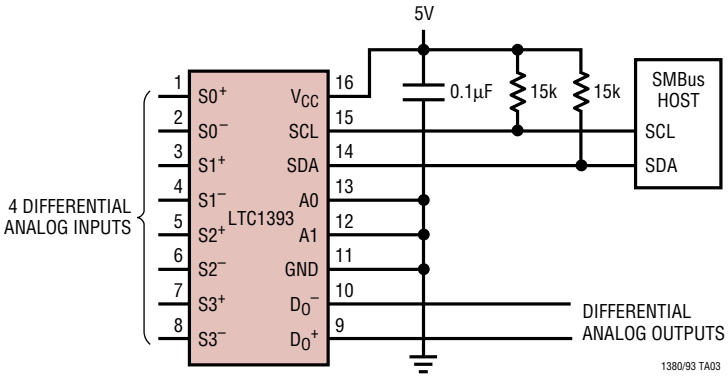
The multiplexer switches are selected as shown in Table 2. Both the LTC1380 and the LTC1393 have an enable bit (EN). A Low disables all switches while a High enables the selected switch as programmed by bits C2, C1 and C0. A stop bit after a successful send byte sequence for LTC1380/LTC1393 will disable all switches before the new selected switch is connected.

Table 2. Multiplexer Control Bits Truth Table

EN	C2	C1	C0	LTC1380 D_0 CHANNEL STATUS	LTC1393 D_0^+, D_0^- CHANNEL STATUS
0	X	X	X	All Off	All Off
1	0	0	0	S0	$S0^+$, $S0^-$
1	0	0	1	S1	
1	0	1	0	S2	$S1^+$, $S1^-$
1	0	1	1	S3	
1	1	0	0	S4	$S2^+$, $S2^-$
1	1	0	1	S5	
1	1	1	0	S6	$S3^+$, $S3^-$
1	1	1	1	S7	

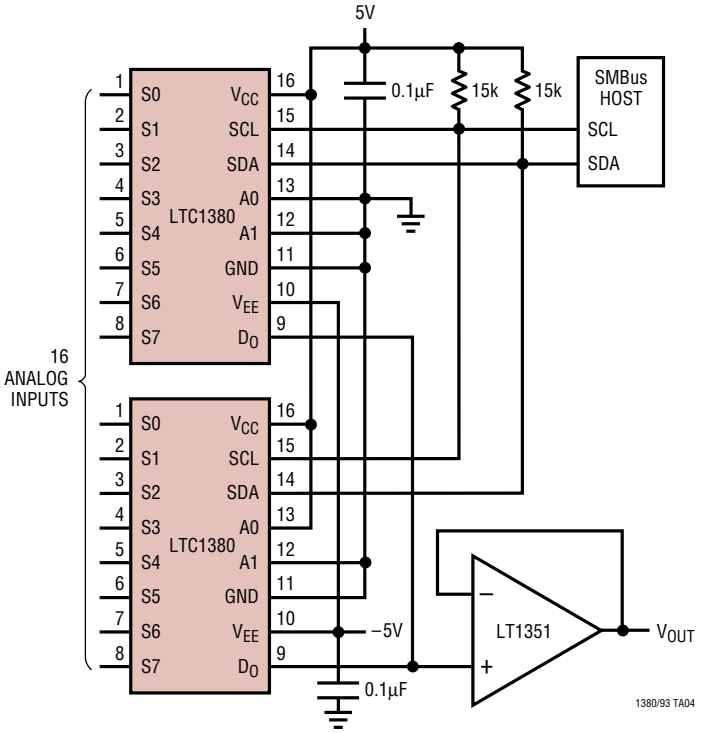
TYPICAL APPLICATIONS

Simplified LTC1393 Application

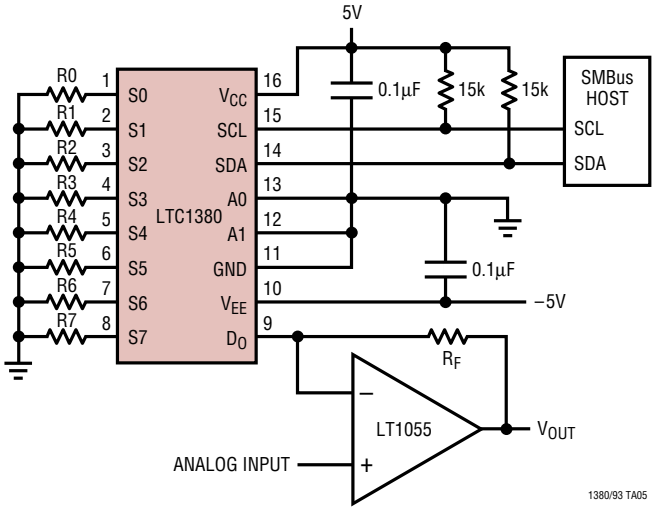


TYPICAL APPLICATIONS

16-Channel Multiplexer with Buffer



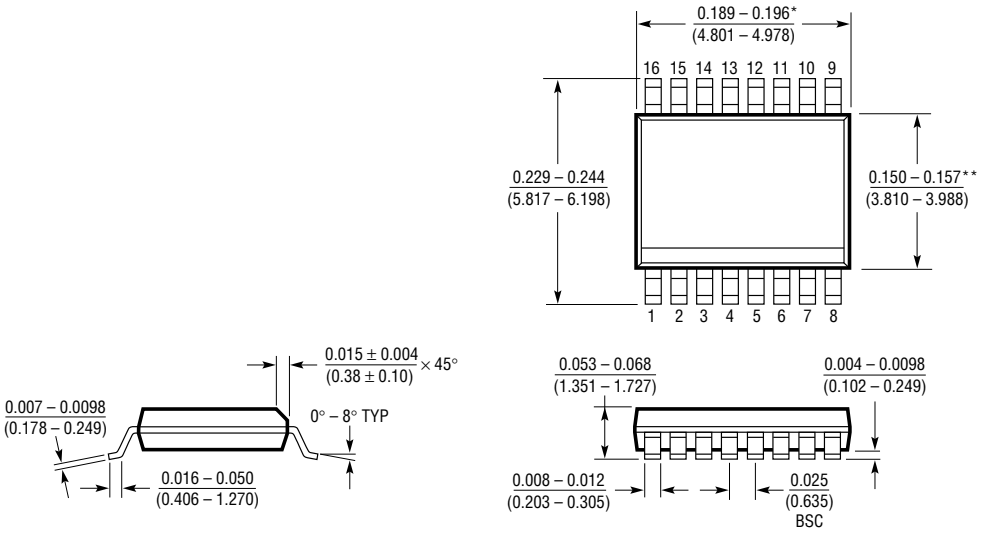
Programmable Gain Amplifier



PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

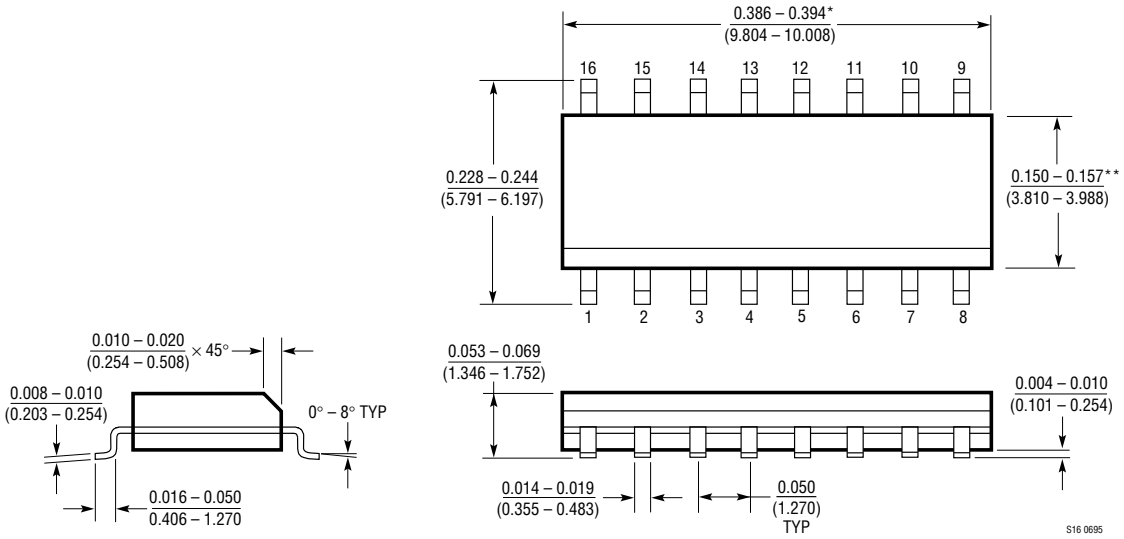
GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)



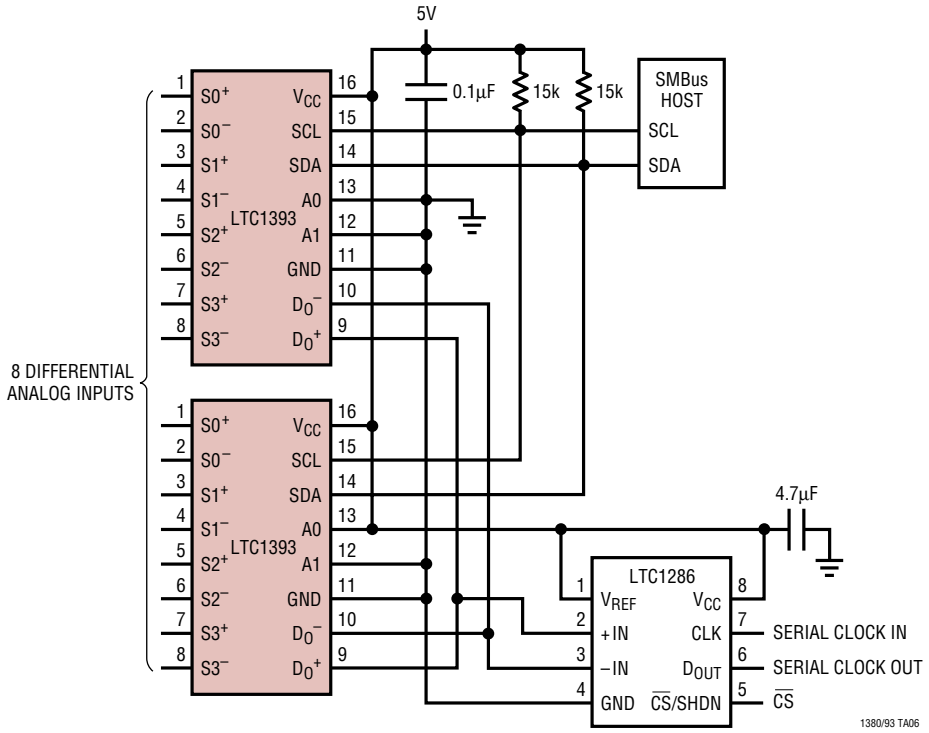
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

8 Differential Channel Multiplexer with A/D Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC201A/LTC202/ LTC203	Micropower, Low Charge Injection, Quad CMOS Analog Switches with Data Latches	Each Channel is Independently Controlled
LTC221/LTC222	Micropower, Low Charge Injection, Quad CMOS Analog Switches	Parallel Controlled with Data Latches
LTC1390/LTC1391	8-Channel, Analog Multiplexer with Serial Interface	3V to ±5V in 16-Pin SO and PDIP
LTC1623	High Side Switch with SMBus Interface	Regulated On-Board Charge Pump Drives External N-Channel MOSFETS

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