2.5 V to 5.5 V, 500 µA, 2-Wire Interface Quad Voltage Output, 8-/10-/12-Bit DACs

AD5305/AD5315/AD5325

FEATURES

AD5305: 4 buffered 8-bit DACs in 10-lead MSOP
A version: ±1 LSB INL, B version: ±0.625 LSB INL
AD5315: 4 buffered 10-bit DACs in 10-lead MSOP
A version: ±4 LSB INL, B version: ±2.5 LSB INL
AD5325: 4 buffered 12-bit DACs in 10-lead MSOP
A version: ±16 LSB INL, B version: ±10 LSB INL
Low power operation: 500 µA @ 3 V, 600 µA @ 5 V
2-wire (I^2C®-compatible) serial interface
2.5 V to 5.5 V power supply
Guaranteed monotonic by design over all codes
Power-down to 80 nA @ 3 V, 200 nA @ 5 V
Three power-down modes
Double-buffered input logic
Output range: 0 V to V_{REF}
Power-on reset to 0 V
Simultaneous update of outputs ($\overline{LDAC}$ function)
Software clear facility
Data readback facility
On-chip rail-to-rail output buffer amplifiers
Temperature range: –40°C to +105°C

APPLICATIONS

Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Programmable attenuators
Industrial process control

GENERAL DESCRIPTION

The AD5305/AD5315/AD5325[1] are quad 8-, 10-, and 12-bit buffered voltage output DACs in a 10-lead MSOP that operate from a single 2.5 V to 5.5 V supply, consuming 500 µA at 3 V. Their on-chip output amplifiers allow rail-to-rail output swing with a slew rate of 0.7 V/µs. A 2-wire serial interface that operates at clock rates up to 400 kHz is used. This interface is SMBus compatible at V_{DD} < 3.6 V. Multiple devices can be placed on the same bus.

The references for the four DACs are derived from one reference pin. The outputs of all DACs can be updated simultaneously using the software LDAC function.

The parts incorporate a power-on reset circuit, which ensures that the DAC outputs power up to 0 V and remain there until a valid write takes place to the device. There is also a software clear function to reset all input and DAC registers to 0 V. The parts contain a power-down feature that reduces the current consumption of the devices to 200 nA @ 5 V (80 nA @ 3 V).

The low power consumption of these parts in normal operation makes them ideally suited for portable battery-operated equipment. The power consumption is 3 mW at 5 V, 1.5 mW at 3 V, reducing to 1 µW in power-down mode.

[1] Protected by U.S. Patent No. 5,969,657 and 5,684,481.

FUNCTIONAL BLOCK DIAGRAM

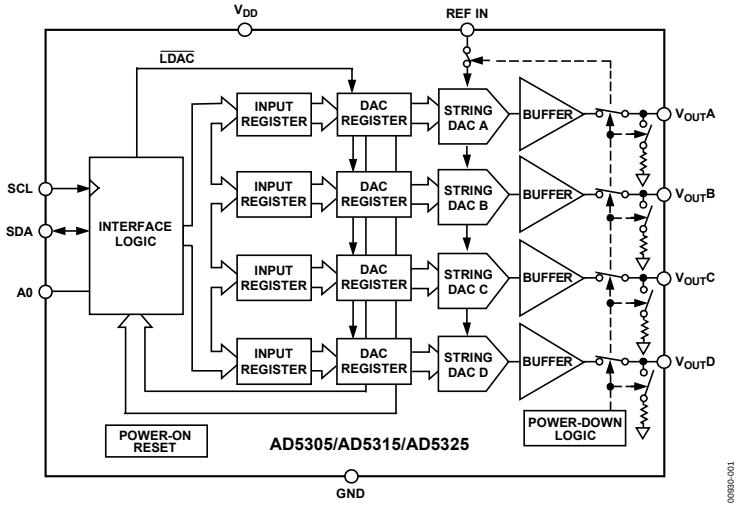

Figure 1.

Rev. G

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SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V, V_{REF} = 2 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Version[1]			B Version[1]				
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
DC PERFORMANCE[3, 4]								
AD5305								
Resolution		8			8		Bits	
Relative Accuracy		±0.15	±1		±0.15	±0.625	LSB	
Differential Nonlinearity		±0.02	±0.25		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes
AD5315								
Resolution		10			10		Bits	
Relative Accuracy		±0.5	±4		±0.5	±2.5	LSB	
Differential Nonlinearity		±0.05	±0.5		±0.05	±0.5	LSB	Guaranteed monotonic by design over all codes
AD5325								
Resolution		12			12		Bits	
Relative Accuracy		±2	±16		±2	±10	LSB	
Differential Nonlinearity		±0.2	±1		±0.2	±1	LSB	Guaranteed monotonic by design over all codes
Offset Error		±0.4	±3		±0.4	±3	% of FSR	
Gain Error		±0.15	±1		±0.15	±1	% of FSR	
Lower Deadband		20	60		20	60	mV	Lower deadband exists only if offset error is negative
Offset Error Drift[5]		−12			−12		ppm of FSR/°C	
Gain Error Drift[5]		−5			−5		ppm of FSR/°C	
Power Supply Rejection Ratio[5]		−60			−60		dB	ΔV_{DD} = ±10%
DC Crosstalk[5]		200			200		μV	R_L = 2 kΩ to GND or V_{DD}
DAC REFERENCE INPUTS[5]								
V_{REF} Input Range	0.25		V_{DD}	0.25		V_{DD}	V	
V_{REF} Input Impedance	37	45		37	45		kΩ	Normal operation
		>10			>10		MΩ	Power-down mode
Reference Feedthrough		−90			−90		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[5]								
Minimum Output Voltage[6]		0.001			0.001		V	A measure of the minimum and maximum drive capability of the output amplifier
Maximum Output Voltage[6]		V_{DD} − 0.001			V_{DD} − 0.001		V	
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		25			25		mA	V_{DD} = 5 V
		16			16		mA	V_{DD} = 3 V
Power-Up Time		2.5			2.5		μs	Coming out of power-down mode V_{DD} = 5 V
		5			5		μs	Coming out of power-down mode V_{DD} = 3 V

Parameter[2]	A Version[1] Min	Typ	Max	B Version[1] Min	Typ	Max	Unit	Conditions/Comments
LOGIC INPUTS (A0)[5]								
Input Current			±1			±1	μA	
Input Low Voltage, V_{IL}			0.8			0.8	V	V_{DD} = 5 V ± 10%
			0.6			0.6	V	V_{DD} = 3 V ± 10%
			0.5			0.5	V	V_{DD} = 2.5 V
Input High Voltage, V_{IH}	2.4			2.4			V	V_{DD} = 5 V ± 10%
	2.1			2.1			V	V_{DD} = 3 V ± 10%
	2.0			2.0			V	V_{DD} = 2.5 V
Pin Capacitance		3			3		pF	
LOGIC INPUTS (SCL, SDA)[5]								
Input High Voltage, V_{IH}	0.7 V_{DD}		V_{DD} + 0.3	0.7 V_{DD}		V_{DD} + 0.3	V	SMBus compatible at V_{DD} < 3.6 V
Input Low Voltage, V_{IL}	−0.3		0.3 V_{DD}	−0.3		0.3 V_{DD}	V	SMBus compatible at V_{DD} < 3.6 V
Input Leakage Current, I_{IN}			±1			±1	μA	
Input Hysteresis, V_{HYST}	0.05 V_{DD}			0.05 V_{DD}			V	
Input Capacitance, C_{IN}		8			8		pF	
Glitch Rejection			50			50	ns	Input filtering suppresses noise spikes of less than 50 ns
LOGIC OUTPUT (SDA)[5]								
Output Low Voltage, V_{OL}			0.4			0.4	V	I_{SINK} = 3 mA
			0.6			0.6	V	I_{SINK} = 6 mA
Three-State Leakage Current			±1			±1	μA	
Three-State Output Capacitance		8			8		pF	
POWER REQUIREMENTS								
V_{DD}	2.5		5.5	2.5		5.5	V	
I_{DD} (Normal Mode)[7]								V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		600	900		600	900	μA	
V_{DD} = 2.5 V to 3.6 V		500	700		500	700	μA	
I_{DD} (Power-Down Mode)								V_{IH} = V_{DD} and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.2	1		0.2	1	μA	I_{DD} = 4 μA (maximum) during 0 readback on SDA
V_{DD} = 2.5 V to 3.6 V		0.08	1		0.08	1	μA	I_{DD} = 1.5 μA (maximum) during 0 readback on SDA

[1] Temperature range (A, B version): −40°C to +105°C; typical at +25°C.
[2] See the Terminology section.
[3] DC specifications tested with the outputs unloaded.
[4] Linearity is tested using a reduced code range: AD5305 (Code 8 to 248); AD5315 (Code 28 to 995); AD5325 (Code 115 to 3981).
[5] Guaranteed by design and characterization, not production tested.
[6] For the amplifier output to reach its minimum voltage, offset error must be negative; to reach its maximum voltage, V_{REF} = V_{DD} and offset plus gain error must be positive.
[7] I_{DD} specification is valid for all DAC codes. Interface inactive. All DACs active and excluding load currents.

AC CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter[2, 3]	A, B Version[1] Min	Typ	Max	Unit	Conditions/Comments
Output Voltage Settling Time					$V_{REF} = V_{DD}$ = 5 V
AD5305		6	8	µs	¼ scale to ¾ scale change (0×40 to 0×C0)
AD5315		7	9	µs	¼ scale to ¾ scale change (0×100 to 0×300)
AD5325		8	10	µs	¼ scale to ¾ scale change (0×400 to 0×C00)
Slew Rate		0.7		V/µs	
Major-Code Transition Glitch Energy		12		nV-s	1 LSB change around major carry
Digital Feedthrough		1		nV-s	
Digital Crosstalk		1		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz

[1] Temperature range (A, B version): −40°C to +105°C; typical at +25°C.
[2] Guaranteed by design and characterization, not production tested.
[3] See the Terminology section.

TIMING CHARACTERISTICS

V_{DD} = 2.5 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (A, B Version)	Unit	Conditions/Comments
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data setup time
t_6[3]	0.9	µs max	$t_{HD,DAT}$, data hold time
	0	µs min	$t_{HD,DAT}$, data hold time
t_7	0.6	µs min	$t_{SU,STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU,STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus-free time between a stop and a start condition
t_{10}	300	ns max	t_R, rise time of SCL and SDA when receiving
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS compatible)
t_{11}	250	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	20 + 0.1 C_B[4]	ns min	t_F, fall time of SCL and SDA when transmitting
C_B[4]	400	pF max	Capacitive load for each bus line

[1] See Figure 2.
[2] Guaranteed by design and characterization; not production tested.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[4] C_B is the total capacitance of one bus line in pF. t_R and t_F measured between 0.3 V_{DD} and 0.7 V_{DD}.

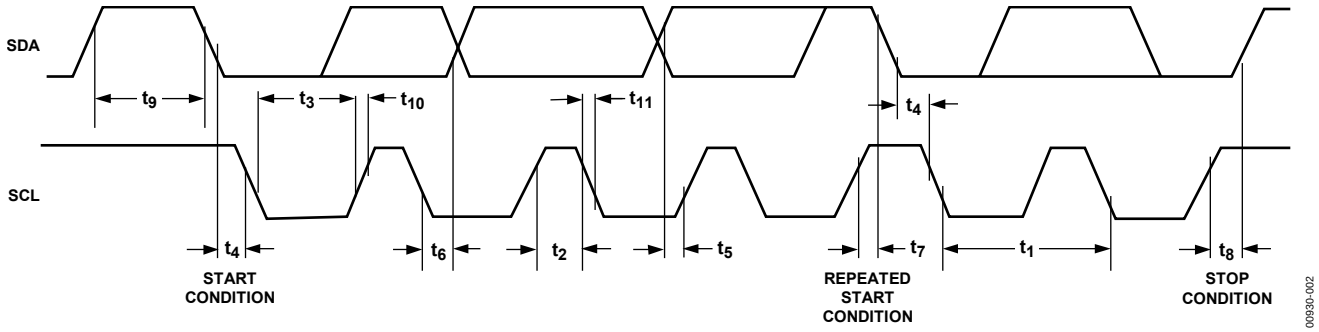


Figure 2. 2-Wire Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter[1]	Rating
V_{DD} to GND	−0.3 V to +7 V
SCL, SDA to GND	−0.3 V to V_{DD} + 0.3 V
A0 to GND	−0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT}A to V_{OUT}D to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (A, B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
MSOP	
Power Dissipation	(T_J max − T_A)/θ_{JA}
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
Reflow Soldering	
Peak Temperature	220°C
Time at Peak Temperature	10 sec to 40 sec

[1] Transient currents of up to 100 mA do not cause SCR latcth-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

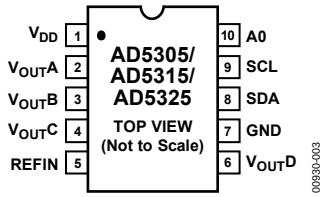


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Power Supply Input. These parts can be operated from 2.5 V to 5.5 V and the supply should be decoupled to GND.
2	$V_{OUT}A$	Buffered Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	$V_{OUT}B$	Buffered Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
4	$V_{OUT}C$	Buffered Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
5	REFIN	Reference Input Pin for All Four DACs. It has an input range from 0.25 V to V_{DD}.
6	$V_{OUT}D$	Buffered Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
7	GND	Ground Reference Point for All Circuitry on the Part.
8	SDA	Serial Data Line. This is used in conjunction with the SCL line to clock data into or out of the 16-bit input shift register. It is a bidirectional open-drain data line that should be pulled to the supply with an external pull-up resistor.
9	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 16-bit input shift register. Clock rates of up to 400 kb/s can be accommodated in the 2-wire interface.
10	A0	Address Input. Sets the least significant bit of the 7-bit slave address.

TYPICAL PERFORMANCE CHARACTERISTICS

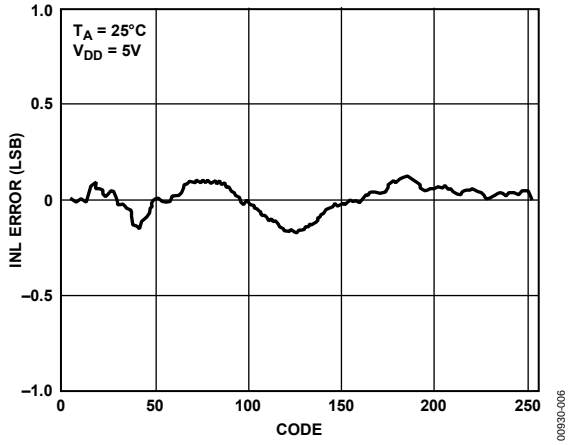


Figure 4. AD5305 Typical INL Plot

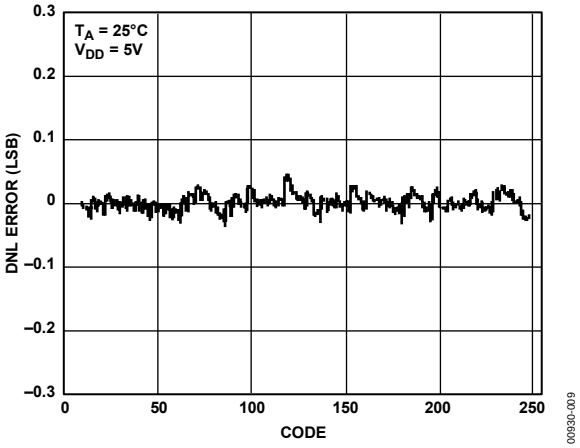


Figure 7. AD5305 Typical DNL Plot

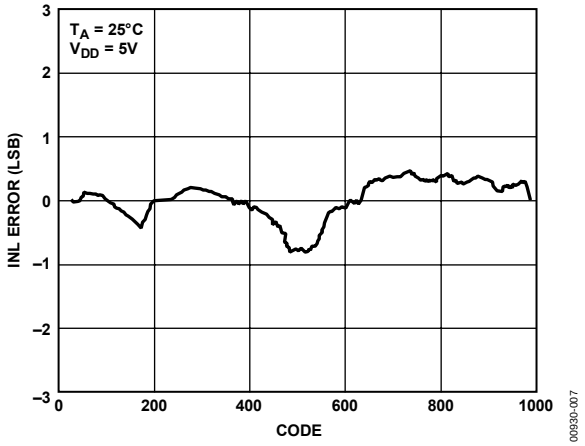


Figure 5. AD5315 Typical INL Plot

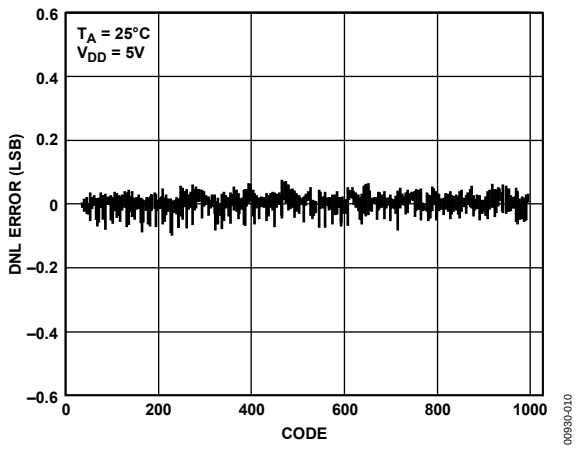


Figure 8. AD5315 Typical DNL Plot

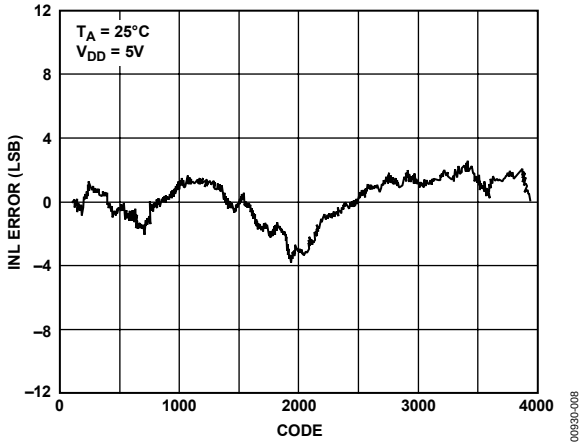


Figure 6. AD5325 Typical INL Plot

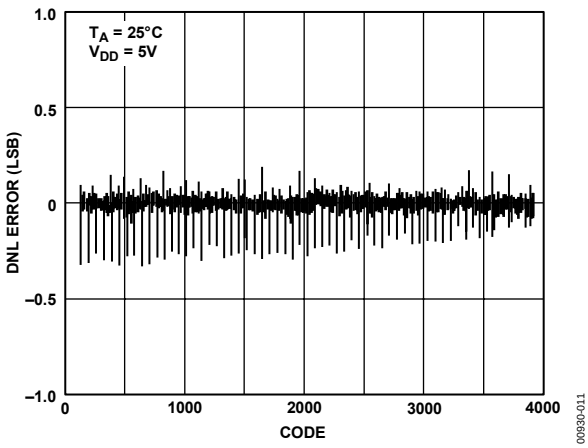


Figure 9. AD5325 Typical DNL Plot

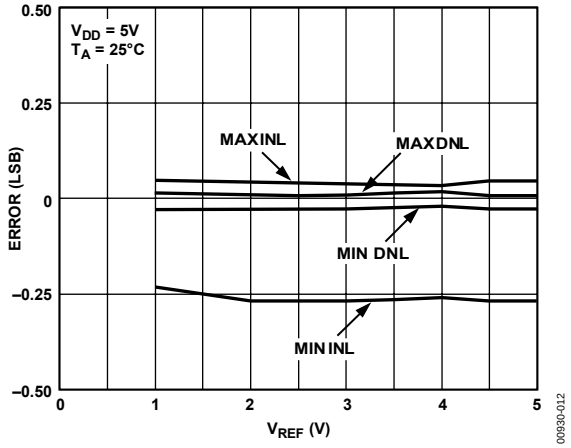


Figure 10. AD5305 INL and DNL Error vs. V_{REF}

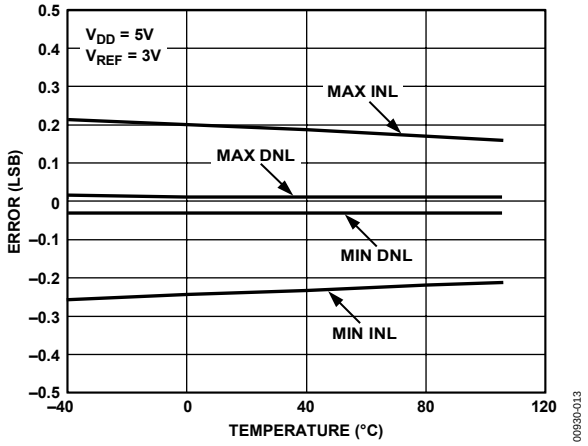


Figure 11. AD5305 INL and DNL Error vs. Temperature

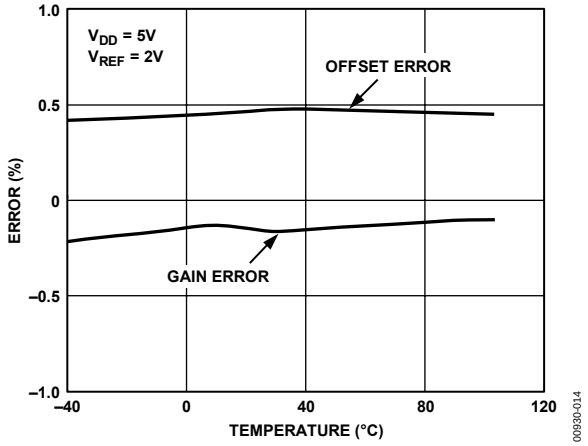


Figure 12. AD5305 Offset Error and Gain Error vs. Temperature

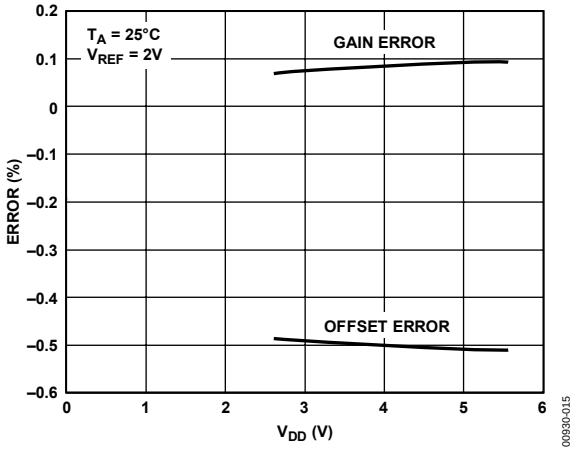


Figure 13. Offset Error and Gain Error vs. V_{DD}

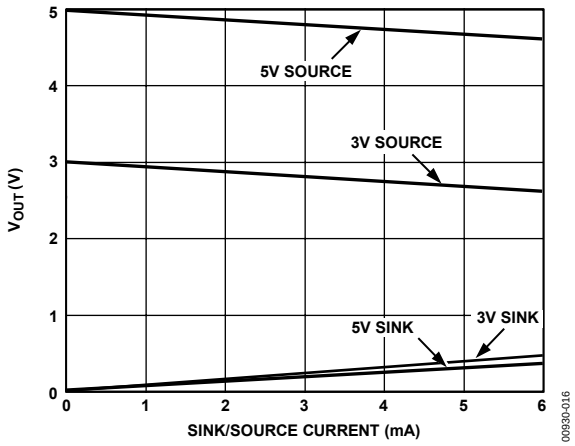


Figure 14. V_{OUT} Source and Sink Current Capability

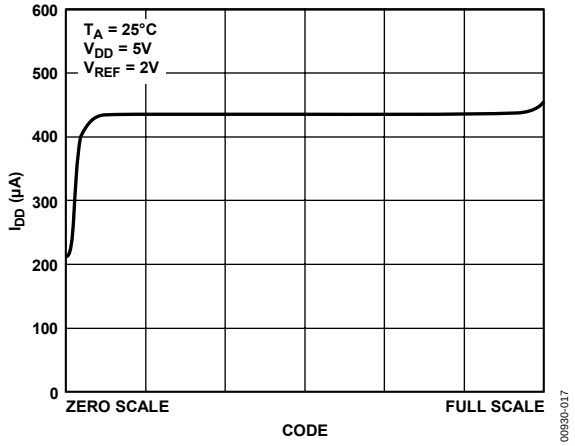


Figure 15. Supply Current vs. DAC Code

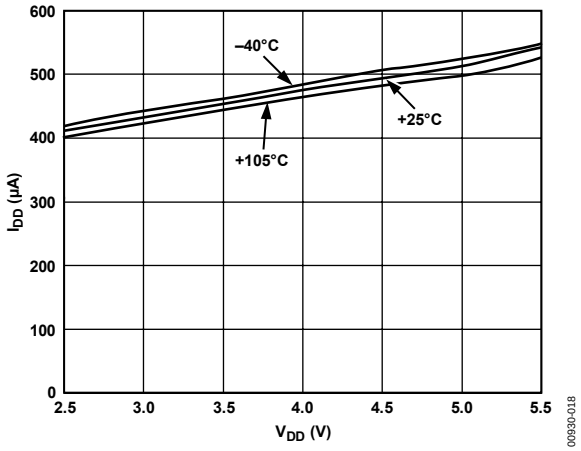


Figure 16. Supply Current vs. Supply Voltage

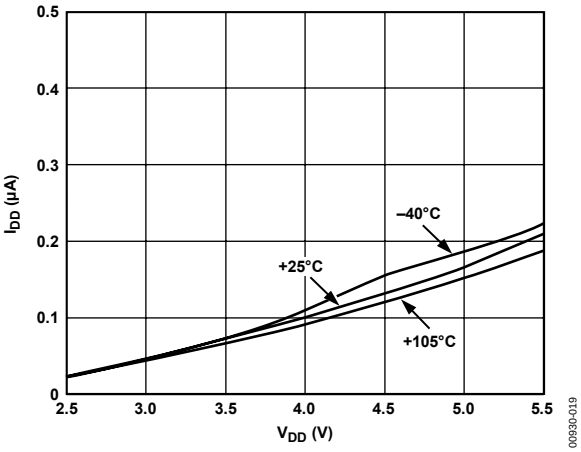


Figure 17. Power-Down Current vs. Supply Voltage

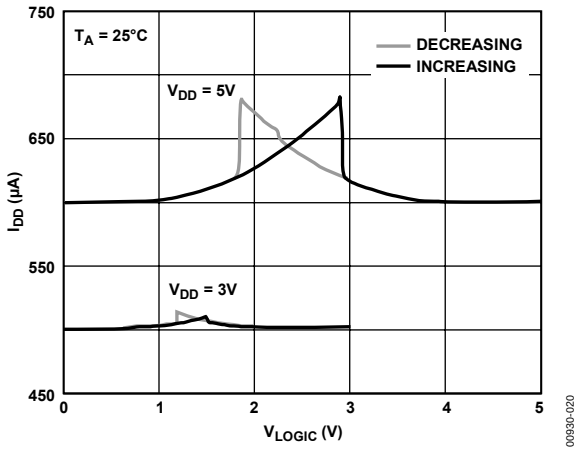


Figure 18. Supply Current vs. Logic Input Voltage for SDA and SCL Voltage Increasing and Decreasing

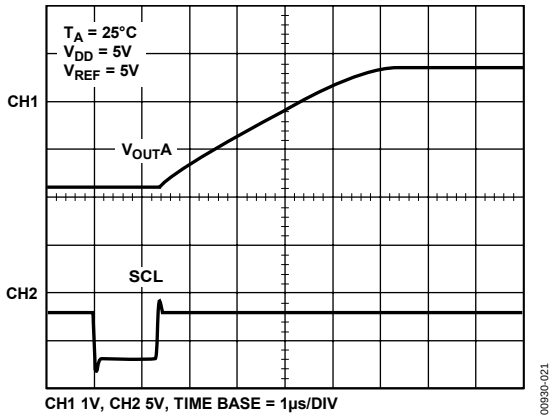


Figure 19. Half-Scale Settling (1/4 to 3/4 Scale Code Change)

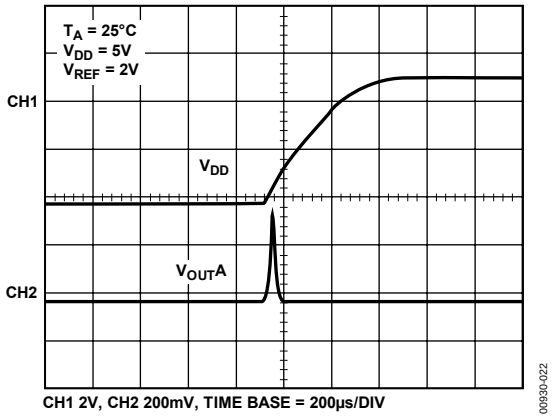


Figure 20. Power-On Reset to 0 V

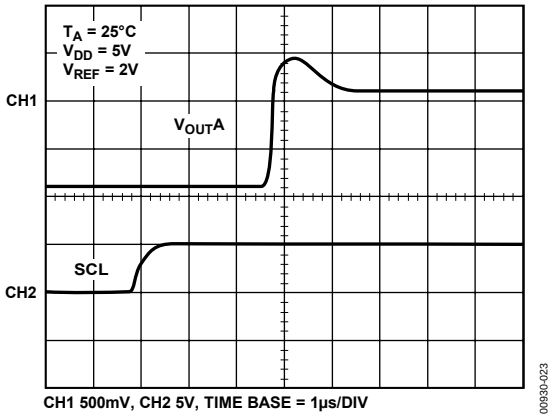


Figure 21. Exiting Power-Down to Midscale

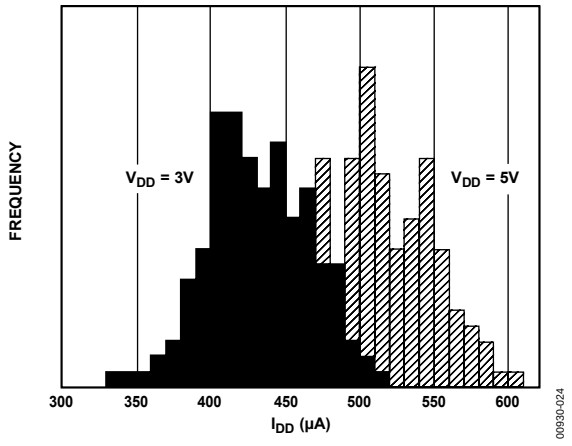


Figure 22. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

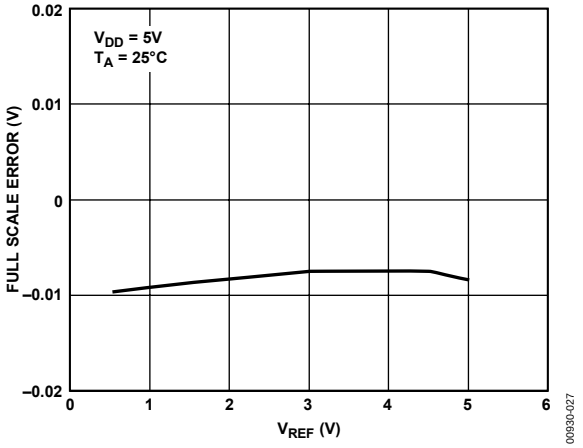


Figure 25. Full-Scale Error vs. V_{REF}

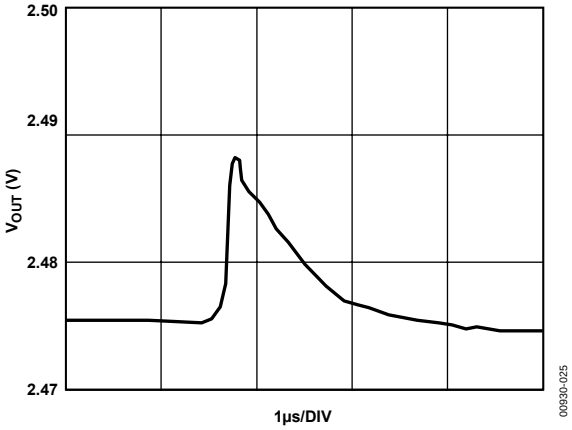


Figure 23. AD5325 Major-Code Transition Glitch Energy

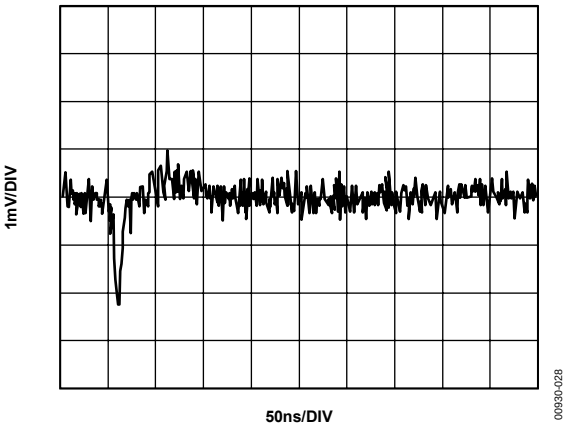


Figure 26. DAC-to-DAC Crosstalk

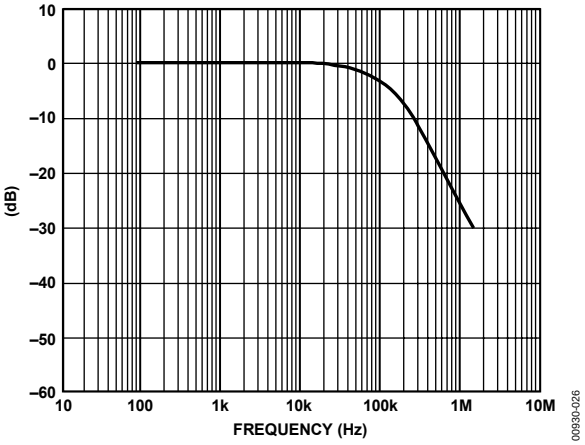


Figure 24. Multiplying Bandwidth (Small-Signal Frequency Response)

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function. Typical INL versus code plots can be seen in Figure 4, Figure 5, and Figure 6.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL vs. code plots can be seen in Figure 7, Figure 8, and Figure 9.

Offset Error
This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the actual DAC transfer characteristic from the ideal expressed as a percentage of the full-scale range.

Offset Error Drift
This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Power Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC Crosstalk
This is the dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in μV.

Reference Feedthrough
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated. It is expressed in dB.

Major-Code Transition Glitch Energy
Major-code transition glitch energy is the energy of the impulse injected into the analog output when the code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00, or 100 . . . 00 to 011 . . . 11).

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device when the DAC output is not being updated. It is specified in nV-s and is measured with a worst-case change on the digital input pins, for example, from all 0s to all 1s or vice versa.

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is expressed in nV-s.

DAC-to-DAC Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with the $\overline{\text{LDAC}}$ bit set low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC and the THD is a measure of the harmonics present on the DAC output. It is measured in dB.

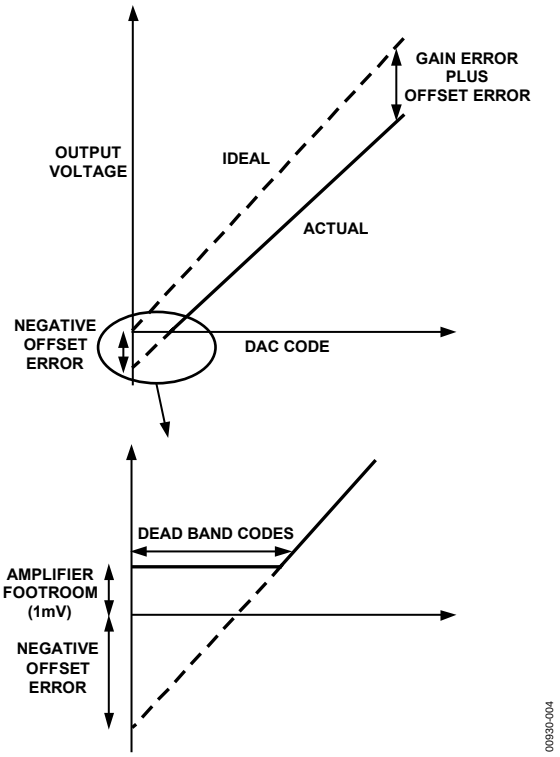


Figure 27. Transfer Function with Negative Offset

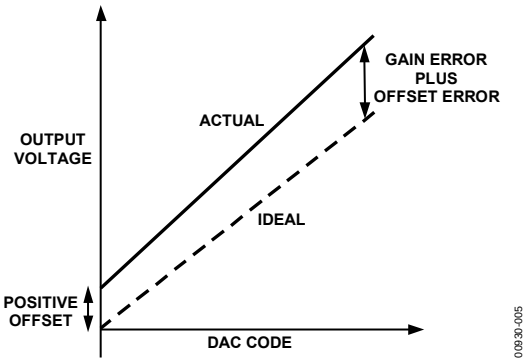


Figure 28. Transfer Function with Positive Offset

FUNCTIONAL DESCRIPTION

The AD5305/AD5315/AD5325 are quad resistor-string DACs fabricated on a CMOS process with resolutions of 8, 10, and 12 bits, respectively. Each contains four output buffer amplifiers and is written to via a 2-wire serial interface. They operate from single supplies of 2.5 V to 5.5 V, and the output buffer amplifiers provide rail-to-rail output swing with a slew rate of 0.7 V/µs. The four DACs share a single reference input pin. The devices have three programmable power-down modes, in which all DACs can be turned off completely with a high impedance output, or the outputs can be pulled low by on-chip resistors.

DIGITAL-TO-ANALOG SECTION

The architecture of one DAC channel consists of a resistor-string DAC followed by an output buffer amplifier. The voltage at the REFIN pin provides the reference voltage for the DAC. Figure 29 shows a block diagram of the DAC architecture. Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

where:

D = decimal equivalent of the binary code, which is loaded to the DAC register:

0 to 255 for AD5305 (8 bits)

0 to 1023 for AD5315 (10 bits)

0 to 4095 for AD5325 (12 bits)

N = DAC resolution

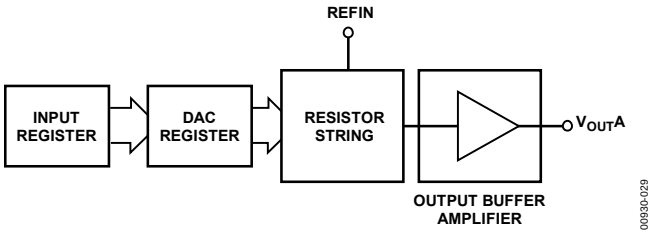


Figure 29. DAC Channel Architecture

RESISTOR STRING

The resistor string section is shown in Figure 30. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

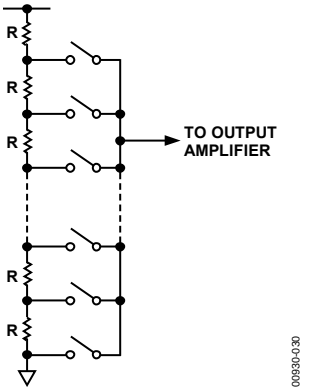


Figure 30. Resistor String

DAC REFERENCE INPUTS

There is a single reference input pin for the four DACs. The reference input is unbuffered. The user can have a reference voltage as low as 0.25 V and as high as V_{DD} because there is no restriction due to headroom and footroom of any reference amplifier.

It is recommended to use a buffered reference in the external circuit (for example, REF192). The input impedance is typically 45 kΩ.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD} when the reference is V_{DD}. It is capable of driving a load of 2 kΩ to GND or V_{DD}, in parallel with 500 pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in the plot in Figure 14.

The slew rate is 0.7 V/µs with a half-scale settling time to ±0.5 LSB (at eight bits) of 6 µs.

POWER-ON RESET

The AD5305/AD5315/AD5325 are provided with a power-on reset function, so that they power up in a defined state. The power-on state is

- Normal operation
- Output voltage set to 0 V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

SERIAL INTERFACE

The AD5305/AD5315/AD5325 are controlled via an I²C compatible serial bus. The DACs are connected to this bus as slave devices (that is, no clock is generated by the AD5305/AD5315/AD5325 DACs). This interface is SMBus compatible at V_{DD} < 3.6 V.

The AD5305/AD5315/AD5325 have a 7-bit slave address. The 6 MSB are 000110 and the LSB is determined by the state of the A0 pin. The facility to make hardwired changes to A0 allows the user to use up to two of these devices on one bus. The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address followed by an R/$\overline{W}$ bit (this bit determines whether data is read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.

2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.

3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. In read mode, the master issues a No Acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master then brings the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a stop condition.

READ/WRITE SEQUENCE

In the case of the AD5305/AD5315/AD5325, all write access sequences and most read sequences begin with the device address (with R/$\overline{W}$ = 0) followed by the pointer byte. This pointer byte specifies the data format and determines which DAC is being accessed in the subsequent read/write operation (see Figure 31). In a write operation, the data follows immediately. In a read operation, the address is resent with R/$\overline{W}$ = 1 and then the data is read back. However, it is also possible to perform a read operation by sending only the address with R/$\overline{W}$ = 1. The previously loaded pointer settings are then used for the readback operation. See Figure 32 for a graphical explanation of the interface.

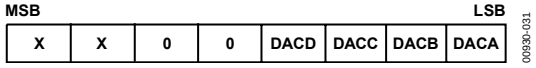


Figure 31. Pointer Byte

POINTER BYTE BITS

Table 6 explains the individual bits that make up the pointer byte.

Table 6. Individual Bits of the Pointer Byte

Bit	Description
X	Don't care bits.
0	Reserved bits. Must be set to 0.
DACD	[1] The following data bytes are for DAC D.
DACC	[1] The following data bytes are for DAC C.
DACB	[1] The following data bytes are for DAC B.
DACA	[1] The following data bytes are for DAC A.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide. Data is loaded into the device as two data bytes on the serial data line, SDA, under the control of the serial clock input, SCL. The timing diagram for this operation is shown in Figure 2. The two data bytes consist of four control bits followed by 8, 10, or 12 bits of DAC data, depending on the device type. The first two bits loaded are the PD1 and PD0 bits that control the mode of operation of the device. See the Power-Down Modes section for a complete description. Bit 13 is $\overline{CLR}$, Bit 12 is $\overline{LDAC}$, and the remaining bits are left justified DAC data bits, starting with the MSB. See Figure 32.

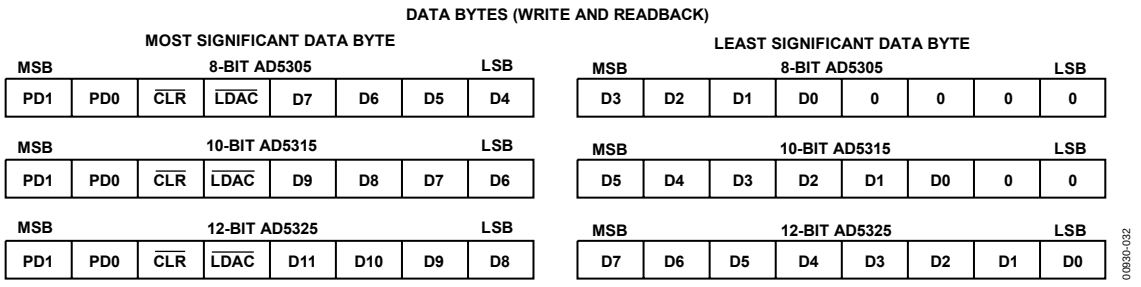


Figure 32. Data Formats for Write and Readback

Table 7. $\overline{\text{CLR}}$ and $\overline{\text{LDAC}}$ Bit Descriptions

Bit	Description
$\overline{\text{CLR}}$	[0] All DAC registers and input registers are filled with 0s on completion of the write sequence. [1] Normal operation.
$\overline{\text{LDAC}}$	[0] All four DAC registers and, therefore, all DAC outputs, are simultaneously updated on completion of the write sequence. [1] Only addressed input register is updated. There is no change in the contents of the DAC registers.

DEFAULT READBACK CONDITION

All pointer byte bits power up to 0. Therefore, if the user initiates a readback without writing to the pointer byte first, no single DAC channel has been specified. In this case, the default readback bits are all 0, except for the $\overline{\text{CLR}}$ bit, which is a 1.

MULTIPLE-DAC WRITE SEQUENCE

Because there are individual bits in the pointer byte for each DAC, it is possible to simultaneously write the same data and control bits to 2, 3, or 4 DACs by setting the relevant bits to 1.

MULTIPLE-DAC READBACK SEQUENCE

If the user attempts to read back data from more than one DAC at a time, the part reads back the default, power-on reset conditions, that is, all 0s except for $\overline{\text{CLR}}$, which is 1.

WRITE OPERATION

When writing to the AD5305/AD5315/AD5325 DACs, the user must begin with an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. This address byte is followed by the pointer byte, which is also acknowledged by the DAC. Two bytes of data are then written to the DAC, as shown in Figure 33. A stop condition follows.

READ OPERATION

When reading data back from the AD5305/AD5315/AD5325 DACs, the user begins with an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. This address byte is usually followed by the pointer byte, which is also acknowledged by the DAC. Following this, there is a repeated start condition by the master and the address is resent with R/$\overline{\text{W}}$ = 1. This is acknowledged by the DAC indicating that it is prepared to transmit data. Two bytes of data are then read from the DAC, as shown in Figure 34. A stop condition follows.

However, if the master sends an ACK and continues clocking SCL (no STOP is sent), the DAC retransmits the same two bytes of data on SDA. This allows continuous readback of data from the selected DAC register.

Alternatively, the user can send a start followed by the address with R/$\overline{\text{W}}$ = 1. In this case, the previously loaded pointer settings are used and readback of data can commence immediately.

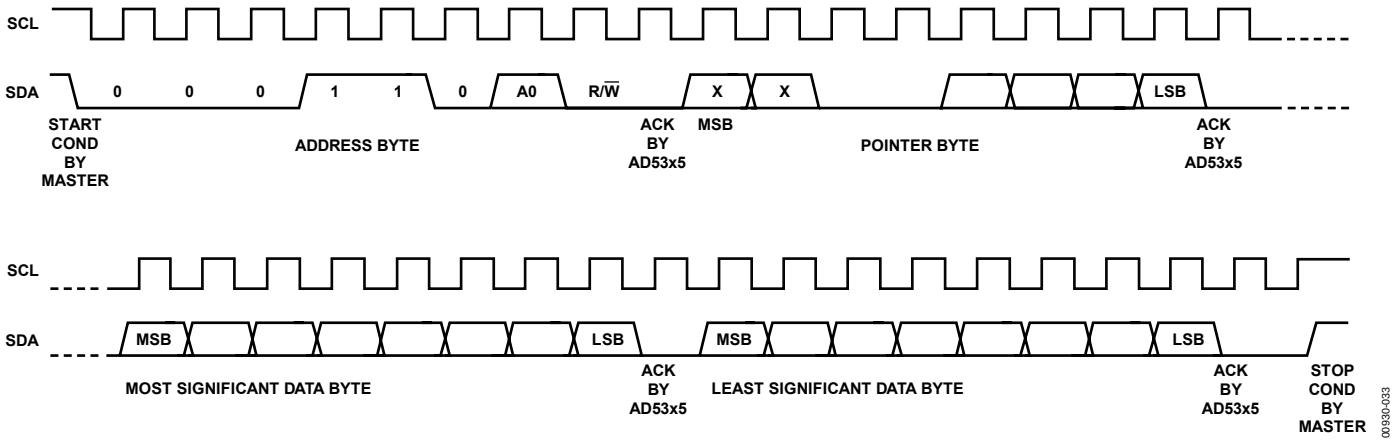
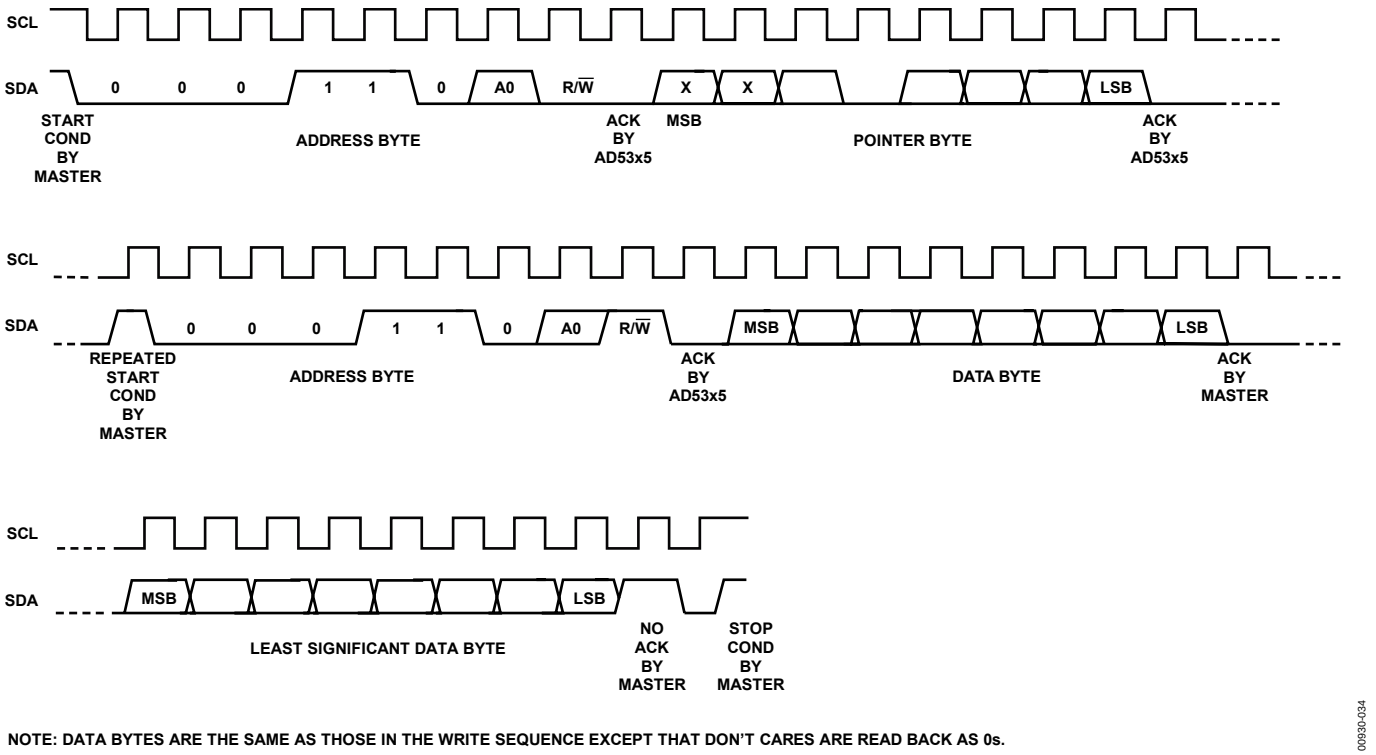


Figure 33. Write Sequence



NOTE: DATA BYTES ARE THE SAME AS THOSE IN THE WRITE SEQUENCE EXCEPT THAT DON'T CARES ARE READ BACK AS 0s.

Figure 34. Readback Sequence

DOUBLE-BUFFERED INTERFACE

The AD5305/AD5315/AD5325 DACs have double-buffered interfaces consisting of two banks of registers—input registers and DAC registers. The input register is directly connected to the input shift register and the digital code is transferred to the relevant input register on completion of a valid write sequence. The DAC register contains the digital code used by the resistor string.

Access to the DAC register is controlled by the $\overline{\text{LDAC}}$ bit. When the $\overline{\text{LDAC}}$ bit is set high, the DAC register is latched and, therefore, the input register can change state without affecting the contents of the DAC register. However, when the $\overline{\text{LDAC}}$ bit is set low, the DAC register becomes transparent and the contents of the input register are transferred to it.

This is useful if the user requires simultaneous updating of all DAC outputs. The user can write to three of the input registers individually and then, by setting the $\overline{\text{LDAC}}$ bit low when writing to the remaining DAC input register, all outputs update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5305/AD5315/AD5325, the part updates the DAC register only if the input register has been changed since the last time the DAC register was updated, thereby removing unnecessary digital crosstalk.

POWER-DOWN MODES

The AD5305/AD5315/AD5325 have very low power consumption, dissipating typically 1.5 mW with a 3 V supply and 3 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into one of three power-down modes, which are selected by Bit 15 and Bit 14 (PD1 and PD0) of the data byte. Table 8 shows how the state of the bits corresponds to the mode of operation of the DAC.

Table 8. PD1/PD0 Operating Modes

PD1	PD0	Operating Mode
0	0	Normal Operation
0	1	Power-Down (1 kΩ load to GND)
1	0	Power-Down (100 kΩ load to GND)
1	1	Power-Down (three-state output)

When both bits are set to 0, the DAC works normally with its normal power consumption of 600 μA at 5 V. However, for the three power-down modes, the supply current falls to 200 nA at 5 V (80 nA at 3 V). Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has an advantageous because the output impedance of the part is known while the part is in power-down mode and provides a defined input condition for whatever is connected to the output of the DAC amplifier. There are three different options. The output is connected internally to GND through a 1 kΩ resistor, a 100 kΩ resistor, or it is left open-circuited (three-state). Resistor tolerance = ±20%. The output stage is illustrated in Figure 35.

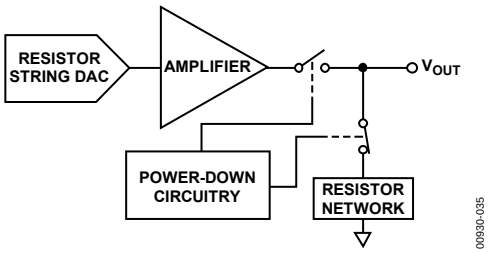


Figure 35. Output Stage During Power-Down

The bias generator, the output amplifiers, the resistor string, and all other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC registers are unchanged when in power-down. The time to exit power-down is typically 2.5 μs for V_{DD} = 5 V and 5 μs when V_{DD} = 3 V. This is the time from the rising edge of the eighth SCL pulse to when the output voltage deviates from its power-down voltage. See Figure 21 for a plot.

APPLICATIONS

TYPICAL APPLICATION CIRCUIT

The AD5305/AD5315/AD5325 can be used with a wide range of reference voltages where the devices offer full, one-quadrant multiplying capability over a reference range of 0 V to V_{DD}. More typically, these devices are used with a fixed, precision reference voltage. Suitable references for 5 V operation are the AD780 and REF192 (2.5 V references). For 2.5 V operation, a suitable external reference is the AD589, a 1.23 V band gap reference. Figure 36 shows a typical setup for the AD5305/AD5315/AD5325 when using an external reference. Note that A0 can be high or low.

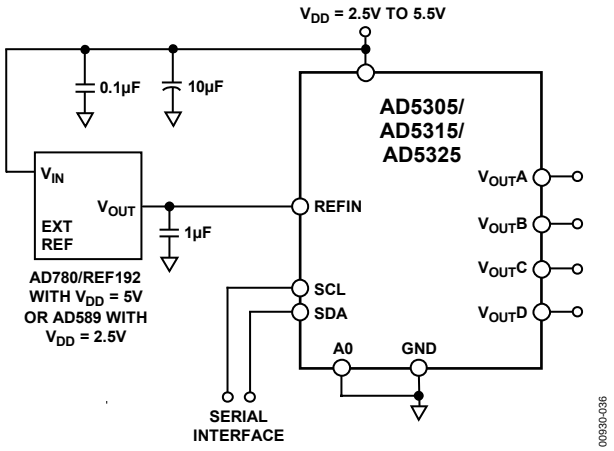


Figure 36. AD5305/AD5315/AD5325 Using External Reference

If an output range of 0 V to V_{DD} is required, the simplest solution is to connect the reference input to V_{DD}. As this supply may not be very accurate and may be noisy, the AD5305/AD5315/AD5325 can be powered from the reference voltage; for example, using a 5 V reference such as the REF195. The REF195 outputs a steady supply voltage for the AD5305/AD5315/AD5325. The typical current required from the REF195 is 600 µA supply current and approximately 112 µA into the reference input. This is with no load on the DAC outputs. When the DAC outputs are loaded, the REF195 also needs to supply the current to the loads. The total current required (with a 10 kΩ load on each output) is

712 µA + 4(5 V/10 kΩ) = 2.70 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in an error of 5.4 ppm (27 µV) for the 2.7 mA current drawn from it. This corresponds to a 0.0014 LSB error at eight bits and 0.022 LSB error at 12 bits.

BIPOLAR OPERATION

The AD5305/AD5315/AD5325 have been designed for single supply operation, but a bipolar output range is also possible using the circuit in Figure 37. This circuit gives an output voltage range of ± 5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

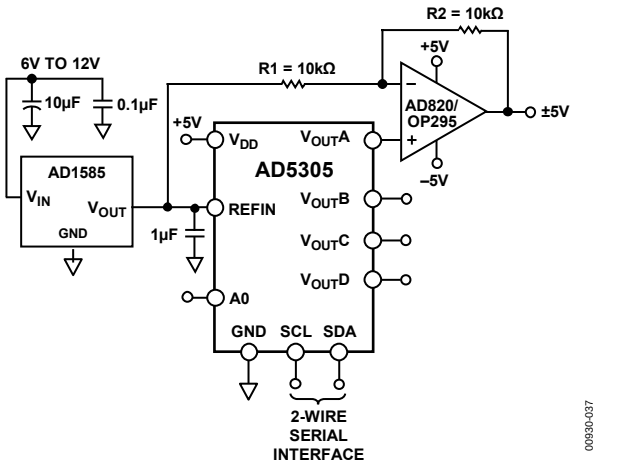


Figure 37. Bipolar Operation with the AD5305

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = \left[\frac{\left(REFIN \times \left(D/2^{N}\right)\right) \times (R1 + R2)}{R1} - REFIN \times (R2/R1)\right]$$

where:

D is the decimal equivalent of the code loaded to the DAC.
N is the DAC resolution.
REFIN is the reference voltage input.

with

REFIN = 5 V, *R1* = *R2* = 10 kΩ, V_{OUT} (10 × *D*/2^{N}) – 5 V

MULTIPLE DEVICES ON ONE BUS

Figure 38 shows two AD5305 devices on the same serial bus. Each has a different slave address because the state of the A0 pin is different. This allows each of eight DACs to be written to or read from independently.

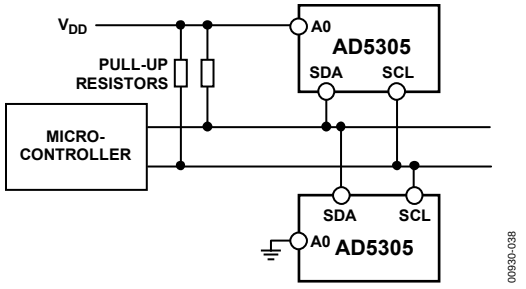


Figure 38. Multiple AD5305 Devices on One Bus

AD5305/AD5315/AD5325 AS A DIGITALLY PROGRAMMABLE WINDOW DETECTOR

A digitally programmable upper/lower limit detector using two of the DACs in the AD5305/AD5315/AD5325 is shown in Figure 39. The upper and lower limits for the test are loaded to DAC A and DAC B, which, in turn, set the limits on the CMP04. If the signal at the V_{IN} input is not within the programmed window, an LED indicates the fail condition. Similarly, DAC C and DAC D can be used for window detection on a second V_{IN} signal.

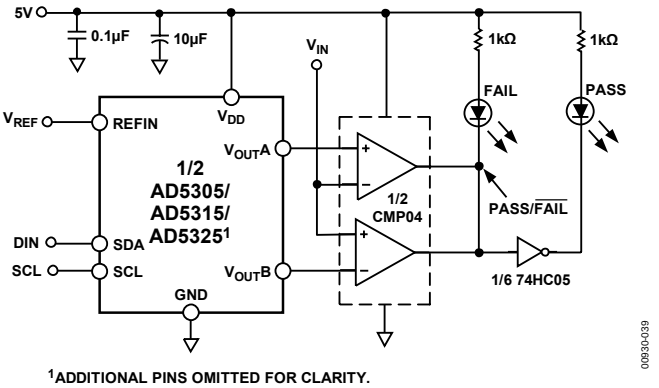


Figure 39. Window Detection

COARSE AND FINE ADJUSTMENT USING THE AD5305/AD5315/AD5325

Two of the DACs in the AD5305/AD5315/AD5325 can be paired together to form a coarse and fine adjustment function, as shown in Figure 40. DAC A is used to provide the coarse adjustment while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 changes the relative effect of the coarse and fine adjustments. With the resistor values and external reference shown in Figure 40, the output amplifier has unity gain for the DAC A output. As a result, the output range is 0 V to 2.5 V − 1 LSB. For DAC B, the amplifier has a gain of 7.6×10^{-3}, giving DAC B a range equal to 19 mV. Similarly, DAC C and DAC D can be paired together for coarse and fine adjustment.

The circuit is shown with a 2.5 V reference, but reference voltages up to V_{DD} can be used. The op amps indicated allows a rail-to-rail output swing.

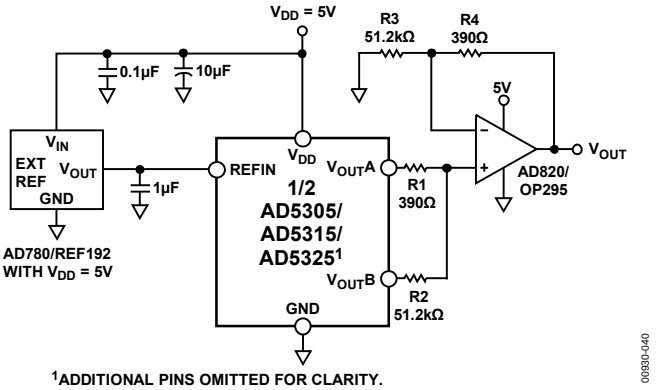


Figure 40. Coarse/Fine Adjustment

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5305/AD5315/AD5325 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5305/AD5315/AD5325 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device. The AD5305/AD5315/AD5325 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5305/AD5315/AD5325 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. A ground line routed between the SDA and SCL lines helps reduce crosstalk between them (not required on a multilayer board as there is a separate ground plane, but separating the lines does help).

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane while signal traces are placed on the solder side.

Table 9. Overview of All AD53xx Serial Devices

Part No.	Resolution	No. of DACs	DNL	Interface	Settling Time (µs)	Package	Pins
SINGLES							
AD5300	8	1	±0.25	SPI®	4	SOT-23, MSOP	6, 8
AD5310	10	1	±0.5	SPI	6	SOT-23, MSOP	6, 8
AD5320	12	1	±1.0	SPI	8	SOT-23, MSOP	6, 8
AD5301	8	1	±0.25	2-Wire	6	SOT-23, MSOP	6, 8
AD5311	10	1	±0.5	2-Wire	7	SOT-23, MSOP	6, 8
AD5321	12	1	±1.0	2-Wire	8	SOT-23, MSOP	6, 8
DUALS							
AD5302	8	2	±0.25	SPI	6	MSOP	8
AD5312	10	2	±0.5	SPI	7	MSOP	8
AD5322	12	2	±1.0	SPI	8	MSOP	8
AD5303	8	2	±0.25	SPI	6	TSSOP	16
AD5313	10	2	±0.5	SPI	7	TSSOP	16
AD5323	12	2	±1.0	SPI	8	TSSOP	16
QUADS							
AD5304	8	4	± 0.25	SPI	6	MSOP	10
AD5314	10	4	± 0.5	SPI	7	MSOP	10
AD5324	12	4	±1.0	SPI	8	MSOP	10
AD5305	8	4	±0.25	2-Wire	6	MSOP	10
AD5315	10	4	±0.5	2-Wire	7	MSOP	10
AD5325	12	4	±1.0	2-Wire	8	MSOP	10
AD5306	8	4	±0.25	2-Wire	6	TSSOP	16
AD5316	10	4	±0.5	2-Wire	7	TSSOP	16
AD5326	12	4	±1.0	2-Wire	8	TSSOP	16
AD5307	8	4	±0.25	SPI	6	TSSOP	16
AD5317	10	4	±0.5	SPI	7	TSSOP	16
AD5327	12	4	±1.0	SPI	8	TSSOP	16
OCTALS							
AD5308	8	8	±0.25	SPI	6	TSSOP	16
AD5318	10	8	±0.5	SPI	7	TSSOP	16
AD5328	12	8	±1.0	SPI	8	TSSOP	16

Table 10. Overview of AD53xx Parallel Devices

Part No.	Resolution	DNL	V_{REF} Pins	Settling Time (µs)	Additional Pin Functions				Package	Pins
SINGLES					**BUF**	**GAIN**	**HBEN**	**$\overline{CLR}$**		
AD5330	8	±0.25	1	6	✓	✓		✓	TSSOP	20
AD5331	10	±0.5	1	7		✓		✓	TSSOP	20
AD5340	12	±1.0	1	8	✓	✓		✓	TSSOP	24
AD5341	12	±1.0	1	8	✓	✓	✓	✓	TSSOP	20
DUALS										
AD5332	8	±0.25	2	6				✓	TSSOP	20
AD5333	10	±0.5	2	7	✓	✓		✓	TSSOP	24
AD5342	12	±1.0	2	8	✓	✓		✓	TSSOP	28
AD5343	12	±1.0	1	8			✓	✓	TSSOP	20
QUADS										
AD5334	8	±0.25	2	6		✓		✓	TSSOP	24
AD5335	10	±0.5	2	7			✓	✓	TSSOP	24
AD5336	10	±0.5	4	7		✓		✓	TSSOP	28
AD5344	12	±1.0	4	8					TSSOP	28

OUTLINE DIMENSIONS

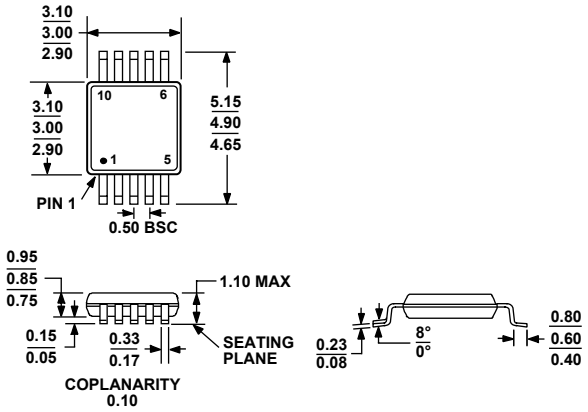


Figure 41. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD5305ARM	−40°C to +105°C	10-Lead MSOP	RM-10	DEA
AD5305ARM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	DEA
AD5305ARMZ[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D99
AD5305ARMZ-REEL7[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D99
AD5305BRM	−40°C to +105°C	10-Lead MSOP	RM-10	DEB
AD5305BRM-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	DEB
AD5305BRM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	DEB
AD5305BRMZ[1]	−40°C to +105°C	10-Lead MSOP	RM-10	DEB #
AD5305BRMZ-REEL7[1]	−40°C to +105°C	10-Lead MSOP	RM-10	DEB #
AD5315ARM	−40°C to +105°C	10-Lead MSOP	RM-10	DFA
AD5315ARM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	DFA
AD5315ARMZ[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D8E
AD5315BRM	−40°C to +105°C	10-Lead MSOP	RM-10	DFB
AD5315BRM-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	DFB
AD5315BRM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	DFB
AD5315BRMZ[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D6N
AD5315BRMZ-REEL[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D6N
AD5315BRMZ-REEL7[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D6N
AD5325ARM	−40°C to +105°C	10-Lead MSOP	RM-10	DGA
AD5325ARM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	DGA
AD5325ARMZ[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D8G
AD5325BRM	−40°C to +105°C	10-Lead MSOP	RM-10	DGB
AD5325BRM-REEL	−40°C to +105°C	10-Lead MSOP	RM-10	DGB
AD5325BRM-REEL7	−40°C to +105°C	10-Lead MSOP	RM-10	DGB
AD5325BRMZ[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D8H
AD5325BRMZ-REEL[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D8H
AD5325BRMZ-REEL7[1]	−40°C to +105°C	10-Lead MSOP	RM-10	D8H

[1] Z = Pb-free part; # denotes lead-free product may be top or bottom marked.

NOTES

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