

#### FEATURES

- 4 Matched NPN Transistors
  - 300 typical  $h_{fe}$  of 100
  - 300A minimum  $h_{fe}$  of 150
  - 300B minimum  $h_{fe}$  of 300
- 4 Matched PNP Transistors
  - 320 typical  $h_{fe}$  of 75
- 2 Matched PNP and 2 Matched NPN Transistors
  - 340 PNP typical  $h_{fe}$  of 75
  - 340 NPN typical  $h_{fe}$  of 100
- Low Voltage Noise
  - 0.75 nV/√Hz (PNP)
  - 0.8 nV/√Hz (NPN)
- High Speed
  - $f_T = 350$  MHz (NPN)
  - $f_T = 325$  MHz (PNP)
- 500  $\mu$ V matching between devices
- Dielectrically Isolated for low crosstalk and high DC isolation
- 36V  $V_{CEO}$

#### APPLICATIONS

- Low Noise Front Ends
- Microphone Preamplifiers
- Log/Antilog Amplifiers
- Current Sources
- Current Mirrors
- Multipliers

#### Description

The THAT 300, 320 and 340 are large geometry, 4-transistor, monolithic NPN and/or PNP arrays. They exhibit both high speed and low noise, with excellent parameter matching between transistors of the same gender. Typical base-spreading resistance is 25  $\Omega$  for the PNP devices (30  $\Omega$  for the low-gain NPNs), so their resulting voltage noise is under 1 nV/√Hz. This makes the 300 series ideally suited for low-noise amplifier input stages, log amplifiers, and many other applications. The four-NPN transistor array is available in versions selected for  $h_{fe}$  with minimums of 150 (300A) or 300 (300B).

Fabricated in a dielectrically isolated, complementary bipolar process, each transistor is electrically insulated from the others by a layer of insulating oxide (not the reverse-biased PN junctions

used in conventional arrays). As a result, they exhibit inter-device crosstalk and DC isolation similar to that of discrete transistors. The resulting low collector-to-substrate capacitance produces a typical NPN  $f_T$  of 350 MHz (325 MHz for the PNPs). Substrate biasing is not required for normal operation, though the substrate should be ac-grounded to optimize speed and minimize crosstalk.

An eight-transistor bare-die array with similar performance characteristics (the THAT 380G) is also available from THAT Corporation. Please contact us directly or through your local distributor for more information. Military-grade temperature range packages are available from TT Semiconductor (see [www.ttsemiconductor.com](http://www.ttsemiconductor.com) for more information).

Part Number	Configuration	Package
300P14-U	4-Matched NPN Transistors, Beta = 60 min.	DIP14
300S14-U		SO14
300AS14-U	4-Matched NPN Transistors, Beta = 150 min.	SO14
300BS14-U	4-Matched NPN Transistors, Beta = 300 min.	SO14
320P14-U	4-Matched PNP Transistors	DIP14
320S14-U		SO14
340P14-U	2-Matched NPN Transistors and 2-Matched PNP Transistors	DIP14
340S14-U		SO14

Table 1. Ordering Information

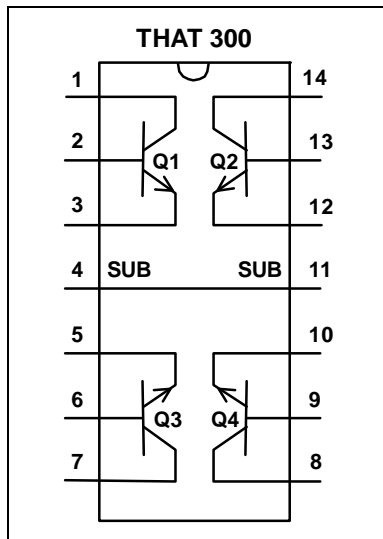


Figure 1. 300 Pinout

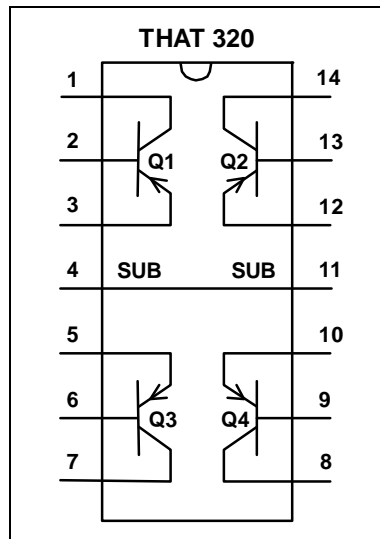


Figure 2. 320 Pinout

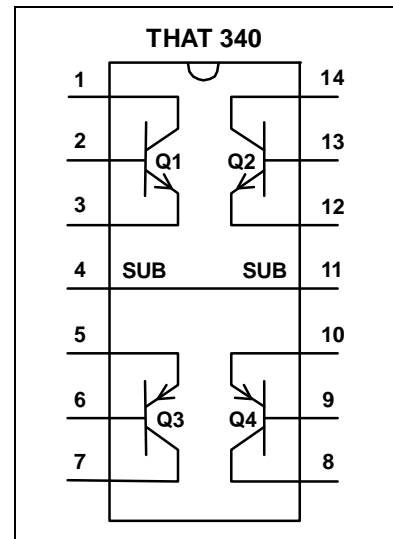


Figure 3. 340 Pinout

## SPECIFICATIONS<sup>1</sup>

### Absolute Maximum Ratings<sup>2,3</sup>

NPN Collector-Emitter Voltage ( $V_{CE0}$ )	36 V	Collector Current	30 mA
NPN Collector-Base Voltage ( $V_{CBO}$ )	36V	Emitter Current	30 mA
PNP Collector-Emitter Voltage ( $V_{CE0}$ )	-36 V	Operating Temperature Range ( $T_{OP}$ )	-40 to +85 °C
PNP Collector-Base Voltage ( $V_{CBO}$ )	-36 V	Maximum Junction Temperature ( $T_{JMAX}$ )	+125 °C
Collector-Substrate Voltage ( $V_{CS}$ )	$\pm 100$ V	Storage Temperature ( $T_{ST}$ )	-45 to +125 °C

### NPN Electrical Characteristics<sup>2</sup>

Parameter	Symbol	Conditions	300 / 340(Q1,Q2)			300A			300B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
NPN Current gain	$h_{fe}$	$V_{CB} = 10$ V, $I_C = 1$ mA $I_C = 10$ $\mu$ A	60	100	—	150	—	—	300	—	—	
NPN Current Gain Matching	$\Delta h_{fe}$	$V_{CB} = 10$ V, $I_C = 1$ mA	—	4	—	—	4	—	—	4	—	%
NPN Noise Voltage Density	$e_N$	$V_{CB} = 10$ V, $I_C = 1$ mA, 1kHz	—	0.8	—	—	0.9	—	—	1	—	nV $\sqrt$ Hz
NPN Gain-Bandwidth Product	$f_T$	$I_C = 1$ mA, $V_{CB} = 10$ V	—	350	—	—	350	—	—	350	—	MHz
NPN $\Delta V_{BE}$ 300: $ V_{BE1}-V_{BE2} $ ; $ V_{BE3}-V_{BE4} $ 340: $ V_{BE1}-V_{BE2} $	$V_{OS}$	$I_C = 1$ mA $I_C = 10$ mA	—	0.5	3	—	0.5	3	—	0.5	3	mV mV
NPN $\Delta I_B$ 300: $ I_{B1}-I_{B2} $ ; $ I_{B3}-I_{B4} $ 340: $ I_{B1}-I_{B2} $	$I_{OS}$	$I_C = 1$ mA $I_C = 10$ $\mu$ A	—	500	1500	—	200	600	—	100	300	nA nA
NPN Collector-Base Leakage Current	$I_{CBO}$	$V_{CB} = 25$ V	—	25	—	—	25	—	—	25	—	pA
NPN Bulk Resistance	$r_{BE}$	$V_{CB} = 0$ V, $10$ $\mu$ A $< I_C < 10$ mA	—	2	—	—	2	—	—	2	—	$\Omega$
NPN Base Spreading Resistance	$r_{bb}$	$V_{CB} = 10$ V, $I_C = 1$ mA	—	30	—	—	TBD	—	—	TBD	—	$\Omega$
NPN Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1$ mA, $I_B = 100$ $\mu$ A	—	0.05	—	—	0.05	—	—	0.05	—	V

**SPECIFICATIONS<sup>1</sup> (Cont'd)**

<b>NPN Electrical Characteristics<sup>2</sup> (cont'd)</b>												
Parameter	Symbol	Conditions	300 / 340(Q1,Q2)			300A			300B			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
NPN Output Capacitance	C <sub>OB</sub>	V <sub>CB</sub> = 10V, I <sub>E</sub> = 0mA, 100kHz	—	3	—	—	3	—	—	3	—	pF
NPN Breakdown Voltage	BV <sub>CEO</sub>	I <sub>C</sub> = 10 μAdc, I <sub>B</sub> = 0	36	40	—	36	40	—	36	40	—	V
Input Capacitance	C <sub>EBO</sub>	I <sub>C</sub> = 0 mA, V <sub>EB</sub> = 0 V	—	5	—	—	5	—	—	5	—	pF

<b>PNP Electrical Characteristics<sup>2</sup></b>						
Parameter	Symbol	Conditions	Min	Typ	Max	Units
PNP Current Gain	h <sub>ie</sub>	V <sub>CB</sub> = -10 V I <sub>C</sub> = -1 mA I <sub>C</sub> = -10 μA	50 —	75 75	— —	
PNP Current Gain Matching	Δh <sub>ie</sub>	V <sub>CB</sub> = -10 V, I <sub>C</sub> = -1 mA	—	5	—	%
PNP Noise Voltage Density	e <sub>N</sub>	V <sub>CB</sub> = -10 V, I <sub>C</sub> = -1 mA, 1 kHz	—	0.75	—	nV√Hz
PNP Gain-Bandwidth Product	f <sub>T</sub>	I <sub>C</sub> = -1 mA, V <sub>CB</sub> = -10 V	—	325	—	MHz
PNP ΔV <sub>BE</sub> 320:  V <sub>BE1</sub> -V <sub>BE2</sub>   ;  V <sub>BE3</sub> -V <sub>BE4</sub>   340:  V <sub>BE1</sub> -V <sub>BE2</sub>	V <sub>OS</sub>	I <sub>C</sub> = -1 mA I <sub>C</sub> = -10 μA	— —	0.5 0.5	3 —	mV mV
PNP ΔI <sub>B</sub> 320:  I <sub>B1</sub> -I <sub>B2</sub>   ;  I <sub>B3</sub> -I <sub>B4</sub>   340:  I <sub>B1</sub> -I <sub>B2</sub>	I <sub>OS</sub>	I <sub>C</sub> = -1 mA I <sub>C</sub> = -10 μA	— —	700 7	1800 —	nA nA
PNP Collector-Base Leakage Current	I <sub>CB0</sub>	V <sub>CB</sub> = -25 V	—	-25	—	pA
PNP Bulk Resistance	r <sub>BE</sub>	V <sub>CB</sub> = 0 V, -10μA > I <sub>C</sub> > -10 mA	—	2	—	Ω
PNP Base Spreading Resistance	r <sub>bb</sub>	V <sub>CB</sub> = -10 V, I <sub>C</sub> = -1 mA	—	25	—	Ω
PNP Collector Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>C</sub> = -1 mA, I <sub>B</sub> = -100 μA	—	-0.05	—	V
PNP Output Capacitance	C <sub>OB</sub>	V <sub>CB</sub> = -10 V, I <sub>E</sub> = 0 mA, 100 kHz	—	3	—	pF
PNP Breakdown Voltage	BV <sub>CEO</sub>	I <sub>C</sub> = -10 mAdc, I <sub>B</sub> = 0	-36	-40	—	V
Input Capacitance	C <sub>EBO</sub>	I <sub>C</sub> = 0 mA, V <sub>EB</sub> = 0 V	—	6	—	pF

1. All specifications are subject to change without notice.
2. Unless otherwise noted, T<sub>A</sub> = 25°C.
3. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### Packaging and Soldering Information

The THAT 300, 320 and 340 are available in 14-pin PDIP and 14-pin surface mount (SOIC) packages. Package dimensions are shown below.

The 300-series packages are entirely lead-free. The lead-frames are copper, plated with successive layers of nickel, palladium, and gold. This approach makes it possible to solder these devices using lead-free and lead-bearing solders.

Neither the lead-frames nor the plastic mold compounds used in the 300-series contains any hazardous substances as specified in the European Union's Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment 2002/95/EG of January 27, 2003. The surface-mount package is suitable for use in a 100% tin solder process.

Package Characteristics				
Parameter	Symbol	Conditions	Typ	Units
Through-hole package		See Fig. 4 for dimensions	14 Pin PDIP	
Thermal Resistance	$\theta_{JA}$	DIP package soldered to board	100	$^{\circ}\text{C/W}$
Environmental Regulation Compliance		Complies with January 27, 2003 RoHS requirements		
Surface mount package		See Fig. 5 for dimensions	14 Pin SOP	
Thermal Resistance	$\theta_{JA}$	SO package soldered to board	100	$^{\circ}\text{C/W}$
Soldering Reflow Profile		JEDEC JESD22-A113-D (250 $^{\circ}\text{C}$ )		
Moisture Sensitivity Level	MSL	Above-referenced JEDEC soldering profile	1	
Environmental Regulation Compliance		Complies with RoHS requirements		

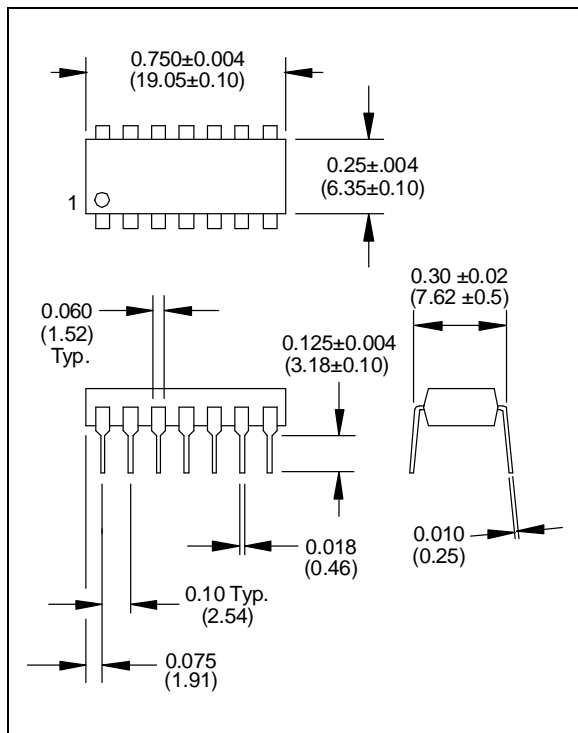


Figure 4. Dual-In-Line Package Outline

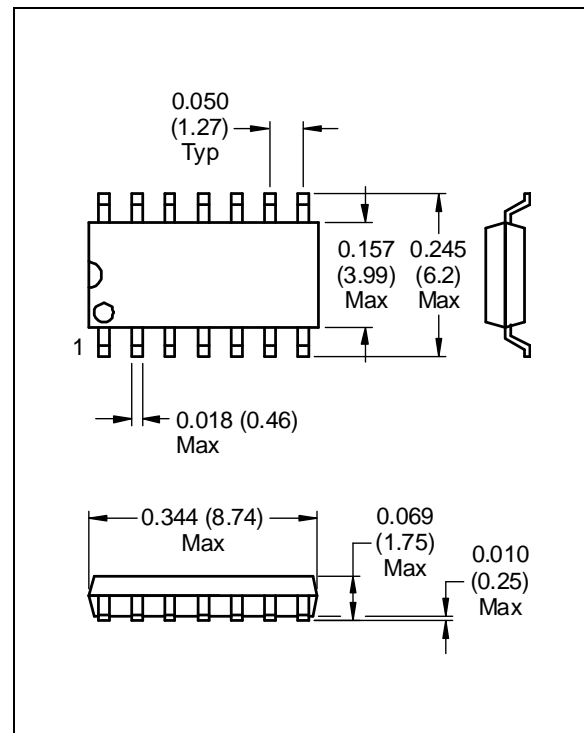


Figure 5. Surface-Mount Package Outline

THAT Corporation believes all the information furnished in this data sheet is accurate and reliable. However we assume no responsibility for its use nor for any infringements of third-party intellectual property which may result from its use.

**LIFE SUPPORT POLICY**

THAT Corporation ICs are not designed for use in life support equipment where a malfunction of our ICs might reasonably result in injury or death. Customers who use or sell our ICs for such life support application do so at their own risk, and shall hold THAT Corporation harmless from any and all claims, damages, suits, or expenses resulting from such use or sale.

**CAUTION: THIS IS AN ESD (ELECTROSTATIC DISCHARGE) SENSITIVE DEVICE**

Electrostatic charges in the range of several kV can accumulate on the human body as well as test and assembly equipment. This device can be damaged by the currents generated by electrostatic discharge from bodies and equipment. Moreover, the transistors in this device are unprotected in order to maximize performance and flexibility. Accordingly, they are more sensitive to ESD damage than many other ICs which include protection devices at their inputs. Note that all of the pins are susceptible.

Use ESD-preventative measures when storing and handling this device. Unused devices should be stored in conductive packaging. Packaging should be discharged to the destination socket before the devices are removed from their packages. ESD damage can occur to these devices even after they are installed in a board-level assembly. Circuits should include specific and appropriate ESD protection.

**Revision History**

<b>Revision</b>	<b>ECO</b>	<b>Date</b>	<b>Changes</b>	<b>Page</b>
00	—	April 2004	Release	
01	2393	April 2010	Changed Max. Operating Temperature from 70 °C to 85 °C.	2
02	2460	Sept. 2010	-Added high $h_{fe}$ versions Models 300A and 300B with accompanying specifications and information. -Revised Features, Applications, and Description sections -Revised Maximum Rating section -Added NPN Breakdown Voltage spec. -Added PNP Breakdown Voltage spec. -Added Packaging Characteristics Table. -Revised disclaimer text	— 1 2 3 3 4 5

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