



# PSMN1R0-40YLD

**N-channel 40 V, 1.1 mΩ, 280 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology**

30 November 2017

Product data sheet

## 1. General description

280 Amp, logic level gate drive N-channel enhancement mode MOSFET in 150 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

## 2. Features and benefits

- 280 A capability
- Avalanche rated, 100% tested at  $I_{AS} = 190$  A
- NextPower-S3 technology delivers 'superfast switching with soft recovery'
- Low  $Q_{RR}$ ,  $Q_G$  and  $Q_{GD}$  for high system efficiency and low EMI designs
- Schottky-Plus body-diode, gives soft switching without the associated high  $I_{DSS}$  leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power SO8) package, copper-clip, solder die attach and qualified to 150 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

## 3. Applications

- Synchronous rectification
- DC-to-DC converters
- High performance & high efficiency server power supply
- Motor control
- Power ORing

## 4. Quick reference data

**Table 1. Quick reference data**

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10$ V; $T_{mb} = 25$ °C; <a href="#">Fig. 2</a>	[1]	-	-	280	A
$P_{tot}$	total power dissipation	$T_{mb} = 25$ °C; <a href="#">Fig. 1</a>		-	-	198	W
$T_j$	junction temperature			-55	-	150	°C

**Static characteristics**

$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 25$ A; $T_j = 25$ °C; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>		-	1.1	1.4	mΩ
		$V_{GS} = 10$ V; $I_D = 25$ A; $T_j = 25$ °C; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>		-	0.93	1.1	mΩ

**nexperia**

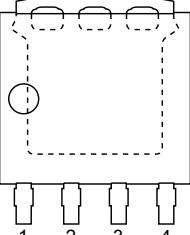
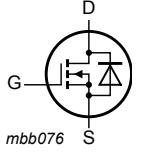
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Dynamic characteristics</b>							
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>		-	17	-	nC
Q <sub>G(tot)</sub>	total gate charge			-	59	-	nC

[1] 280A continuous current has been successfully demonstrated during application tests. Practically, the current will be limited by PCB, thermal design and operation temperature.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain	 <b>LFPAK56; Power-SO8 (SOT1023)</b>	

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-40YLD	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56); 4 leads	SOT1023

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-40YLD	1D040L

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}$		-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \leq 20 \text{ ns}; f \leq 500 \text{ kHz}; E_{DS(AL)} \leq 200 \text{ nJ}$ ; pulsed		-	45	V
$V_{DGR}$	drain-gate voltage	$25^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}; R_{GS} = 20 \text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25^{\circ}\text{C}$ ; <a href="#">Fig. 1</a>		-	198	W
$I_D$	drain current	$V_{GS} = 10 \text{ V}; T_{mb} = 25^{\circ}\text{C}$ ; <a href="#">Fig. 2</a>	[1]	-	280	A
		$V_{GS} = 10 \text{ V}; T_{mb} = 100^{\circ}\text{C}$ ; <a href="#">Fig. 2</a>		-	198	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \mu\text{s}; T_{mb} = 25^{\circ}\text{C}$ ; <a href="#">Fig. 3</a>		-	1284	A
$T_{stg}$	storage temperature			-55	150	°C
$T_j$	junction temperature			-55	150	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
$V_{ESD}$	electrostatic discharge voltage	HBM		2	-	kV

### Source-drain diode

$I_S$	source current	$T_{mb} = 25^{\circ}\text{C}$		-	165	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10 \mu\text{s}; T_{mb} = 25^{\circ}\text{C}$		-	1284	A

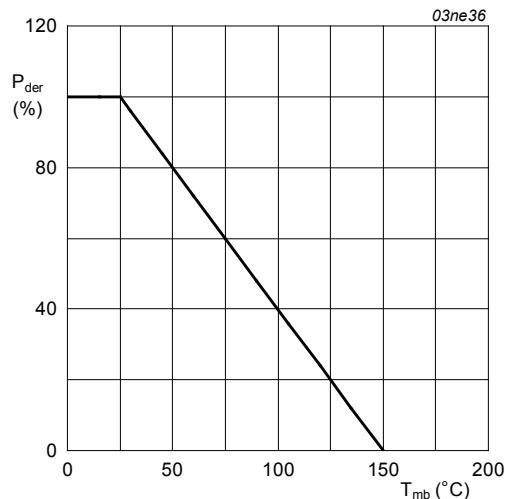
### Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 85 \text{ A}; V_{sup} \leq 40 \text{ V}; R_{GS} = 50 \Omega; V_{GS} = 10 \text{ V}; T_{j(init)} = 25^{\circ}\text{C}$ ; unclamped; $t_p = 0.26 \text{ ms}$	[2]	-	578	mJ
		$I_D = 25 \text{ A}; V_{sup} \leq 40 \text{ V}; R_{GS} = 50 \Omega; V_{GS} = 10 \text{ V}; T_{j(init)} = 25^{\circ}\text{C}$ ; unclamped; $t_p = 3.8 \text{ ms}$	[2]	-	2472	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 40 \text{ V}; V_{GS} = 10 \text{ V}; T_{j(init)} = 25^{\circ}\text{C}; R_{GS} = 50 \Omega$	[2]	-	190	A

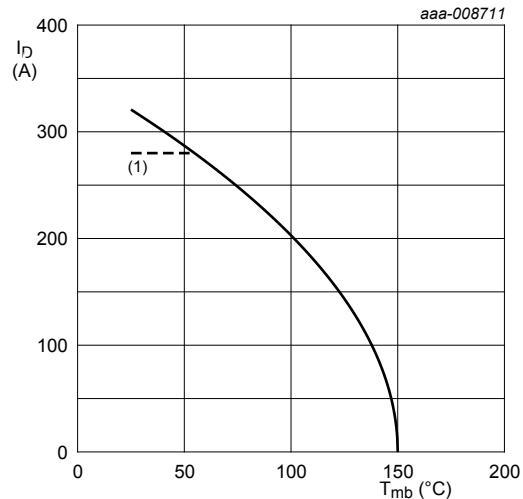
[1] 280A continuous current has been successfully demonstrated during application tests. Practically, the current will be limited by PCB, thermal design and operation temperature.

[2] Protected by 100% test

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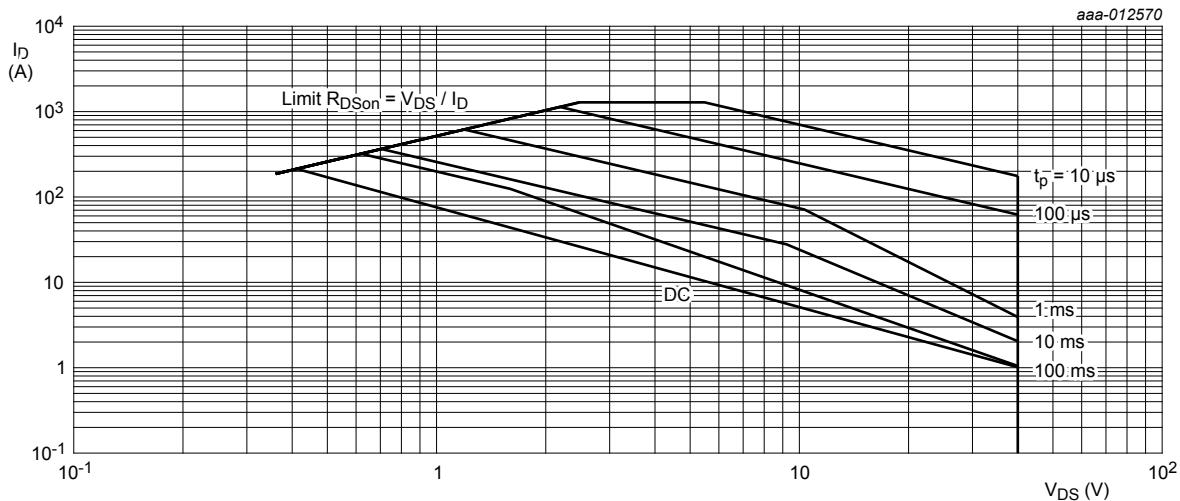


**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



(1) 280A continuous current has been successfully demonstrated during applications tests. Practically, the current will be limited by PCB, thermal design and operating temperature.  
 $V_{GS} \geq 10V$

**Fig. 2. Continuous drain current as a function of mounting base temperature**



**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 4</a>	-	0.56	0.63	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 5</a> <a href="#">Fig. 6</a>	-	50	-	K/W
			-	125	-	K/W

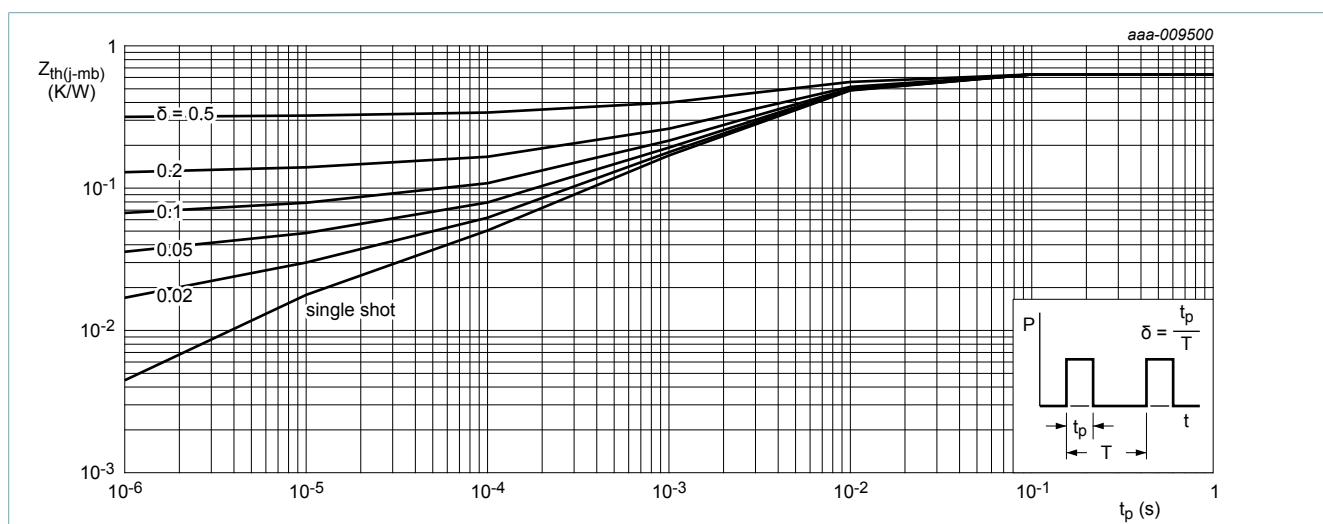


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

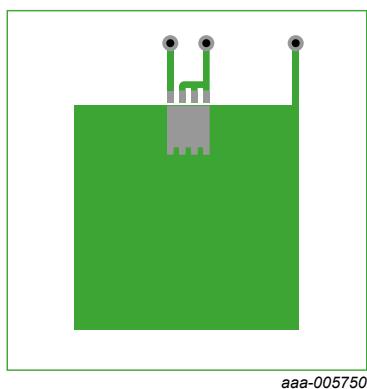


Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

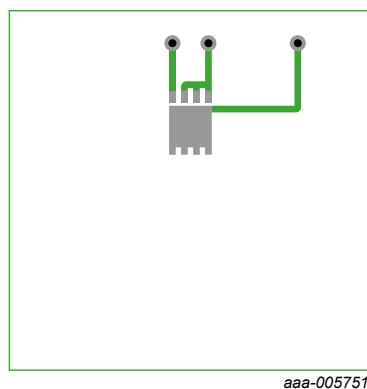


Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

## 10. Characteristics

Table 7. Characteristics

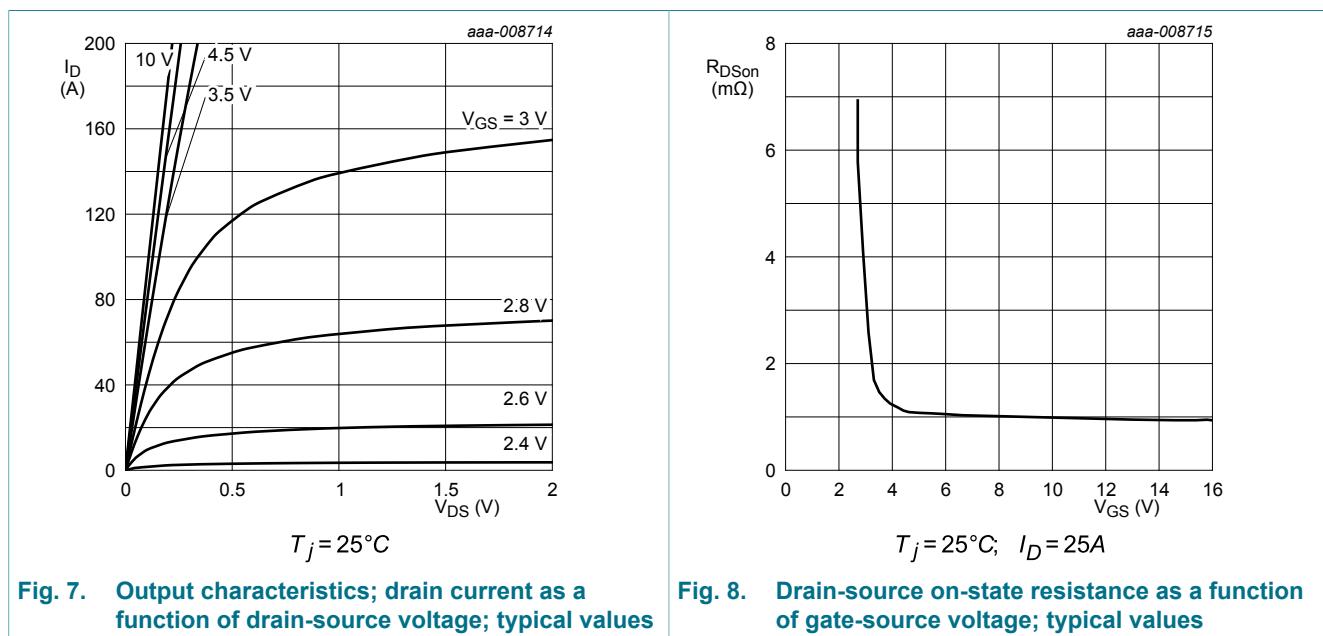
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 µA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	40	-	-	V
		I <sub>D</sub> = 250 µA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	36	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C	1.05	1.7	2.2	V
ΔV <sub>GS(th)/ΔT</sub>	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	-5.1	-	mV/K
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	1	µA
		V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 125 °C	-	9	-	µA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
		V <sub>GS</sub> = -16 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	-	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	0.93	1.1	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 150 °C; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	1.93	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	1.1	1.4	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 150 °C; <a href="#">Fig. 10</a> ; <a href="#">Fig. 11</a>	-	-	2.45	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz	-	1.3	-	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 10 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	127	-	nC
		I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	59	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V	-	115	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 4.5 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	19	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	12	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	8	-	nC
Q <sub>GD</sub>	gate-drain charge		-	17	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 20 V; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	-	2.7	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 20 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 14</a>	-	8845	-	pF
C <sub>oss</sub>	output capacitance		-	1878	-	pF
C <sub>rss</sub>	reverse transfer capacitance		-	382	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	turn-on delay time	$V_{DS} = 20 \text{ V}; R_L = 0.8 \Omega; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 5 \Omega$	-	52	-	ns
$t_r$	rise time		-	62	-	ns
$t_{d(off)}$	turn-off delay time		-	65	-	ns
$t_f$	fall time		-	38	-	ns
$Q_{oss}$	output charge	$V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	-	51	-	nC

**Source-drain diode**

$V_{SD}$	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}; \text{Fig. 15}$	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 20 \text{ V}; \text{Fig. 16}$	-	48	-	ns
$Q_r$	recovered charge		[1]	67	-	nC
$t_a$	reverse recovery rise time		-	28.6	-	ns
$t_b$	reverse recovery fall time		-	23.8	-	ns

[1] includes capacitive recovery



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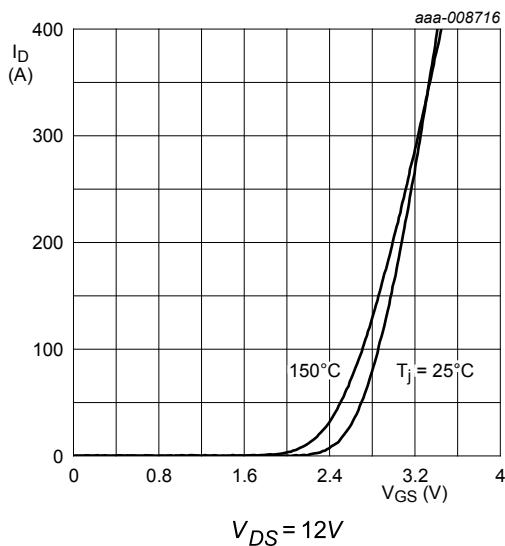


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

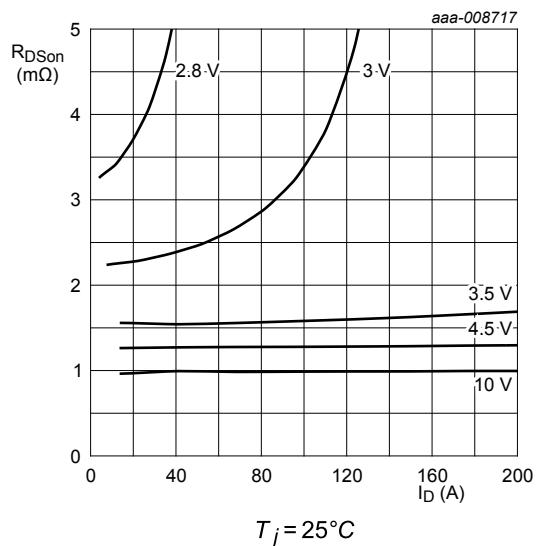


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

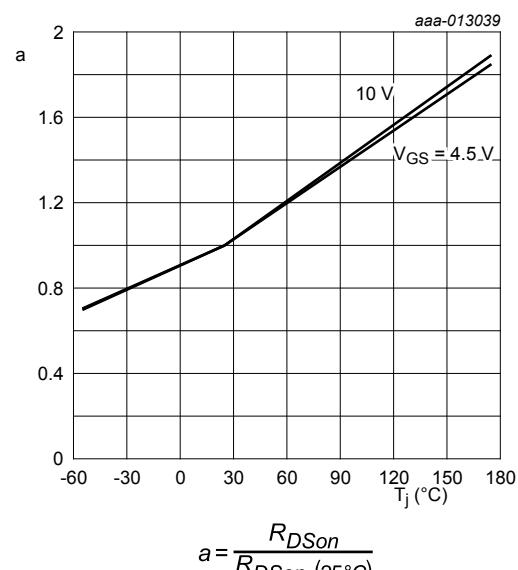


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

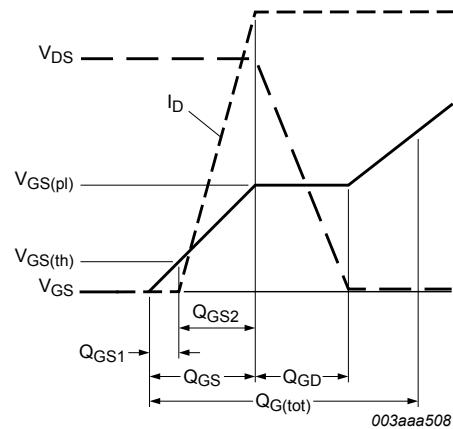


Fig. 12. Gate charge waveform definitions

N-channel 40 V, 1.1 mΩ, 280 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology

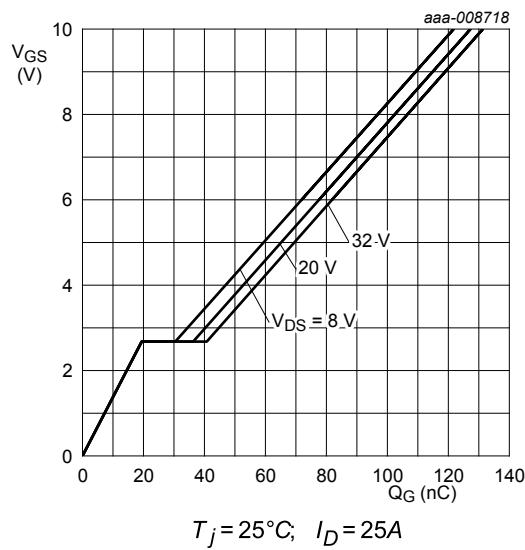


Fig. 13. Gate-source voltage as a function of gate charge; typical values

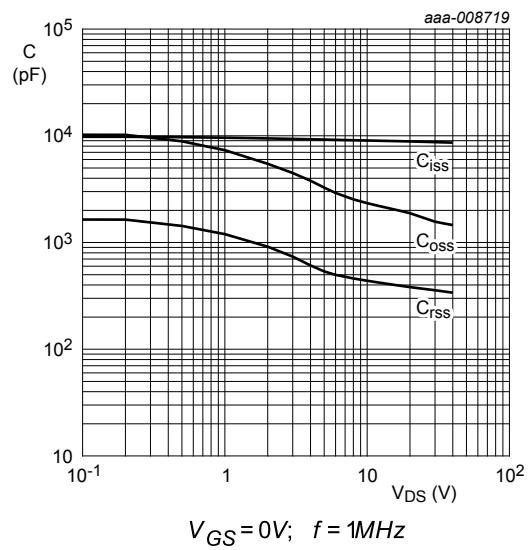


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

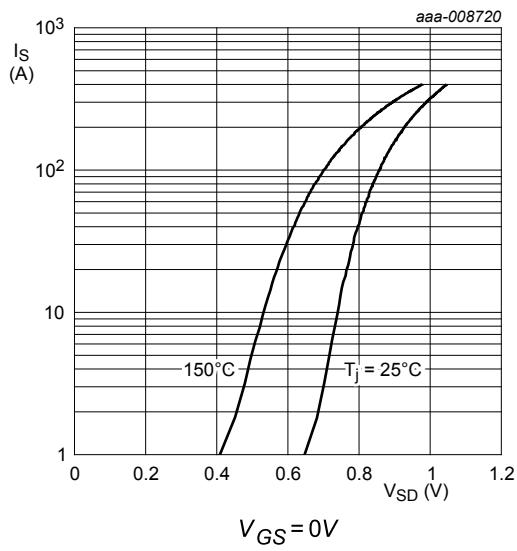


Fig. 15. Source current as a function of source-drain voltage; typical values

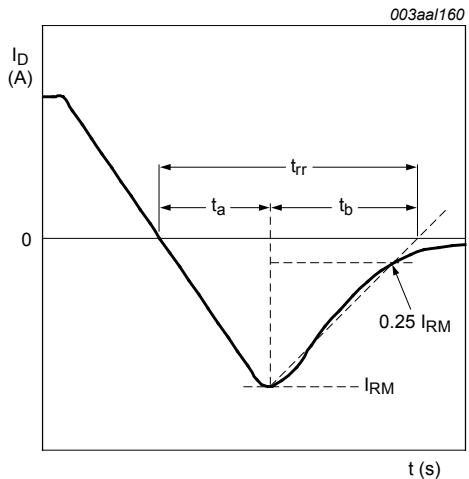
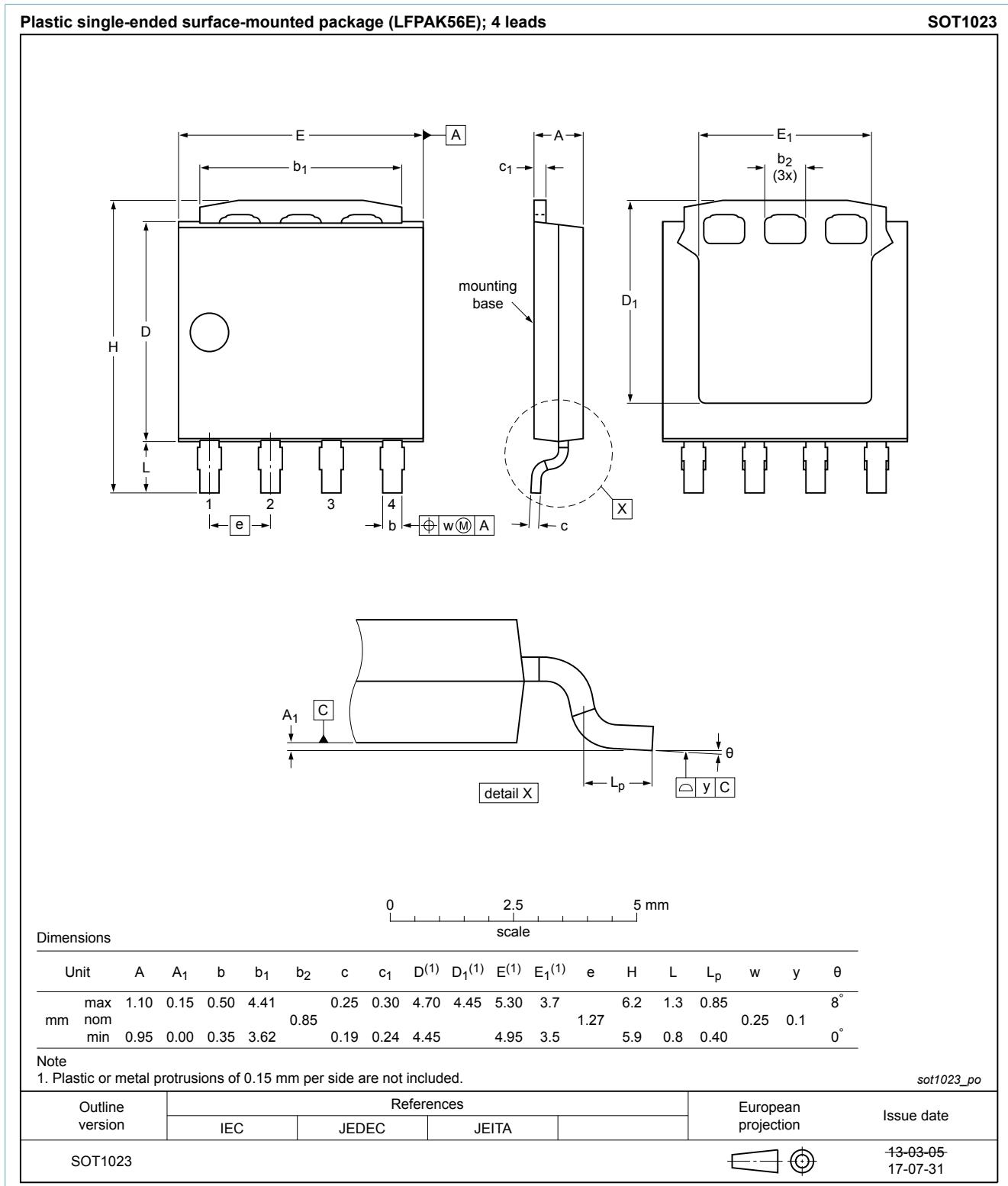


Fig. 16. Reverse recovery timing definition

## 11. Package outline



## 12. Soldering

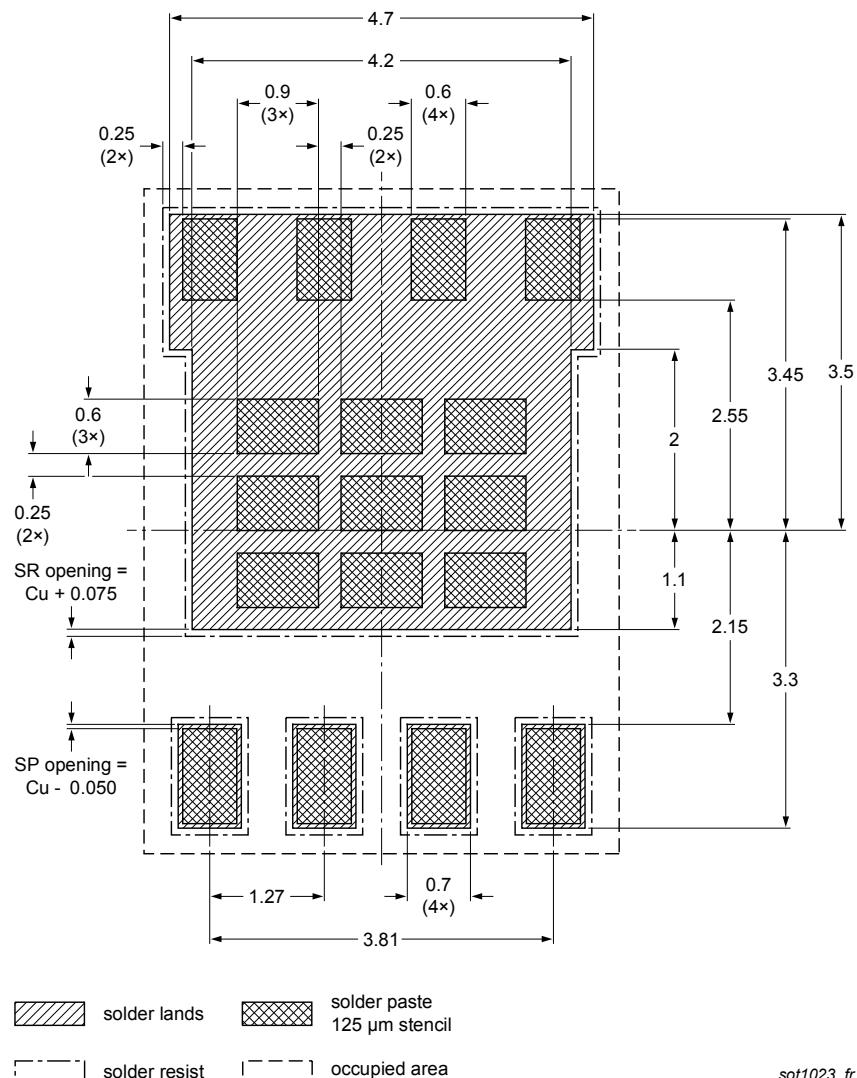


Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT1023)

## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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