NXP Semiconductors
Technical Data

Document Number: A2T14H450-23N
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RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 93 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1452 to 1511 MHz.

1500 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 31 Vdc, I_{DQA} = 1000 mA, V_{GSB} = 0.5 Vdc, P_{out} = 93 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

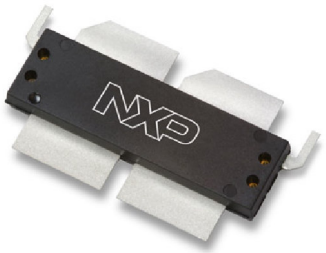
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1452 MHz	18.8	48.2	8.1	–38.2
1480 MHz	19.0	48.0	7.9	–39.2
1511 MHz	19.0	48.7	7.7	–38.6

Features

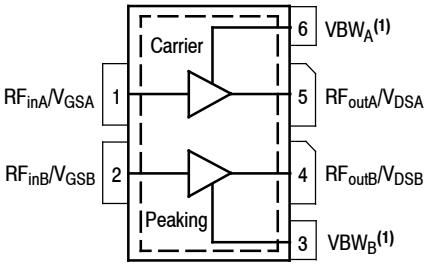
- Advanced high performance in-package Doherty
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems

A2T14H450-23NR6

1452–1511 MHz, 93 W AVG., 31 V AIRFAST RF POWER LDMOS TRANSISTOR



OM-1230-4L2S PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

1. Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 93 W Avg., W-CDMA, 31 Vdc, I_{DQA} = 1000 mA, V_{GSB} = 0.5 Vdc, 1482 MHz	$R_{\theta JC}$	0.27	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 200 μAdc)	$V_{GS(th)}$	1.05	1.2	2.2	Vdc
Gate Quiescent Voltage (V_{DD} = 31 Vdc, I_D = 1000 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.1	2.5	2.9	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$V_{DS(on)}$	0.05	0.15	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 300 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.0 Adc)	$V_{DS(on)}$	0.05	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests – 1452 MHz (1,2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 31 Vdc, I_{DQA} = 1000 mA, V_{GSB} = 0.5 Vdc, P_{out} = 93 W Avg., f = 1452 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.0	18.8	20.0	dB
Drain Efficiency	η_D	45.0	48.2	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	8.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	–38.2	–32.0	dBc
Functional Tests – 1511 MHz (1,2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 31 Vdc, I_{DQA} = 1000 mA, V_{GSB} = 0.5 Vdc, P_{out} = 93 W Avg., f = 1511 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.0	19.0	20.0	dB
Drain Efficiency	η_D	45.0	48.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	7.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	–38.6	–32.0	dBc
Load Mismatch (2) (In NXP Doherty Test Fixture, 50 ohm system) I_{DQA} = 1000 mA, V_{GSB} = 0.5 Vdc, f = 1480 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 560 W Pulsed CW Output Power (3 dB Input Overdrive from 417 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (2) (In NXP Doherty Test Fixture, 50 ohm system) V_{DD} = 31 Vdc, I_{DQA} = 1000 mA, V_{GSB} = 0.5 Vdc, 1452–1511 MHz Bandwidth					
P_{out} @ 3 dB Compression Point (3)	P3dB	—	560	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1452–1511 MHz frequency range)	Φ	—	–10	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	68	—	MHz
Gain Flatness in 59 MHz Bandwidth @ P_{out} = 93 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.023	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.021	—	dB/°C

Table 6. Ordering Information

Device	Tape and Reel Information	Package
A2T14H450-23NR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	OM-1230-4L2S

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

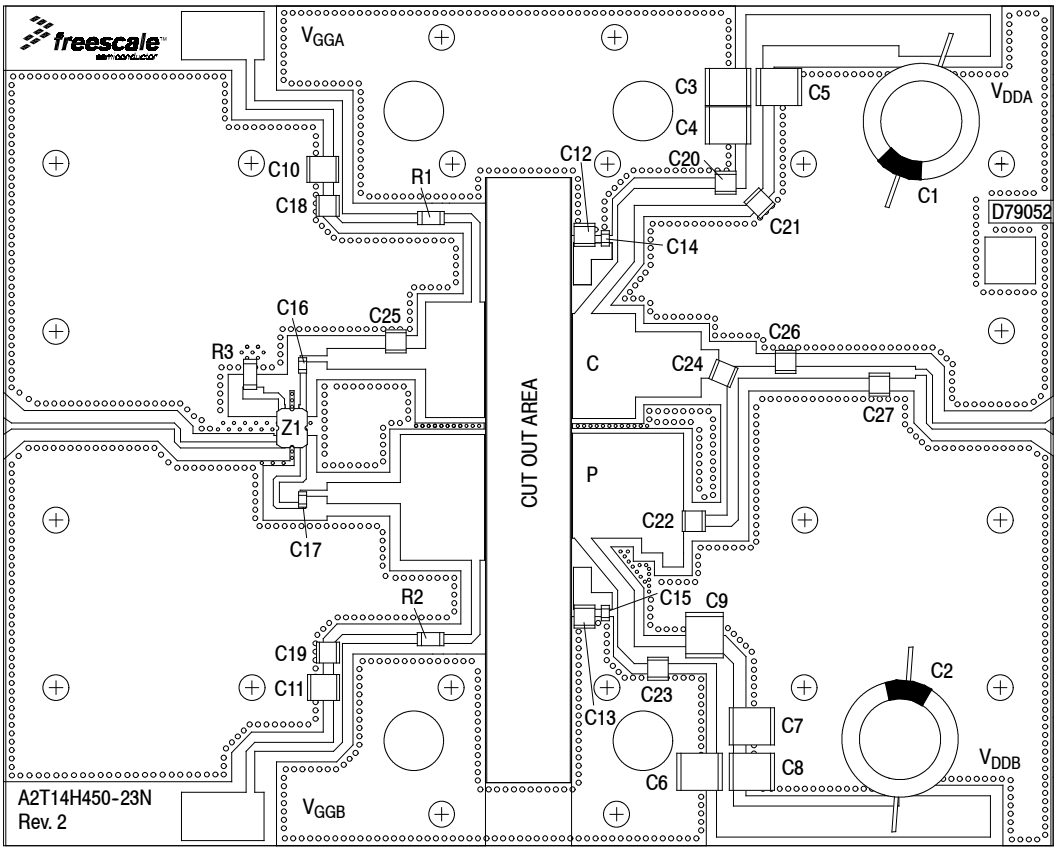


Figure 2. A2T14H450-23NR6 Test Circuit Component Layout

Table 7. A2T14H450-23NR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26RH	Multicomp
C3, C4, C5, C6, C7, C8, C9	10 μF Chip Capacitor	C5750X7S2A106M230KE	TDK
C10, C11	220 nF Chip Capacitor	C1812C224K5RACTU	Kemet
C12, C13	10 μF Chip Capacitor	GRM32ER61H106KA12L	Murata
C14, C15, C16, C17	18 pF Chip Capacitor	GQM2195C2E180JB12D	Murata
C18, C19, C20, C21, C22, C23	18 pF Chip Capacitor	ATC100B180GT500XT	ATC
C24	8.2 pF Chip Capacitor	ATC100B8R2BT500XT	ATC
C25	1.8 pF Chip Capacitor	ATC100B1R8BT500XT	ATC
C26	0.2 pF Chip Capacitor	ATC100B0R2BT500XT	ATC
C27	0.4 pF Chip Capacitor	ATC100B0R4BT500XT	ATC
R1, R2	3.3 Ω, 1/4 W Chip Resistor	WCR1206-3R3FI	Welwyn
R3	50 Ω, 8 W Surface Mount Terminator	C8A50Z4A	Anaren
Z1	1800–2200 MHz Band, 90°, 2 dB Doherty Coupler	X3C20F1-02S	Anaren
PCB	Rogers RO4360G2, 0.020″, ε_r = 6.15	D79052	MTL

TYPICAL CHARACTERISTICS — 1452–1511 MHz

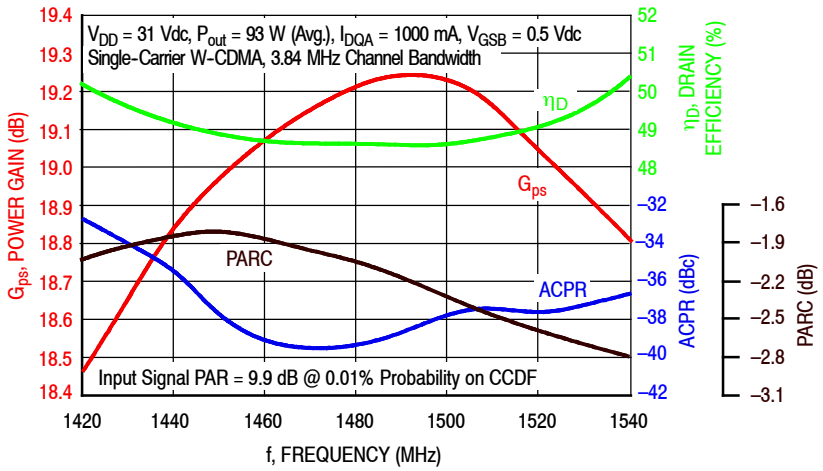


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 93 Watts Avg.

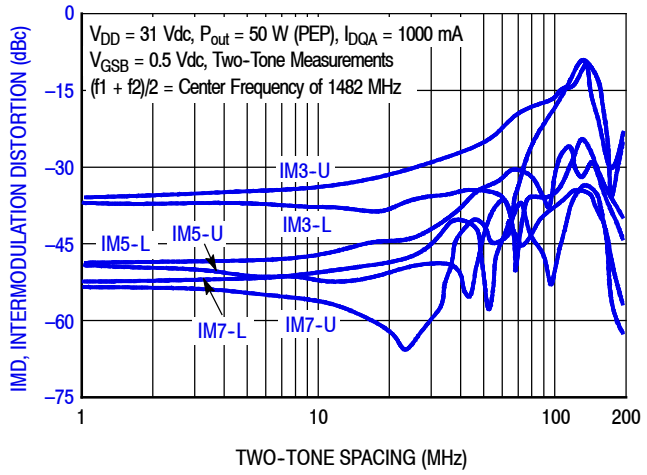


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

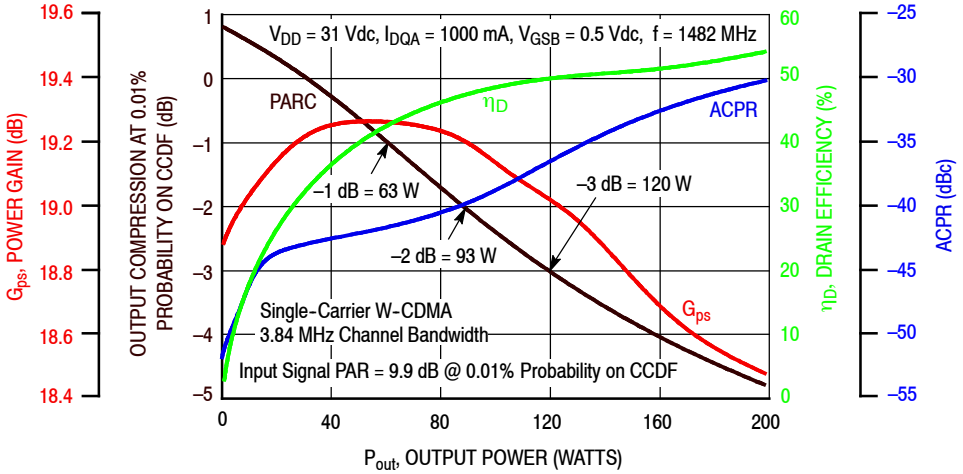


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1452–1511 MHz

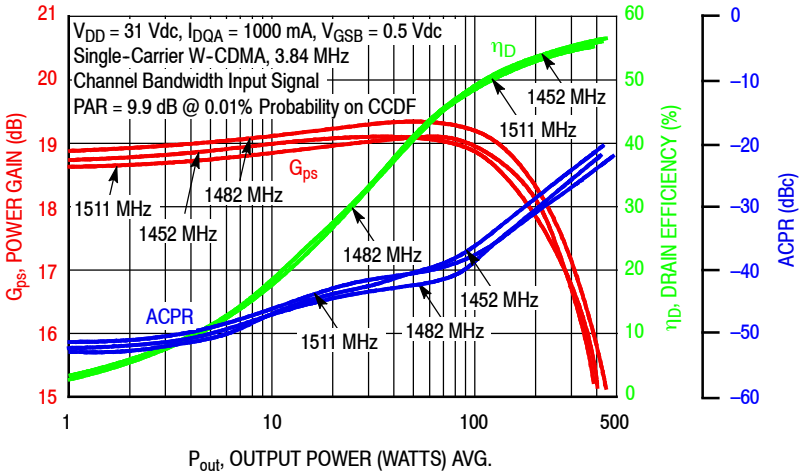


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

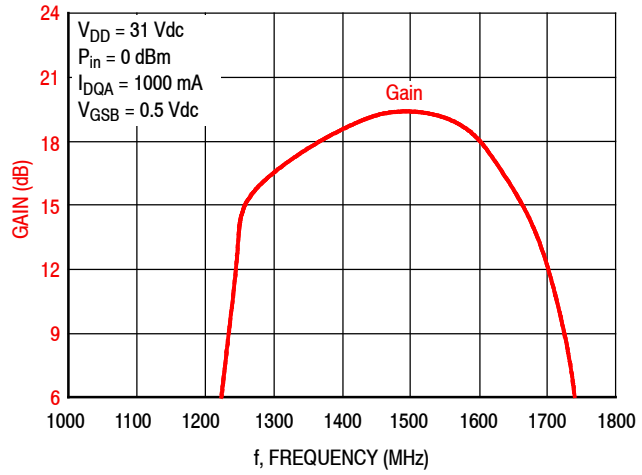


Figure 7. Broadband Frequency Response

Table 8. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, I_{DQA} = 880 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.91 – j4.66	2.03 + j4.44	0.83 – j2.39	19.3	53.5	224	55.2	–14
1475	2.84 – j4.94	2.51 + j4.37	0.80 – j2.41	19.2	53.5	224	54.1	–14
1510	4.51 – j4.97	3.95 + j4.30	0.83 – j2.58	19.4	53.3	214	54.4	–15

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.91 – j4.66	1.97 + j4.74	0.86 – j2.49	17.2	54.2	263	57.2	–19
1475	2.84 – j4.94	2.54 + j4.71	0.81 – j2.50	17.1	54.2	263	55.8	–20
1510	4.51 – j4.97	4.27 + j4.74	0.83 – j2.68	17.2	54.0	251	55.2	–20

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

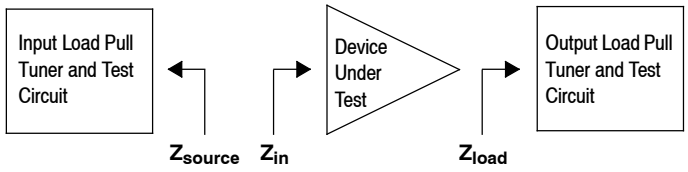
Table 9. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 30 Vdc, I_{DQA} = 880 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.91 – j4.66	2.10 + j4.60	1.91 – j1.26	22.8	50.9	123	67.9	–23
1475	2.84 – j4.94	2.62 + j4.65	1.69 – j1.37	22.7	51.3	135	67.7	–23
1510	4.51 – j4.97	4.30 + j4.44	1.55 – j1.35	23.2	50.7	117	67.1	–25

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.91 – j4.66	2.04 + j4.78	1.77 – j1.51	20.4	52.0	158	68.8	–29
1475	2.84 – j4.94	2.55 + j4.93	1.53 – j1.50	20.5	52.2	166	68.5	–30
1510	4.51 – j4.97	4.37 + j4.87	1.44 – j1.66	20.6	52.1	162	67.8	–31

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1475 MHz

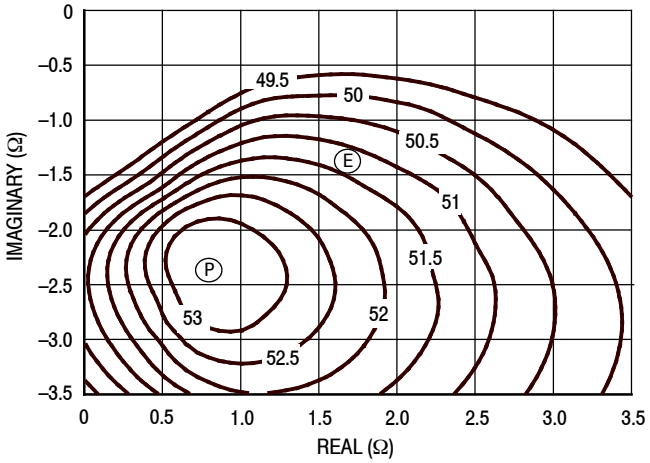


Figure 8. P1dB Load Pull Output Power Contours (dBm)

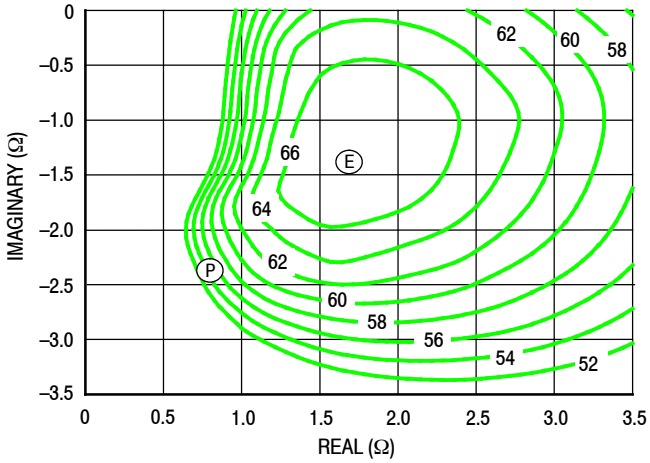


Figure 9. P1dB Load Pull Efficiency Contours (%)

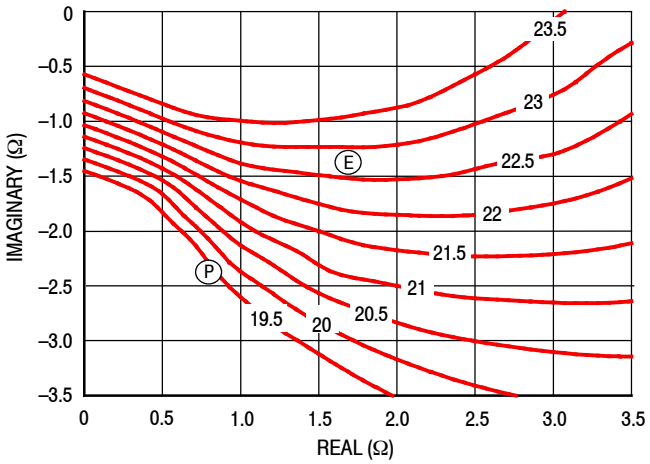


Figure 10. P1dB Load Pull Gain Contours (dB)

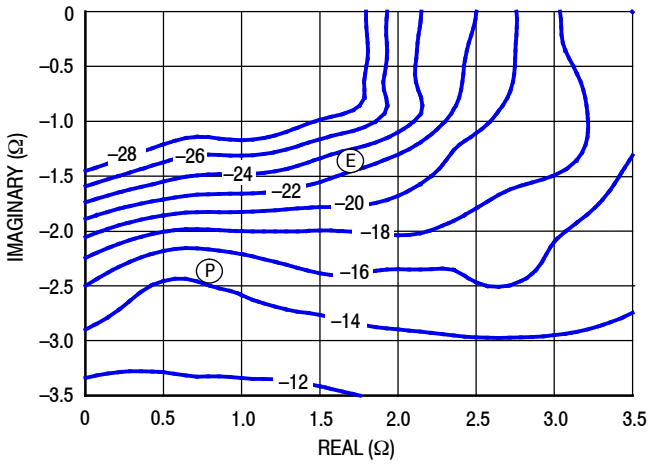


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 1475 MHz

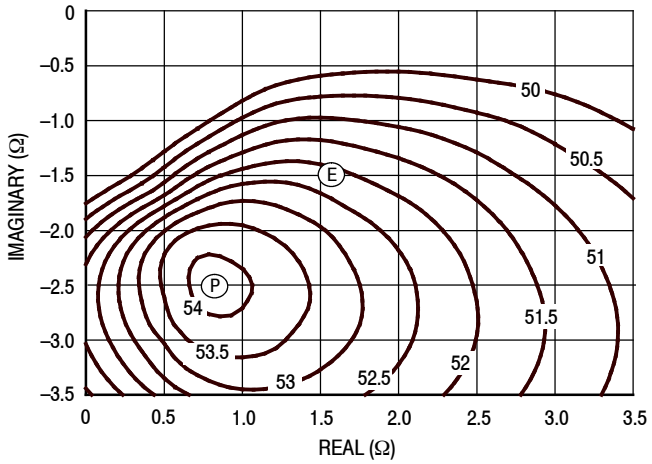


Figure 12. P3dB Load Pull Output Power Contours (dBm)

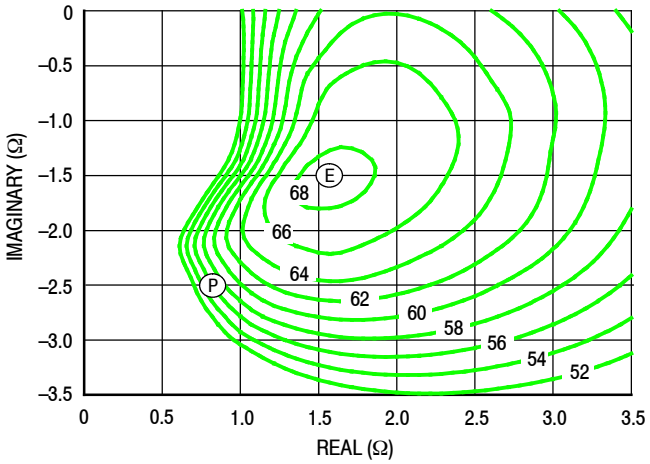


Figure 13. P3dB Load Pull Efficiency Contours (%)

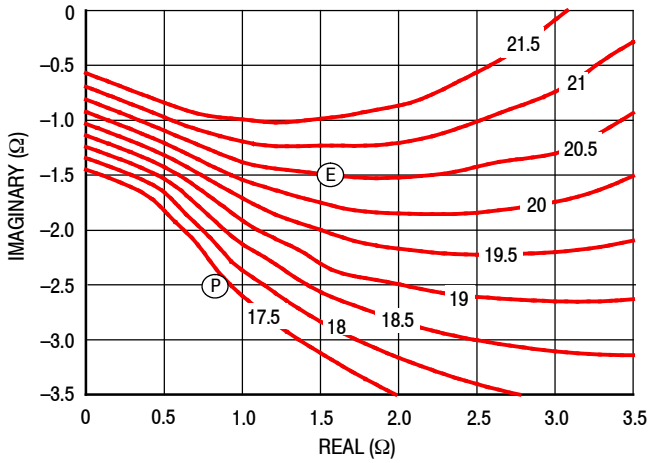


Figure 14. P3dB Load Pull Gain Contours (dB)

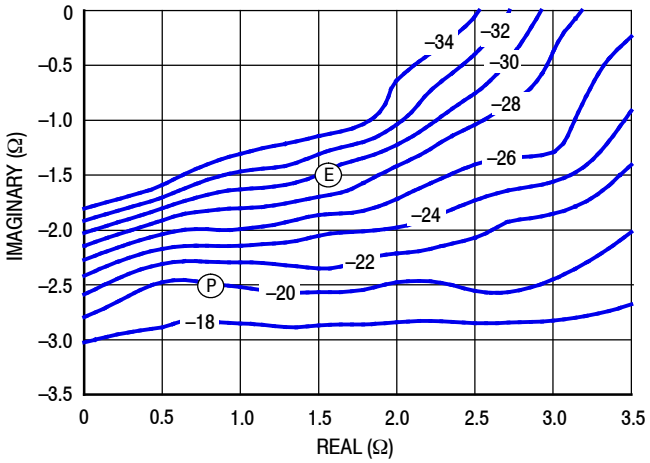


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

Table 10. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 30 Vdc, V_{GSB} = 0.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.11 – j3.84	1.04 + j3.72	0.83 – j2.35	15.3	55.4	347	53.7	–29
1475	1.21 – j3.76	1.28 + j3.67	0.87 – j2.32	15.7	55.4	347	55.2	–31
1510	2.32 – j4.12	2.18 + j4.03	0.88 – j2.51	16.0	55.7	372	55.8	–32

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.11 – j3.84	1.02 + j3.90	0.90 – j2.45	13.3	56.3	427	58.5	–38
1475	1.21 – j3.76	1.27 + j3.85	0.87 – j2.41	13.5	56.2	417	57.4	–39
1510	2.32 – j4.12	2.43 + j4.32	0.92 – j2.61	13.9	56.3	427	58.2	–40

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

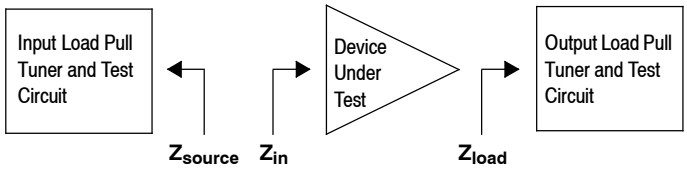
Table 11. Peaking Side Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 30 Vdc, V_{GSB} = 0.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.11 – j3.84	0.93 + j3.72	1.87 – j1.55	16.9	54.0	251	68.0	–34
1475	1.21 – j3.76	1.12 + j3.70	1.84 – j1.21	17.2	53.5	224	67.7	–36
1510	2.32 – j4.12	1.89 + j4.12	1.61 – j1.68	17.3	54.2	263	67.7	–37

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1452	1.11 – j3.84	0.99 + j3.91	1.85 – j1.93	14.6	54.9	309	66.6	–43
1475	1.21 – j3.76	1.24 + j3.90	1.79 – j1.75	15.0	54.8	302	66.6	–46
1510	2.32 – j4.12	2.24 + j4.45	1.78 – j1.84	15.1	54.9	309	66.6	–46

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1475 MHz

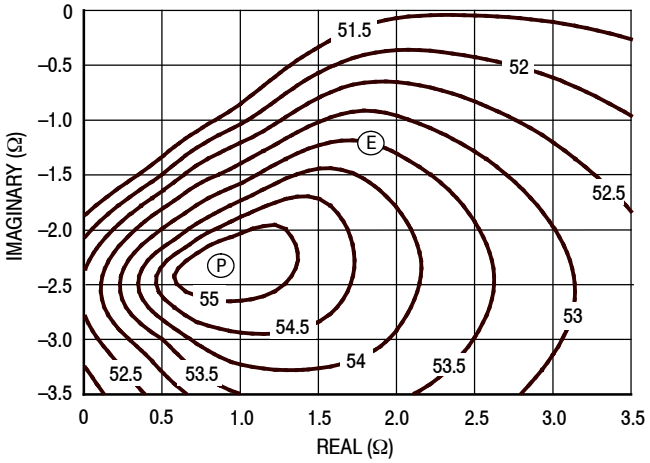


Figure 16. P1dB Load Pull Output Power Contours (dBm)

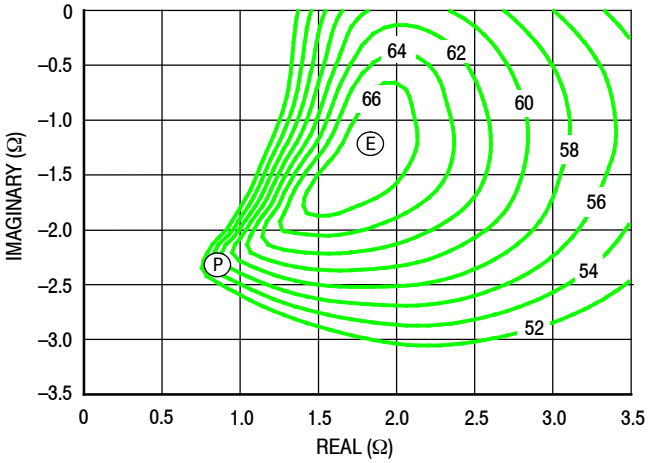


Figure 17. P1dB Load Pull Efficiency Contours (%)

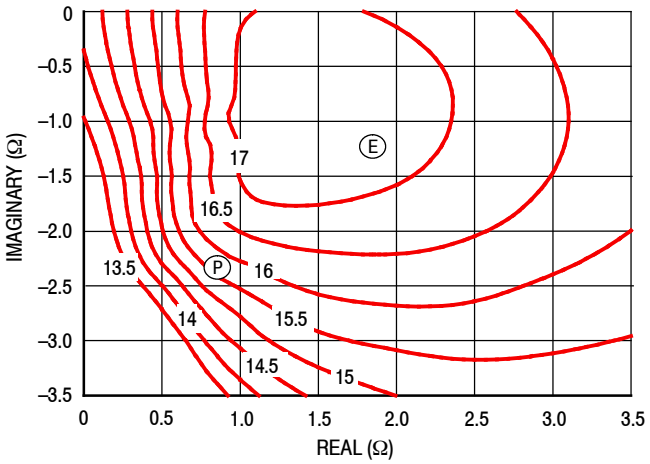


Figure 18. P1dB Load Pull Gain Contours (dB)

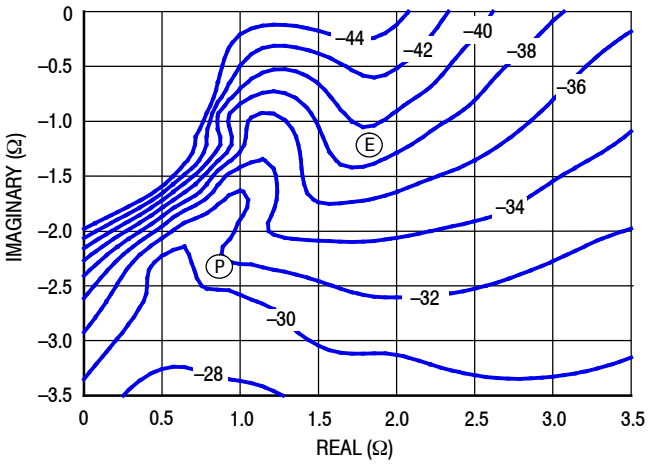


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 1475 MHz

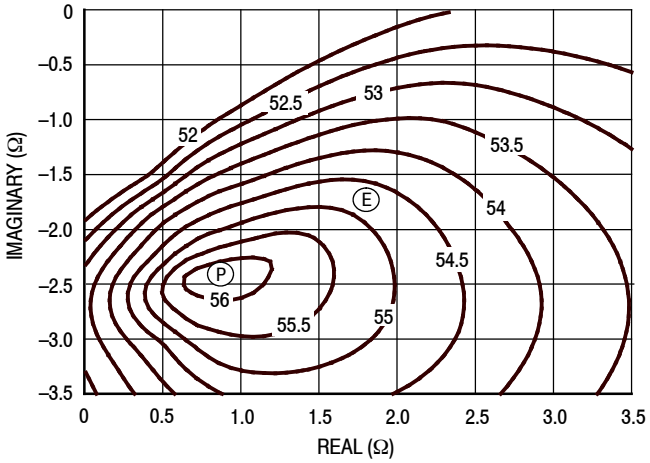


Figure 20. P3dB Load Pull Output Power Contours (dBm)

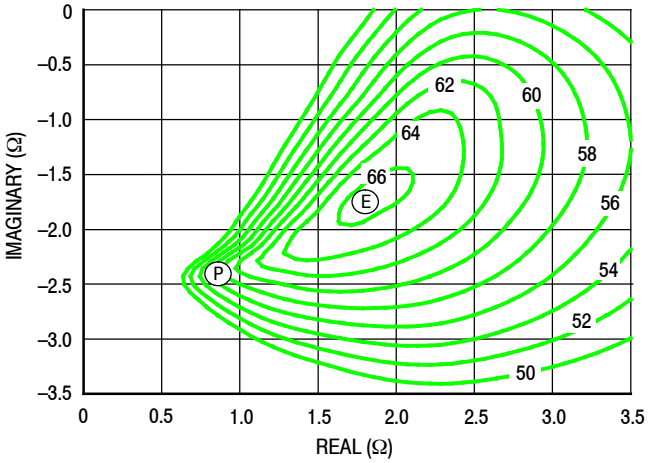


Figure 21. P3dB Load Pull Efficiency Contours (%)

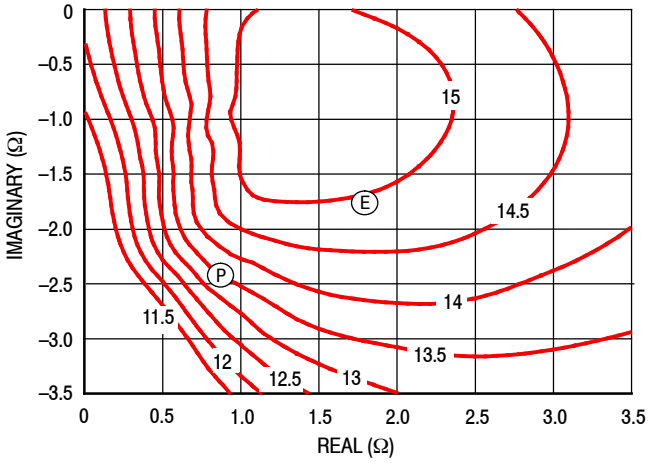


Figure 22. P3dB Load Pull Gain Contours (dB)

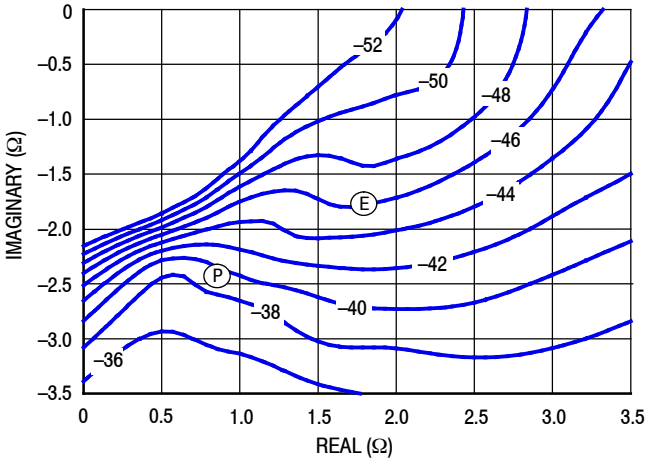


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

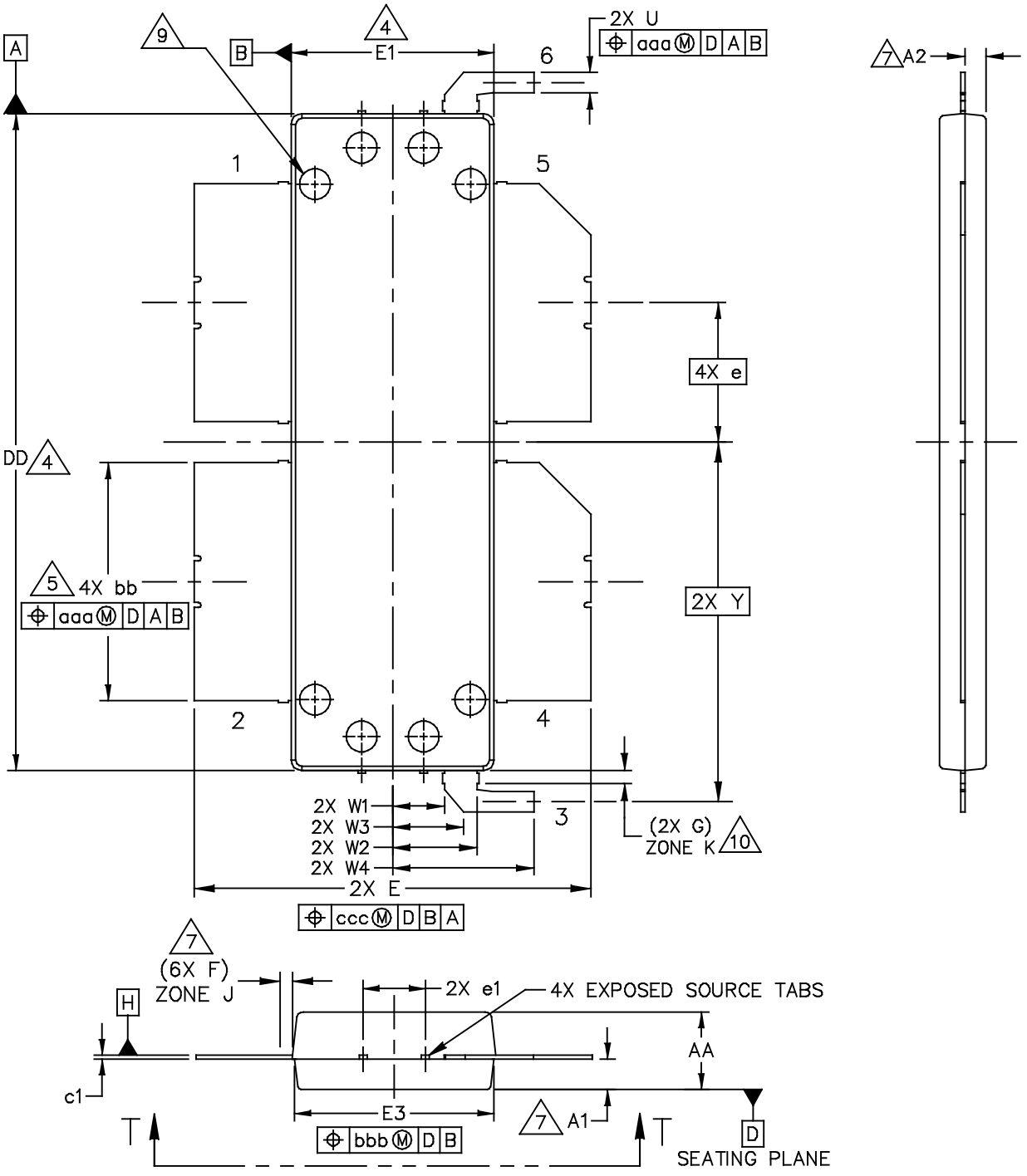
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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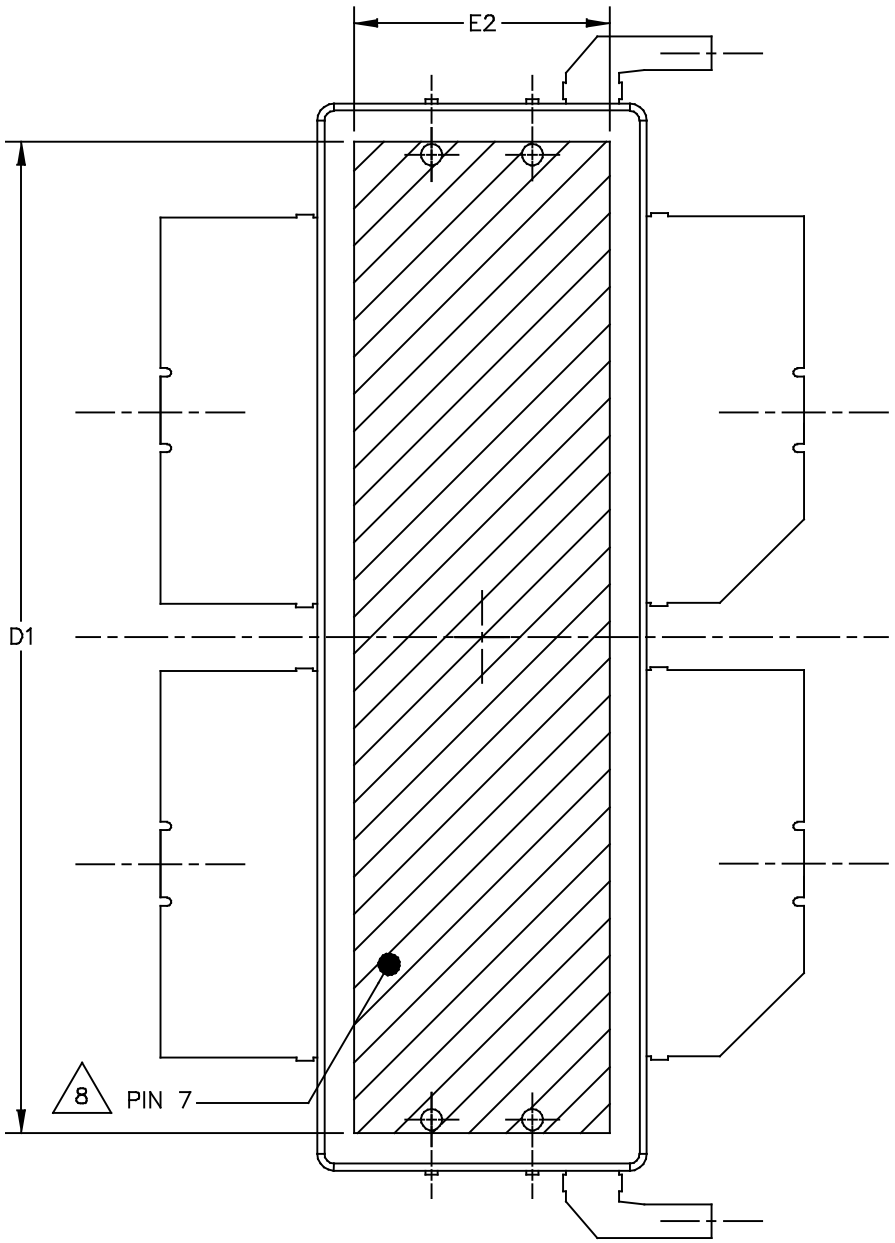
	STANDARD: NON-JEDEC	
	SOT1819-2	18 FEB 2016



BOTTOM VIEW
VIEW T–T

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	STANDARD: NON–JEDEC	
	SOT1819–2	18 FEB 2016

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DD AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 INCH (0.15 MM) PER SIDE. DIMENSIONS DD AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION bb DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 INCH (0.13 MM) TOTAL IN EXCESS OF THE bb DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS A AND B TO BE DETERMINED AT DATUM PLANE H.
7. DIMENSIONS A1 AND A2 APPLY WITHIN ZONE J ONLY. A1 APPLIES TO PINS 1, 2, 4 AND 5. A2 APPLIES TO PINS 3 AND 6.
8. HATCHING REPRESENTS THE EXPOSED AND SOLDERABLE AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.
9. DIMPLED HOLE REPRESENTS INPUT SIDE.
10. ZONE K REPRESENTS NON–SOLDERABLE REGION WHERE MOLD FLASH AND RESIN BLEED ARE PERMITTED ON BOTH SIDES OF THE LEADS.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.148	.152	3.76	3.86	W2	.158	.168	4.01	4.27
A1	.059	.065	1.50	1.65	W3	.132	.142	3.35	3.61
A2	.056	.068	1.42	1.73	W4	.265	.281	6.73	7.14
DD	1.267	1.273	32.18	32.33	U	.037	.043	0.94	1.09
D1	1.180	----	29.97	----	Y	.695 BSC		17.65 BSC	
E	.762	.770	19.35	19.56	bb	.457	.463	11.61	11.76
E1	.390	.394	9.91	10.01	c1	.007	.011	0.18	0.28
E2	.306	----	7.77	----	e	.270 BSC		6.86 BSC	
E3	.383	.387	9.73	9.83	e1	.116	.124	2.95	3.15
F	.025 REF		0.64 REF		aaa	.004		0.10	
G	.030 REF		0.76 REF		bbb	.006		0.15	
W1	.095	.105	2.41	2.67	ccc	.010		0.25	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Jan. 2017	• Initial release of data sheet

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