Small Size, Low-Power, Unidirectional, CURRENT SHUNT MONITOR Zerø-Drift Series

Check for Samples: INA216

FEATURES

- **CHIP-SCALE PACKAGE**
- **COMMON-MODE RANGE: +1.8V to +5.5V**
- **OFFSET VOLTAGE: ±30μV**
- **GAIN ERROR: ±0.2% MAX**
- **CHOICE OF GAINS:**
  - **INA216A1: 25V/V**
  - **INA216A2: 50V/V**
  - **INA216A3: 100V/V**
  - **INA216A4: 200V/V**
- **QUIESCENT CURRENT: 13μA**
- **BUFFERED VOLTAGE OUTPUT: No Additional Op Amp Needed**

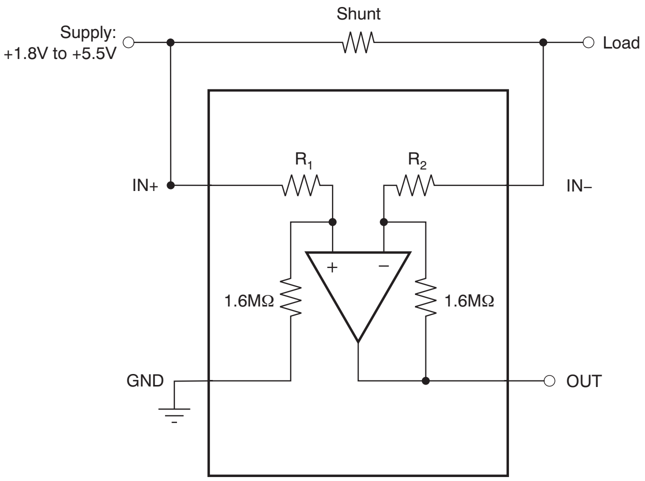
APPLICATIONS

- **NOTEBOOK COMPUTERS**
- **CELL PHONES**
- **TELECOM EQUIPMENT**
- **POWER MANAGEMENT**
- **BATTERY CHARGERS**

DESCRIPTION

The INA216 is a high-side voltage output current shunt monitor that can sense drops across shunts at common-mode voltages from +1.8V to +5.5V. Four fixed gains are available: 25V/V, 50V/V, 100V/V, and 200V/V. The low offset of the Zerø-Drift architecture enables current sensing with maximum drops across the shunt as low as 10mV full-scale, or with wide dynamic ranges of over 1000:1.

These devices operate from a single +1.8V to +5.5V power supply, drawing a maximum of 25μA of supply current. The INA216 series are specified over the temperature range of –40°C to +125°C, and offered in a chip-scale package.



PRODUCT	GAIN	$R_1 = R_2$
INA216A1	25	64kΩ
INA216A2	50	32kΩ
INA216A3	100	16kΩ
INA216A4	200	8kΩ

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	GAIN	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
INA216A1	25V/V	WCSP-4	YFF	OW
INA216A2	50V/V	WCSP-4	YFF	OX
INA216A3	100V/V	WCSP-4	YFF	OY
INA216A4	200V/V	WCSP-4	YFF	OZ

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

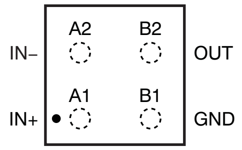
Over operating free-air temperature range, unless otherwise noted.

		INA216	UNIT
Supply Voltage		+7	V
Analog Inputs, V_{IN+}, V_{IN-}(2)	Differential $(V_{IN+})–(V_{IN-})$	–5.5 to +5.5	V
	Common-Mode(3)	GND–0.3V to +5.5	V
Output(3)		GND–0.3V to (V+)+0.3	V
Input Current into Any Pin(3)		5	mA
Operating Temperature		–55 to +150	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings:	Human Body Model	2.5	kV
	Charged Device Model	1	kV
	Machine Model	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{IN+} and V_{IN-} are the voltages at the IN+ and IN– pins, respectively.
(3) Input voltage at any pin may exceed the voltage shown if the current at that pin is limited to 5mA.

PIN CONFIGURATION

YFF PACKAGE
WCSP-4
(TOP VIEW)



(1) Bump side down. Drawing not to scale.

(2) Power supply is derived from shunt (minimum common-mode range = 1.8V)

THERMAL INFORMATION

THERMAL METRIC[1]		INA216A1YFF, INA216A2YFF INA216A3YFF, INA216A4YFF	UNITS
		YFF	
		4	
θ_{JA}	Junction-to-ambient thermal resistance[2]	160	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance[3]	75	
θ_{JB}	Junction-to-board thermal resistance[4]	76	
ψ_{JT}	Junction-to-top characterization parameter[5]	3	
ψ_{JB}	Junction-to-board characterization parameter[6]	74	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance[7]	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C and V_{CM} = V_{IN+}= 4.2V, unless otherwise noted.

PARAMETER		CONDITIONS	INA216			UNIT
			MIN	TYP	MAX	
INPUT						
Offset Voltage, RTI(1)	V_{OS}					
INA216A1				±30	±100	μV
vs Temperature	**dV_{OS}/dT**			**0.06**	**0.2**	**μV/°C**
INA216A2				±20	±75	μV
vs Temperature	**dV_{OS}/dT**			**0.05**	**0.25**	**μV/°C**
INA216A3				±20	±75	μV
vs Temperature	**dV_{OS}/dT**			**0.03**	**0.25**	**μV/°C**
INA216A4				±20	±75	μV
vs Temperature	**dV_{OS}/dT**			**0.1**	**0.3**	**μV/°C**
Common-Mode Input Range	V_{CM}		1.8		5.5	V
Common-Mode Rejection(2)	**CMRR**	**V_{IN+} = +1.8V to +5.5V**	**90**	**108**		**dB**
Power-Supply Rejection	**PSRR**		**90**	**108**		**dB**
Input Bias Current	I_{IN-}			3		μA
OUTPUT						
Gain	G					
INA216A1				25		V/V
INA216A2				50		V/V
INA216A3				100		V/V
INA216A4				200		V/V
Gain Error						
INA216A1		V_{OUT} = 0.2V to V_{OUT} = 2.5V		±0.01	±0.2	%
vs Temperature		**V_{OUT} = 0.2V to V_{OUT} = 2.5V**		**0.01**	**0.025**	**m%/°C**
INA216A2				0.05	±0.2	%
vs Temperature				**0.017**	**0.1**	**m%/°C**
INA216A3				0.06	±0.2	%
vs Temperature				**0.023**	**0.1**	**m%/°C**
INA216A4				0.03	±0.2	%
vs Temperature				**0.076**	**0.3**	**m%/°C**
Nonlinearity Error				±0.01		%
Maximum Capacitive Load		No sustained oscillation		750		pF
VOLTAGE OUTPUT(3)		**R_L = 10kΩ to GND**				
Swing to V+ Power-Supply Rail				**(V+) –0.1**	**(V+) –0.3**	**V**
Swing to GND(3)				**(V_{GND}) +0.001**	**(V_{GND}) +0.002**	**V**
Output Impedance				42		Ω
FREQUENCY RESPONSE						
Bandwidth	BW	C_{LOAD} = 10pF				
INA216A1				20		kHz
INA216A2				10		kHz
INA216A3				5		kHz
INA216A4				2.5		kHz

(1) RTI: Referred-to-input.
(2) CMRR and PSRR are the same because V_{CM} is the supply voltage.
(3) See Typical Characteristics graph, *Output Swing to Rail* (Figure 9).

ELECTRICAL CHARACTERISTICS (continued)

Boldface limits apply over the specified temperature range, **T_A = –40°C to +125°C.**
At T_A = +25°C and V_{CM} = V_{IN+}= 4.2V, unless otherwise noted.

PARAMETER		CONDITIONS	INA216			UNIT
			MIN	TYP	MAX	
FREQUENCY RESPONSE, *continued*						
Slew Rate	SR			0.03		V/µs
NOISE, RTI [4]						
Voltage Noise Density				60		nV/√Hz
POWER SUPPLY						
Specified Range	**V_{IN+}**		**+1.8**		**+5.5**	**V**
Quiescent Current	I_Q			13	25	µA
Over Temperature					**30**	**µA**
TURN-ON TIME		V_{IN+} = 0 to +2.5V; V_{SENSE} = 10mV; V_{OUT} ±0.5%		200		µs
TEMPERATURE RANGE						
Specified Temperature Range			–40		+125	°C

(4) RTI: Referred-to-input.

TYPICAL CHARACTERISTICS

The INA216A1 is used for typical characteristic measurements at $T_A = +25°C$, $V_S = +4.2V$, unless otherwise noted.

INPUT OFFSET VOLTAGE PRODUCTION DISTRIBUTION

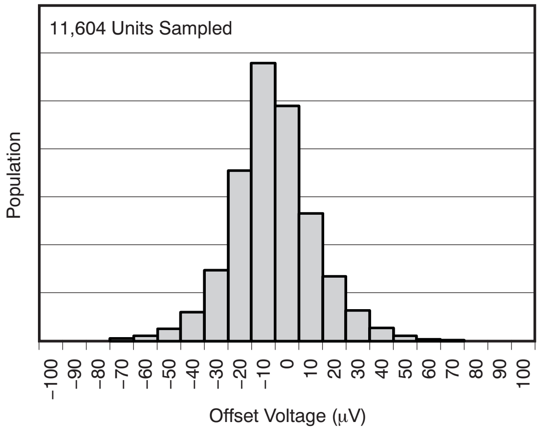


Figure 1.

OFFSET VOLTAGE vs TEMPERATURE

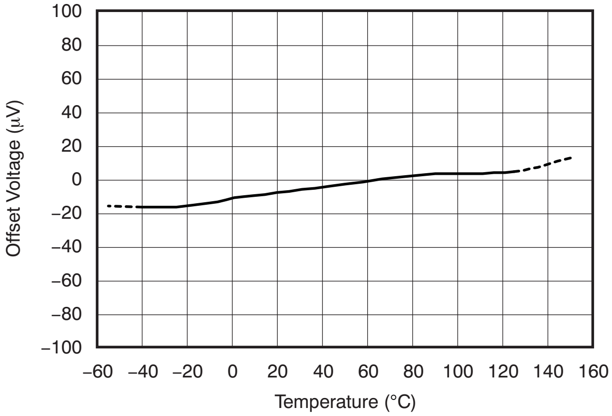


Figure 2.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

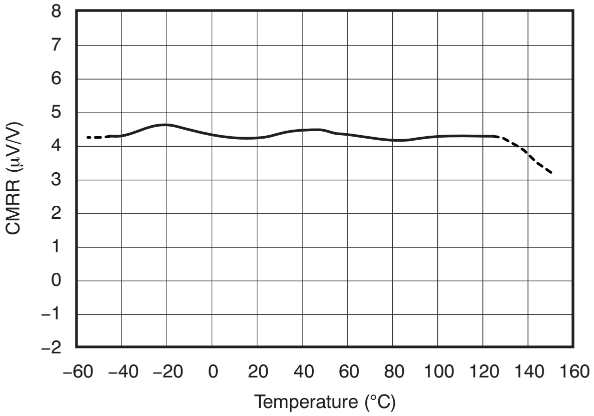


Figure 3.

GAIN ERROR vs TEMPERATURE

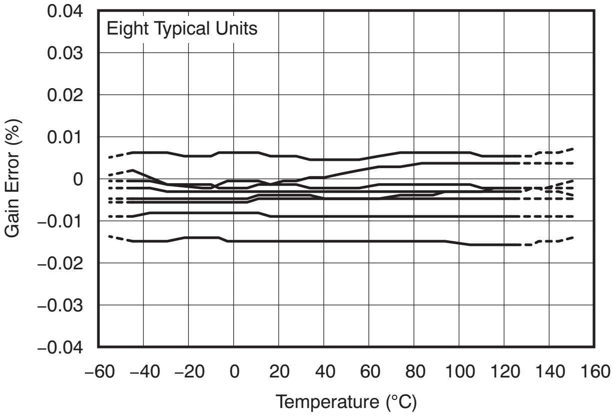


Figure 4.

QUIESCENT CURRENT AND NEGATIVE INPUT BIAS CURRENT vs TEMPERATURE

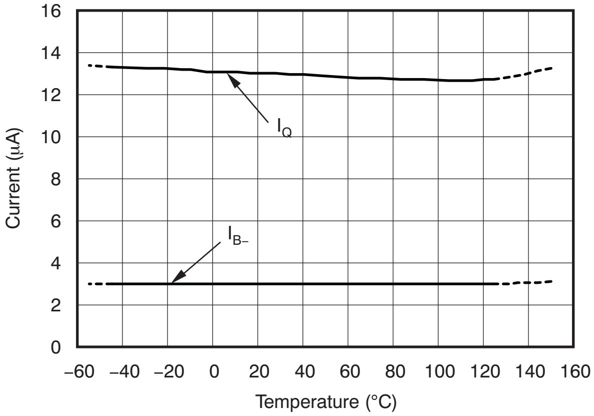


Figure 5.

GAIN vs FREQUENCY

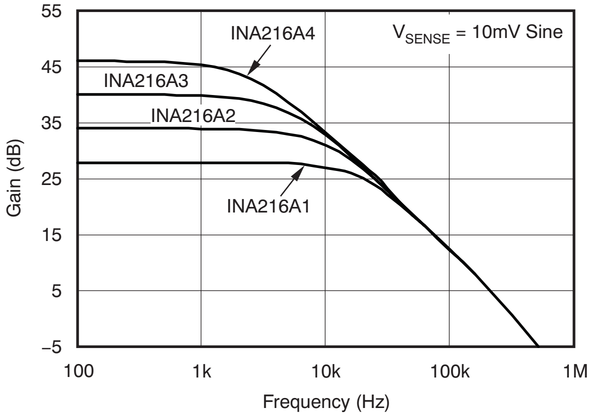


Figure 6.

TYPICAL CHARACTERISTICS (continued)

The INA216A1 is used for typical characteristic measurements at $T_A = +25°C$, $V_S = +4.2V$, unless otherwise noted.

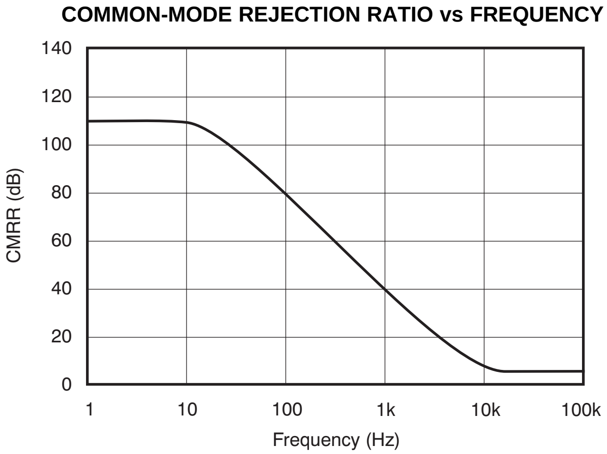

COMMON-MODE REJECTION RATIO vs FREQUENCY

Figure 7.

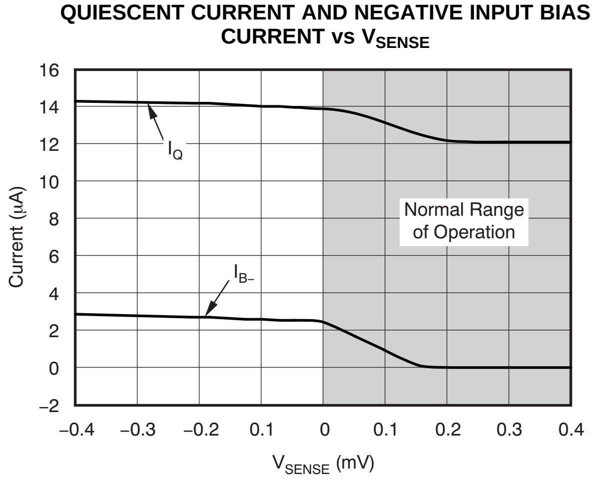

QUIESCENT CURRENT AND NEGATIVE INPUT BIAS CURRENT vs V_{SENSE}

Figure 8.

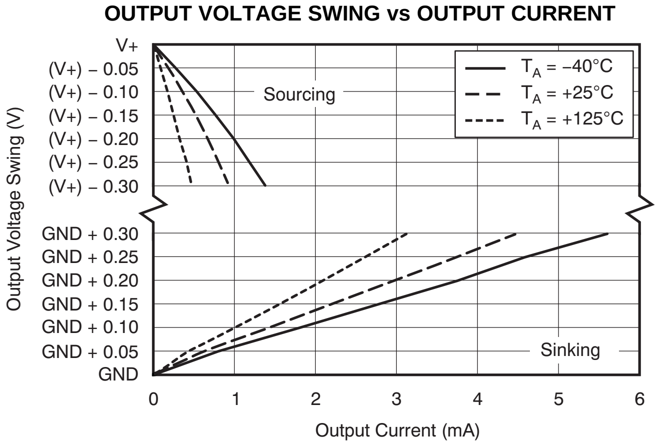

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

Figure 9.

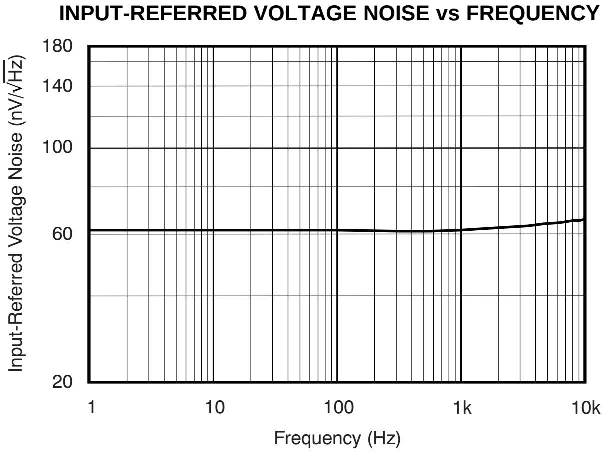

INPUT-REFERRED VOLTAGE NOISE vs FREQUENCY

Figure 10.

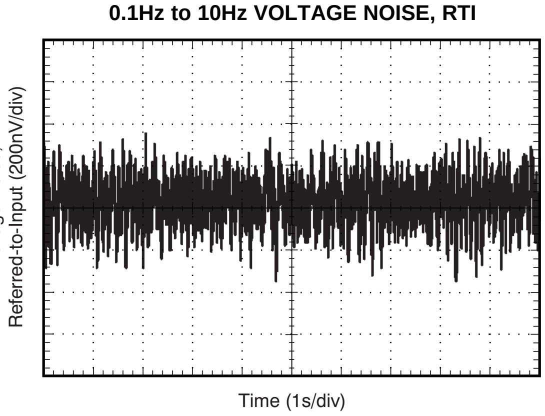

0.1Hz to 10Hz VOLTAGE NOISE, RTI

Figure 11.

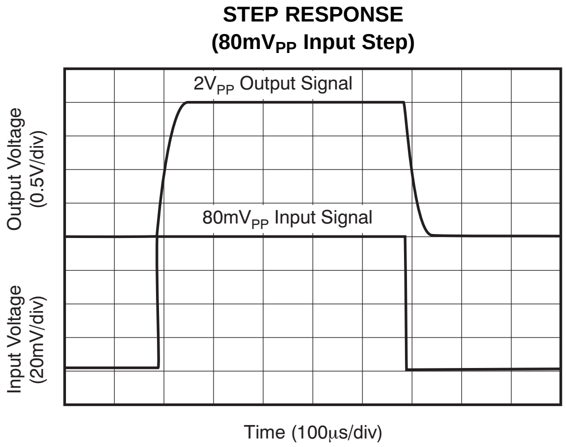

STEP RESPONSE ($80mV_{PP}$ Input Step)

Figure 12.

TYPICAL CHARACTERISTICS (continued)

The INA216A1 is used for typical characteristic measurements at T_A = +25°C, V_S = +4.2V, unless otherwise noted.

COMMON-MODE VOLTAGE TRANSIENT RESPONSE

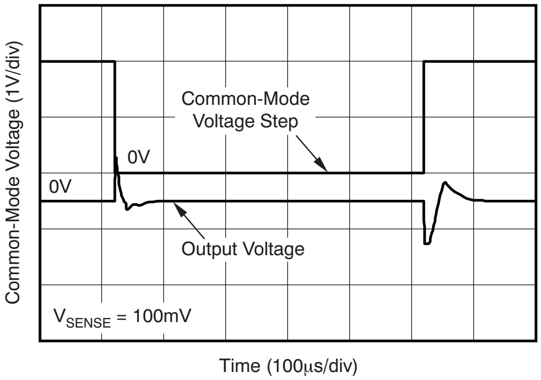


Figure 13.

INVERTING DIFFERENTIAL INPUT OVERLOAD

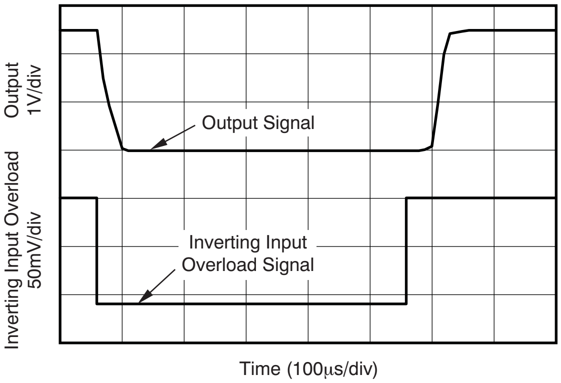


Figure 14.

NONINVERTING DIFFERENTIAL INPUT OVERLOAD

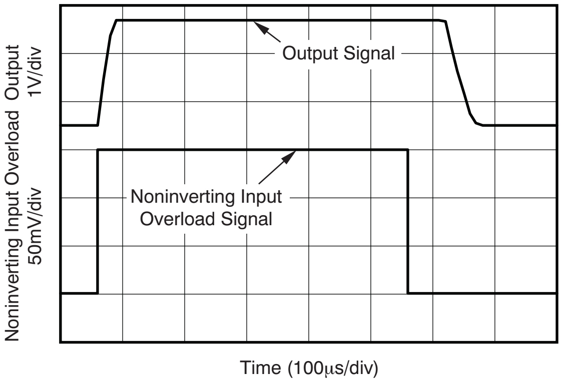


Figure 15.

STARTUP RESPONSE

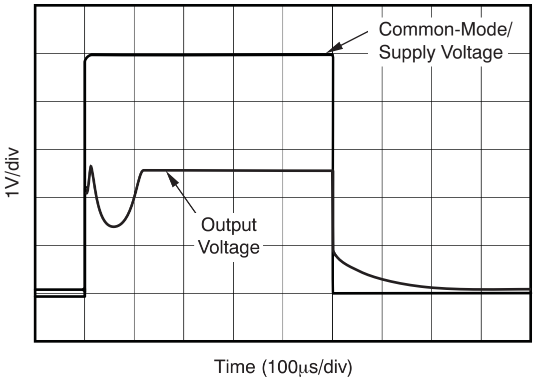


Figure 16.

BROWNOUT RECOVERY

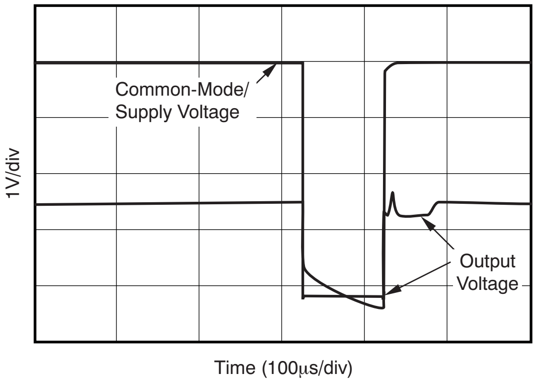


Figure 17.

APPLICATION INFORMATION

Basic Connections

Figure 18 shows the basic connections of the INA216. The input pins, IN+ and IN–, should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

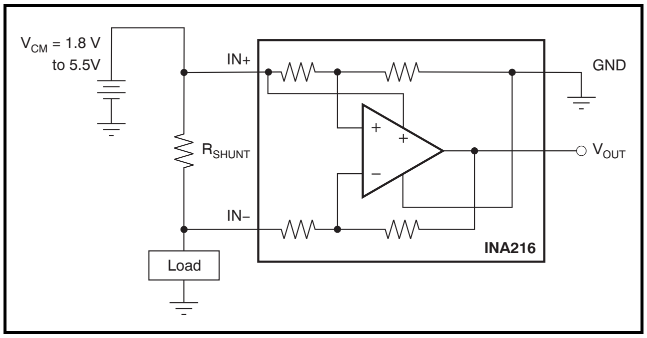


Figure 18. Typical Application

Figure 19 illustrates the INA216 connected to a shunt resistor with additional trace resistance in series with the shunt placed between where the current shunt monitors the input pins. With the typically low shunt resistor values commonly used in these applications, even small amounts of additional impedance in series with the shunt resistor can significantly affect the differential voltage present at the INA216 input pins.

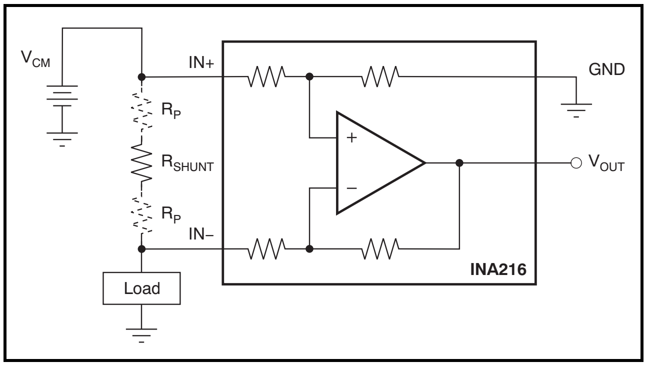


Figure 19. Shunt Resistance Measurement Including Trace Resistance, R_P

Figure 20 shows a proper Kelvin, or four-wire, connection of the shunt resistor to the INA216 input pins. This connection helps ensure that the only impedance between the current monitor input pins is the shunt resistor.

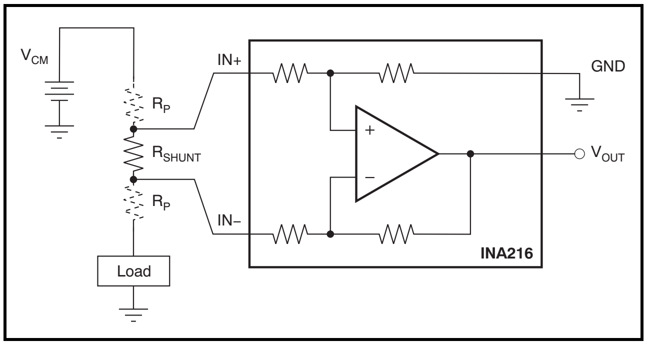


Figure 20. Shunt Resistance Measurement Using a Kelvin Connection

Power Supply

The INA216 does not have a dedicated power-supply pin. Instead, an internal connection to the IN+ pin serves as the power supply for this device. Because the INA216 is powered from the IN+ pin, the common-mode input range is limited on the low end to 1.8V. Therefore, the INA216 cannot be used as a low-side current shunt monitor.

Selecting R_S

The selection of the value of the shunt resistor (R_S) to use with the INA216 is based on the specific operating conditions and requirements of the application. The starting point for selecting the resistor is to first determine the desired full-scale output from the INA216. The INA216 is available in four gain options: 25, 50, 100, and 200. By dividing the desired full-scale output by each of the gain options, there are then four available differential input voltages that can achieve the desired full-scale output voltage, given that the appropriate gain device is used. With four values for the total voltage that is to be dropped across the shunt, the decision on how much of a drop is allowed in the application must be made. Most applications have a maximum drop allowed to ensure that the load receives the required voltage necessary to operate. Assuming that there are now multiple shunt voltages that are acceptable (based on the design criteria), the choice of what value shunt resistor to use can be made based on accuracy. As a result of the INA216 auto-zero architecture, the input offset voltage is extremely low. However, even the 100µV maximum input offset voltage specification plays a role in the decision of which shunt resistor value to choose. With a larger shunt voltage present at the current shunt monitor input, less error is introduced by the input offset voltage.

These comments have framed the decision on what the shunt resistor value should be, based on the full-scale value; but many applications require accurate measurements at levels as low as 10% of the full-scale value. At this level, the input offset voltage of the current shunt monitor becomes a larger percentage of the shunt voltage, and thus contributes a larger error to the output. The percentage of error created by the input offset voltage relative to the shunt voltage is shown in Equation 1.

$$\text{Error\_V}_{OS} = \frac{V_{OS}}{V_{SENSE}} \bullet 100 \tag{1}$$

Ideally, the differential input voltage at 10% would be increased to minimize the effects of the input offset voltage; however, we are bound by the full-scale value. The full-scale output voltage on the INA216 is limited to 200mV below the supply voltage (IN+). Selecting a shunt resistor to increase the shunt voltage at the low operating range of the load current could easily saturate the output of the current shunt monitor at the full-scale load current. For applications where accuracy over a larger range is needed, a lower gain option (and therefore, a larger differential input voltage) is selected. For applications where a minimal voltage drop on the line that powers the load is required, a higher gain option (and so, a smaller differential input voltage) is selected.

For example, consider a design that requires a full-scale output voltage of 4V, a maximum load current of 10A, and a maximum voltage drop on the common-mode line of 25mV. The 25mV maximum voltage drop requirement and a 4V full-scale output limits the gain option to the 200V/V device. A 100V/V setting would require a maximum voltage drop of 40mV with the other two lower gain versions creating larger voltage drops. Based on the gain of 200 on a 4V full-scale output, the maximum differential input voltage would be 20mV. The shunt resistor needed to create a 20mV drop with a 10A load current is 2mΩ.

When choosing the proper shunt resistor, it is also important to consider that at higher currents, the power dissipation in the shunt resistor becomes greater. Therefore, it is important to evaluate the drift of the sense resistor as a result of power dissipation, and choose an appropriate resistor based on its power wattage rating.

Calculating Total Error

The electrical specifications for the INA216 include the typical individual errors terms such as gain error, offset error, and nonlinearity error. Total error including all of these individual error components is not specified in the *Electrical Characteristics* table. To accurately calculate the error that can be expected from the device, we must first know the operating conditions to which the device is subjected. Some current shunt monitors specify a total error in the product data sheet. However, this total error term is accurate under only one particular set of operating conditions. Specifying the total error at this one point has little practical value, though, because any deviation from these specific operating conditions no longer yields the same total error value. This section discusses the individual error sources, with information on how to apply them in order to calculate the total error value for the device under normal operating conditions.

The typical error sources that have the largest impact on the total error of the device are input offset voltage, common-mode voltage rejection, gain error, and nonlinearity error.

The nonlinearity error of the INA216 is relatively low compared to the gain error specification, which results in a gain error that can be expected to be relatively constant throughout the linear input range of the device. While the gain error remains constant across the linear input range of the device, the error associated with the input offset voltage does not. As the differential input voltage developed across a shunt resistor at the input of the INA216 decreases, the inherent input offset voltage of the device becomes a larger percentage of the measured input signal, resulting in an increase in measurement error. This varying error is present among all current shunt monitors, given the input offset voltage ratio to the voltage being sensed by the device. The low input offset voltages present in the INA216 devices, however, limit the amount of contribution the offset voltage has on the total error term.

Two examples are provided that detail how different operating conditions can affect the total error calculations. Typical and maximum calculations are shown as well to provide the user more information on how much error variance could be present from device to device.

Example 1

Conditions: INA216A3; $V_{CM} = V_S = 3.3V$; $V_{SENSE} = 20mV$

Table 1. Example 1

TERM	LABEL	EQUATION	TYPICAL	MAXIMUM
Maximum initial input offset voltage	VIO	—	20μV	75μV
Added input offset voltage as result of common-mode voltage	VIO_CM	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \cdot \lvert 4.2V - V_{CM} \rvert$	3.6μV	28μV
Total input offset voltage	VIO_Total	$\sqrt{(VIO)^2 + (VIO\_CM)^2}$	20μV	80μV
Error because of input offset voltage	Error_VIO	$\frac{VIO\_Total}{V_{SENSE}} \cdot 100$	0.1%	0.4%
Gain error	Error_Gain	—	0.06%	0.2%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
Total error		$\sqrt{(Error\_VIO)^2 + (Error\_Gain)^2 + (Error\_Lin)^2}$	0.12%	0.45%

Example 2

Conditions: INA216A1; $V_{CM} = V_S = 5V$; $V_{SENSE} = 160mV$

Table 2. Example 2

TERM	LABEL	EQUATION	TYPICAL	MAXIMUM
Maximum initial input offset voltage	VIO	—	30μV	100μV
Added input offset voltage as result of common-mode voltage	VIO_CM	$\frac{1}{10^{\left(\frac{CMRR\_dB}{20}\right)}} \cdot \lvert 4.2V - V_{CM} \rvert$	3.1μV	25.2μV
Total input offset voltage	VIO_Total	$\sqrt{(VIO)^2 + (VIO\_CM)^2}$	30μV	100μV
Error because of input offset voltage	Error_VIO	$\frac{VIO\_Total}{V_{SENSE}} \cdot 100$	0.02%	0.06%
Gain error	Error_Gain	—	0.01%	0.2%
Nonlinearity error	Error_Lin	—	0.01%	0.01%
Total error		$\sqrt{(Error\_VIO)^2 + (Error\_Gain)^2 + (Error\_Lin)^2}$	0.025%	0.21%

Input Filtering

An ideal location where filtering is implemented is at the inputs for a device. Placing an input filter in front of the INA216, though, is not recommended but can be implemented if it is determined to be necessary. This location is not recommended for filtering because adding input filters induces an additional gain error to the device that can easily exceed the device maximum gain error specification of 0.2%. In the INA216, the nominal current into the IN+ pin is in the range of 13µA while the bias current into the IN– pin is in the range of approximately 3µA. The current flowing into the IN+ pin includes both the input bias current as well as the quiescent current. Where the issue of input filtering begins to become more of an issue is that as the quiescent current of the INA216 also flows through the IN+ pin, when the output begins to drive current, this additional current also flows through the IN+ pin, creating an even larger error.

Placing a typical common-mode filter of 10Ω in series with each input and a 0.1µF capacitor across the input pins, as shown in Figure 21, introduces an additional gain error into the system. For example, consider an application using the INA216A3 with a full-scale output of 4V, assuming that the device is not driving any output current. The shunt voltage needed to create the 4V output with a gain of 100 is 40mV. With 10Ω filter resistors on each input, there is a difference voltage created that subtracts from the 40mV full-scale differential current. The error can be calculated using Equation 2.

$$\text{Error\_R}_{\text{FILTER}} = \frac{(I_{IN+} - I_{IN-}) \bullet R_{\text{FILTER}}}{V_{\text{SHUNT}}} \bullet 100 \qquad (2)$$

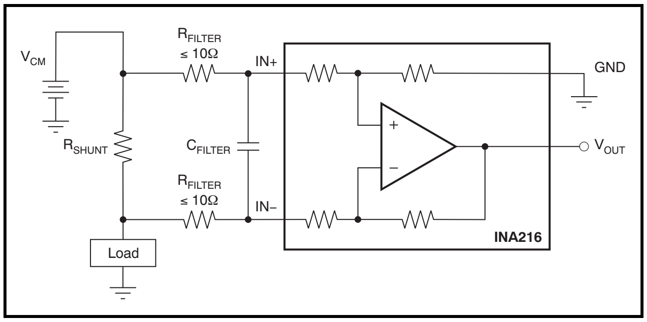


Figure 21. Input Filter

As mentioned previously, the current flowing into the IN+ pin increases once the output begins to drive current because of the quiescent current also flowing into the IN+ pin. The previous example resulted in an additional gain error of 0.3% as a result of the 10Ω filter resistors (assuming the output stage was not driving any current). Connecting a 100kΩ load to the 4V output now increases the current by an additional 40µA. This increase in current flowing through the IN+ pin would change the additional gain error from 0.3% to 1.3%.

If filtering is required for the application and the gain error introduced by the input filter resistors exceeds the available error budget for this circuit, a filter can be implemented following the INA216. Placing a filter at the output of the current shunt monitor is not typically the ideal location because the benefit of the low impedance output of the amplifier is lost. Applications that require the low impedance output require an additional buffer amplifier that follows the post current shunt monitor filter.

Using the INA216 With Transients Above 5.5V

With a small amount of additional circuitry, INA216 can be used in circuits subject to transients higher than 5.5V. Use only zener diode or zener-type transient absorbers, which are sometimes referred to as *Transzorbs*. Any other type of transient absorber has an unacceptable time delay. To use these protection devices, resistors are required in series with the INA216 inputs, as shown in Figure 22. These resistors serve as a working impedance for the zener. It is desirable to keep these resistors as small as possible because of the error described in the *Input Filtering* section. These protection resistors are most often around 10Ω. Larger values can be used with a greater impact to the total gain error. Because this circuit limits only short-term transients, many applications are satisfied with a 10Ω resistor along with conventional zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523. The use of these protection components may allow the INA216 to survive from being damaged in environments where large transients are common.

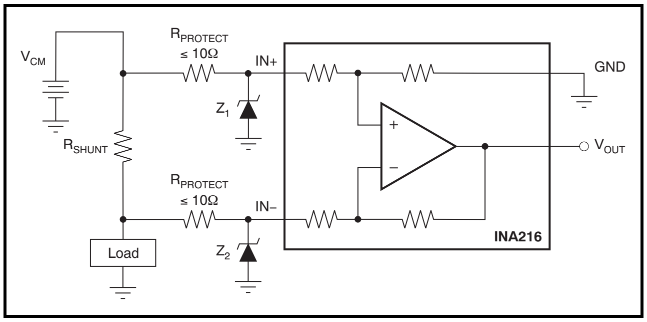


Figure 22. Transient Protection Using Dual Zener Diodes

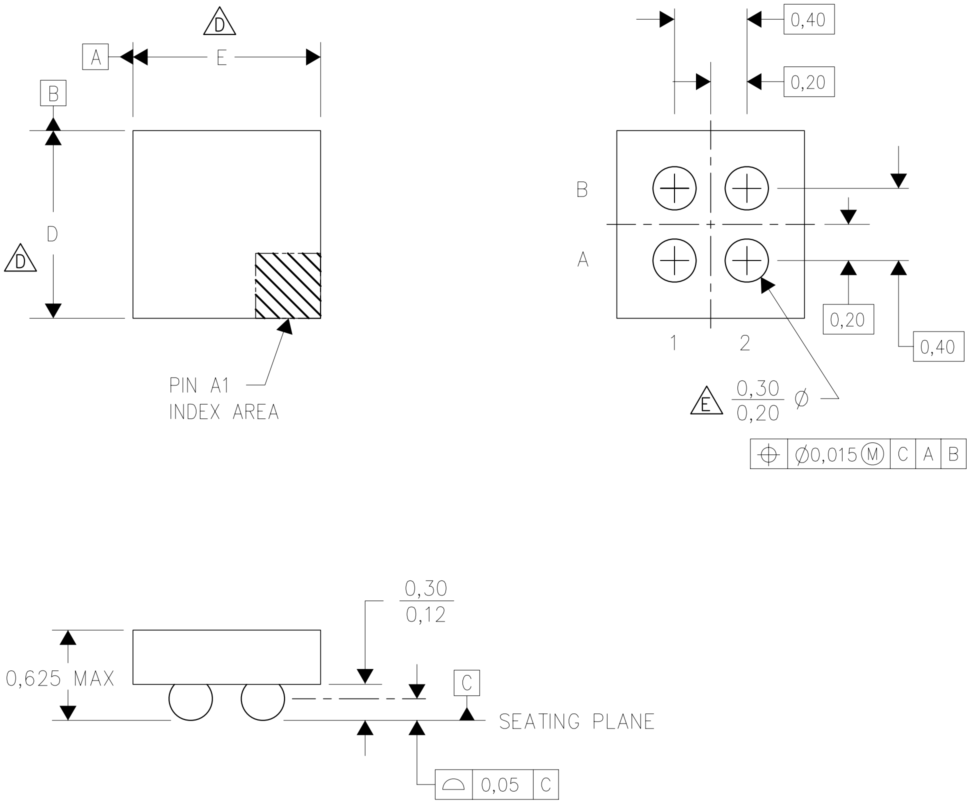
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June, 2010) to Revision B	**Page**
• Removed product preview status of INA216A2, INA216A3, and INA216A4 devices	2
• Added offset voltage specifications for INA216A2, INA216A3, and INA216A4	4
• Added gain and gain error specifications for INA216A2, INA216A3, and INA216A4	4
• Added bandwidth specifications for INA216A2, INA216A3, and INA216A4	4
• Updated graph grid for Figure 2 through Figure 5	6
• Revised Table 1 and Table 2	11
• Changed description of nominal current into IN+ pin to 13μA and bias current into IN– pin to 3μA	12

Changes from Original (June, 2010) to Revision A	**Page**
• Changed *offset voltage vs temperature* specification	4
• Changed *gain error vs temperature* specification and units	4

YFF (S-XBGA-N4) DIE-SIZE BALL GRID ARRAY



D: Max = 790 µm, Min = 730 µm

E: Max = 790 µm, Min = 730 µm

4207625-2/Y 05/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M—1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Devices in YFF package can have dimensions D ranging from 0.76 to 1.45 mm and dimension E ranging from 0.76 to 1.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
- F. This package contains Pb—free balls.

NanoFree is a trademark of Texas Instruments.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
INA216A1YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
INA216A1YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples
INA216A2YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples
INA216A2YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
INA216A3YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples
INA216A3YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
INA216A4YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
INA216A4YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples

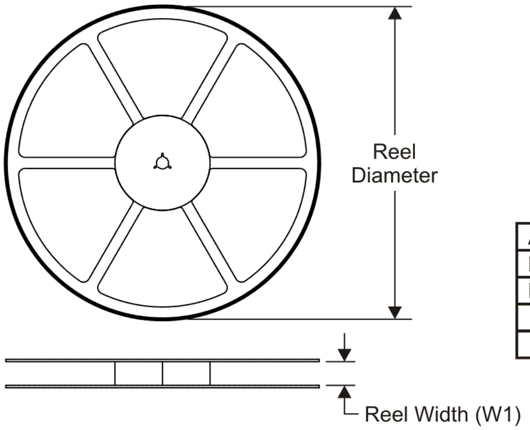
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

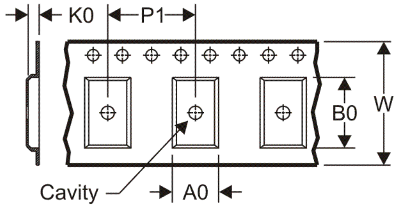
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

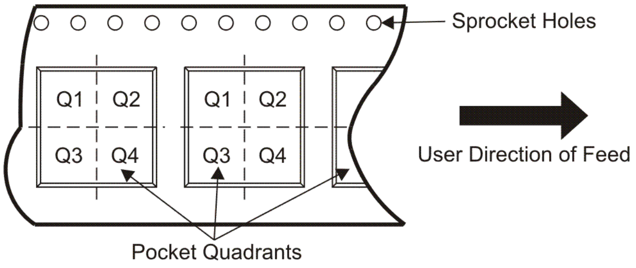


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

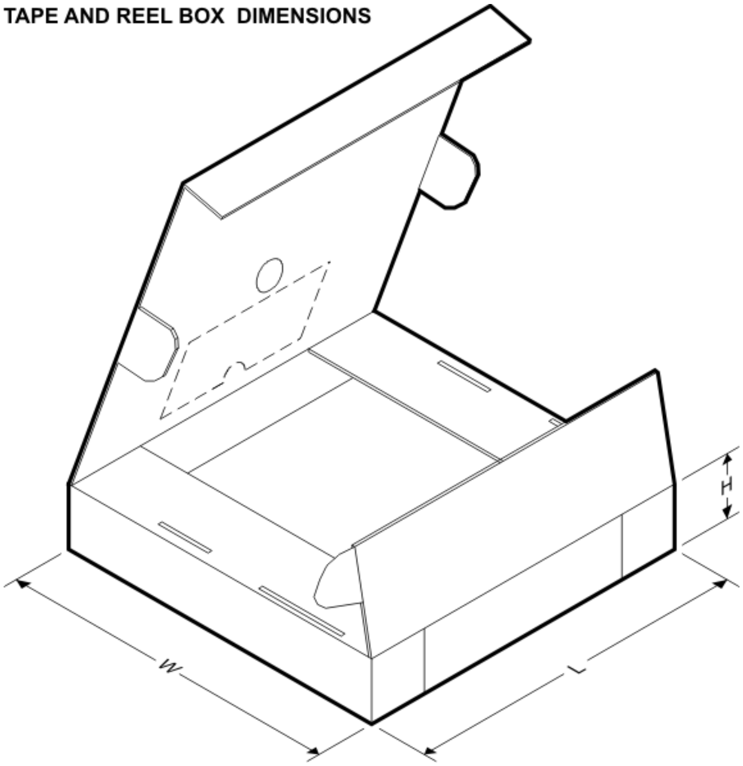
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA216A1YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	0.89	0.58	4.0	8.0	Q1
INA216A1YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	0.89	0.58	4.0	8.0	Q1
INA216A2YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
INA216A2YFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
INA216A3YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
INA216A3YFFT	DSBGA	YFF	4	250	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1
INA216A4YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.85	0.85	0.64	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA216A1YFFR	DSBGA	YFF	4	3000	190.5	212.7	31.8
INA216A1YFFT	DSBGA	YFF	4	250	190.5	212.7	31.8
INA216A2YFFR	DSBGA	YFF	4	3000	190.5	212.7	31.8
INA216A2YFFT	DSBGA	YFF	4	250	190.5	212.7	31.8
INA216A3YFFR	DSBGA	YFF	4	3000	190.5	212.7	31.8
INA216A3YFFT	DSBGA	YFF	4	250	190.5	212.7	31.8
INA216A4YFFR	DSBGA	YFF	4	3000	190.5	212.7	31.8

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