

NVMFS5C673NL

MOSFET – Power, Single N-Channel

60 V, 9.2 mΩ, 50 A

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C673NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DS}	60	V
Gate-to-Source Voltage			V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	50	A
		$T_C = 100^\circ\text{C}$		35	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D	46	W
		$T_C = 100^\circ\text{C}$		23	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	14	A
		$T_A = 100^\circ\text{C}$		10	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	3.6	W
		$T_A = 100^\circ\text{C}$		1.8	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM}	290	A	
Operating Junction and Storage Temperature			T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)			I_S	52	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 2.3 \text{ A}$)			E_{AS}	88	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	3.2	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	42	

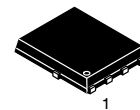
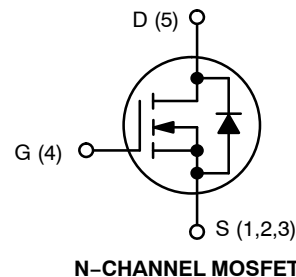
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



ON Semiconductor®

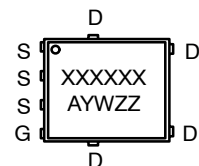
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	9.2 mΩ @ 10 V	50 A
	13 mΩ @ 4.5 V	



DFN5
(SO-8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



XXXXXX = 5C673L
(NVMFS5C673NL) or
673LWF
(NVMFS5C673NLWF)

A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFS5C673NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			28		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 60 V	T _J = 25°C		10	μA
			T _J = 125°C		250	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 35 μA	1.2		2.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-4.5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 25 A		7.7	9.2	mΩ
		V _{GS} = 4.5 V, I _D = 25 A		11	13	
Forward Transconductance	g _{FS}	V _{DS} = 15 V, I _D = 25 A		37		S

CHARGES AND CAPACITANCES

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		880		pF
Output Capacitance	C _{OSS}			450		
Reverse Transfer Capacitance	C _{RSS}			11		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 25 A		4.5		nC
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 48 V; I _D = 25 A		9.5		nC
Threshold Gate Charge	Q _{G(TH)}	V _{GS} = 10 V, V _{DS} = 48 V; I _D = 25 A		1.0		nC
Gate-to-Source Charge	Q _{GS}			2.0		
Gate-to-Drain Charge	Q _{GD}			0.8		
Plateau Voltage	V _{GP}			2.9		

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DS} = 48 V, I _D = 25 A, R _G = 2.5 Ω		6.0		ns
Rise Time	t _r			25		
Turn-Off Delay Time	t _{d(OFF)}			16		
Fall Time	t _f			2.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 25 A	T _J = 25°C		0.9	1.2	V
			T _J = 125°C		0.8		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 25 A		28		ns	
Charge Time	t _a			14			
Discharge Time	t _b			14			
Reverse Recovery Charge	Q _{RR}			18		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

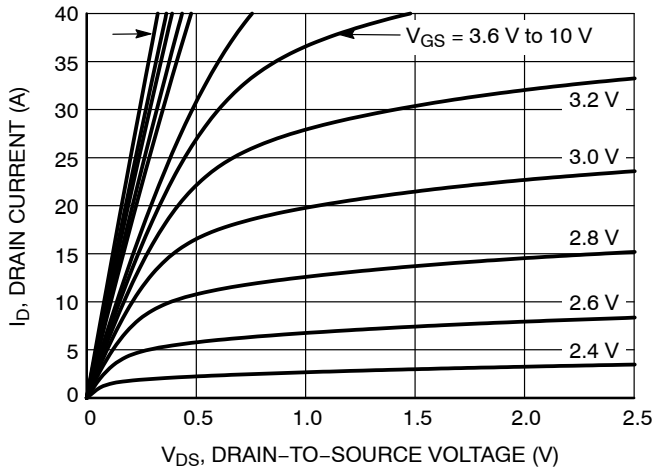


Figure 1. On-Region Characteristics

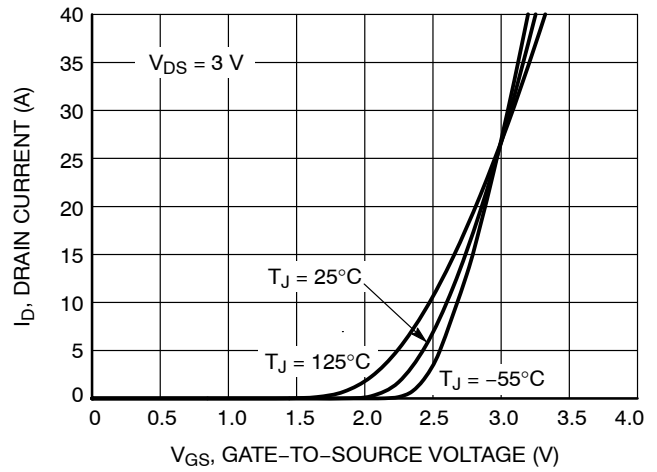


Figure 2. Transfer Characteristics

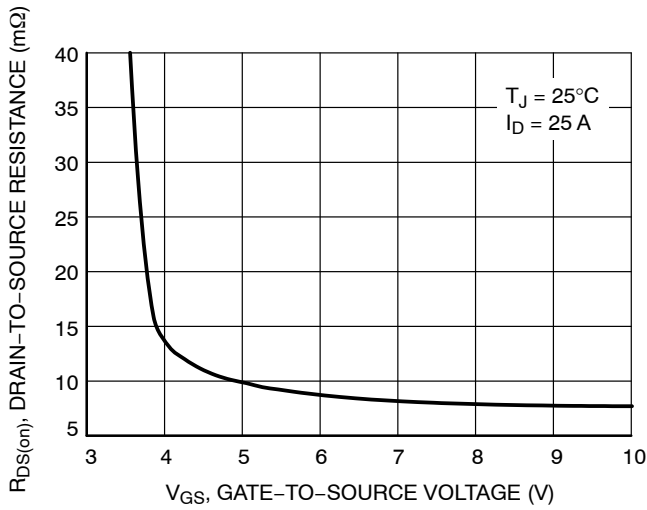


Figure 3. On-Resistance vs. Gate-to-Source Voltage

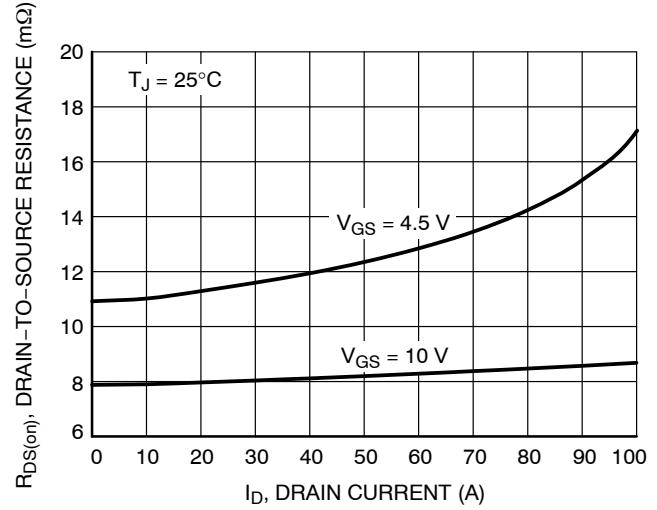


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

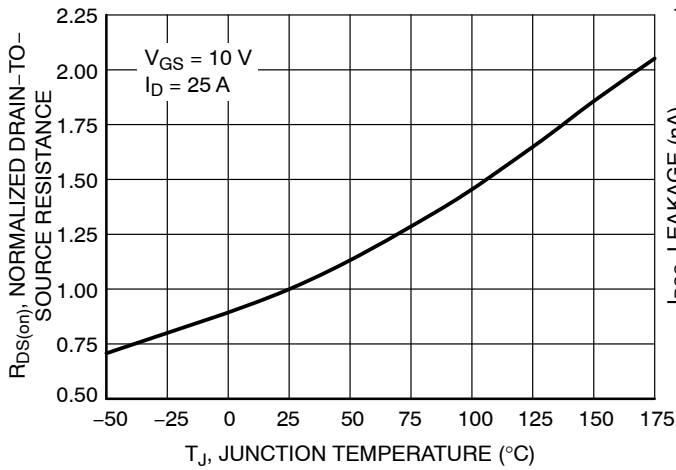


Figure 5. On-Resistance Variation with Temperature

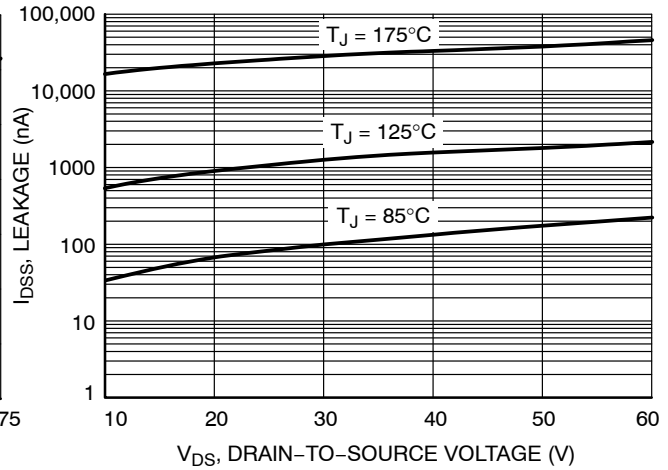


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

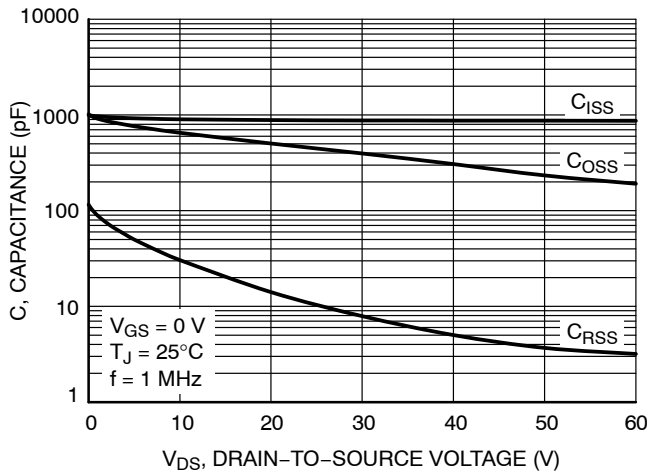


Figure 7. Capacitance Variation

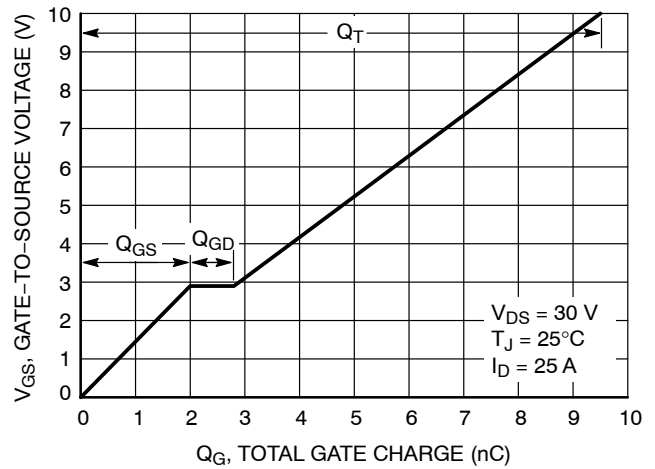


Figure 8. Gate-to-Source vs. Total Charge

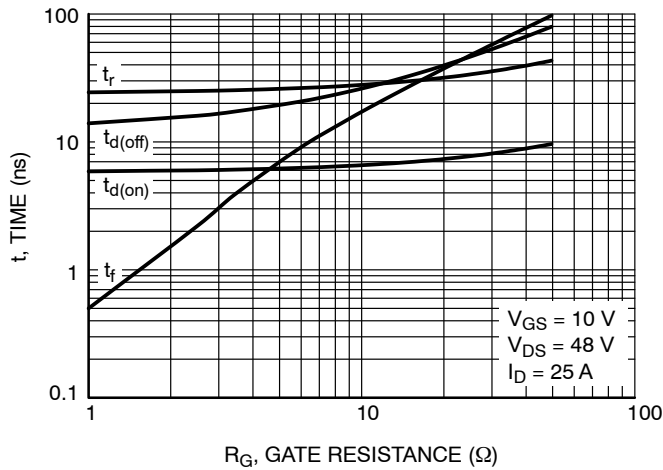


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

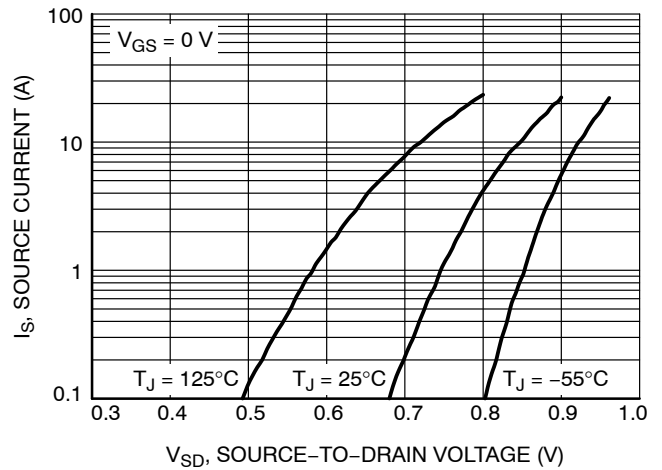


Figure 10. Diode Forward Voltage vs. Current

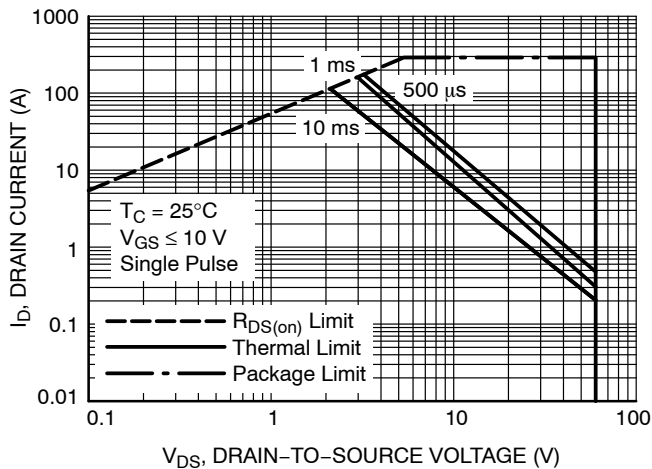


Figure 11. Maximum Rated Forward Biased Safe Operating Area

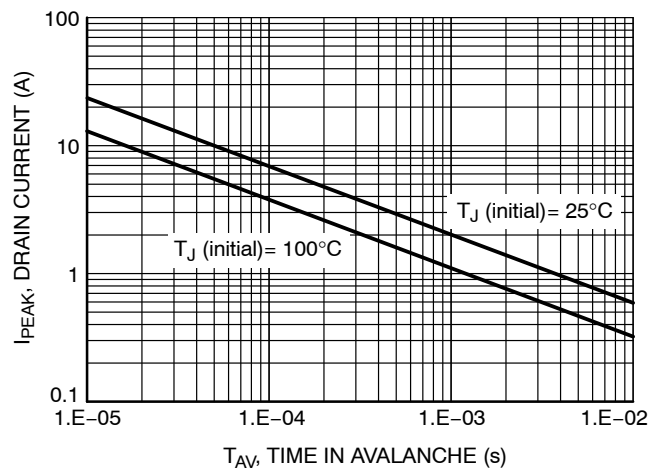


Figure 12. Maximum Drain Current vs. Time in Avalanche

NVMFS5C673NL

TYPICAL CHARACTERISTICS

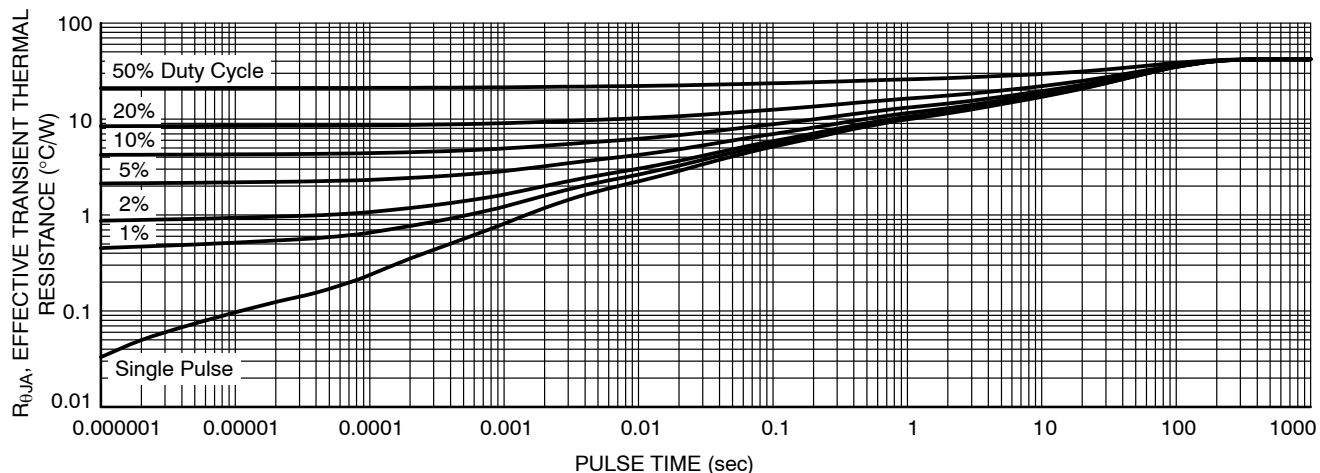


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C673NLT1G	5C673L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C673NLWFT1G	673LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C673NLT3G	5C673L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C673NLWFT3G	673LWF	DFN5 (Pb-Free, Wettable Flanks)	5000 / Tape & Reel
NVMFS5C673NLAFT1G	5C673L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C673NLWFAFT1G	673LWF	DFN5 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVMFS5C673NL

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE M

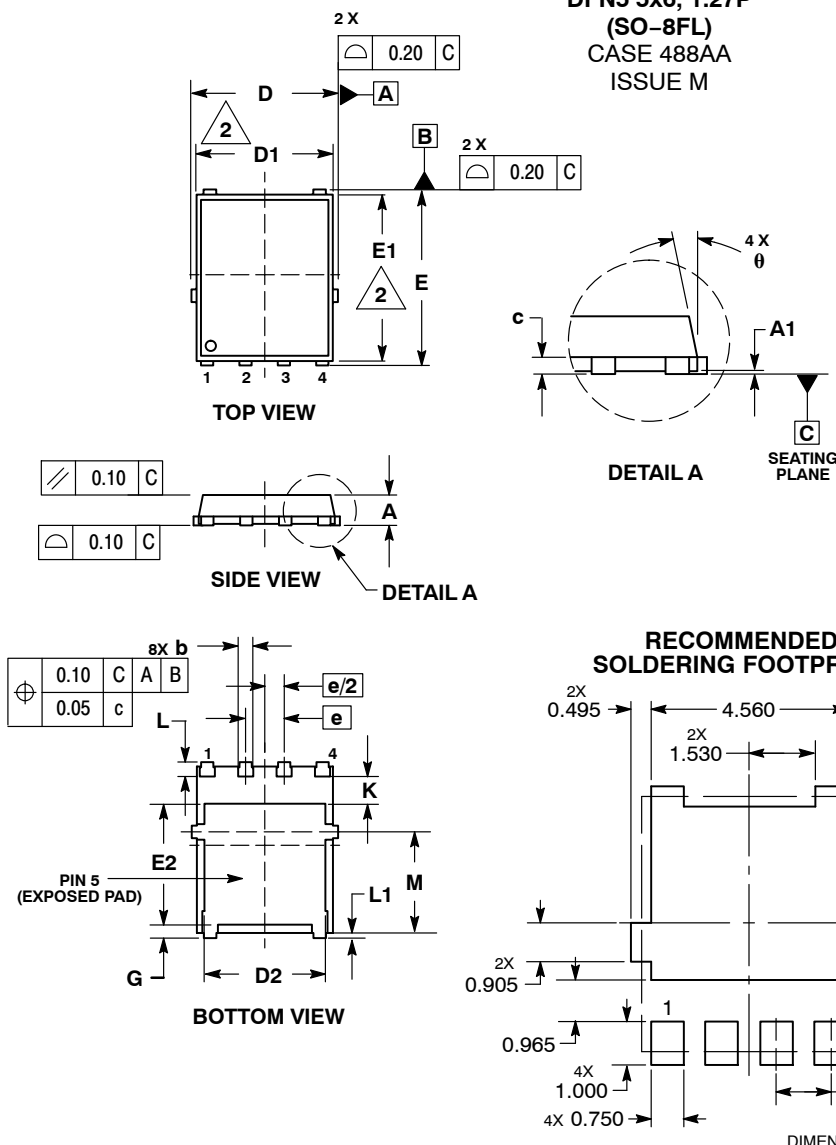
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

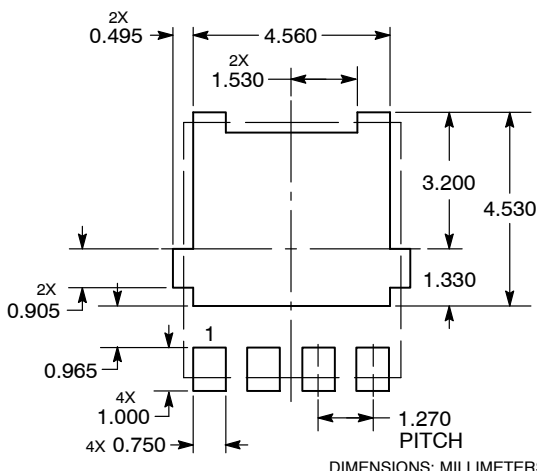
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

STYLE 1:

- PIN 1. SOURCE
- SOURCE
- SOURCE
- GATE
- DRAIN



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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