

Automotive-grade N-channel 30 V, 4.5 mΩ typ., 80 A STripFET™ H5 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

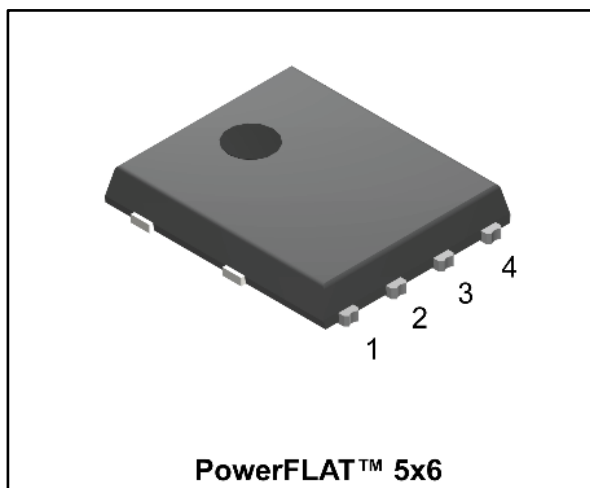
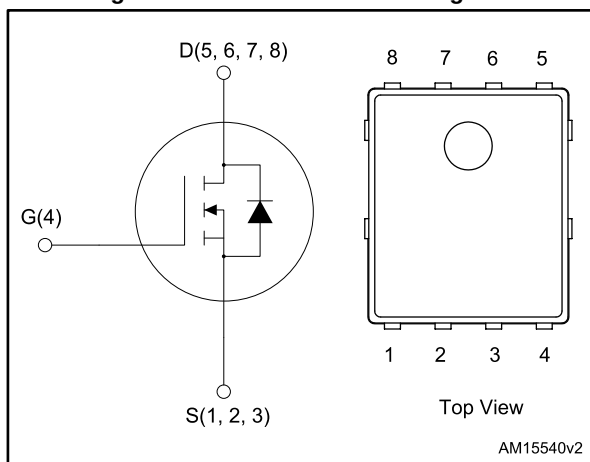


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STL66N3LLH5	30 V	5.8 mΩ	80 A

- AEC-Q101 qualified
- Low on-resistance R_{DS(on)}
- High avalanche ruggedness
- Low gate drive power loss
- Wetable flank package



Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STMicroelectronics' STripFET™ H5 technology. The device has been optimized to achieve very low on-state resistance, contributing to a FoM that is among the best in its class.

Table 1: Device summary

Order code	Marking	Package	Packing
STL66N3LLH5	66N3LLH5	PowerFLAT™ 5x6	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	±22	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	80	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	57	
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ °C}$	21	A
	Drain current (continuous) at $T_{pcb} = 100\text{ °C}$	14.5	
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	84	A
$P_{TOT}^{(1)}$	Total dissipation at $T_{case} = 25\text{ °C}$	72	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ °C}$	4.8	
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

- (1) This value is rated according to R_{thj-c}
 (2) This value is rated according to $R_{thj-pcb}$
 (3) Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

Notes:

- (1) When mounted on a 1-inch² FR-4, 2 Oz copper board, $t < 10\text{ s}$.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AV}	Avalanche current, not repetitive	10.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$, $I_D = I_{AV}$, $V_{DD} = 24\text{ V}$)	180	mJ

2 Electrical characteristics

($T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	30			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 30\text{ V}$, $T_{\text{C}} = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			10	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 22\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		3	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 10.5\text{ A}$		4.5	5.8	m Ω
		$V_{\text{GS}} = 4.5\text{ V}$, $I_{\text{D}} = 10.5\text{ A}$		6	7.5	

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	1500	-	pF
C_{OSS}	Output capacitance		-	295	-	
C_{RSS}	Reverse transfer capacitance		-	39	-	
Q_{g}	Total gate charge	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 21\text{ A}$, $V_{\text{GS}} = 0$ to 4.5 V (see Figure 14: "Test circuit for gate charge behavior")	-	12	-	nC
Q_{gs}	Gate-source charge		-	4	-	
Q_{gd}	Gate-drain charge		-	4.7	-	

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 15\text{ V}$, $I_{\text{D}} = 10.5\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	9.3	-	ns
t_{r}	Rise time		-	14.5	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	22.7	-	
t_{f}	Fall time		-	4.5	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		21	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		84	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 19\text{ A}$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 19\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 25\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see <i>Figure 15: "Test circuit for inductive load switching and diode recovery times")</i>)	-	25		ns
Q_{rr}	Reverse recovery charge		-	17.5		nC
I_{RRM}	Reverse recovery current		-	1.4		A

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

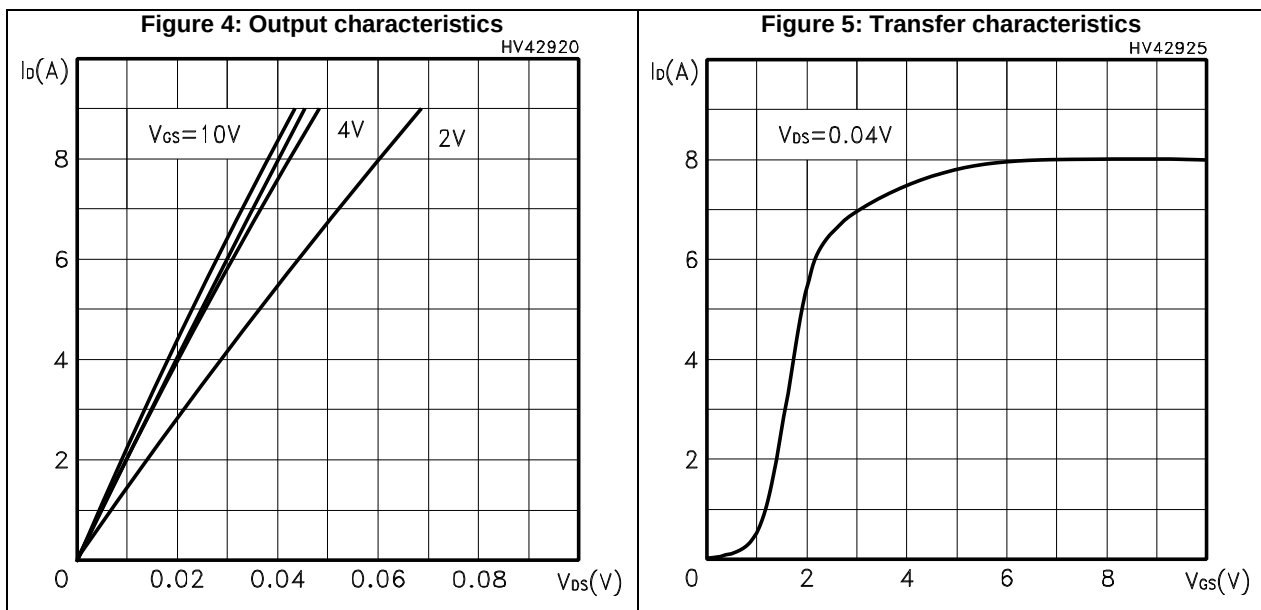
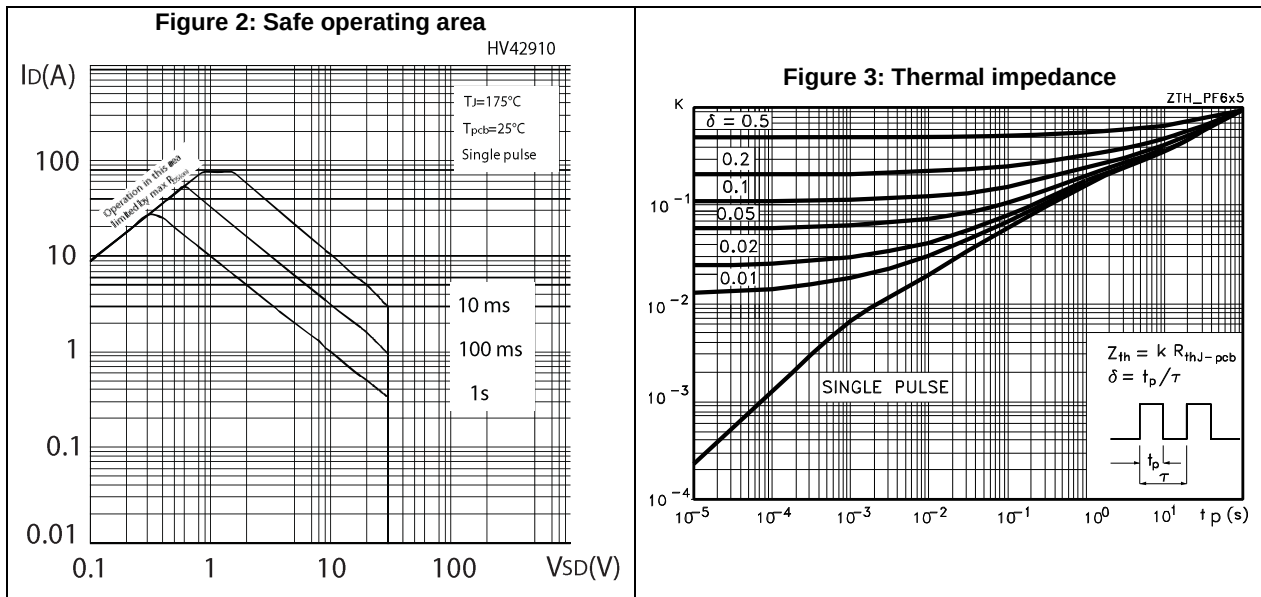


Figure 6: Gate charge vs gate-source voltage

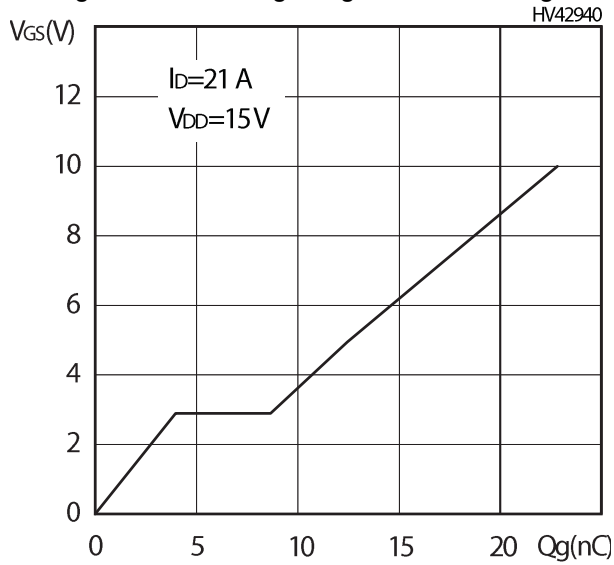


Figure 7: Static drain-source on-resistance

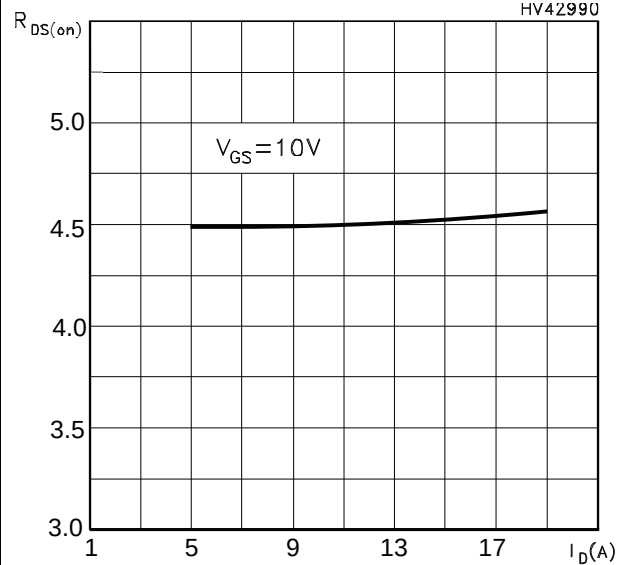


Figure 8: Capacitance variations

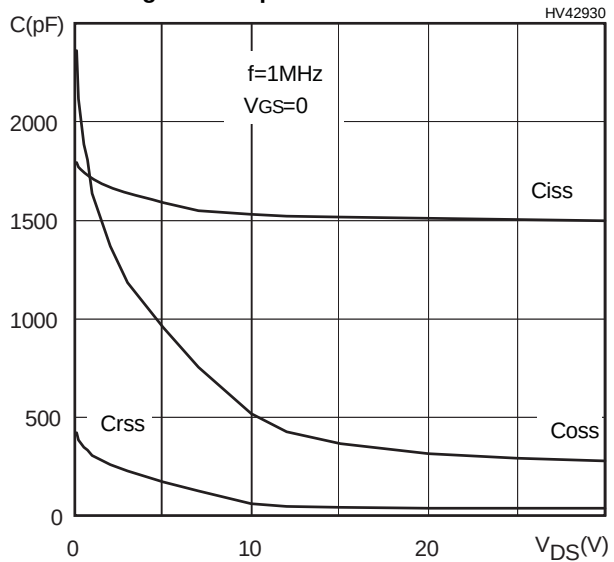


Figure 9: Normalized gate threshold voltage vs temperature

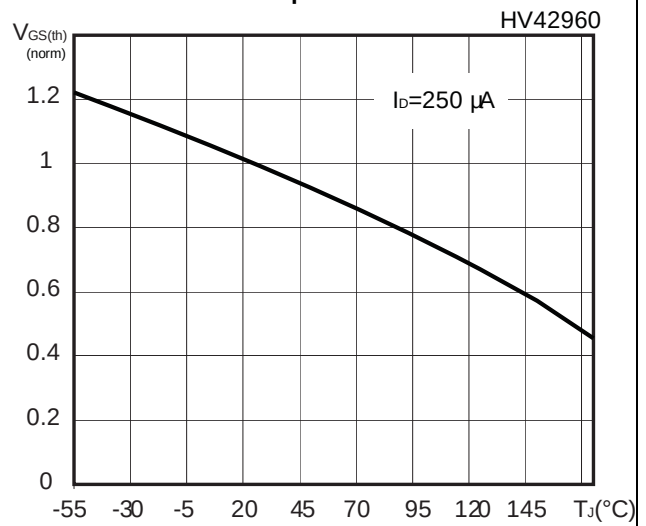


Figure 10: Normalized on-resistance vs temperature

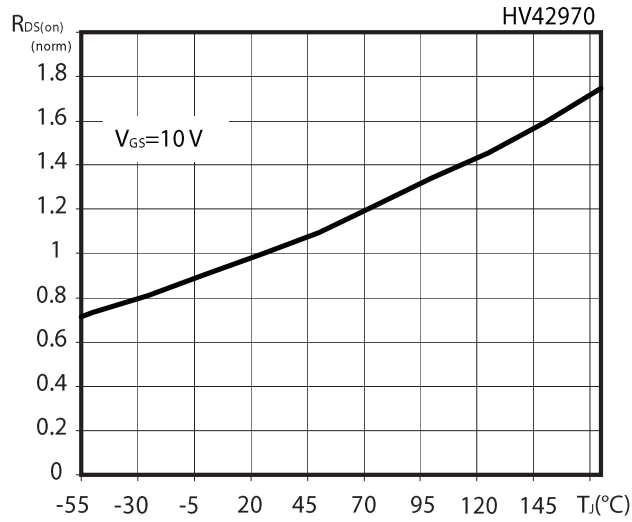
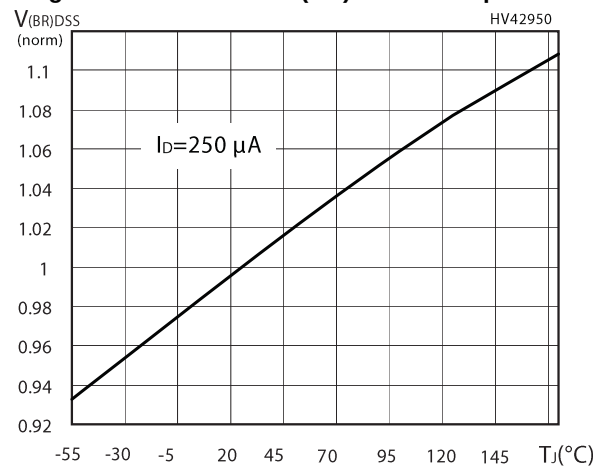
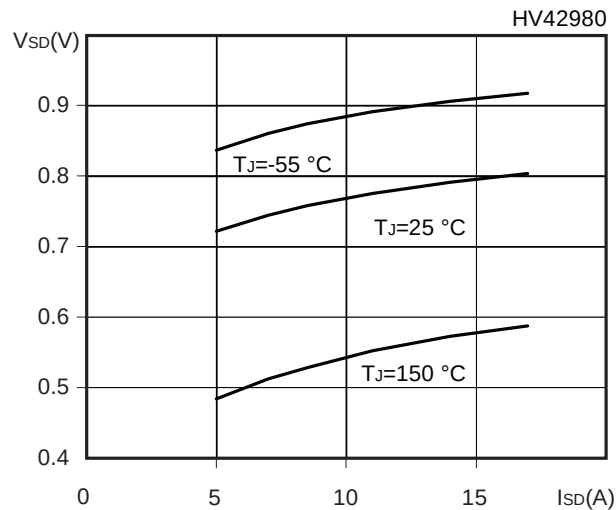
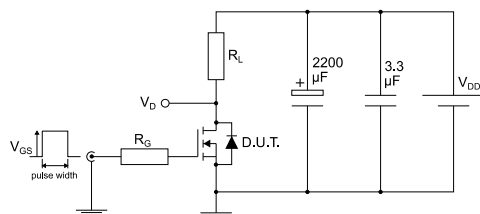
Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

Figure 12: Source-drain diode forward characteristics



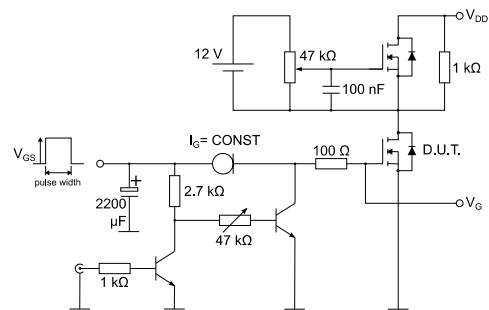
3 Test circuits

Figure 13: Test circuit for resistive load switching times



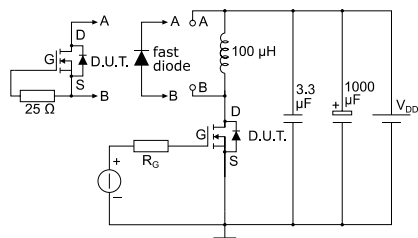
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Figure 14: Test circuit for gate charge behavior



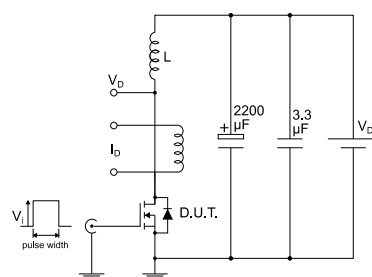
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Figure 15: Test circuit for inductive load switching and diode recovery times



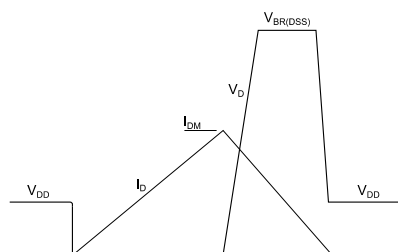
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Figure 16: Unclamped inductive load test circuit



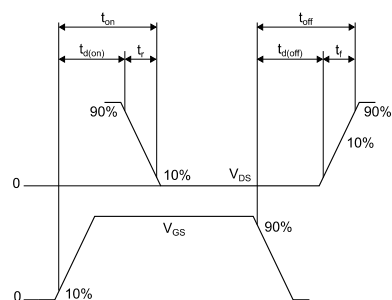
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 package information

Figure 19: PowerFLAT™ 5x6 WF type C package outline

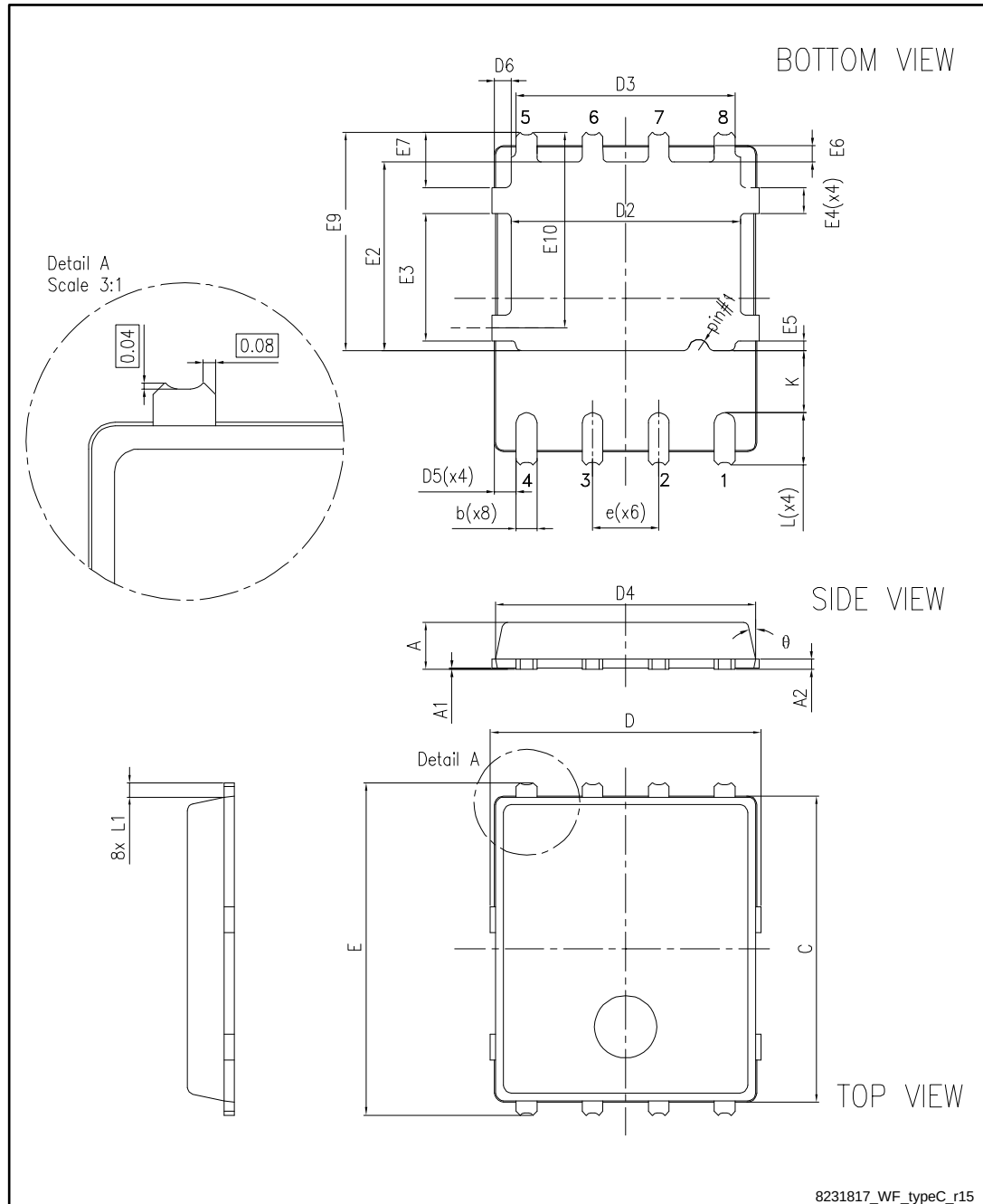
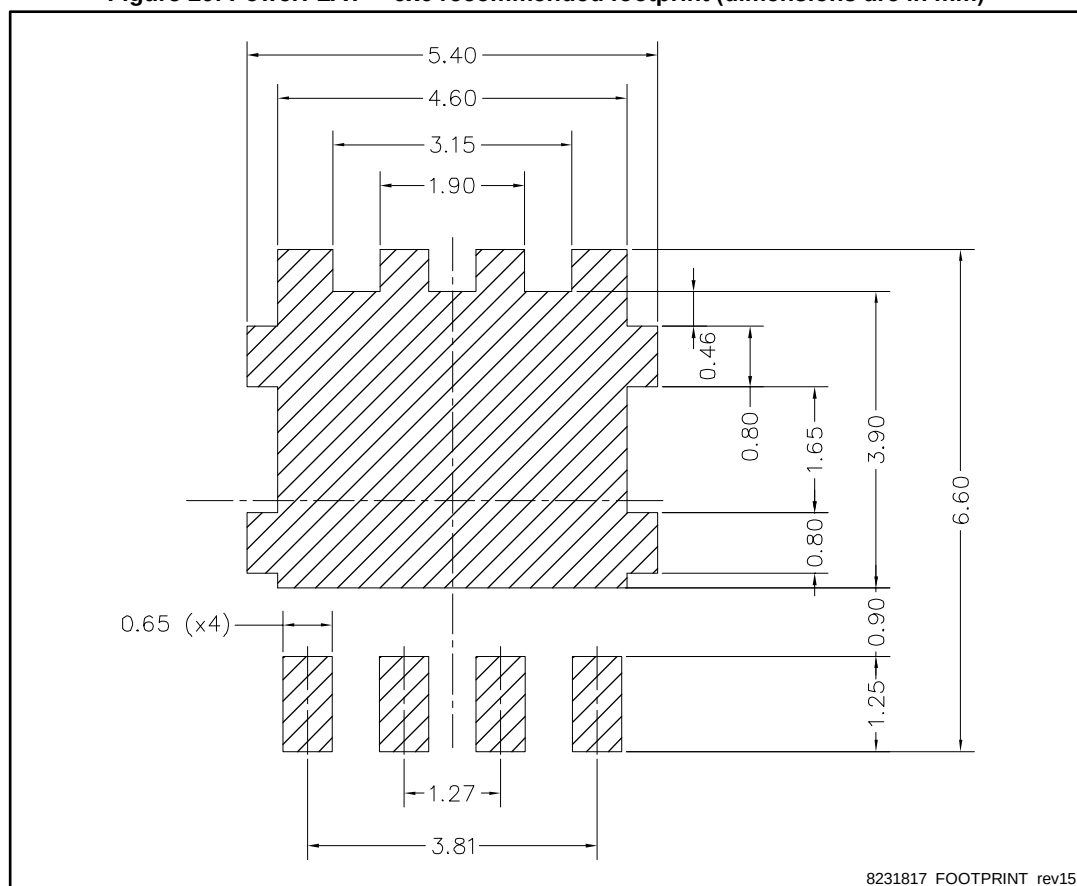


Table 9: PowerFLAT™ 5x6 WF type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.05		1.35
L	0.90	1.00	1.10
L1	0.175	0.275	0.375
θ	0°		12°

Figure 20: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 packing information

Figure 21: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

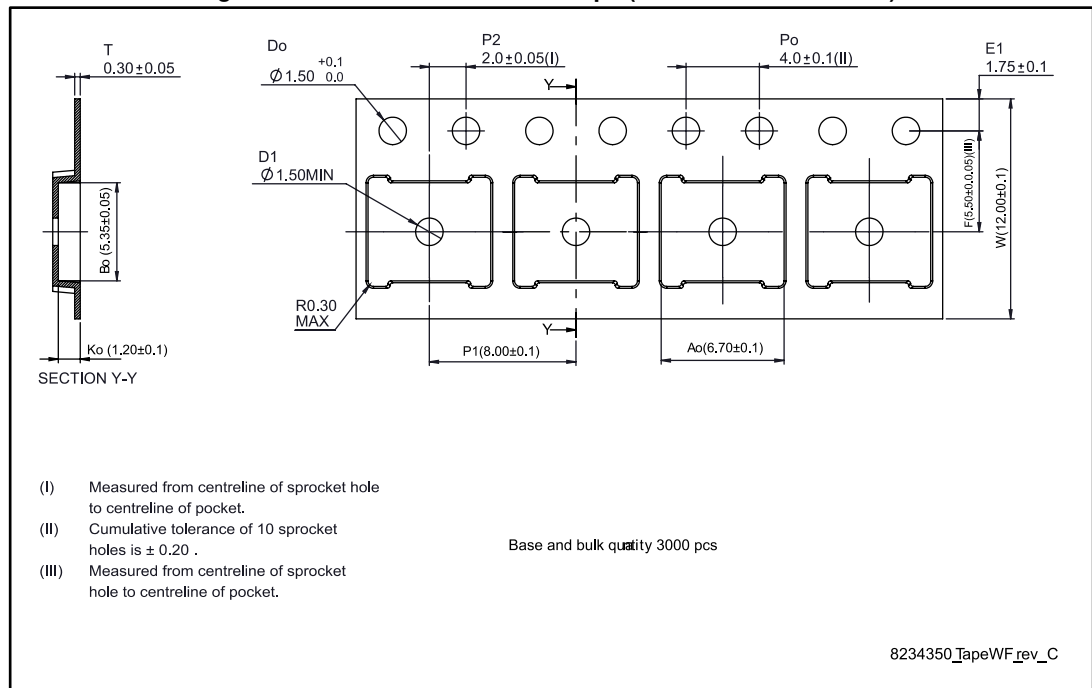


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

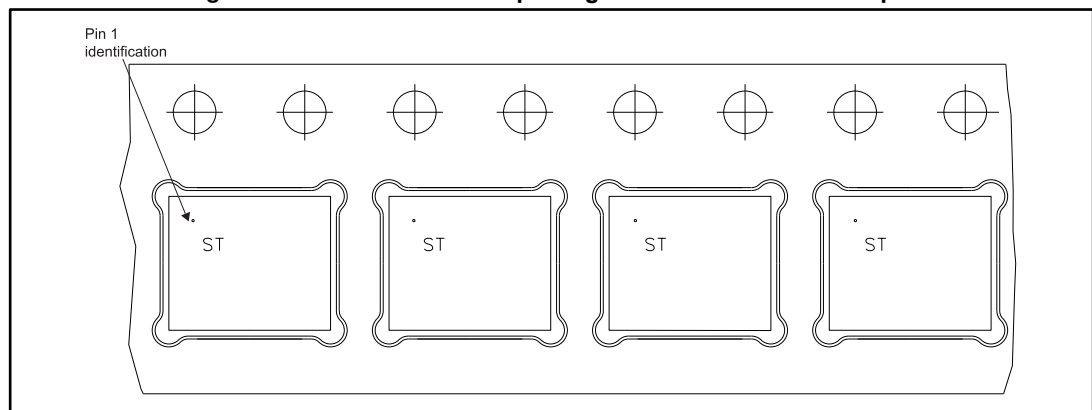
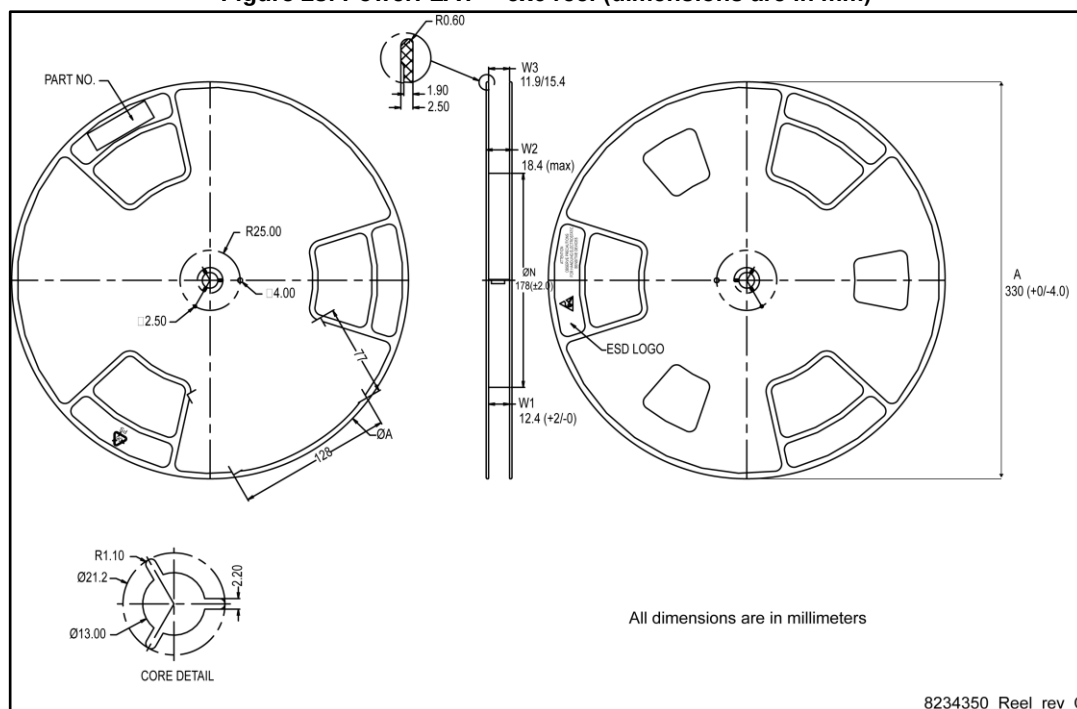


Figure 23: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 10: Document revision history

Date	Revision	Changes
19-Oct-2011	1	First release.
17-dec-2014	2	Document status promoted from preliminary to production data. Updated title, features and description in cover page. Updated Chapter: Package mechanical data and Chapter: Packaging mechanical data.
22-Jan-2016	3	Updated title and features in cover page. Updated <i>Section 4.1: "PowerFLAT™ 5X6 package information"</i> Minor text changes.
09-May-2017	4	Updated title and features in cover page. Updated <i>Section 4.1: "PowerFLAT™ 5x6 package information"</i> . Minor text changes.

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