LMH0387 3 Gbps HD/SD SDI Configurable I/O Adaptive Cable Equalizer / Cable Driver

Check for Samples: LMH0387

FEATURES

- **SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M Compliant**
- **Supports DVB-ASI at 270 Mbps**
- **Data Rates: 125 Mbps to 2.97 Gbps when Receiving (DC to 2.97 Gbps when Driving Cable)**
- **Equalizes up to 120 Meters of Belden 1694A at 2.97 Gbps, up to 200 Meters of Belden 1694A at 1.485 Gbps, or up to 400 Meters of Belden 1694A at 270 Mbps**
- **Integrated Return Loss Network (No External Components Required)**
- **Power Saving Modes**
- **Cable Driver Selectable Slew Rate**
- **Internally Terminated 100Ω LVDS Receiver Outputs with Programmable Common Mode Voltage and Swing**
- **Programmable Launch Amplitude Optimization for Receiver**
- **Cable Length Indication**
- **Single 3.3V Supply Operation**
- **48-Pin Laminate TLGA Package**
- **Industrial Temperature Range: −40°C to +85°C**

APPLICATIONS

- **SMPTE 424M, SMPTE 292M, and SMPTE 259M Serial Digital Interfaces**
- **Digital Video Servers and Modular Equipment**
- **Video Encoders and Decoders**
- **Distribution Amplifiers**

DESCRIPTION

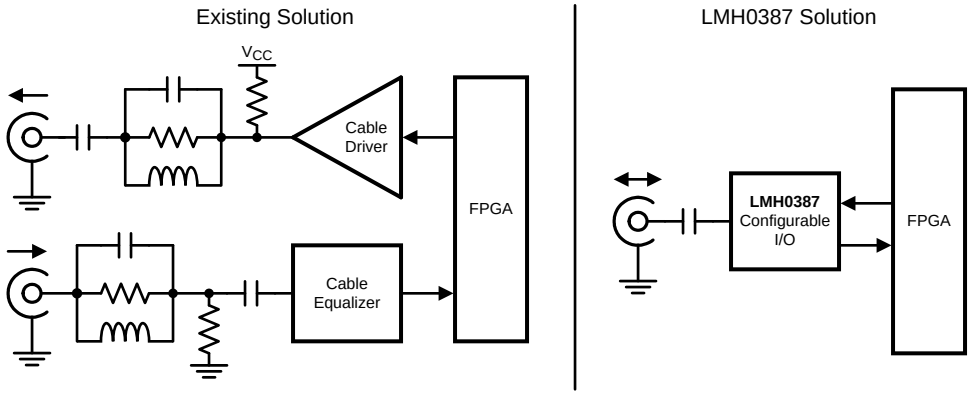
The LMH0387 3 Gbps HD/SD SDI Configurable I/O Adaptive Cable Equalizer / Cable Driver provides a single chip interface to a BNC. The device can be configured either in the input mode as an equalizer to receive data over coaxial cable or in the output mode as a cable driver to transmit data over coaxial cable. The same I/O pin is used both for the input and the output functions of the device, allowing the system designer the flexibility to use a BNC attached to the device as either an input or an output.

The LMH0387 offers designers flexibility in system design and quicker time to market. The device operates over a wide range of data rates from 125 Mbps to 2.97 Gbps (DC to 2.97 Gbps when driving cable) and supports SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M. The return loss network is integrated within the device so no external components are required to meet the SMPTE return loss specification.

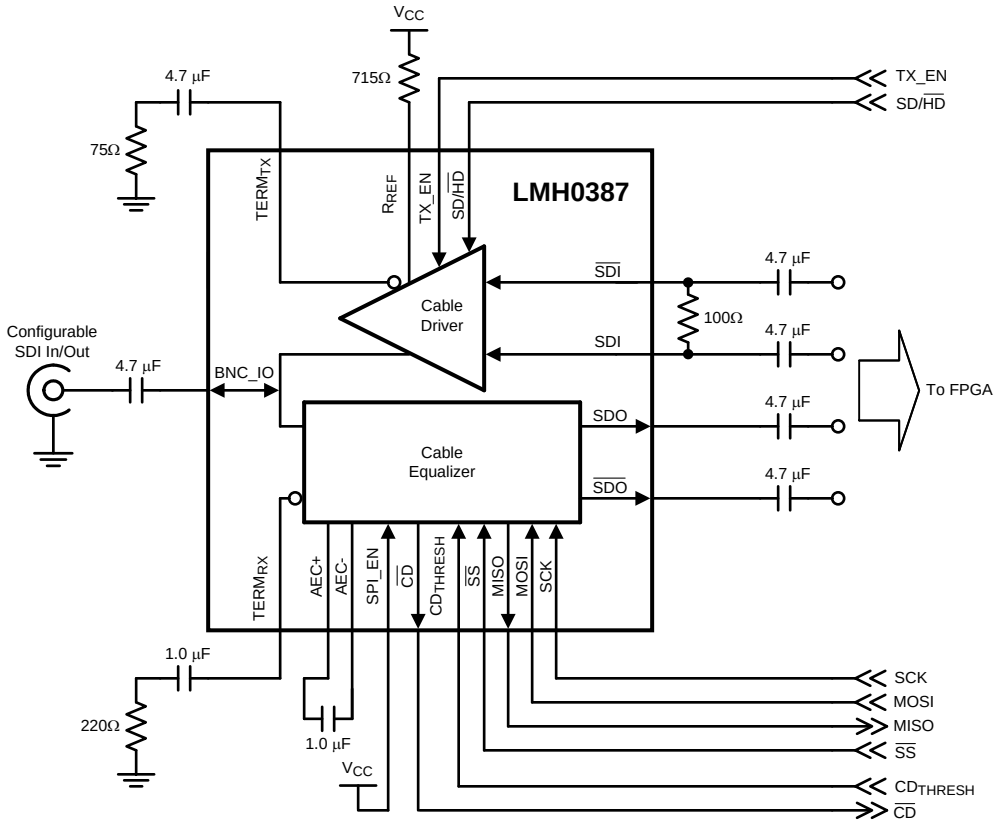
In the input mode, the LMH0387 features include a power-saving sleep mode, programmable output common mode voltage and swing, cable length indication, launch amplitude optimization, input signal detection, and an SPI interface. In the output mode, the LMH0387 features include two selectable slew rates for SMPTE 424M / 292M and SMPTE 259M compliance, and output driver power down control.

The device is available in a 7 x 7 mm 48-pin laminate Thin Chip Scale Package (TLGA).

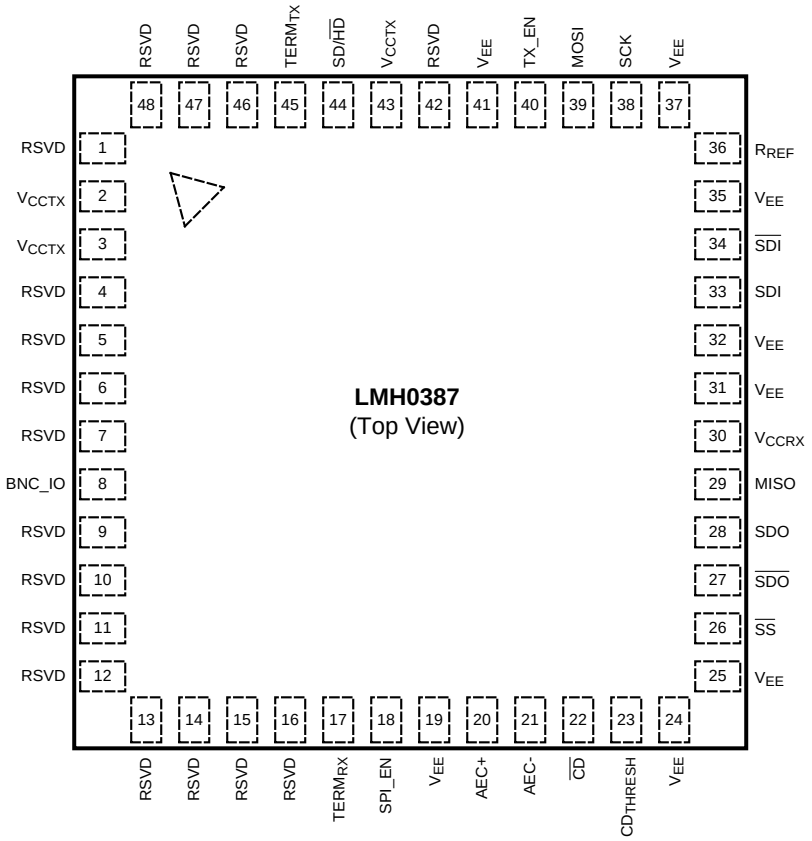
Typical Application



Typical Application Circuit



Connection Diagram



48-Pin Laminate TLGA
See Package Number NPD0048A

PIN DESCRIPTION

Pin	Name	I/O, Type	Description
1, 4-7, 9–16, 42, 46-48	RSVD	N/A	Do not connect.
2, 3, 43	V_{CCTX}	Power	Positive power supply for transmitter (+3.3V).
8	BNC_IO	I/O, SDI	Serial digital interface input or output for connection to a BNC. Connect this pin to the BNC via an AC coupling capacitor (nominally 4.7µF).
17	$TERM_{RX}$	I, SDI	Termination for unused receiver (equalizer) input. This network should consist of a 1.0 µF capacitor followed by a 220Ω resistor to ground.
18	SPI_EN	I, LVCMOS	SPI register access enable (equalizer). This pin should always be high; it must be pulled high while operating in the input mode and may optionally be pulled high while operating in the output mode. This pin has an internal pulldown.
19, 24, 25, 31, 32, 35, 37, 41	V_{EE}	Power	Negative power supply (ground).
20, 21	AEC+, AEC-	I/O, Analog	AEC loop filter external capacitor for equalizer (1.0 µF connected between AEC+ and AEC-).
22	$\overline{CD}$	O, LVCMOS	Carrier detect for BNC_IO pin. H = No input signal detected on BNC_IO pin. L = Input signal detected on BNC_IO pin.
23	CD_{THRESH}	I, Analog	Carrier detect threshold input. Sets the threshold for $\overline{CD}$. CD_{THRESH} may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
26	$\overline{SS}$ (SPI)	I, LVCMOS	SPI slave select. This pin has an internal pullup.
27, 28	$\overline{SDO}$, SDO	O, LVDS	Serial data differential output from receiver (equalizer).
29	MISO (SPI)	O, LVCMOS	SPI Master Input / Slave Output. LMH0387 control data transmit.

PIN DESCRIPTION (continued)

Pin	Name	I/O, Type	Description
30	V_{CCRX}	Power	Positive power supply for receiver (+3.3V).
33, 34	SDI, $\overline{SDI}$	I, SDI	Serial data differential input for transmitter (cable driver).
36	R_{REF}	I, Analog	BNC_IO output driver level control. Connect a resistor (nominally 715Ω) to V_{CC} to set the output voltage swing for the BNC_IO pin.
38	SCK (SPI)	I, LVCMOS	SPI serial clock input.
39	MOSI (SPI)	I, LVCMOS	SPI Master Output / Slave Input. LMH0387 control data receive.
40	TX_EN	I, LVCMOS	Transmitter output driver enable. TX_EN has an internal pullup. H = BNC_IO output driver is enabled. L = BNC_IO output driver is powered off. To configure the LMH0387 as a receiver, the BNC_IO output driver must be disabled by tying TX_EN low. To configure the LMH0387 as a transmitter, the output driver must be enabled by tying TX_EN high and the receiver may be powered down using the sleep mode setting via the SPI.
44	SD/$\overline{HD}$	I, LVCMOS	BNC_IO output slew rate control. SD/$\overline{HD}$ has an internal pulldown. H = BNC_IO output rise/fall time complies with SMPTE 259M (SD). L = BNC_IO output rise/fall time complies with SMPTE 424M / 292M (3G/HD).
45	$TERM_{TX}$	O, SDI	Termination for unused transmitter (cable driver) output. This network should consist of a 4.7 µF capacitor followed by a 75Ω resistor to ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Supply Voltage		4.0V
Input Voltage (all inputs)		−0.3V to V_{CC}+0.3V
Storage Temperature Range		−65°C to +150°C
Junction Temperature		+125°C
Package Thermal Resistance	θ_{JA} 48-pin NPD	65°C/W
	θ_{JC} 48-pin NPD	36°C/W
ESD Rating (HBM)		≥±6 kV
ESD Rating (MM)		≥±300V
ESD Rating (CDM)		≥±2.5 kV

(1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Recommended Operating Conditions

Supply Voltage (V_{CC} – V_{EE})	3.3V ±5%
BNC_IO Input / Output Coupling Capacitance	4.7 µF
AEC Capacitor (Connected between AEC+ and AEC-)	1.0 µF
Operating Free Air Temperature (T_A)	−40°C to +85°C

Control Pin Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic Inputs	2.0		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.8	V
V_{OH}	Output Voltage High Level	I_{OH} = -2 mA	Logic Outputs	2.4			V
V_{OL}	Output Voltage Low Level	I_{OL} = +2 mA				0.4	V

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Input Mode (Equalizer) DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IN}	Input Voltage Swing	0m cable length(3)	BNC_IO	720	800	950	mV_{P-P}
V_{SSP-P}	Differential Output Voltage, P-P	100Ω load, default register settings, Figure 1(4)	SDO, $\overline{SDO}$	500	700	900	mV_{P-P}
V_{OD}	Differential Output Voltage			250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States					50	mV
V_{OS}	Offset Voltage			1.125	1.25	1.375	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States					50	mV
I_{OS}	Output Short Circuit Current					30	mA
	CD_{THRESH} DC Voltage (floating)		CD_{THRESH}		1.3		V
	CD_{THRESH} Range				0.8		V
I_{CC}	Supply Current	Equalizing cable > 120m (Belden 1694A), TX_EN = 0			91	113	mA
		Equalizing cable ≤ 120m (Belden 1694A), TX_EN = 0(5)			71		mA
		Power save mode (equalizer in sleep mode, TX_EN = 0)			11		mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.
(3) The LMH0387 equalizer can be optimized for different launch amplitudes via the SPI.
(4) The differential output voltage and offset voltage are adjustable via the SPI.
(5) The equalizer automatically shifts equalization stages at cable lengths less than or equal to 120m (Belden 1694A) to reduce power consumption. This power savings is also achieved by setting Extended 3G Reach Mode = 1 via the SPI. (Note: Forcing the Extended 3G Reach Mode in this way increases the cable reach for 3G data rates but also limits the achievable cable lengths at HD and SD data rates).

Output Mode (Cable Driver) DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1)(2).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CMOUT}	Output Common Mode Voltage		BNC_IO		V_{CC} – V_{OUT}		V
V_{OUT}	Output Voltage Swing	R_{REF} = 715Ω 1%		720	800	880	mV_{P-P}
V_{CMIN}	Input Common Mode Voltage		SDI, $\overline{SDI}$	0.9 + V_{ID}/2		V_{CC} – V_{ID}/2	V
V_{ID}	Input Voltage Swing	Differential		100		2200	mV_{P-P}
I_{CC}	Supply Current	SD/$\overline{HD}$ = 0, equalizer in sleep mode			57	71	mA
		SD/$\overline{HD}$ = 1, equalizer in sleep mode			50		mA
		Power save mode (TX_EN = 0, equalizer in sleep mode)			11		mA
		Loopback mode (Tx and Rx both enabled), SD/$\overline{HD}$ = 0			117		mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Input Mode (Equalizer) AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR_{MIN}	Minimum Input Data Rate		BNC_IO		125		Mbps
DR_{MAX}	Maximum Input Data Rate					2970	Mbps
t_{jit}	Equalizer Jitter for Various Cable Lengths	270 Mbps, Belden 1694A, 0-350 meters(2)(3)	SDO, $\overline{SDO}$			0.2	UI
		270 Mbps, Belden 1694A, 350-400 meters(3)			0.2		UI
		1.485 Gbps, Belden 1694A, 0-170 meters(2)(3)				0.25	UI
		1.485 Gbps, Belden 1694A, 170-200 meters(3)			0.3		UI
		2.97 Gbps, Belden 1694A, 0-100 meters(2)(3)				0.3	UI
		2.97 Gbps, Belden 1694A, 100-120 meters(3)			0.35		UI
t_r, t_f	Output Rise Time, Fall Time	20% – 80%, 100Ω load, Figure 1(4)			80	130	ps
Δt_r, Δt_f	Mismatch in Rise/Fall Time	See(4)			2	15	ps
t_{OS}	Output Overshoot				1	5	%
RL_{IN}	Input Return Loss	5 MHz - 1.5 GHz(4)(5)	BNC_IO	15			dB
		1.5 GHz - 3.0 GHz(4)(5)		10			dB

(1) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.
(2) Based on design and characterization data over the full range of recommended operating conditions of the device. Jitter is measured in accordance with SMPTE RP 184, SMPTE RP 192, and the applicable serial data transmission standard: SMPTE 424M, SMPTE 292M, or SMPTE 259M.
(3) LMH0387 equalizer launch amplitude fine tuning set to nominal via the SPI by writing 30h (“00110000 binary”) to SPI register 02h.
(4) Specification is guaranteed by characterization.
(5) Return loss is dependent on board design. The LMH0387 exceeds this specification on the SD387 evaluation board.

Output Mode (Cable Driver) AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified(1).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
DR_{MAX}	Maximum Input Data Rate		SDI, $\overline{SDI}$			2970	Mbps
t_{jit}	Additive Jitter	2.97 Gbps(2)	BNC_IO		20		ps_{P-P}
		1.485 Gbps(2)			18		ps_{P-P}
		270 Mbps(2)			15		ps_{P-P}
t_r, t_f	Output Rise Time, Fall Time	SD/$\overline{HD}$ = 0, 20% – 80%			65	130	ps
		SD/$\overline{HD}$ = 1, 20% – 80%		400		800	ps
Δt_r, Δt_f	Mismatch in Rise/Fall Time	SD/$\overline{HD}$ = 0				30	ps
		SD/$\overline{HD}$ = 1				50	ps
	Duty Cycle Distortion	SD/$\overline{HD}$ = 0(3)				30	ps
		SD/$\overline{HD}$ = 1(3)				100	ps
t_{OS}	Output Overshoot	SD/$\overline{HD}$ = 0(3)				10	%
		SD/$\overline{HD}$ = 1(3)				8	%
RL_{OUT}	Output Return Loss	5 MHz - 1.5 GHz(3)(4)		15			dB
		1.5 GHz - 3.0 GHz(3)(4)		10			dB

(1) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.
(2) Cable driver additive jitter is measured with the input AC coupled.
(3) Specification is guaranteed by characterization.
(4) Return loss is dependent on board design. The LMH0387 exceeds this specification on the SD387 evaluation board.

Input Mode (Equalizer) SPI Interface AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
Recommended Input Timing Requirements							
f_{SCK}	SCK Frequency		SCK			20	MHz
t_{PH}	SCK Pulse Width High	Figure 2, Figure 3		40			% SCK period
t_{PL}	SCK Pulse Width Low			40			% SCK period
t_{SU}	MOSI Setup Time	Figure 2, Figure 3	MOSI	4			ns
t_H	MOSI Hold Time			4			ns
t_{SSSU}	$\overline{SS}$ Setup Time	Figure 2, Figure 3	$\overline{SS}$	4			ns
t_{SSH}	$\overline{SS}$ Hold Time			4			ns
t_{SSOF}	$\overline{SS}$ Off Time			10			ns
Switching Characteristics							
t_{ODZ}	MISO Driven-to-Tristate Time	Figure 3	MISO			15	ns
t_{OZD}	MISO Tristate-to-Driven Time					15	ns
t_{OD}	MISO Output Delay Time					15	ns

(1) Typical values are stated for V_{CC} = +3.3V and T_A = +25°C.

Timing Diagrams

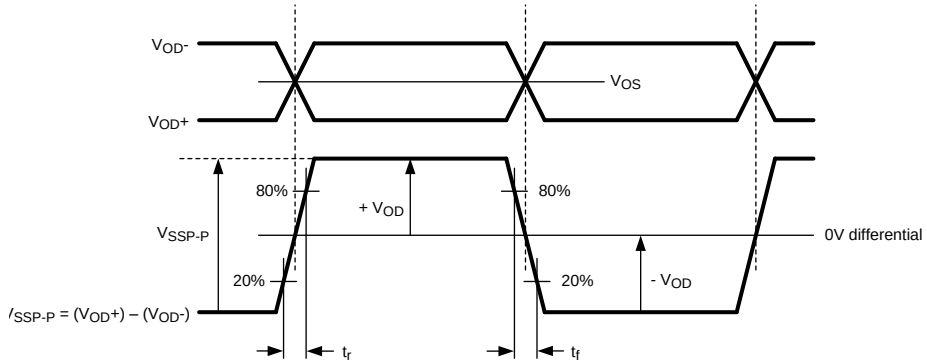


Figure 1. LVDS Output Voltage, Offset, and Timing Parameters

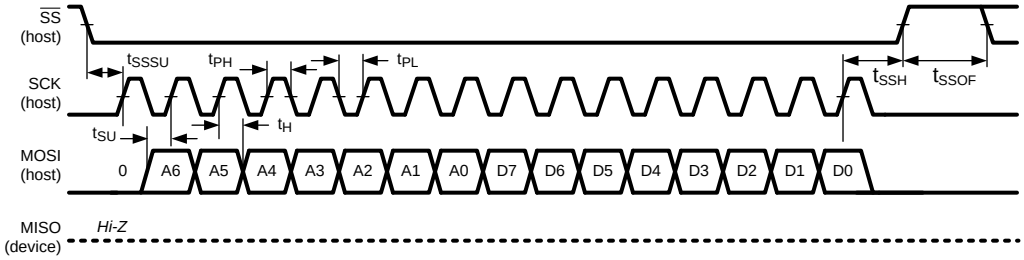


Figure 2. SPI Write

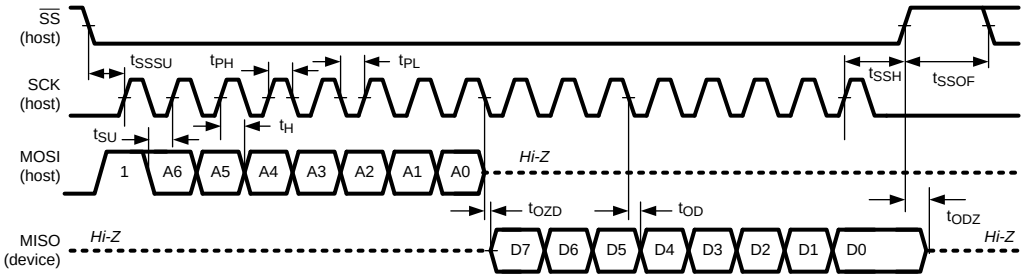


Figure 3. SPI Read

Device Description

The LMH0387 3 Gbps HD/SD SDI Configurable I/O Adaptive Cable Equalizer / Cable Driver is used at the input or output port of digital video equipment. It is designed to allow the sharing of a single BNC connector for either input or output.

CONFIGURING THE INPUT (EQUALIZER) OR OUTPUT (CABLE DRIVER) MODE

The LMH0387 must be configured in either the input mode as an equalizer, or the output mode as a cable driver.

Input Mode (Equalizer)

To configure the LMH0387 in the input mode, the equalizer must be enabled and the cable driver must be disabled as described in the following steps:

1. Disable the cable driver by pulling the TX_EN pin low.
2. Enable the equalizer by setting the sleep mode via the SPI to either auto sleep or disabled (never sleep). To do this, write either “01” (auto sleep – default) or “00” (never sleep) to bits [4:3] of SPI register 00h.
3. Set the equalizer launch amplitude fine tuning to the nominal setting via the SPI. To do this, write 30h (“00110000” binary) to SPI register 02h.

Output Mode (Cable Driver)

To configure the LMH0387 in the output mode, the cable driver must be enabled. The equalizer may either be disabled for power savings or enabled to provide a loopback path for the data being transmitted. For the normal output mode (equalizer disabled for power savings) follow these steps:

1. Disable the equalizer by forcing it to sleep via the SPI. To do this, write “10” (force sleep) to bits [4:3] of SPI register 00h.
2. Enable the cable driver by pulling the TX_EN pin high.

To configure the LMH0387 for the output mode with the loopback path, the equalizer can be enabled in output mode by writing either “01” (auto sleep – default) or “00” (never sleep) to bits [4:3] of SPI register 00h. In this case, the LMH0387 input/output mode may be configured simply by toggling the TX_EN pin since the equalizer remains active in either mode (TX_EN set low for input mode and high for output mode).

Input Mode (Equalizer) Description

SPI register access is required while operating the LMH0387 in the input mode. The equalizer launch amplitude fine tuning must be set to nominal via the SPI for correct equalizer operation. To do this, write 30h (“00110000 binary”) to SPI register 02h. The SPI registers provide access to many other useful LMH0387 features while in the input mode. Refer to the Input Mode (Equalizer) SPI Register Access section for details.

INPUT INTERFACING

The LMH0387 accepts single-ended input at the BNC_IO pin. The input must be AC coupled. The Typical Application Circuit diagram shows the typical configuration. The $TERM_{RX}$ input must be properly terminated with a 1.0 µF capacitor followed by a 220Ω resistor to ground as shown.

The LMH0387 BNC_IO input can be optimized for different launch amplitudes via the SPI (see LAUNCH AMPLITUDE OPTIMIZATION (REGISTER 02h) in the Input Mode (Equalizer) SPI Register Access section).

The LMH0387 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

OUTPUT INTERFACING

The LMH0387 equalizer outputs, SDO and $\overline{SDO}$, are internally terminated 100Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

The default output common mode voltage (V_{OS}) is 1.25V. The output common mode voltage may be adjusted via the SPI in 200 mV increments, from 1.05V to 1.85V (see OUTPUT DRIVER ADJUSTMENTS (REGISTER 01h) in the Input Mode (Equalizer) SPI Register Access section). This adjustable output common mode voltage offers flexibility for interfacing to many types of receivers.

The default differential output swing (V_{SSP-P}) is 700 mV_{P-P}. The differential output swing may be adjusted via the SPI in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P} (see OUTPUT DRIVER ADJUSTMENTS (REGISTER 01h) in the Input Mode (Equalizer) SPI Register Access section).

The LMH0387 equalizer output should be DC coupled to the input of the receiving device as long as the common mode ranges of both devices are compatible. 100Ω differential transmission lines should be used to connect between the LMH0387 outputs and the input of the receiving device where possible.

The LMH0387 allows flexibility when interfacing to low voltage crosspoint switches (i.e. 1.8V) and other devices with limited input ranges. The LMH0387 equalizer outputs can be DC coupled to these devices in most cases, avoiding the need to AC couple.

The LMH0387 may be AC coupled to the receiving device when necessary. For example, the LMH0387 equalizer outputs are not strictly compatible with 3.3V CML and thus should not be connected via 50Ω resistors to 3.3V. If the input common mode range of the receiving device is not compatible with the output common mode range of the LMH0387, then AC coupling is required. Following the AC coupling capacitors, the signal may have to be biased at the input of the receiving device.

CARRIER DETECT ($\overline{CD}$)

Carrier detect $\overline{CD}$ indicates if a valid signal is present at the LMH0387 BNC_IO pin. If CD_{THRESH} is used, the carrier detect threshold will be altered accordingly. $\overline{CD}$ provides a high voltage when no signal is present at the LMH0387 BNC_IO pin. $\overline{CD}$ is low when a valid input signal is detected.

CARRIER DETECT THRESHOLD (CD_{THRESH})

The CD_{THRESH} pin sets the threshold for the carrier detect. The carrier detect threshold is set by applying a voltage inversely proportional to the length of cable to equalize before loss of carrier is triggered. The applied voltage must be greater than the CD_{THRESH} floating voltage (typically 1.3V) in order to change the $\overline{CD}$ threshold. As the applied CD_{THRESH} voltage is increased, the amount of cable that will be equalized before carrier detect is de-asserted is decreased. CD_{THRESH} may be left unconnected or connected to ground for normal $\overline{CD}$ operation.

Figure 4 shows the minimum CD_{THRESH} input voltage required to force carrier detect to inactive vs. Belden 1694A cable length. The results shown are valid for Belden 1694A cable lengths of 0-120m at 2.97 Gbps, 0-200m at 1.485 Gbps, and 0-400m at 270 Mbps.

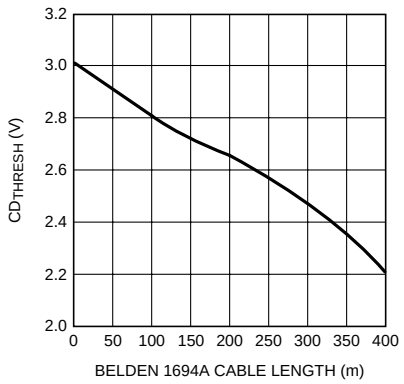


Figure 4. CD_{THRESH} vs. Belden 1694A Cable Length

AUTO SLEEP

The LMH0387 equalizer is set for auto sleep operation by default. The equalizer portion of the LMH0387 powers down when no input signal is detected on the BNC_IO pin. The equalizer powers on again once an input signal is detected. The auto sleep functionality can be changed to force sleep or turned off completely via the SPI registers.

In auto sleep mode, the time to power down the equalizer when the input signal is removed is less than 200 µs and should not have any impact on the system timing requirements. The equalizer will wake up automatically once an input signal is detected, and the delay between signal detection and full functionality of the equalizer is negligible. The overall system will be limited only by the settling time constant of the equalizer adaptation loop.

Input Mode (Equalizer) SPI Register Access

SPI register access is required for correct input mode (equalizer) operation. The SPI registers provide access to all of the equalizer features along with a cable length indicator, programmable output common mode voltage and swing, and launch amplitude optimization. There are four supported 8-bit registers in the device (see Table 1).

Note: The SPI_EN pin must always be pulled high while using the LMH0387 in the input mode (equalizer), and may optionally be pulled high while using the LMH0387 in the output mode (cable driver) as well.

SPI Write

The SPI write is shown in Figure 2. The MOSI payload consists of a “0” (write command), seven address bits, and eight data bits. The $\overline{SS}$ signal is driven low, and the 16 bits are sent to the LMH0387's MOSI input. Data is latched on the rising edge of SCK. The MISO output is normally tri-stated during this operation. After the SPI write, $\overline{SS}$ must return high.

SPI Read

The SPI read is shown in Figure 3. The MOSI payload consists of a “1” (read command) and seven address bits. The $\overline{SS}$ signal is driven low, and the eight bits are sent to the LMH0387's MOSI input. The addressed location is accessed immediately after the rising edge of the 8th clock and the eight data bits are shifted out on MISO starting with the falling edge of the 8th clock. MOSI must be tri-stated immediately after the rising edge of the 8th clock. After the SPI read, $\overline{SS}$ must return high.

GENERAL CONTROL (REGISTER 00h)

SPI Register 00h, General Control, provides access to many basic features of the equalizer, including the carrier detect status and the mute, sleep mode, and extended 3G reach mode controls.

Carrier Detect

This bit shows the status of the carrier detect for the BNC_IO pin.

Mute

The mute control can be used to manually mute or enable SDO and $\overline{SDO}$. Setting this bit to “1” will mute the equalizer outputs by forcing them to logic zero. Setting the mute bit to “0” will force the equalizer outputs to be active.

Sleep Mode

The sleep mode is used to automatically or selectively power down the equalizer for power savings when it is not needed. The auto sleep mode allows the equalizer to power down when no input signal is detected, and is activated by default or by writing “01” to bits [4:3] of SPI register 00h. If the auto sleep mode is active, the equalizer goes into a deep power save mode when no input signal is detected on the BNC_IO pin. The device powers on again once an input signal is detected. The sleep functionality can be turned off completely (equalizer will never sleep) by writing “00” to bits [4:3] of SPI register 00h. Additionally, the equalizer can be forced to power down regardless of whether there is an input signal or not by writing “10” to bits [4:3] of SPI register 00h. The sleep mode has precedence over the mute mode.

Extended 3G Reach Mode

The LMH0387 equalizer provides a mode to extend the 3G cable reach in systems which have margin in the jitter budget. This allows for additional cable reach at 2.97 Gbps at the expense of slightly higher output jitter. The extended 3G reach mode provides 10m of additional Belden 1694A cable reach, with an increase of output jitter at this longer cable length of 0.05 to 0.1 UI. (Note: In Extended 3G Reach Mode, the maximum equalizable cable lengths for HD and SD data rates will be limited to less than what can be achieved in normal mode).

OUTPUT DRIVER ADJUSTMENTS (REGISTER 01h)

The equalizer output driver swing (amplitude) and offset voltage (common mode voltage) are adjustable via SPI register 01h.

Output Swing

The output swing is adjustable via bits [7:5] of SPI register 01h. The default value for these register bits is “011” for a peak to peak differential output voltage of 700 mV_{P-P}. The output swing can be adjusted in 100 mV increments from 400 mV_{P-P} to 800 mV_{P-P}.

Offset Voltage

The offset voltage is adjustable via bits [4:2] of SPI register 01h. The default value for these register bits is “001” for an output offset of 1.25V. The output common mode voltage may be adjusted in 200 mV increments, from 1.05V to 1.85V. It can also be set to “101” for the maximum offset voltage. At this maximum offset voltage setting, the outputs are referenced to the positive supply and the offset voltage is around 2.1V.

LAUNCH AMPLITUDE OPTIMIZATION (REGISTER 02h)

The LMH0387 can compensate for attenuation of the input signal prior to the equalizer. This compensation is useful for applications with a passive splitter at the equalizer input or a non-ideal input termination network, and is controlled by SPI register 02h.

For correct equalizer operation with the default SMPTE 800 mV_{P-P} launch amplitude and no external attenuation, the equalizer launch amplitude fine tuning must be set to the “nominal” setting via the SPI. To do this, write 30h (“00110000” binary) to SPI register 02h.

Coarse Control

Bit 7 of SPI register 02h is used for coarse control of the launch amplitude setting. At the default setting of “0”, the equalizer operates normally and expects a launch amplitude of 800 mV_{P-P}. Bit 7 may be set to “1” to optimize the equalizer for input signals with 6 dB of attenuation (400 mV_{P-P}).

Fine Control

Once the coarse control is set, the equalizer input compensation may be further fine tuned by bits [6:3] of SPI register 02h. These bits may be used to tweak the input gain stage -2% to +60% around the coarse control setting. For typical equalizer operation, bits [6:3] of SPI register 02h should be changed from the default setting of “0000” to the nominal setting of “0110”.

CABLE LENGTH INDICATOR (CLI) (REGISTER 03h)

The Cable Length Indicator (CLI) provides an indication of the length of cable attached to the equalizer input. CLI is accessible via bits [7:3] of SPI register 03h. The 5-bit CLI ranges in decimal value from 0 to 25 (“00000” to “11001” binary) and increases as the cable length is increased. Figure 5 shows typical CLI values vs. Belden 1694A cable length. CLI is valid for Belden 1694A cable lengths of 0-120m at 2.97 Gbps, 0-200m at 1.485 Gbps, and 0-400m at 270 Mbps.

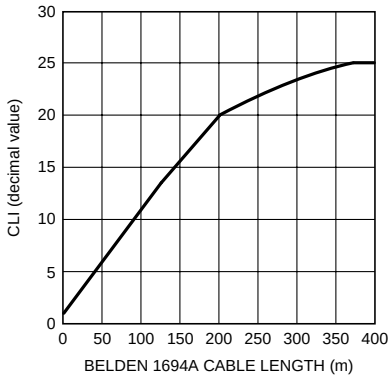


Figure 5. CLI vs. Belden 1694A Cable Length

Output Mode (Cable Driver) Description

INPUT INTERFACING

The LMH0387 cable driver accepts differential input signals which can be DC or AC coupled.

OUTPUT INTERFACING

The LMH0387 cable driver uses 75Ω internally terminated current mode outputs. The output level is 800 mV_{P-P} with an R_{REF} resistor of 715Ω. The R_{REF} resistor is connected between the R_{REF} pin and V_{CC}, and should be placed as close as possible to the R_{REF} pin.

The output should be AC coupled as shown in the Typical Application Circuit diagram. The $TERM_{TX}$ output must be properly terminated with a 4.7 µF capacitor followed by a 75Ω resistor to ground as shown.

OUTPUT SLEW RATE CONTROL

The LMH0387 cable driver output rise and fall times are selectable for either SMPTE 259M or SMPTE 424M / 292M compliance via the SD/$\overline{HD}$ pin. For slower rise and fall times, or SMPTE 259M compliance, SD/$\overline{HD}$ is set high. For faster rise and fall times, or SMPTE 424M and SMPTE 292M compliance, SD/$\overline{HD}$ is set low. SD/$\overline{HD}$ has an internal pulldown.

OUTPUT ENABLE

The LMH0387 cable driver can be enabled or disabled with the TX_EN pin. When set low, the cable driver is powered off. TX_EN has an internal pullup to enable the cable driver by default. When using the LMH0387 in the input mode (as an equalizer), the cable driver must be disabled by setting the TX_EN pin low.

APPLICATION INFORMATION

PCB LAYOUT RECOMMENDATIONS

For information on layout and soldering of the laminate TLGA package, pease refer to the following application note: **AN-1125, "Laminate CSP/FBGA."**

For a CSP package, it is a general requirement not to have any metal (traces or vias) on the top layer in the area directly underneath the device, other than the footprint. This is intended to provide a flat planar surface for the package.

The SMPTE 424M, 292M, and 259M standards have stringent requirements for the input and output return loss of receivers and transmitters, which essentially specify how closely they must resemble a 75Ω network. Any non-idealities in the network between the BNC and the LMH0387 will degrade the return loss. Care must be taken to minimize impedance discontinuities both for the BNC footprint and for the trace between the BNC and the LMH0387 to ensure that the characteristic impedance is 75Ω. Best return loss performance is achieved with the LMH0387 placed closely to the BNC to minimize the trace length between the BNC and the LMH0387's BNC_IO pin. Please consider the following PCB recommendations:

- Place the LMH0387 in close proximity to the BNC.
- Use surface mount components, and use the smallest components available. In addition, use the smallest size component pads.
- Select trace widths that minimize the impedance mismatch between the BNC and the LMH0387.
- Select a board stack up that supports both 75Ω single-ended traces and 100Ω loosely-coupled differential traces.
- Maintain symmetry on the complimentary signals.
- Route 100Ω traces uniformly (keep trace widths and trace spacing uniform along the trace).
- Avoid sharp bends in the signal path; use 45° or radial bends.
- Place bypass capacitors close to each power pin, and use the shortest path to connect device power and ground pins to the respective power or ground planes.
- Remove ground plane under input/output components to minimize parasitic capacitance.

Typical Performance Characteristics

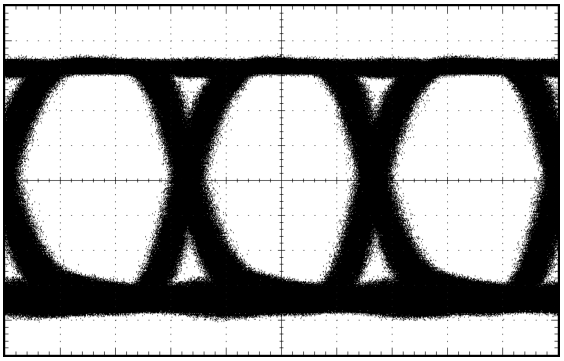


Figure 6. Equalizer Output at 2.97 Gbps with 120m Belden 1694A, H: 100 ps / div, V: 50 mV / div (SDO output shown)

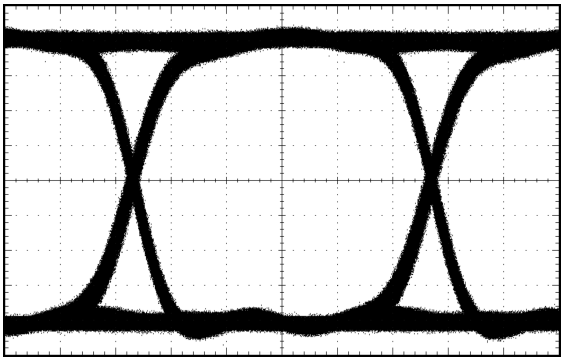


Figure 7. Cable Driver Output at 2.97 Gbps H: 62.5 ps / div, V: 100 mV / div (BNC_IO output shown)

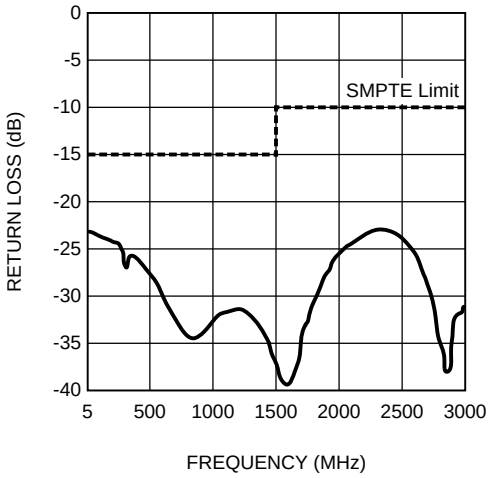


Figure 8. Output Return Loss

SPI Registers

Table 1. SPI Registers

Address	R/W	Name	Bits	Field	Default	Description
00h	R/W	General Control	7	Carrier Detect		Read only. 0: No carrier detected on BNC_IO pin. 1: Carrier detected on BNC_IO pin.
			6	Mute	0	0: Normal operation. 1: Equalizer outputs muted.
			5	Reserved	0	Reserved as 0. Always write 0 to this bit.
			4:3	Sleep Mode	01	Equalizer sleep mode control. Sleep has precedence over Mute. 00: Never sleep. Disable sleep mode (force equalizer to stay enabled). 01: Auto sleep. Sleep mode active when no input signal detected. 10: Force sleep. Force equalizer into sleep mode (powered down) regardless of whether there is an input signal or not. 11: Reserved.
			2	Extended 3G Reach Mode	0	Extended 3G reach mode to extend the equalizable cable length for 2.97 Gbps applications. 0: Normal operation. 1: Extended 3G reach mode.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.
01h	R/W	Output Driver	7:5	Output Swing	011	Equalizer output driver swing (V_{SSP-P}). 000: V_{SSP-P} = 400 mV_{P-P}. 001: V_{SSP-P} = 500 mV_{P-P}. 010: V_{SSP-P} = 600 mV_{P-P}. 011: V_{SSP-P} = 700 mV_{P-P}. 100: V_{SSP-P} = 800 mV_{P-P}. 101, 110, 111: Reserved.
			4:2	Offset Voltage	001	Equalizer output driver offset voltage (common mode voltage). 000: V_{OS} = 1.05V. 001: V_{OS} = 1.25V. 010: V_{OS} = 1.45V. 011: V_{OS} = 1.65V. 100: V_{OS} = 1.85V. 101: V_{OS} referenced to positive supply. 110, 111: Reserved.
			1:0	Reserved	00	Reserved as 00. Always write 00 to these bits.

Table 1. SPI Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
02h	R/W	Launch Amplitude	7	Coarse Control	0	Coarse launch amplitude optimization for equalizer input. 0: Normal optimization with no external attenuation (800 mV_{P-P} launch amplitude). 1: Optimized for 6 dB external attenuation (400 mV_{P-P} launch amplitude).
			6:3	Fine Control	0000	Launch amplitude optimization fine tuning for equalizer input. 0000: +20% from nominal. 0001: +16% from nominal. 0010: +12% from nominal. 0011: +9% from nominal. 0100: +6% from nominal. 0101: +3% from nominal. **0110: Nominal.** (The default setting must be changed to this nominal setting for most applications). 0111: -2% from nominal. 1001: +24% from nominal. 1010: +29% from nominal. 1011: +34% from nominal. 1100: +40% from nominal. 1101: +46% from nominal. 1110: +53% from nominal. 1111: +60% from nominal. 1000: Reserved.
			2:0	Reserved	000	Reserved as 000. Always write 000 to these bits.
03h	R	CLI	7:3	CLI		Cable Length Indicator. Provides an indication of the length of cable attached to the equalizer input. CLI increases as the cable length increases.
			2:0	Reserved	000	Reserved.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH0387SL/NOPB	ACTIVE	TLGA	NPD	48	1000	Green (RoHS & no Sb/Br)	NIAU	Level-3-260C-168 HR		LMH0387SL	Samples
LMH0387SLE/NOPB	ACTIVE	TLGA	NPD	48	250	Green (RoHS & no Sb/Br)	NIAU	Level-3-260C-168 HR		LMH0387SL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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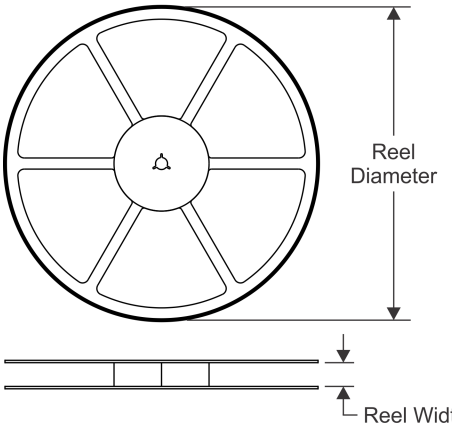
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

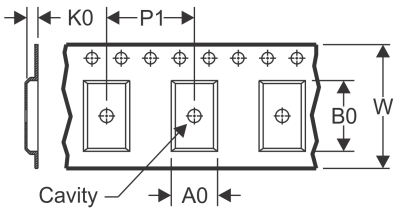
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

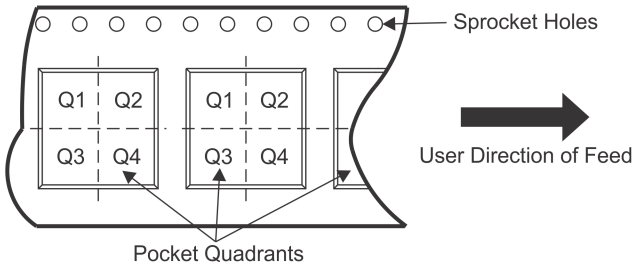


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

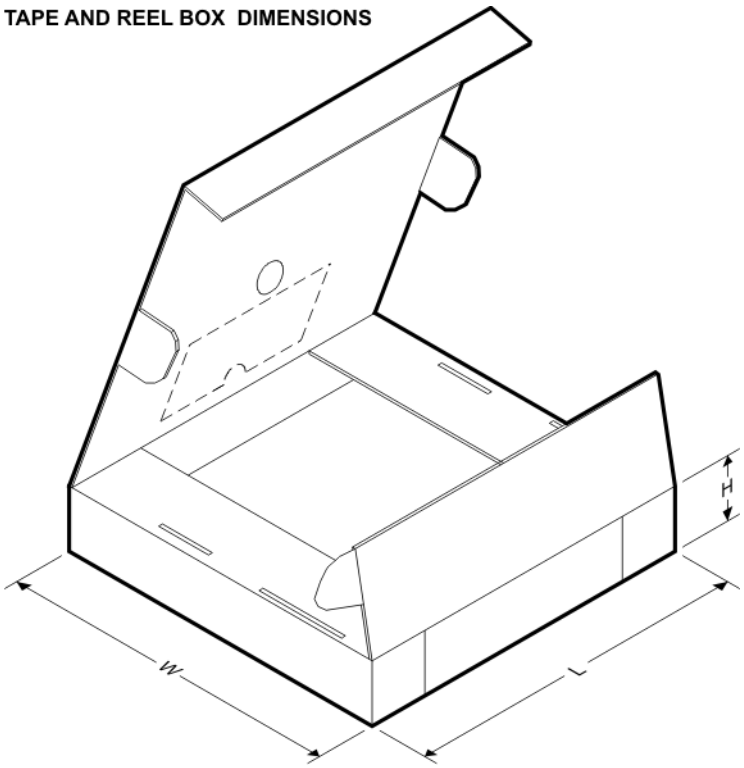
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0387SL/NOPB	TLGA	NPD	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
LMH0387SLE/NOPB	TLGA	NPD	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

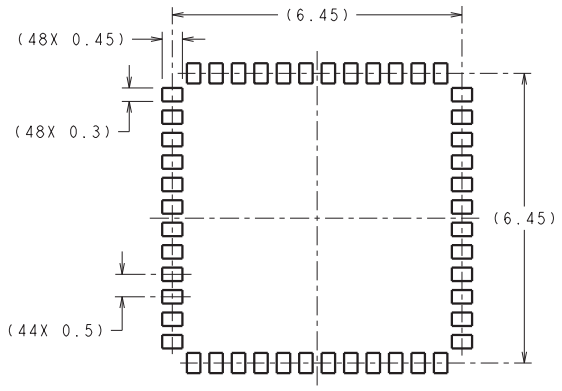
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

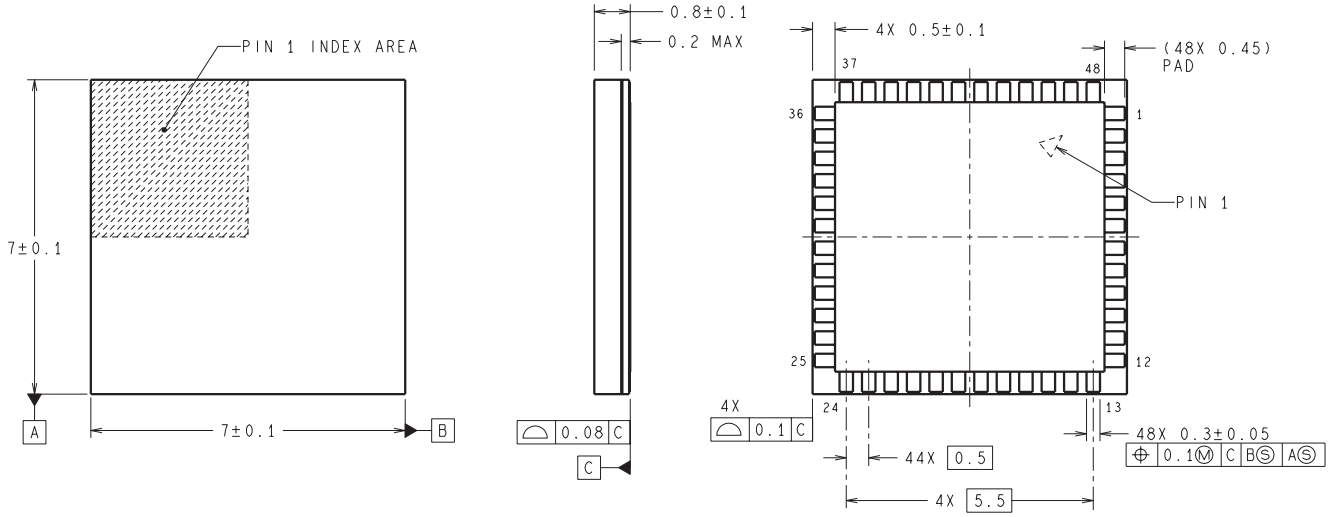
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0387SL/NOPB	TLGA	NPD	48	1000	367.0	367.0	38.0
LMH0387SLE/NOPB	TLGA	NPD	48	250	213.0	191.0	55.0

NPD0048A



RECOMMENDED LAND PATTERN
1:1 RATIO WITH PACKAGE SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



SLD48A (Rev B)

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