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Kind regards,

Team Nexperia

PEMD48; PUMD48

NPN/PNP resistor-equipped transistors; R1 = 47 kΩ, R2 = 47 kΩ and R1 = 2.2 kΩ, R2 = 47 kΩ

Rev. 6 — 24 January 2012 Product data sheet

1. Product profile

1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in small Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		Package configuration
	NXP	JEITA	
PEMD48	SOT666	-	ultra small and flat lead
PUMD48	SOT363	SC-88	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

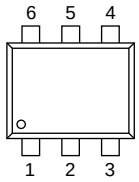
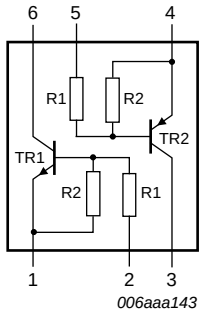
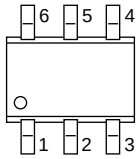
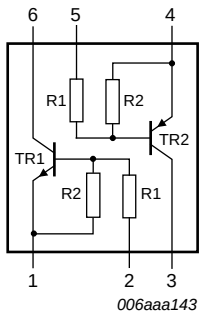
1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CEO}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA
Transistor TR1 (NPN)						
R1	bias resistor 1 (input)		33	47	61	kΩ
R2/R1	bias resistor ratio		0.8	1.0	1.2	
Transistor TR2 (PNP)						
R1	bias resistor 1 (input)		1.54	2.20	2.86	kΩ
R2/R1	bias resistor ratio		17	21	26	

2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
PEMD48 (SOT666)			
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		
PUMD48 (SOT363)			
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PEMD48	-	plastic surface-mounted package; 6 leads	SOT666
PUMD48	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code[1]
PEMD48	48
PUMD48	4*8

[1] * = placeholder for manufacturing site code.

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5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor; for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector				
	TR1 (NPN)			-	10	V
	TR2 (PNP)			-	−5	V
V_I	input voltage TR1					
	positive			-	+40	V
	negative			-	−10	V
	input voltage TR2					
	positive			-	+5	V
	negative			-	−12	V
I_O	output current			-	100	mA
I_{CM}	peak collector current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD48 (SOT666)		[1][2]	-	200	mW
	PUMD48 (SOT363)		[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD48 (SOT666)		[1][2]	-	300	mW
	PUMD48 (SOT363)		[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			−65	+150	°C
T_{stg}	storage temperature			−65	+150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

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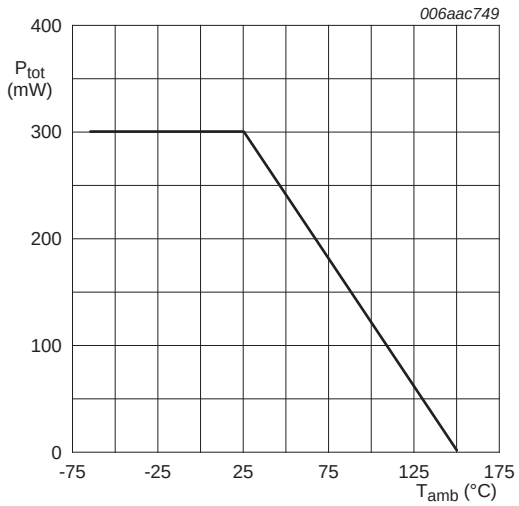
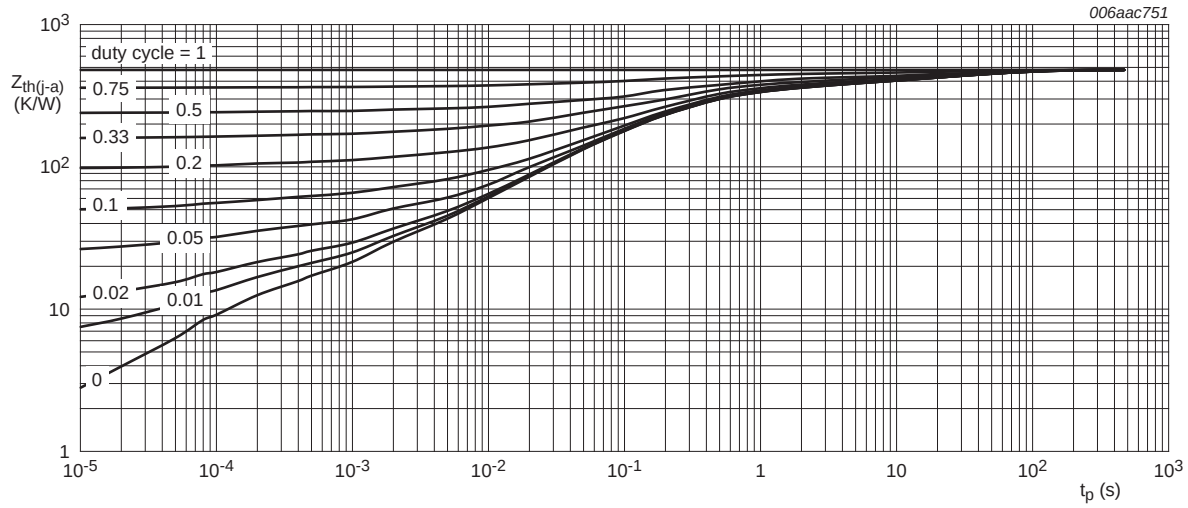


SOT363 and SOT666; FR4 PCB, standard footprint

Fig 1. Per device: Power derating curve

6. Thermal characteristics



FR4 PCB, standard footprint

Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration for PEMD48 (SOT666); typical values

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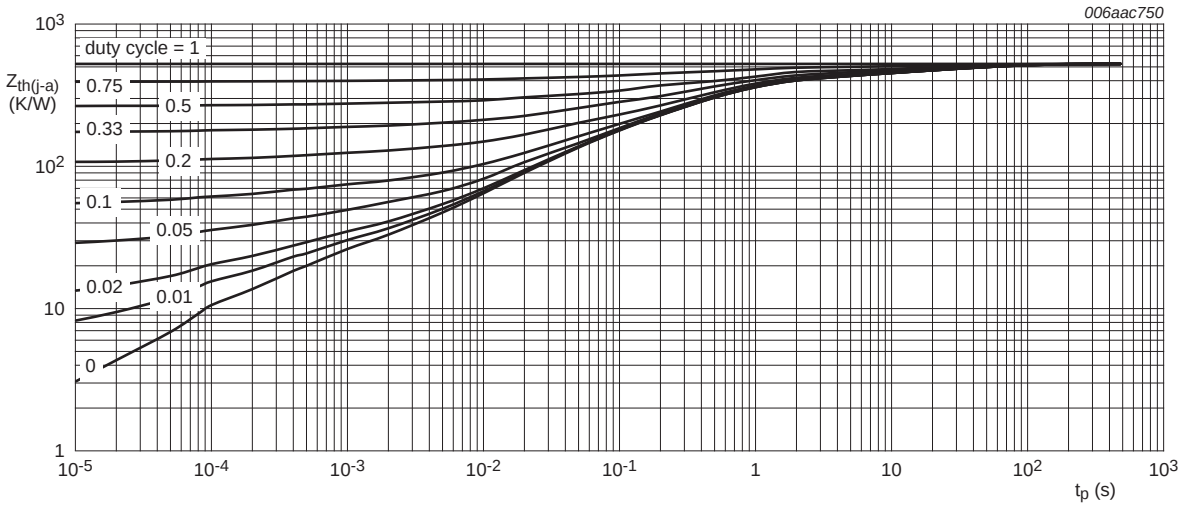

FR4 PCB, standard footprint

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration for PUMD48 (SOT363); typical values

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25$ °C					
	PEMD48 (SOT666)		[1][2]	-	-	625	K/W
	PUMD48 (SOT363)		[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	$T_{amb} \leq 25$ °C					
	PEMD48 (SOT666)		[1][2]	-	-	417	K/W
	PUMD48 (SOT363)		[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.

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7. Characteristics

Table 8. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor; for the PNP transistor with negative polarity							
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A		-	-	1	μA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	5	μA
Transistor TR1 (NPN)							
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 A		-	-	90	μA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA		80	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 10 mA; I_B = 0.5 mA		-	-	150	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 μA		-	1.2	0.8	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 2 mA		3	1.6	-	V
R1	bias resistor 1 (input)			33	47	61	kΩ
R2/R1	bias resistor ratio			0.8	1.0	1.2	
C_c	collector capacitance	V_{CB} = 10 V; I_E = i_e = 0 A; f = 1 MHz		-	-	2.5	pF
f_T	transition frequency	V_{CB} = 5 V; I_C = 10 mA; f = 100 MHz	[1]	-	230	-	MHz
Transistor TR2 (PNP)							
I_{EBO}	emitter-base cut-off current	V_{EB} = –5 V; I_C = 0 A		-	-	–180	μA
h_{FE}	DC current gain	V_{CE} = –5 V; I_C = –10 mA		100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = –5 mA; I_B = –0.25 mA		-	-	–100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = –5 V; I_C = –100 μA		-	–0.6	–0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = –0.3 V; I_C = –5 mA		–1.1	–0.75	-	V
R1	bias resistor 1 (input)			1.54	2.20	2.86	kΩ
R2/R1	bias resistor ratio			17	21	26	
C_c	collector capacitance	V_{CB} = –10 V; I_E = i_e = 0 A; f = 1 MHz		-	-	3	pF
f_T	transition frequency	V_{CB} = -5 V; I_C = -10 mA; f = 100 MHz	[1]	-	180	-	MHz

[1] Characteristics of built-in transistor.

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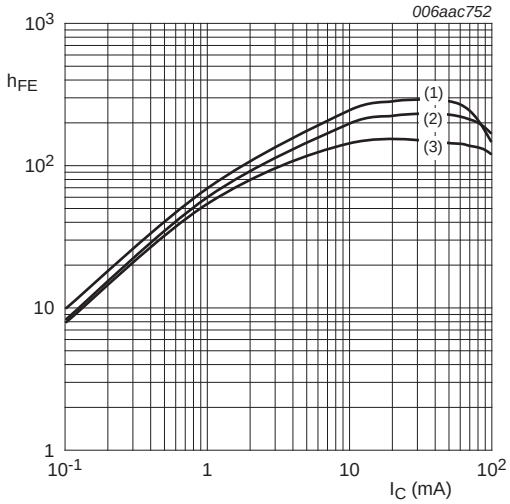


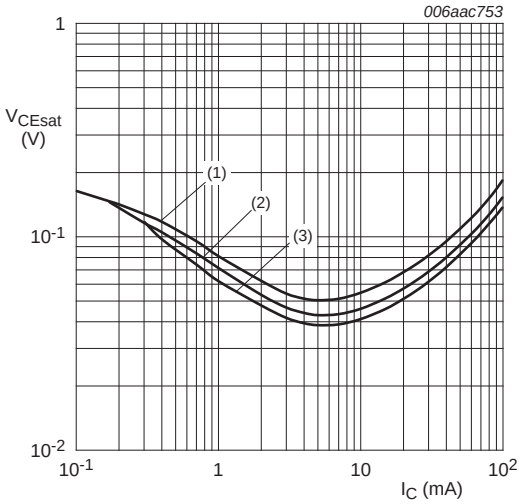
V_{CE} = 5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 4. TR1 (NPN): DC current gain as a function of collector current; typical values



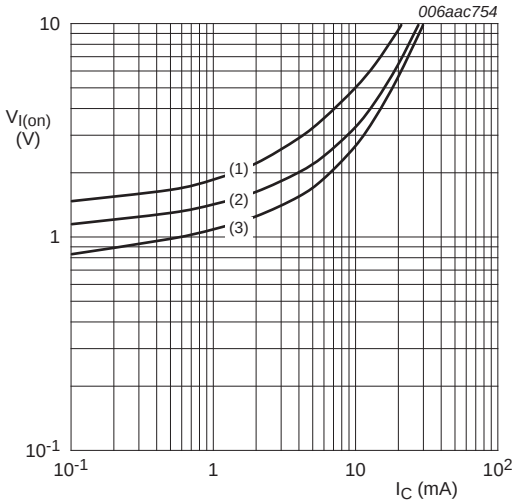
I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



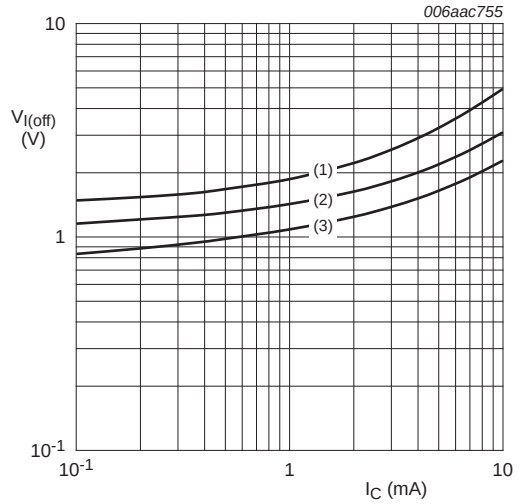
V_{CE} = 0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values



V_{CE} = 5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

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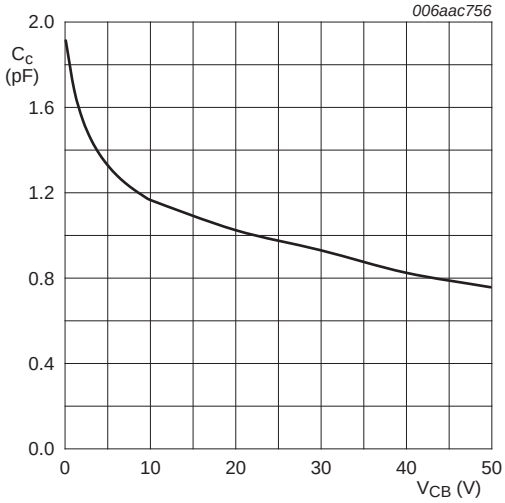
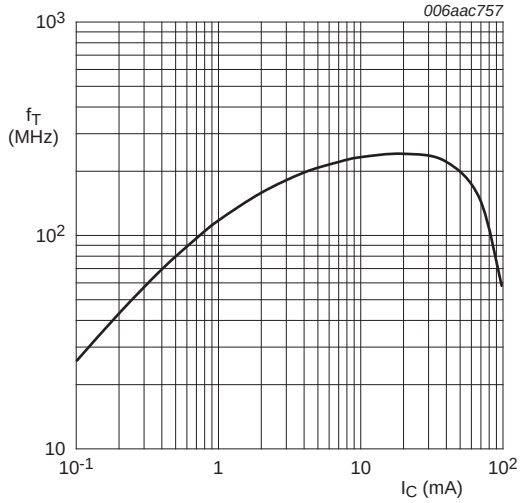


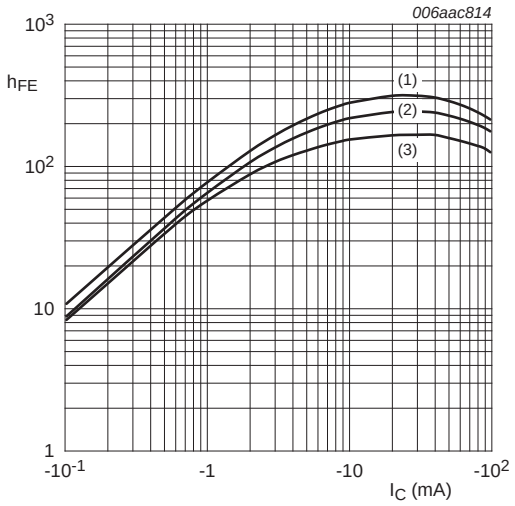
f = 1 MHz; T_{amb} = 25 °C

Fig 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values



V_{CE} = 5 V; T_{amb} = 25 °C

Fig 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



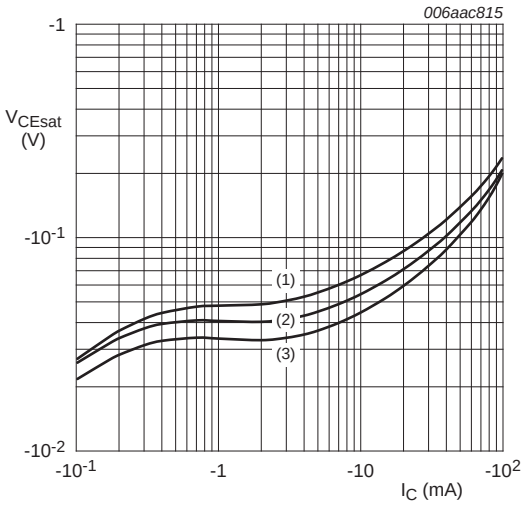
V_{CE} = −5 V

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 10. TR2 (PNP): DC current gain as a function of collector current; typical values



I_C/I_B = 20

(1) T_{amb} = 100 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = −40 °C

Fig 11. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

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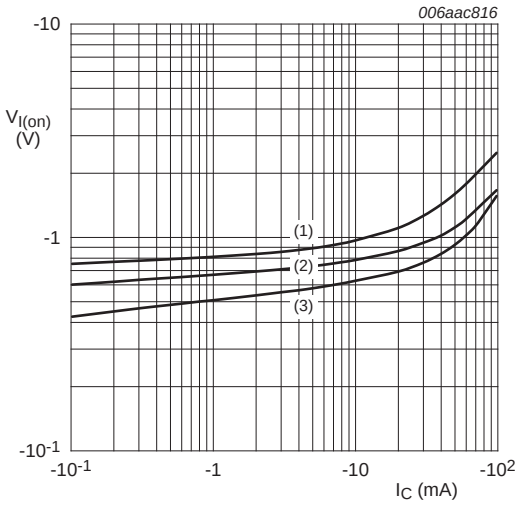


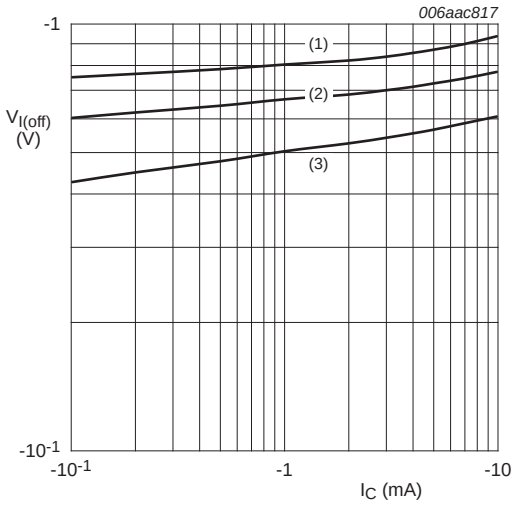
V_{CE} = −0.3 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

(3) T_{amb} = 100 °C

Fig 12. TR2 (PNP): On-state input voltage as a function of collector current; typical values



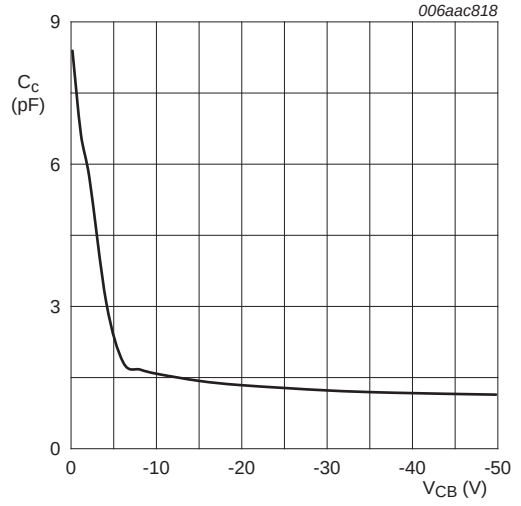
V_{CE} = −5 V

(1) T_{amb} = −40 °C

(2) T_{amb} = 25 °C

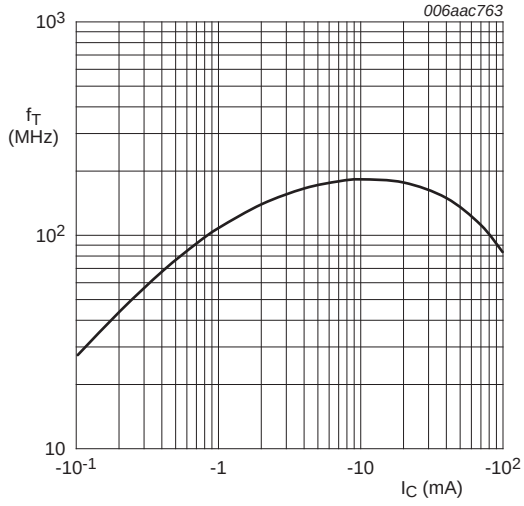
(3) T_{amb} = 100 °C

Fig 13. TR2 (PNP): Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig 14. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values



V_{CE} = −5 V; T_{amb} = 25 °C

Fig 15. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

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8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

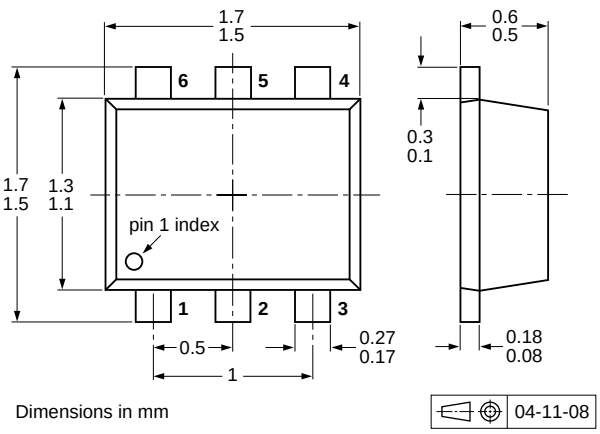

Fig 16. Package outline PEMD48 (SOT666)

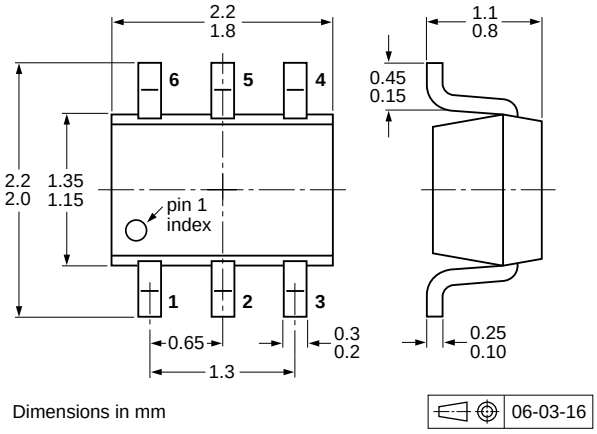

Fig 17. Package outline PUMD48 (SOT363/SC-88)

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10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.[1]

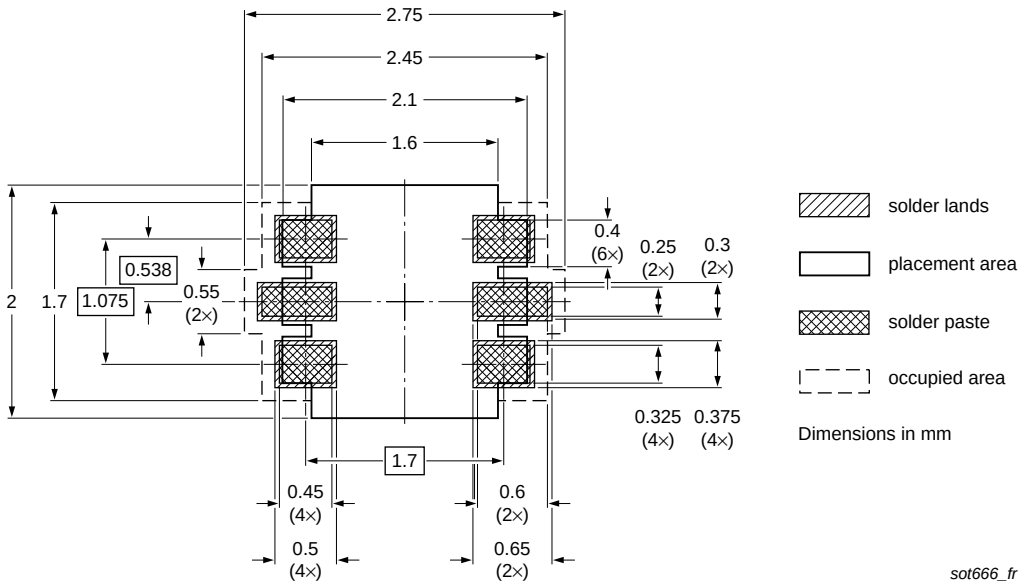
Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMD48	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMD48	SOT363	4 mm pitch, 8 mm tape and reel; T1 [2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 [3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see Section 14.

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering



Reflow soldering is the only recommended soldering method.

Fig 18. Reflow soldering footprint PEMD48 (SOT666)

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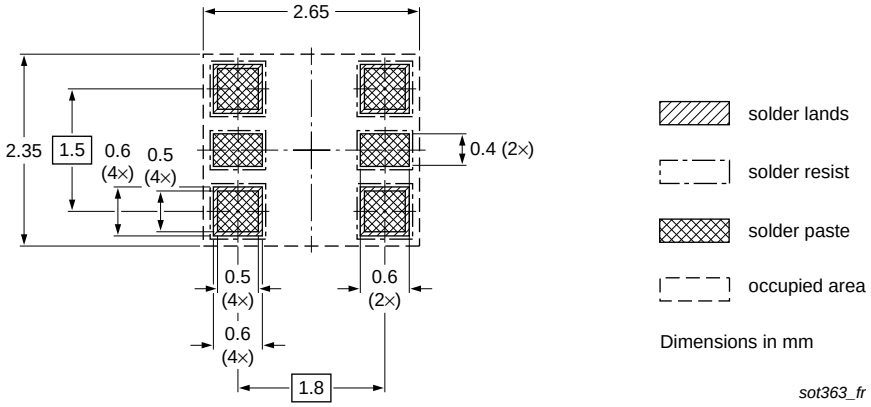

Fig 19. Reflow soldering footprint PUMD48 (SOT363/SC-88)

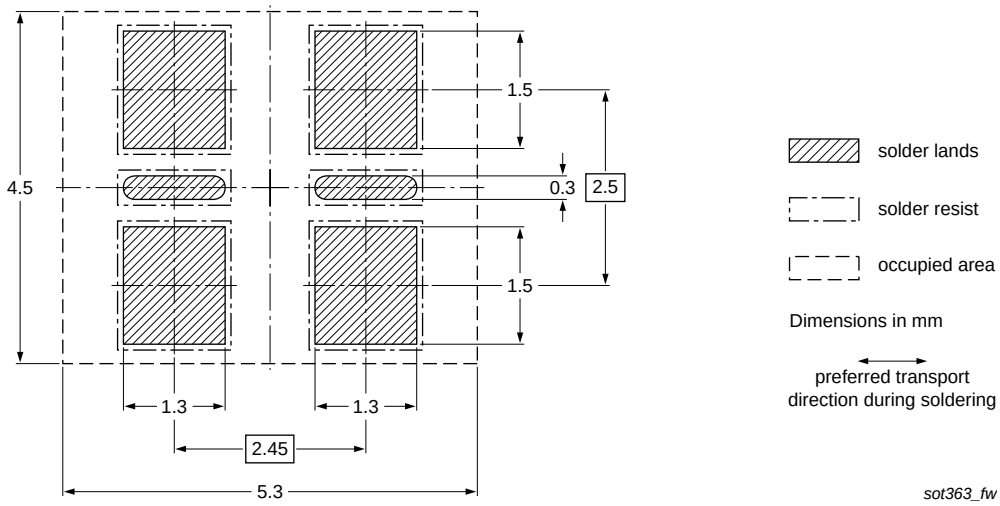

Fig 20. Wave soldering footprint PUMD48 (SOT363/SC-88)

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12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD48_PUMD48 v.6	20120124	Product data sheet	-	PEMD48_PUMD48 v.5
Modifications:	• Section 1 “Product profile”: updated • Section 4 “Marking”: updated • Table 7 “Thermal characteristics”: updated according to the latest measurements • Table 6 “Limiting values”: updated according to the latest measurements • Table 8 “Characteristics”: I_{CEO} updated according to the latest measurements, f_T added • Figure 1 to 3, 8, 9, 14 and 15: added • Figure 4 to 7 and Figure 10 to 13: updated • Section 8 “Test information”: added • Section 11 “Soldering”: added • Section 13 “Legal information”: updated			
PEMD48_PUMD48 v.5	20100413	Product data sheet	-	PEMD48_PUMD48 v.4
PEMD48_PUMD48 v.4	20040624	Product specification	-	PEMD48_PUMD48 v.3
PEMD48_PUMD48 v.3	20040602	Product specification	-	PEMD48 v.2 PUMD48 v.2
PUMD48 v.2	20010201	Product specification		PUMD48 v.1
PUMD48 v.1	19990422	Product specification		-
PEMD48 v.2	20011107	Product specification		PEMD48 v.1
PEMD48 v.1	20010924	Preliminary specification	-	-

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13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For more information, please visit: **http://www.nxp.com**

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