Short Form Data Sheet
April 2012

MAX24288

IEEE 1588 Packet Timestamper and Clock and 1Gbps Parallel-to-Serial MII Converter

General Description

The MAX24288 is a flexible, low-cost IEEE 1588 clock and timestamper with an SGMII or 1000BASE-X serial interface and a parallel MII interface that can be configured for GMII, RGMII, or 10/100 MII. The device provides all required hardware support for high-accuracy time and frequency synchronization using the IEEE1588 Precision Time Protocol. In both the transmit and receive directions 1588 packets are identified and timestamped with high precision. System software makes use of these timestamps to determine the time offset between the system and its timing master. Software can then correct any time error by steering the device's 1588 clock subsystem appropriately. The device provides the necessary I/O to time-synchronize with a 1588 master elsewhere in the same system or to be the master to which slave components can synchronize.

In addition, the MAX24288 is a full-featured, gigabit parallel-to-serial MII converter. It provides full SGMII revision 1.8 compliance and also interfaces directly to 1Gbps 1000BASE-X SFP optical modules.

Applications

1588-Enabled Equipment with 1G Ethernet Ports
Wireless Base Stations and Controllers
Switches, Routers, DSLAMs, PON Equipment
Pseudowire Circuit Emulation Equipment
Test and Measurement Systems
Industrial and Factory Automation Equipment
Medical Equipment

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX24288ETK+	-40°C to +85°C	68 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

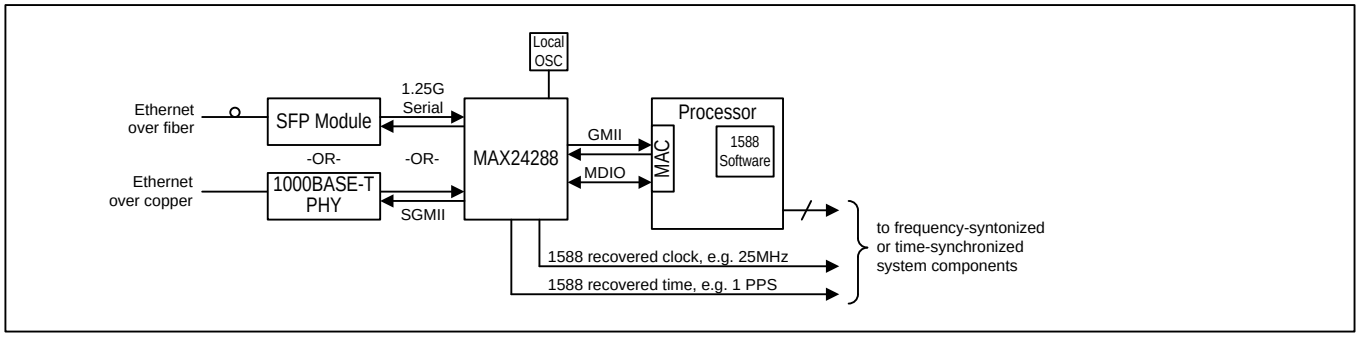
SPI is a trademark of Motorola, Inc.

Highlighted Features

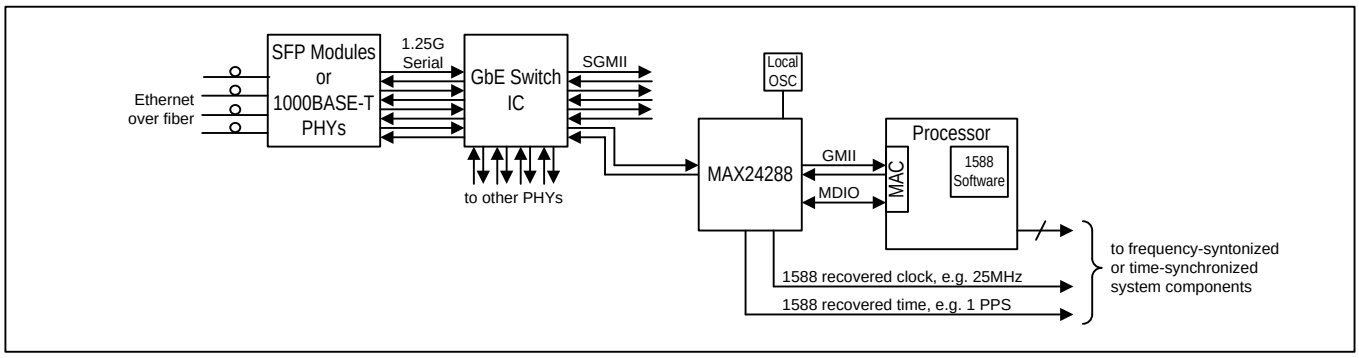
- **Complete Hardware Support for IEEE 1588**
- **Ordinary, Boundary, and Transparent Clocks**
- **Flexible Block for Any 1588 Architecture**
- **1588 Clock Hardware**
  - Steerable by Software with 2^{-8}ns Time Resolution and 2^{-32}ns Period Resolution
  - 1ns Input Timestamp Accuracy and Output Edge Placement Accuracy
  - Three Time/Frequency Controls: Direct Time Write, Time Adjustment, and High-Resolution Frequency Adjustment
  - Programmable Clock and Time-Alignment I/O
  - Input Event Timestamper Detects Incoming Time Alignment (e.g., 1 PPS) or Clock Edges
  - Output Event Generator Provides Output Clock Signal or Time Alignment Signal
  - Built-In Support for Telecom Equipment Timing Architecture with Dual Redundant Timing Cards
- **1588 Timestamping Hardware**
  - 1588 v1 and v2 Packets, Transmit and Receive
  - Packet Classifier Supports 1588 Over Ethernet, IPv4/UDP, IPv6/UDP, or MPLS and Is Programmable for More Complex Stacks
  - Supports 802.1Q VLAN Tags and MAC-in-MAC
  - One-Step Operation: On-the-Fly Timestamp Insertion or Transparent Clock Corrections; No Need for Follow-Up Packets
  - Can Insert All Timestamps, Receive **and** Transmit, Into Packets for Easy Software Access
  - Optional Two-Step Operation
- **Parallel-to-Serial MII Conversion**
  - Bidirectional Wire-Speed Interface Conversion
  - Serial: 1000BASE-X or SGMII v1.8 (4, 6, or 8 Pin)
  - Parallel: GMII, RGMII, or 10/100 MII
  - Translates Link Speed and Duplex Mode Negotiation Between MDIO and SGMII PCS
- **Full Support for 1588 + Synchronous Ethernet**
- **MDIO and SPI™ Interfaces**
- **1.2V Operation with 3.3V I/O**

Application Examples

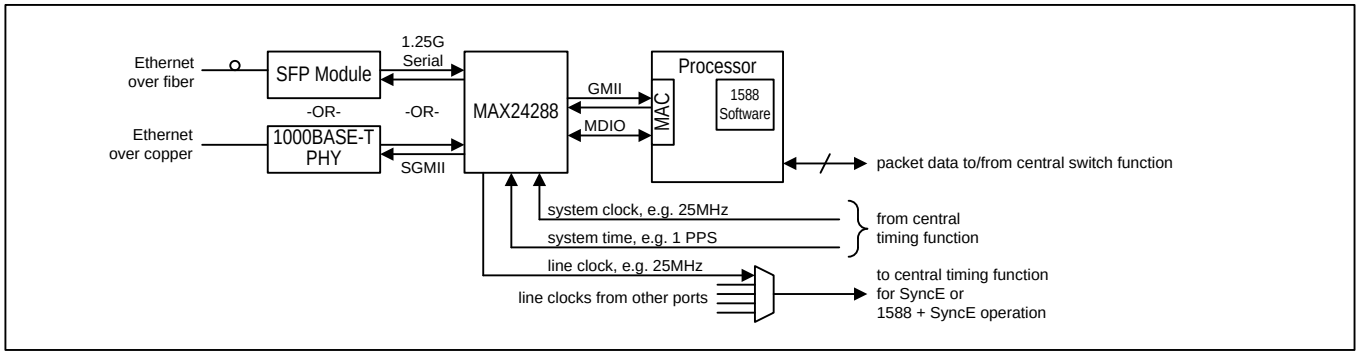
Example 1: Single-Port 1588 Slave Node



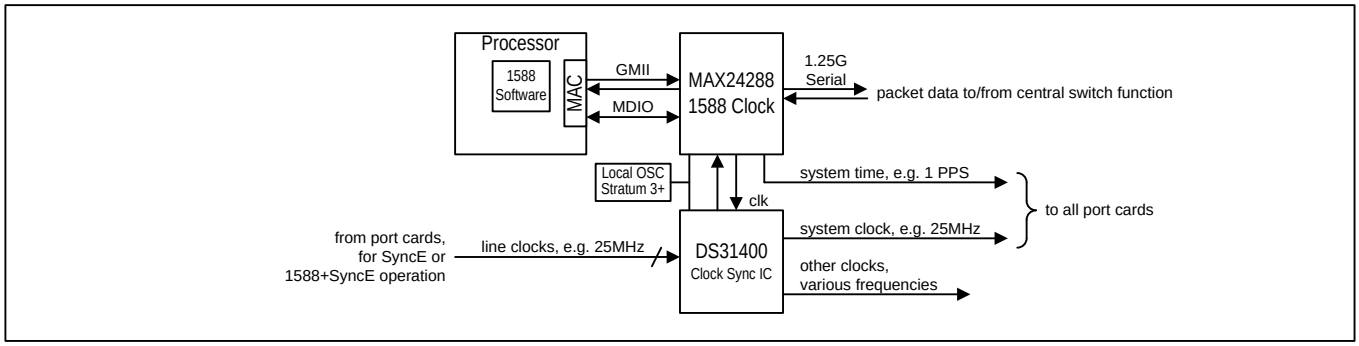
Example 2: Multiport System with Switch-Connected 1588 Slave Node



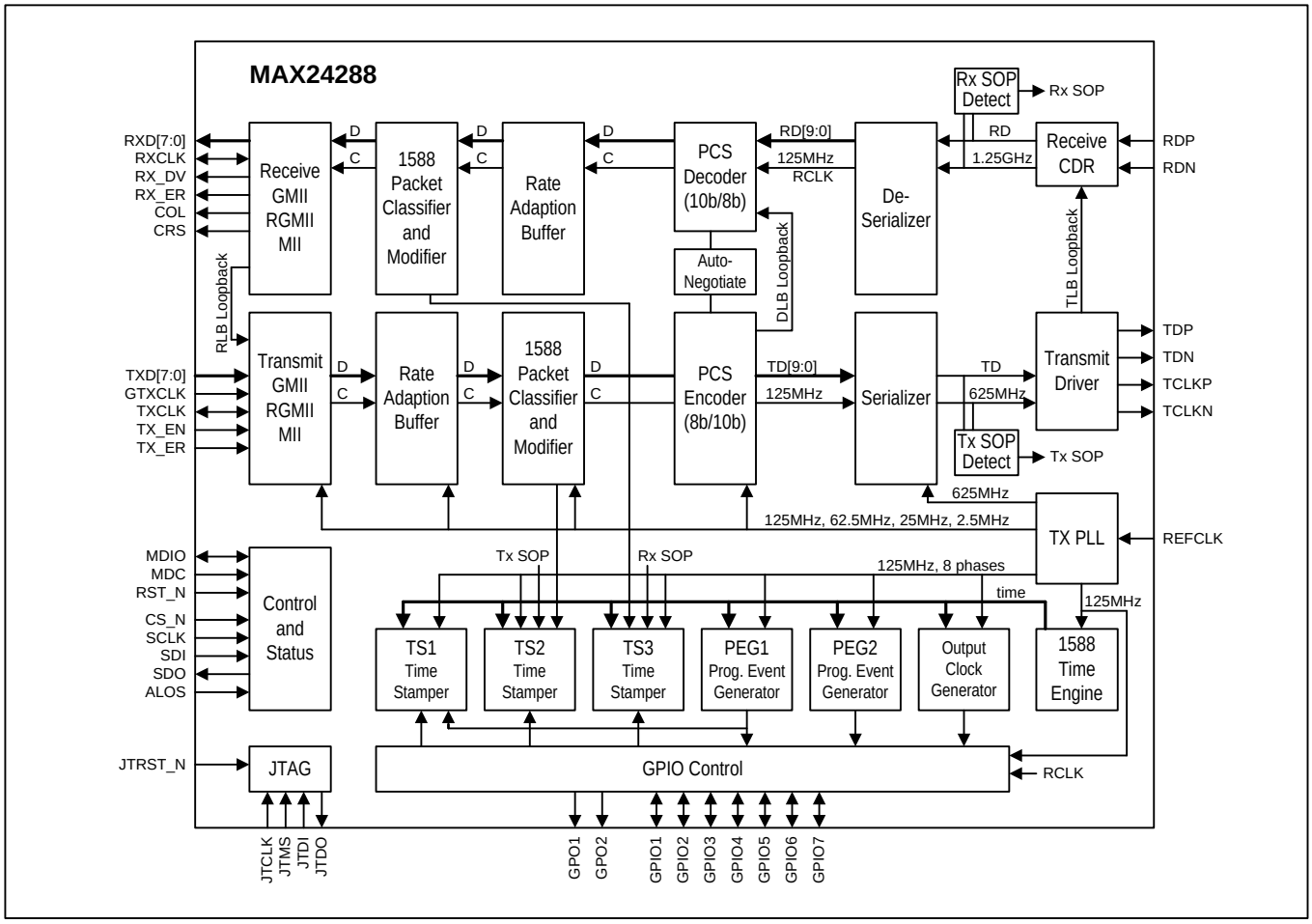
Example 3: Multiport System, Boundary or Transparent Clock, Port Card Logic



Example 4: Multiport System, Boundary or Transparent Clock, Central Timing Function



Block Diagram



Detailed Features

General Features

- Control and status through MDIO interface or SPI interface
- High-speed MDIO interface (12.5MHz slave only) with optional preamble suppression
- Optional SPI 4-wire serial microprocessor interface (25MHz, slave only)
- Operates from a 10, 12.8, 25, or 125MHz reference clock
- Optional 125MHz output clock for MAC to use as GTXCLK

Parallel-Serial MII Conversion Features

- Bidirectional wire-speed interface conversion
- Serial Interface: 1000BASE-X or SGMII revision 1.8 (4, 6, or 8 Pins)
- Parallel Interface: GMII, RGMII (10, 100, and 1000Mbps) or 10/100 MII (DTE or DCE)
- 8-pin source-clocked SGMII mode
- 4-pin 1000BASE-X SerDes mode to interface with optical modules
- Connects processors with parallel MII interfaces to 1000BASE-X SFP optical modules
- Connects processors with parallel MII interfaces to PHY or switch ICs with SGMII interfaces
- Interface conversion is transparent to MAC layer and higher layers
- Translates link speed and duplex mode between GMII/MII MDIO and SGMII PCS

1588 Clock Features

- Steerable by software with 2^{-8}ns time resolution and 2^{-32}ns period resolution
- 1ns input timestamp accuracy and output edge placement accuracy
- Initialized and steered by software on an external processor to follow an external 1588 master
- Three time/frequency controls: direct time write, time adjustment, and high-resolution frequency adjustment
- Programmable clock and time-alignment I/O to synchronize all boards in large systems
  - Can frequency-lock to an input clock signal from elsewhere in the system
  - Can timestamp an input time alignment signal to time-lock to a master elsewhere in the system (e.g., 1 PPS)
  - Can provide an output clock signal to slave components elsewhere in the system (125MHz/N , 1 ≤ N ≤ 255)
  - Can provide an output time alignment signal to slave components elsewhere in the system (e.g., 1 PPS)
- Input signal timestamper can stamp rising edges, falling edges or both
- Flexible programmable event generator (PEG) can output 1 PPS, one pulse per period, and a wide variety of clock signals
- Full support for dual redundant timing cards to match architecture used in SONET/SDH
- Full support for switches and routers as transparent clocks or boundary clocks
- Compatible with a wide variety of 1588 system architectures

1588 Timestamper Features

- Identifies and timestamps 1588 v1 and v2 packets in both transmit and receive directions
- Programmable packet classifier can identify packets transported by a variety of protocol stacks
  - 1588 over Ethernet
  - 1588 over IPv4/UDP
  - 1588 over IPv6/UDP
  - 1588 over MPLS
  - Configurable for more complex stacks as well
  - Recognizes 802.1Q VLAN tags and 802.1ah MAC-in-MAC
  - Can be configured to identify CESoP or SAToP for timing over adaptive-mode circuit emulation
- Transmit and receive timestamping with 1ns resolution
- One-step operation minimizes network bandwidth consumption
  - On-the-fly timestamp insertion
  - On-the-fly corrections in transparent clocks
  - No need for follow-up packets
- Can insert ALL timestamps (receive **and** transmit) into packets for easy software access
  - Three insert methods: direct overwrite, read-add-write, and read-subtract-write
  - Eliminates reads from timestamp FIFOs
  - Minimizes processor bus traffic
- Optional two-step operation
- Optional 8-entry timestamp FIFOs

Synchronous Ethernet Features

- Full support for 1588 over Synchronous Ethernet
- Receive path bit clock can be output on a GPIO pin to line-time the system from the Ethernet port
- Transmit path can be frequency-locked to a system clock signal connected to the REFCLK pin

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