

RTKA2108502H00000BU

User's Manual: Evaluation Board

Industrial Analog and Power

RTKA2108502H00000BU

Evaluation Board

UG178
Rev.0.00
Sept 12, 2018

1. Overview

The RTKA2108502H00000BU evaluation board is a 8-layer FR4 board with 2oz. copper on all layers. The board measures 4.7in x 4.8in. The evaluation board includes placeholders for the pin-strap resistor population that allow for the adjustment of the output voltage, switching frequency, soft-start/stop timing, input UVLO, ASCR (Gain and Residual) parameters, and the device PMBus address. Also, fault limits can be programmed or changed easily with the PMBus compliant serial bus interface.

The evaluation board makes use of the [RAA210850](#), a 50A step-down DC/DC power supply module with an integrated digital PWM controller, dual-phase synchronous power switches, inductors, and passives. Only input, output capacitors and minimal passives are required to finish the design. The board can output a continuous current at 50A without airflow or heatsink. The RAA210850 uses a ChargeMode™ control (ASCR) architecture that responds to a transient load within a single switching cycle.

Provided with the evaluation kit, the ZLUSBEVAL3Z (a USB to PMBus adapter) connects the evaluation board with a PC to activate the PMBus communication interface. The PMBus command set is accessed by using the [PowerNavigator™](#) evaluation software from a PC running Microsoft Windows.

The RTKA2108502H00000BU can operate in Pin-Strap mode without needing the ZLUSBEVAL3Z adapter or PMBus communication.

1.1 Key Features

- V_{IN} range of 4.5V to 14V, V_{OUT} adjustable from 0.6V to 5V
- Programmable V_{OUT} , input and output UVP/OVP, OTP/UTP, soft-start/stop, and external synchronization
- Monitor: V_{IN} , V_{OUT} , I_{OUT} , temperature, duty cycle, switching frequency, and faults
- ChargeMode control tunable with PMBus
- Mechanical switch for enable and a power-good LED indicator

1.2 Specifications

The board has default configurations for the following operating conditions:

- V_{IN} = 4.5V to 12V
- V_{OUT} = 1.2V
- I_{MAX} = 50A
- f_{SW} = 421kHz
- Peak efficiency: >91% at 70% load
- ASCR gain = 200, ASCR residual = 90
- On/off delay = 5ms, On/off ramp time = 5ms

1.3 Ordering Information

Part Number	Description
RTKA2108502H00000BU	RAA210850 Kit (Evaluation Board, ZLUSBEVAL3Z Adapter, USB Cable)

1.4 Related Literature

For a full list of related documents, visit our website.

- [RAA210850](#) product page

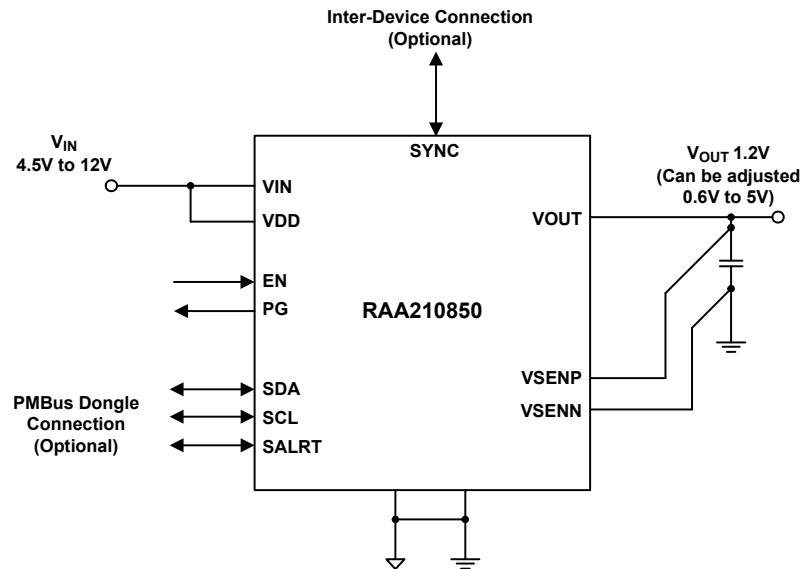


Figure 1. Block Diagram

1.5 Recommended Equipment

- DC power supply with minimum 15V/25A sourcing capacity
- Electronic load capable of sinking current up to 50A
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

2. Functional Description

The RTKA2108502H00000BU provides all circuitry required to evaluate the features of the RAA210850. A majority of the features of the RAA210850 are available on the RTKA2108502H00000BU evaluation board, such as compensation-free ChargeMode control and soft-start delay and ramp times. For interleave functionality evaluation, the board can connect to another Renesas digital module evaluation board.

[Figures 5](#) and [6](#) show the board images of the RTKA2108502H00000BU evaluation board.

2.1 Operating Range

By default, the RTKA2108502H00000BU is configured to operate at $V_{OUT} = 1.2V$, $f_{SW} = 421kHz$. V_{IN} ranges from 4.5V to 12V. The board can also support a wider operating range to meet the requirements of specific applications. The V_{OUT} can be adjusted from 0.6V to 5V. Load current range is 0A to 50A. Note that airflow across the board may be needed for continuous operation at 50A at elevated ambient temperatures. The f_{SW} and output voltage can also be tuned. However, to ensure sufficient stability margins, switching frequency and output capacitors can only be selected using the “RAA210850 Design Guide Matrix and Output Voltage Response” table in the [RAA210850](#) datasheet. If input voltage is less than 5V, tie the VDRV/VCC test point directly to V_{IN} or to a separate 5V power supply for normal operation and best efficiency.

If external synchronization is used, connect the SYNC test point to the external clock. Note that the external clock signal should be active before the module is enabled.

2.2 Quick Start Guide

2.2.1 Pin-Strap Option

RTKA2108502H00000BU can be configured in pin-strap mode with standard 1% 0603 resistors. The PMBus interface is not required to evaluate the RAA210850 in pin-strap mode. The output voltage (V_{OUT}), switching frequency (f_{SW}), soft-start/stop delay and ramp time, input undervoltage protection (UVLO) threshold, Interleave, ASCR gain and residual, and the device PMBus address can be changed by populating recommended resistors at placeholders provided in the evaluation board. By default, the evaluation board operates in Pin-Strap mode and regulates at $V_{OUT} = 1.2V$, $f_{SW} = 421kHz$, soft-start/stop delay time = 5ms, soft-start/stop ramp time = 5ms, UVLO = 4.2V, ASCR gain = 200, ASCR residual = 90, and PMBus address = 28h. Complete the following steps to evaluate the RAA210870 in Pin-Strap mode.

Complete the following steps to evaluate the RAA210850 in Pin-Strap mode.

- (1) Set the ENABLE switch to “DISABLE”.
- (2) Connect the load to the VOUT lug connectors (J_7 - J_8 and J_9 - J_{10}).
- (3) Connect the power supply to the VIN connectors (J_5 and J_6). Make sure the power supply is not enabled when making the connection.
- (4) Turn on the power supply.
- (5) Set the ENABLE switch to “ENABLE”.
- (6) Measure 1.2V V_{OUT} at the probe point labeled “VOUT REGULATION MONITOR” (J_{11}).
- (7) Observe the switching frequency of 421kHz at the probe points labeled PHASE1 (TP_{10}) and PHASE2 (TP_{11}).
- (8) To measure the module efficiency, connect the multimeter voltage probes at probe points labeled VIN (TP_1), GND (TP_2), and VOUT (TP_{12}).
- (9) To change the V_{OUT} , disconnect the board from the setup and populate a 1% standard 0603 resistor at the RVSET_CRS placeholder location on bottom layer. If additional output voltage fine tuning is required then populate a resistor at the RVSET_FINE placeholder. Refer to the “Output Voltage Selection” section in the [RAA210850](#) datasheet to determine the correct selection of resistors for programming the output voltage. By default, V_{OUT_MAX} is set to 110% of V_{OUT} set by pin-strap resistor.

- (10) To change the switching frequency, disconnect the board from the setup and populate a 1% standard 0603 resistor at the RFSET placeholder on the bottom layer. For recommended resistor values, refer to the “Switching Frequency and PLL” section in the [RAA210850](#) datasheet.
- (11) To change the soft-start/stop delay and ramp time, disconnect the board from the setup and populate a 1% standard 0603 resistor at the bottom layer R₆ placeholder location. For the recommended resistor values, refer to the “Soft-Start/Stop Delay, and Ramp Times” section in the [RAA210850](#) datasheet.
- (12) To change the UVLO, disconnect the board from the setup and populate a 1% standard 0603 resistor on the bottom layer R₆ placeholder. Notice that the UVLO programming shares the same pin with the soft-start/stop programming. For the recommended resistor values, refer to the “Input Undervoltage Lockout (UVLO)” section in the [RAA210850](#) datasheet.
- (13) To change the ASCR gain and residual, disconnect the board from the setup and populate a 1% standard 0603 resistor on the bottom layer R₇ placeholder location. For the recommended resistor values, refer to the “Loop Compensation” and the design guide matrix in the [RAA210850](#) datasheet.

2.2.2 PMBus Option

The features of the RTKA2108502H00000BU can be evaluated using the provided ZLUSBEVAL3Z dongle and PowerNavigator evaluation software. Follow these steps to evaluate the RAA210850 with PMBus option.

- (1) Install PowerNavigator from the [Renesas website](#).
- (2) Set the ENABE switch to “DISABLE”.
- (3) Connect the load to the VOUT lug connectors (J₇-J₈ and J₉-J₁₀).
- (4) Connect the power supply to the VIN connectors (J₅ and J₆). Make sure the power supply is not enabled when making the connection.
- (5) Turn on the power supply.
- (6) Connect the ZLUSBEVAL3Z dongle (USB to PMBus adapter) to the RTKA2108502H00000BU board with the 6-pin male connector labeled “PMBus DONGLE IN”.
- (7) Connect the supplied USB cable from the computer USB to the ZLUSBEVAL3Z dongle.
- (8) Launch PowerNavigator.
- (9) By factory default, the RAA210850 device on the board operates in Pin-Strap mode, but the user can modify the operating parameters with PowerNavigator. The default pin-strap configurations are overwritten if PowerNavigator is used.
- (10) Set the ENABLE switch to “ENABLE”. Alternatively, the PMBus ON_OFF_CONFIG and OPERATION commands may be used from the PowerNavigator™ software for enabling the module.
- (11) Monitor and configure the RTKA2108502H00000BU board using the PMBus commands in PowerNavigator.
- (12) PowerNavigator tutorial videos are available at the [Renesas website](#).
- (13) For evaluating Interleave functionality for multiple Renesas digital power products using a single ZLUSBEVAL3Z dongle, RAA210850 can be daisy chained with other digital power evaluation boards. The PMBus address can be changed by placing a 1% standard 0603 resistor at the R4 placeholder location on the bottom layer. Refer to the “SMBus Module Address Selection” section in the [RAA210850](#) datasheet for recommended values.

3. Evaluation Board Information

If the input voltage is less than 5.3V, tie the VCC test point directly to the VIN, or for operational efficiency, tie the VCC test point to a separate 5V power supply. For external synchronization, connect the SYNC test point to the external clock.

Note: The external clock signal should be active before the module is enabled.

3.1 External Clock Synchronization

The RAA210850 can synchronize to an external clock. External clock synchronization allows the user to operate multiple converters at the same switching frequency and can lead to improved EMI characteristics. The RTKA2108502H00000BU evaluation board can assess this functionality. A function generator is required. Complete the following steps to operate RAA210850 with an external clock frequency of 593kHz:

- (1) Set the Enable switch to "DISABLE" position.
- (2) Solder a 17.8k Ω resistor at RSET on the CFG pin (R₁₃).
- (3) Program the function generator to output a continuous square pulse waveform of 593kHz. Program the pulse width to be at least 150ns.
- (4) Ensure that the clock signal is stable by monitoring the waveform on an oscilloscope.
- (5) After verifying clock stability, connect the output cables from the function generator to test points TP₃ (labeled "SYNC").
- (6) Turn the output of the function generator ON.
- (7) Enable the module by setting the Enable switch to "ENABLE".
- (8) Observe the switching frequency at test points TP₁₀ "PHASE1" and TP₁₁ "PHASE2".
- (9) The module synchronizes to the 593kHz external clock from the function generator.
- (10) Ensure that the module is always disabled before changing the frequency of the external clock.
- (11) Loss of Sync fault is generated when the external clock is lost.

3.2 Bode Plot Measurement

Assessing the stability of the converter is an important step in the design process. Bode plots can be a useful and reliable tool to identify the loop response of the converter. Phase and gain margins give an insight into the stability of the system. Bandwidth can indicate how quickly the converter responds to disturbances in input voltage or load transients. Correctly measuring the loop response is critical for designing stable converter systems.

A network analyzer is required to perform the frequency response measurements on the RTKA2108502H00000BU evaluation board. Complete the following steps to evaluate the converter loop response for RAA210850 on the RTKA2108502H00000BU evaluation board.

- (1) Break the feedback loop by removing the R₁₀ resistor in remote sense path, connected between VSEN and VOUT.
- (2) Solder a 20 Ω resistor in its place. The value of the resistor could be in the range 10 Ω to 50 Ω .
- (3) Solder a twisted wire pair to the 20 Ω resistor. Ensure that the wires are short in length. A small twisted pair works well by minimizing noise pickup, which is important for a good measurement.
- (4) Enable the converter.
- (5) Use a Network Analyzer to inject a small AC signal (~20mV) across the 20 Ω resistor as shown in [Figure 2 on page 7](#).
- (6) Measure the amplitudes of the signals at points A and B as shown in [Figure 2](#).
- (7) Sweep the frequency using the Network Analyzer to observe the bandwidth and the phase and gain margins.

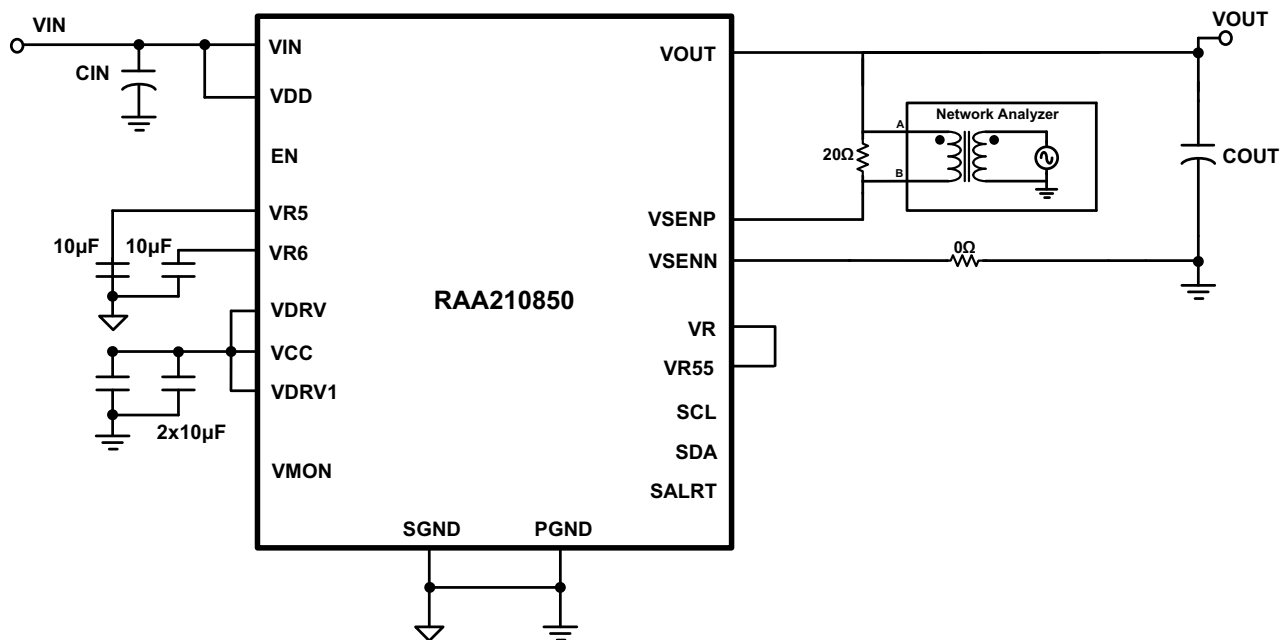


Figure 2. Schematic for Evaluating a Converter Loop Response

[Figure 3](#) shows an example bode plot generated by the Network Analyzer for RAA210850 at 12V input, 1.2V output, and 50A load at 727kHz with 8x100µF ceramic + 2x470µF POS output capacitors. The ASCR gain is set at 320, and the ASCR residual is set at 90. The plot shows a crossover frequency of 70kHz with a phase margin of 64°. A 10dB gain margin is observed at 194kHz.

Refer to the RAA210850 Design Guide Matrix and Output Voltage Response Table in the [RAA210850](#) datasheet for detailed design guidelines. The guidelines include a selection of input/output capacitors and different ASCR gain and residual values.

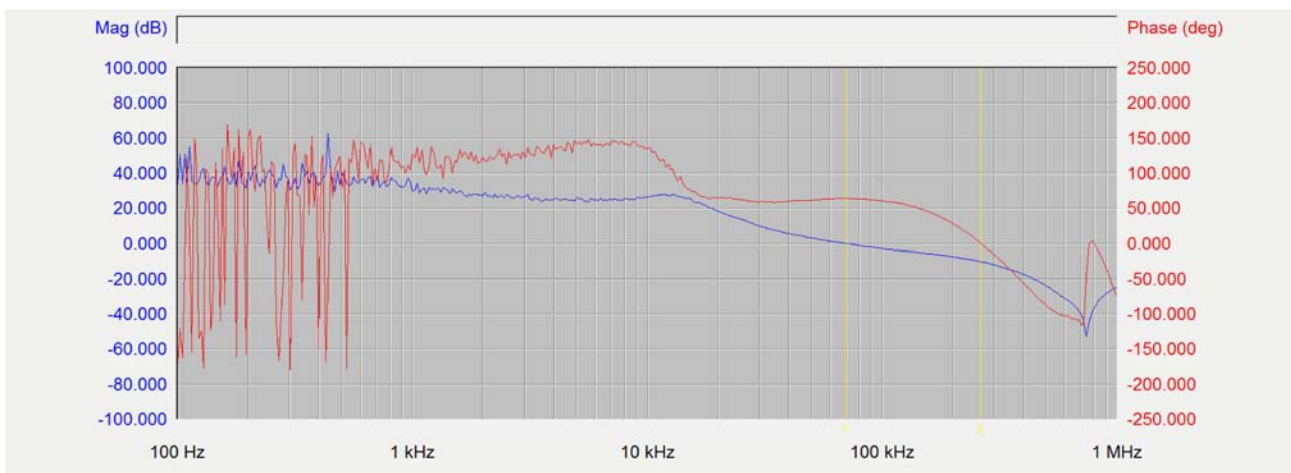


Figure 3. Generated Bode Plot by the Network Analyzer for RAA210850

3.3 Interleave Operation

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device, so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the

peak current drawn at any given moment is reduced. In fact, the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading in a multi-module operation, all converters must be synchronized to the same switching clock. The phase offset of each device may be set to any value between 0° and 360° in 22.5° increments by choosing the device SMBus address from the “Interleave” table in the [RAA210850](#) datasheet. The lower 4 bits of the SMBus address set the value of INTERLEAVE command. Complete the following steps to implement interleave functionality for a two module operation:

- (1) Choose SA (SMBus Address) for Module 1 and Module 2 from the “Interleave” table in the [RAA210850](#) datasheet based on the desired phase difference. Populate the corresponding RSET for SA (R4) according to the “SMBus Address Resistor Selection” table in the [RAA210850](#) datasheet.
For example, when Module 1 has SA = 28h (INTERLEAVE = 8, 180° phase shift from the rising edge of the external clock) and Module 2 has SA = 24h (INTERLEAVE = 4, 90° phase shift from the rising edge of the external clock), the net phase difference between Module 1 and Module 2 will be $180 - 90 = 90^\circ$.
- (2) Populate RSET on CFG pin for both boards to sync to an external clock source of a particular switching frequency based on the “External Frequency Sync Settings” table in the [RAA210850](#) datasheet.
- (3) Connect the power supply to the VIN connectors (VIN/GND) on both the boards.
- (4) Connect the ZLUSBEVAL3Z dongle to the 6-pin male connector labeled "PMBus DONGLE In" to one of the boards.
- (5) Daisy chain the second board to the first board by connecting "PMBus DONGLE Out" of first board to the "PMBus DONGLE In" of the second board.
- (6) Provide an external clock on the SYNC pins of the two boards from a function generator. External clock frequency from the function generator should be within $\pm 10\%$ of the listed options shown the “External Frequency Sync Settings” table in the [RAA210850](#) datasheet. Incoming clock signal must be stable before the enable pin is asserted. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns.
- (7) Turn the input power supply ON. Next, set the ENABLE switch to the "ENABLE" position.
- (8) Monitor the switch node at the probe point labeled PHASE1 (TP₁₀) on the two boards using an oscilloscope to verify the phase spread set.
- (9) This functionality can also be verified using the INTERLEAVE command in PowerNavigator.

Note: Every module is assigned a unique Rail ID based on the SA setting. These settings can be observed in the Power Map window of PowerNavigator.

3.4 V_{OUT} Transient Response Check

The RTKA2108502H00000BU board has a built-in transient load test circuit ([Figure 4](#)). A 100A N-Channel MOSFET (Manufacturer PN: BSC010NE2LSI) is connected across V_{OUT} and PGND next to the remote voltage sensing location (CVSEN). The $10\text{m}\Omega$ current-sense resistor R_{54} is used for monitoring the drain-to-source current of the MOSFET. For a transient load test, inject the gate drive pulse signal at J_{16} . The load current can be monitored through J_{15} . When the gate turn-on signal is applied, the MOSFET operates in the saturation region (not the linear region). To avoid MOSFET overheating, both the pulse width and duty cycle of the gate signal must be reduced (recommended duty cycle should be less than 2%). The amplitude of the gate driver pulse voltage can be adjusted to obtain the desired step size for a transient load current.

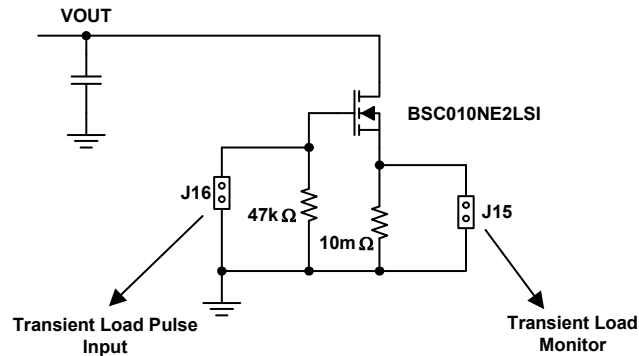


Figure 4. Schematic for Transient Load Measurement

4. PCB Layout Guidelines

The RTKA2108502H00000BU board layout has been optimized for electrical performance, low loss, and excellent thermal performance.

The following are the key features of the RTKA2108502H00000BU layout:

- Large PGND planes and a separate SGND plane, where the SGND plane is connected to PGND on the second layer with a single point connection. Multiple vias are used for small pins such as J₁₆, H₁₆, K₁₆, M₅, M₁₄, M₁₇, and N₅ to connect to inner SGND or PGND layer.
- Ceramic capacitors between VIN and PGND, VOUT and PGND, and bypass capacitors between VDD, VDRV and the ground plane are placed close to the module to minimize high frequency noise. Some output ceramic capacitors are placed close to the VOUT pads in the direction of the load current path to create a low impedance path for the high frequency inductor ripple current.
- Large copper areas are used for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Multiple vias are used to connect the power planes in different layers.
- Remote sensing traces are connected from the regulation point to VSEN_P and VSEN_N pins. The two traces are placed in parallel, to achieve tight output voltage regulation. The regulation point is on the right side of the board in between the VOUT power lugs and the PGND power lugs.
- Multiple vias are used to connect PAD14 and 16 (SW₁ and SW₂) to inner layers for better thermal performance. The inner layer SW1 and SW2 traces are limited in area and are surrounded by PGND planes to avoid noise coupling. Caution was taken that no sensitive traces, such as the remote sensing traces, were placed close to these noisy planes.
- SWD1 (L₃) and SWD2 (P₁₁) pins are connected to SW1 and SW2 pads respectively with short loop wires of 40mil width. The wire width should be at least 20mils.

4.1 Thermal Considerations and Current Derating

The board layout is critical for safely operating the module and delivering maximum allowed power. The board layout requires a proper design to maximize thermal performance in order to function in high temperature environments and carry large currents. A proper design requires a user to select enough trace width, copper weight, and the proper connectors.

The RTKA2108502H00000BU evaluation board is designed for running 50A at room temperature without additional cooling systems. However, if the output voltage increases or the board operates at elevated temperatures, the available current is derated. Refer to the derated current curves in the [RAA210850](#) datasheet to determine the maximum output current the evaluation board can safely supply. Θ_{JA} is measured by inserting a thermocouple inside the module to measure peak junction temperature.

4.2 RTKA2108502H00000BU Evaluation Board

Connect to ZLUSBEVAL3Z Dongle. For Multiple Board Evaluation, Connect to PMBus Dongle Out Connection of Other Board

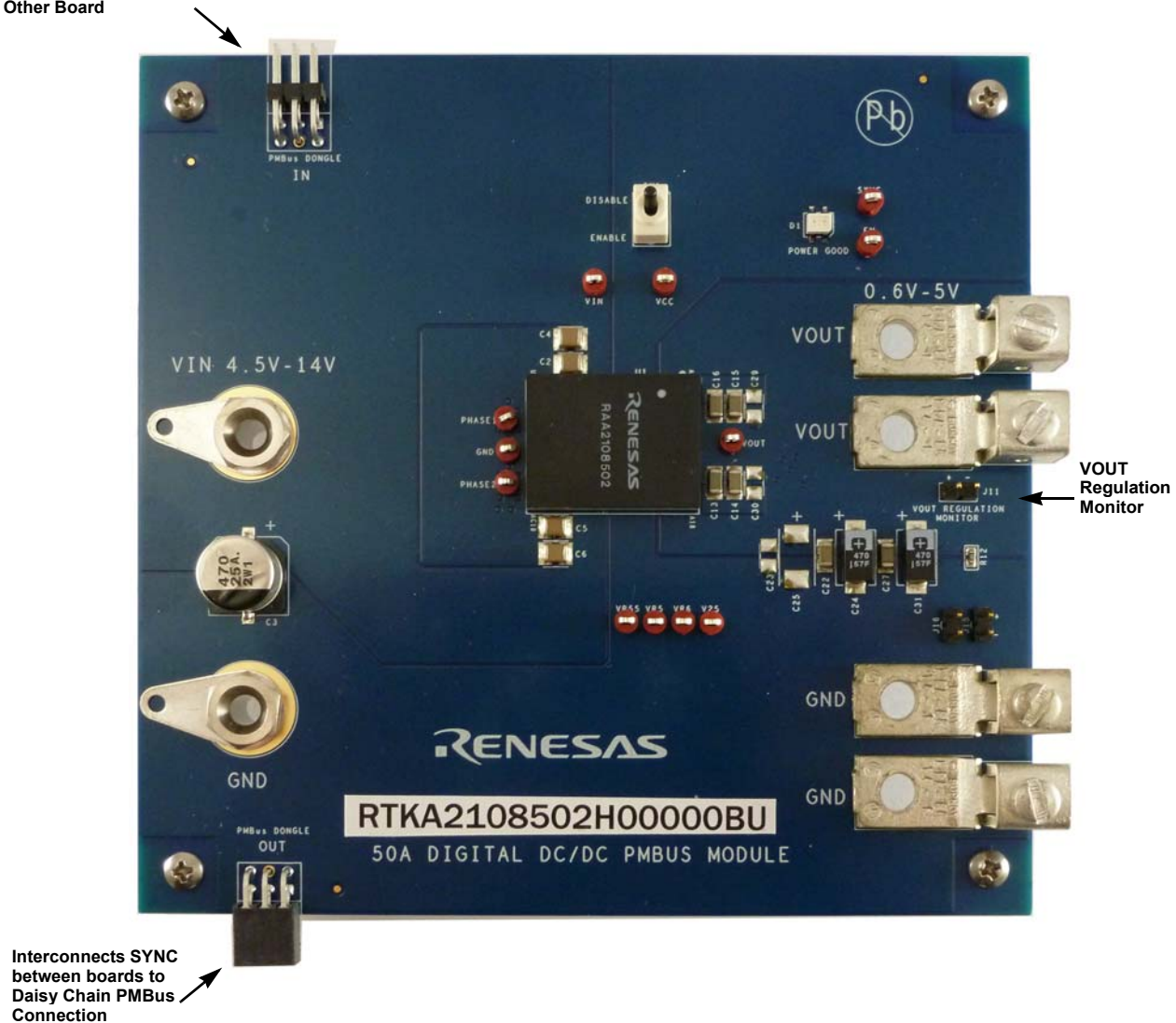


Figure 5. RTKA2108502H00000BU Evaluation Board (Top)



Figure 6. RTKA2108502H00000BU Evaluation Board (Bottom)

4.3 RTKA2108502H00000BU Circuit Schematic

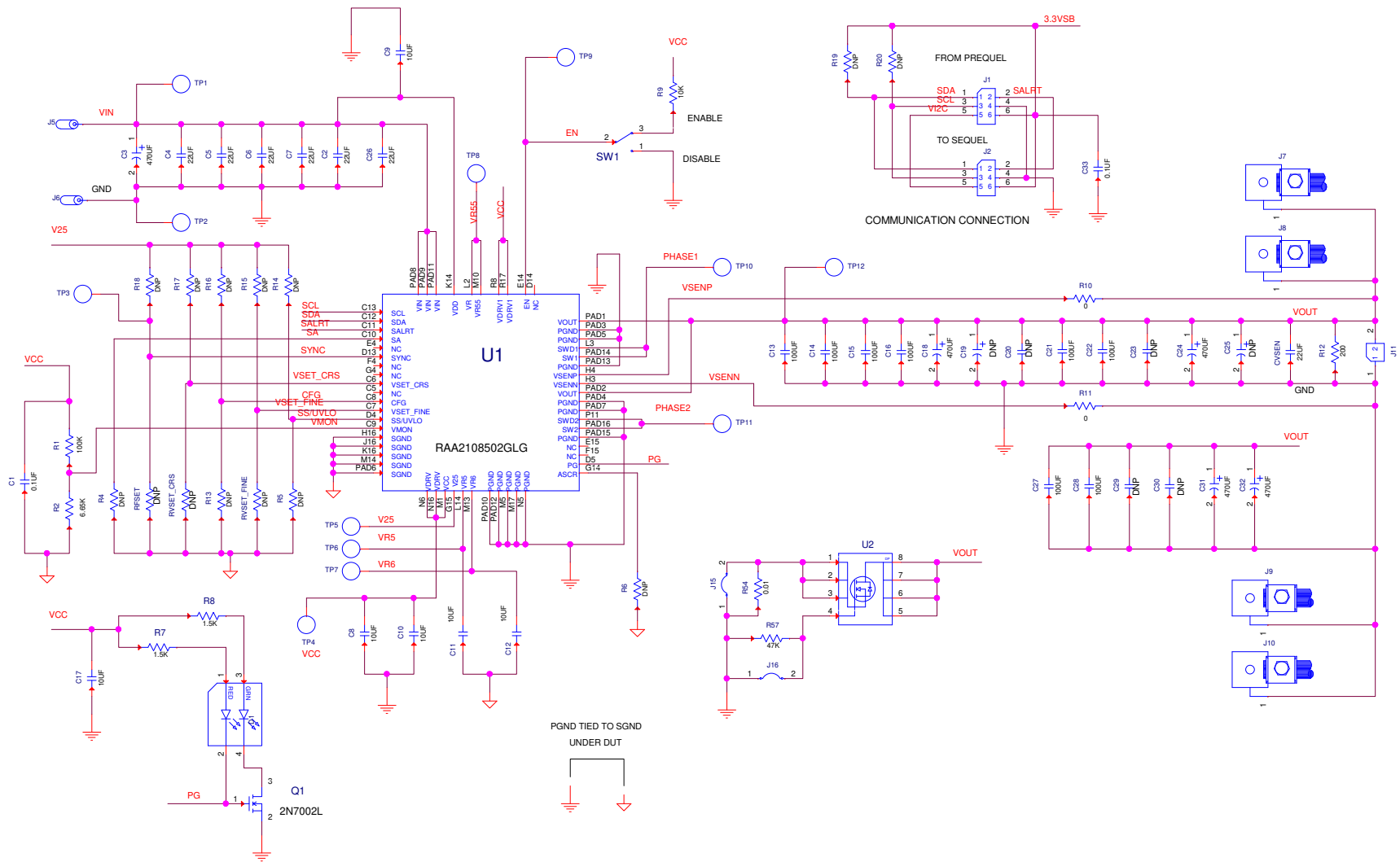


Figure 7. Schematic

4.4 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PCB, RTKA2108502H00000BU, REV.B, RoHS	Multilayer PCB (Hi Tech Circuit)	RTKA2108502H00000BURBPCB
2	C19, C25	DO NOT POPULATE_PLACE HOLDER		
4	C18, C24, C31, C32	CAP TANT POLY 470μF, 6.3V, 20%, 10mΩ, 2917, RoHS	Panasonic	6TPF470MAH
1	CVSEN	CAP CER 22μF, 6.3V, 20%, X5R, 0805, RoHS	TDK	C2012X5R0J226M
1	C3	CAP ALUM 470μF, 25V, 20%, SMD, RoHS	Panasonic	EEE1EA471P
8	C13-C16, C21, C22, C27, C28	CAP CER 100μF, 6.3V, 20%, X5R, 1206, RoHS	Murata	GRM31CR60J107ME39L
4	C20, C23, C29, C30	DO NOT POPULATE_PLACE HOLDER		
5	C8, C10-C12, C17	CAP CER 10μF, 10V, 10%, X7R, 1206, RoHS	Murata	GRM31CR71A106KA01L
6	C2, C4-C7, C26	CAP CER 22μF, 16V, 10%, X7R, 1210, RoHS	Murata	GRM32ER71C226KE18L
1	C33	CAP CER 0.1μF, 25V, 10%, X7R, 0603, RoHS	Kemet	C0603X104K3RACTU
1	C1	CAP CER 0.1μF, 25V, 10%, X7R, 0805, RoHS	Kemet	C0805X104K3RACTU
1	C9	CAP CER 10μF, 25V, 10%, X7R, 1206, RoHS	Kemet	C1206X106K3RAC7800
14	R4-R6, R13-R20, RVSET_FINE, RVSET_CRIS, RFSET	DO NOT POPULATE_PLACE HOLDER		
2	R10, R11	RES SMD 0Ω JUMPER, 1/10W, 0603, RoHS	Panasonic	ERJ-3GEY0R00V
1	R9	RES SMD 10kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1002V
1	R1	RES SMD 100kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1003V
2	R7, R8	RES SMD 1.5kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF1501V
1	R12	RES SMD 200Ω, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF2000V
1	R57	RES SMD 47kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF4702V
1	R2	RES SMD 6.65kΩ, 1%, 1/10W, 0603, RoHS	Panasonic	ERJ-3EKF6651V
1	R54	RES 0.01Ω, 1%, 2W, 2512, RoHS	Vishay	WSL2512R0100FEA
1	U1	50A Digital DC/DC PMBus Power Module, RoHS	Renesas	RAA2108502GLG
1	U2	MOSFET N-CH 25V, 39A, TDSO8-8, RoHS	Infineon	BSC010NE2LS
1	D1	LED GREEN/RED CLEAR AXIAL SMD, RoHS	Lumex Opto	SSL-LXA3025IGC
1	Q1	MOSFET N-CH 60V, 0.115A, SOT-23, RoHS	ON Semiconductor	2N7002L
1	SW1	SWITCH TOGGLE SPDT, 0.4VA, 20V, RoHS	C&K	GT13MCBE
12	TP1-TP12	TEST POINT PC COMPACT 0.063"D RED, RoHS	Keystone Electronics	5005
1	J2	CONN-SOCKET STRIP, TH, 2x3, 2.54mm, TIN, R/A, RoHS	Samtec	SSQ-103-02-T-D-RA
1	J1	CONN-SOCKET STRIP, TH, 2x3, 2.54mm, TIN, R/A, RoHS	Samtec	TSW-103-08-T-D-RA
3	J11, J15, J16	CONN-HEADER, 2x3, BRKAWY, 2.54mm, TIN, R/A, RoHS	Samtec	TSW-102-07-F-S
4	J7-J10	HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, RoHS	Burndy	KPA8CTP

(Continued)

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
2	J5, J6	Conn Jack Banana Unins Panel Mount, RoHS	Cinch Connectivity Solutions Johnson	108-0740-001

4.5 Board Layout

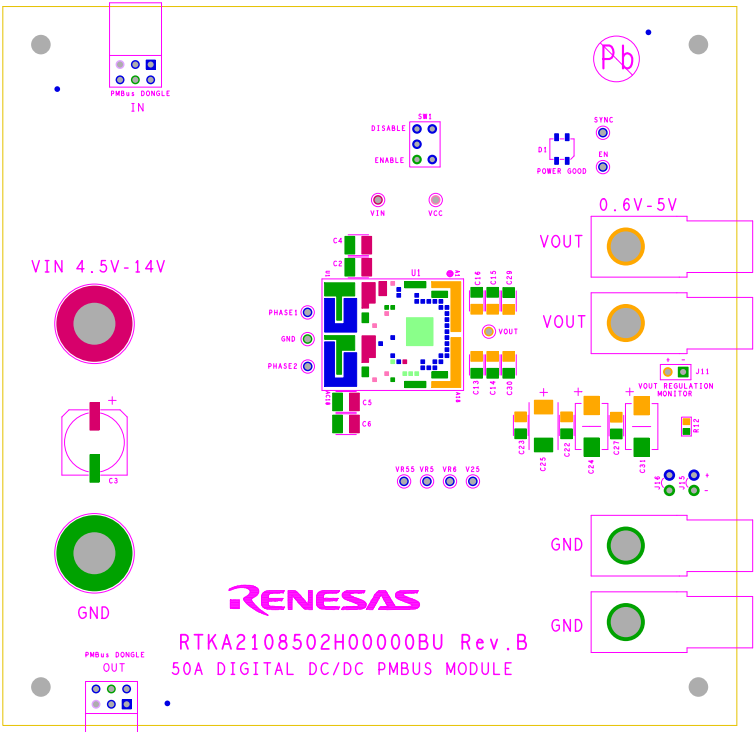


Figure 8. Top Layer Silk Screen

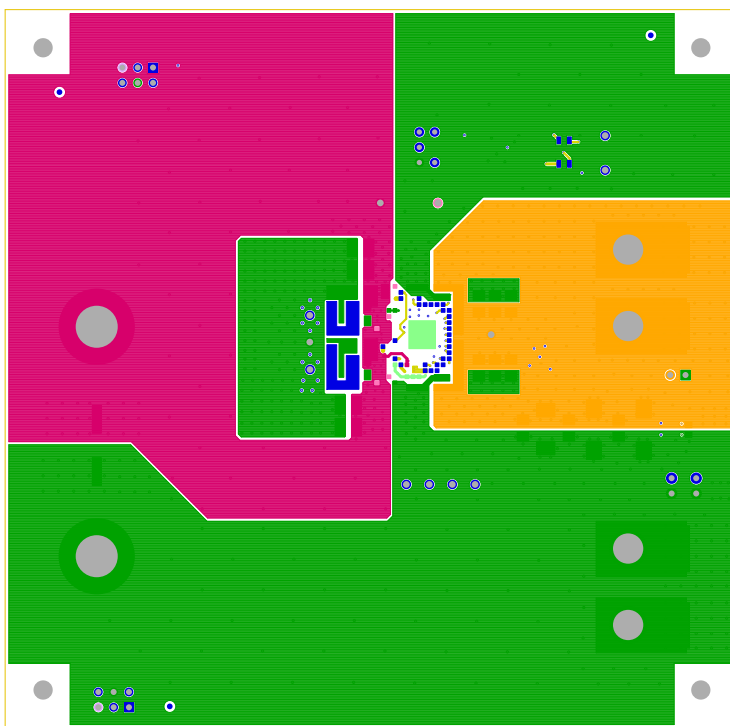


Figure 9. Top Layer Component Side

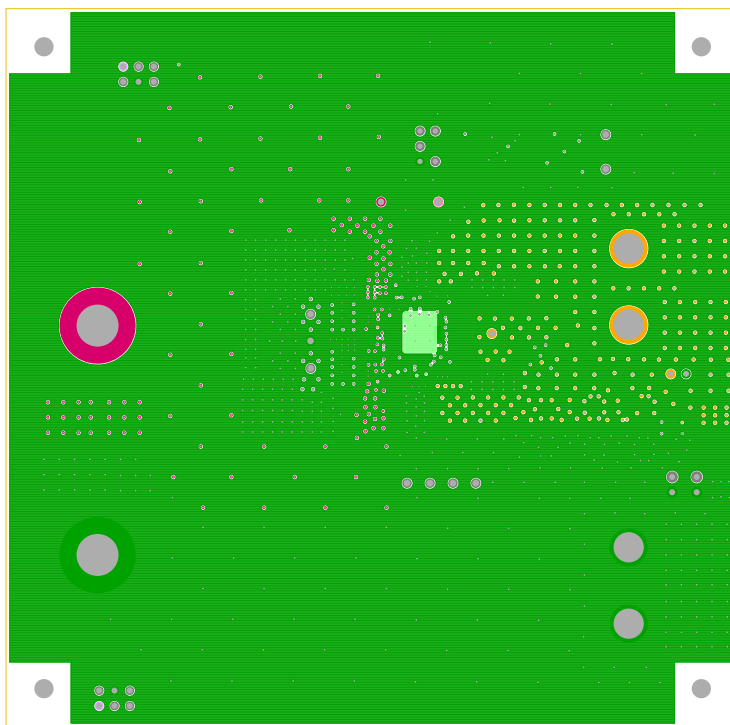


Figure 10. Layer 2

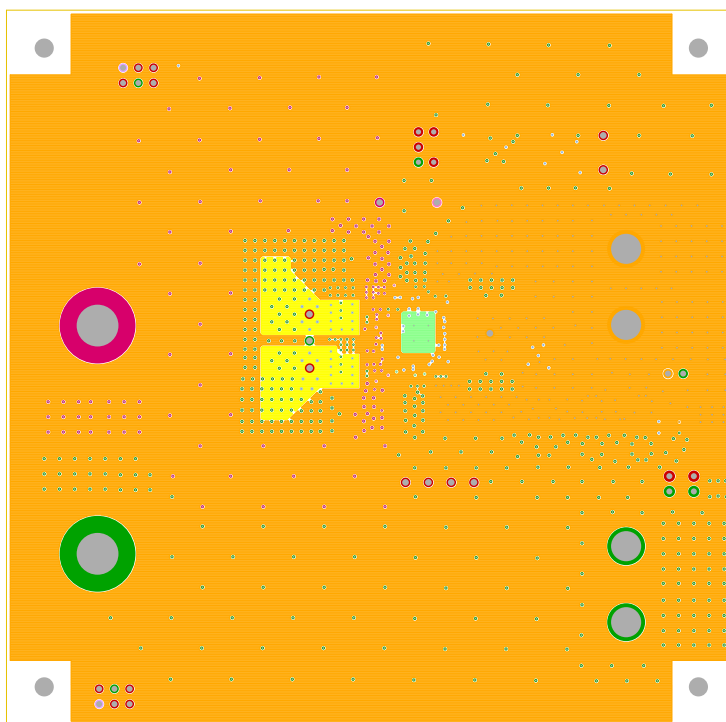


Figure 11. Layer 3

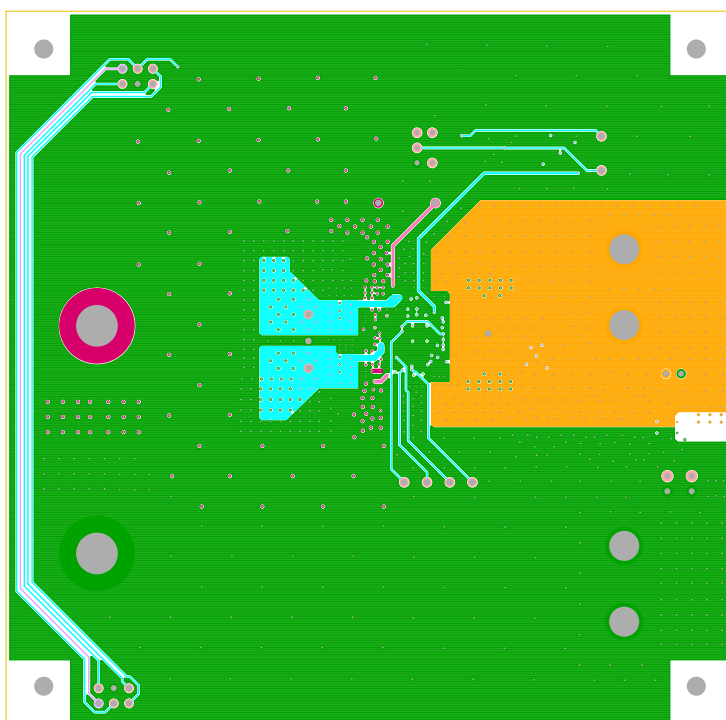


Figure 12. Layer 4

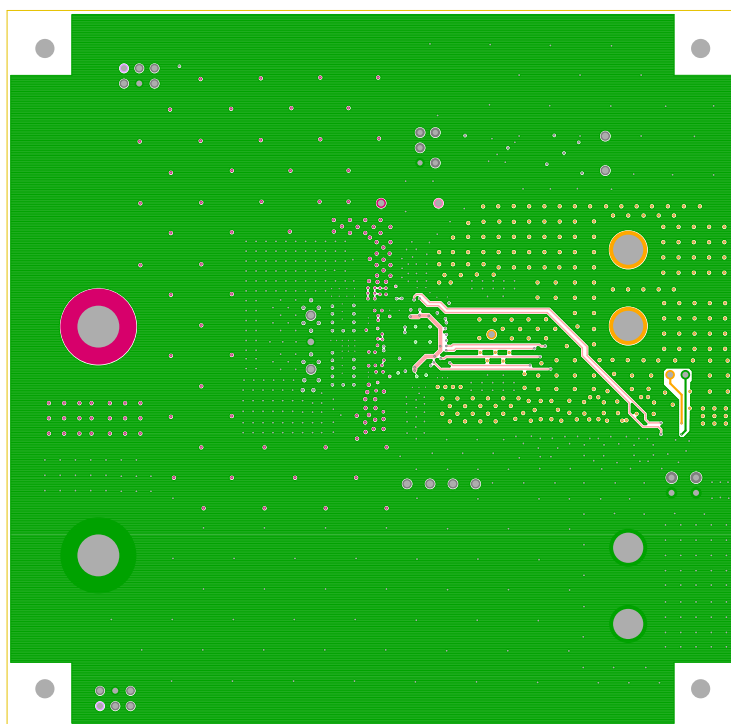


Figure 13. Layer 5

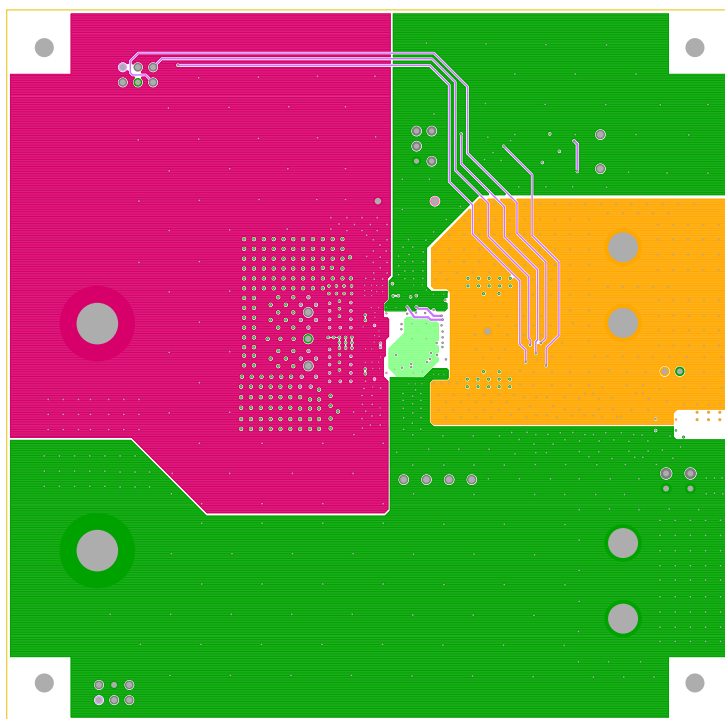


Figure 14. Layer 6

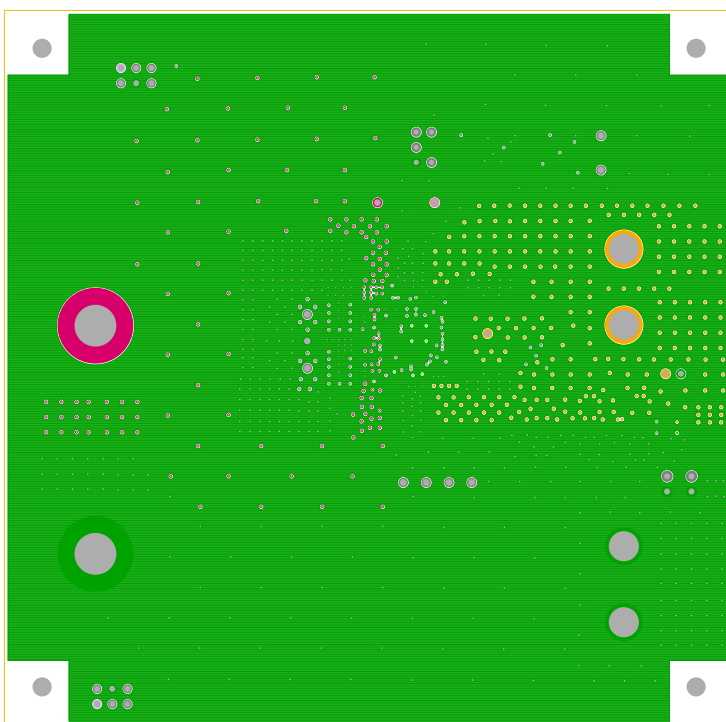


Figure 15. Layer 7

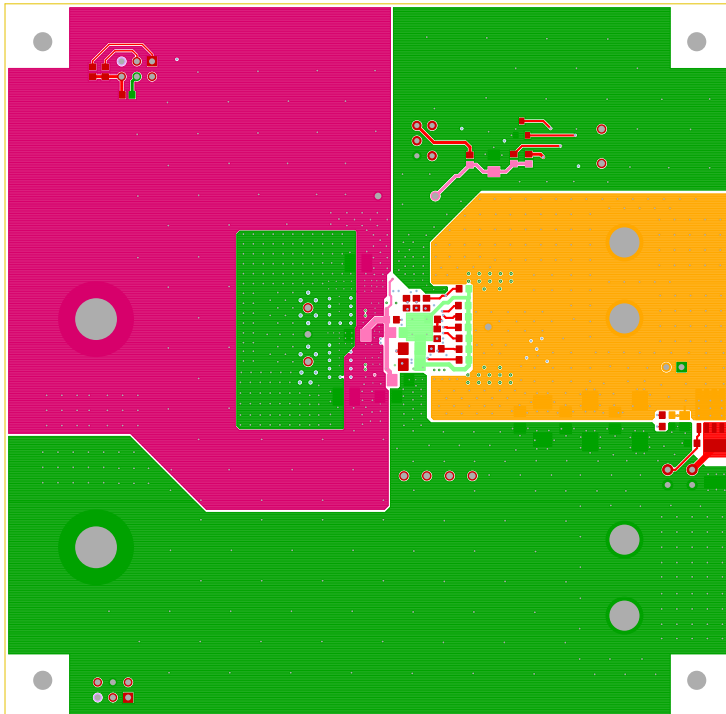


Figure 16. Bottom Layer Solder Side



5. Typical Performance Curves

The following data was acquired using a RTKA2108502H00000BU evaluation board.

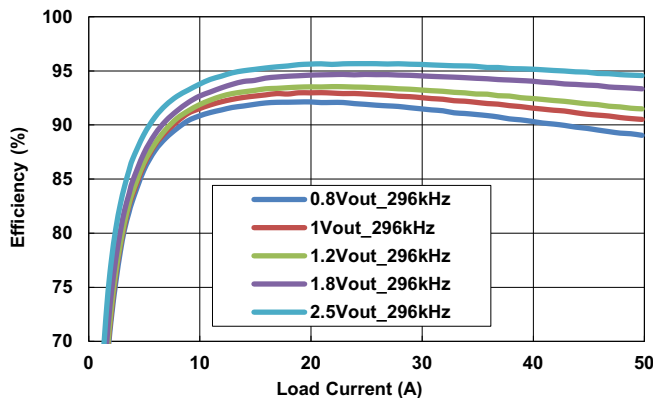


Figure 18. Efficiency vs Output Current at $V_{IN} = 5V$ for Various Output Voltages

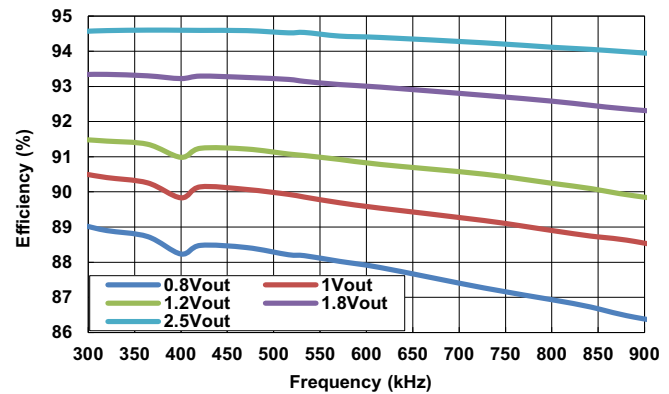


Figure 19. Efficiency vs Output Current at $V_{IN} = 5V$, $I_{OUT} = 50A$ for Various Output Voltages

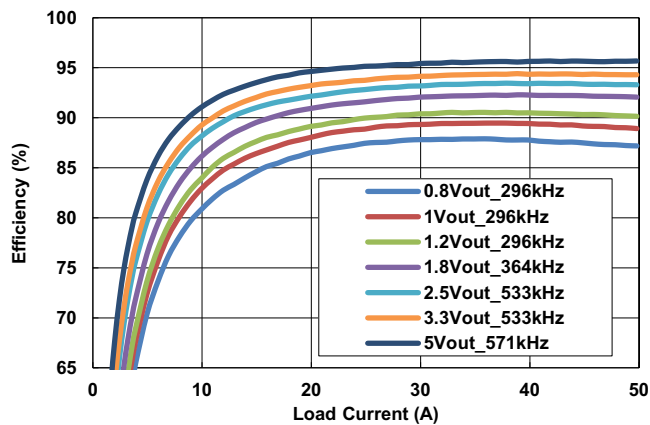


Figure 20. Efficiency vs Output Current at $V_{IN} = 12V$ for Various Output Voltages

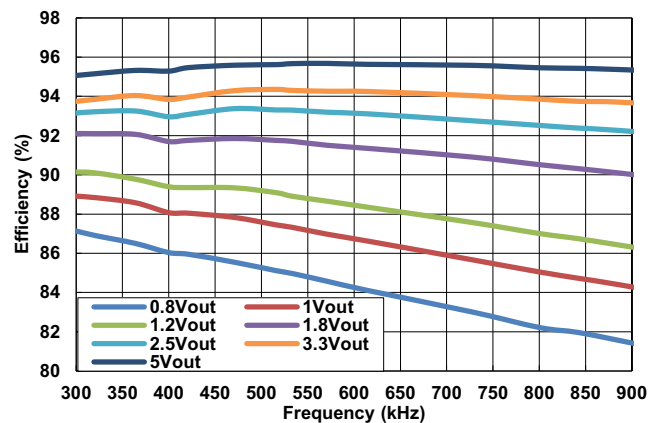


Figure 21. Efficiency vs Output Current at $V_{IN} = 12V$, $I_{OUT} = 50A$ for Various Output Voltages

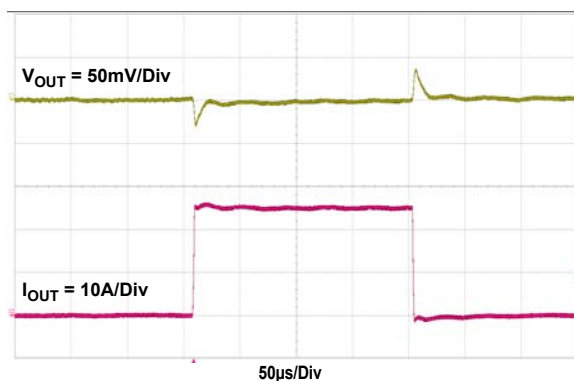


Figure 22. $5V_{IN}$ to $0.8V_{OUT}$ Transient response, $f_{SW} = 615kHz$, $C_{OUT} = 10 \times 100\mu F$ Ceramic + $3 \times 470\mu F$ POSCAP, ACSR Residual = 90, ASCR Gain = 450

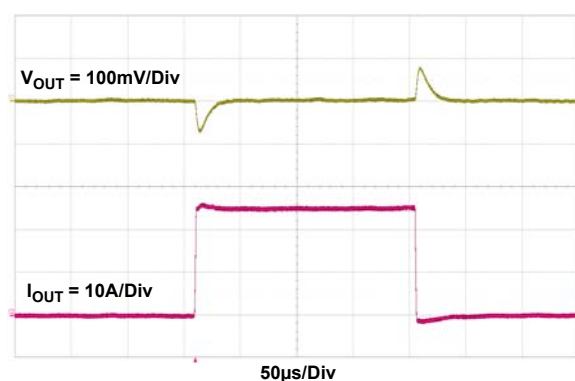


Figure 23. $12V_{IN}$ to $1.8V_{OUT}$ Transient Response, $f_{SW} = 471kHz$, $C_{OUT} = 12 \times 100\mu F$ Ceramic + $1 \times 470\mu F$ POSCAP, ACSR Residual = 100, ASCR Gain = 160

The following data was acquired using a RTKA2108502H00000BU evaluation board. (Continued)

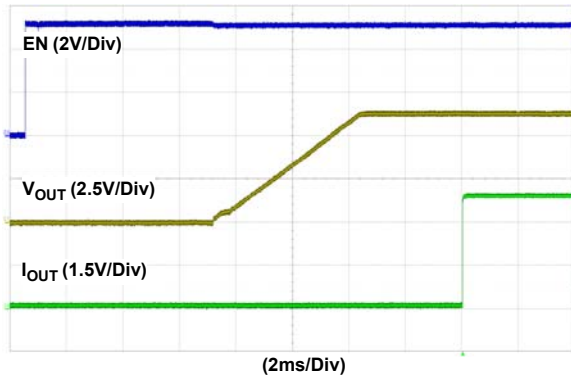


Figure 24. Soft-Start at $V_{IN} = 12V$, $V_{OUT} = 5V$,
 $TON_DELAY = 5ms$, $TON_RISE = 5ms$,
 $POWER_GOOD_DELAY = 3ms$

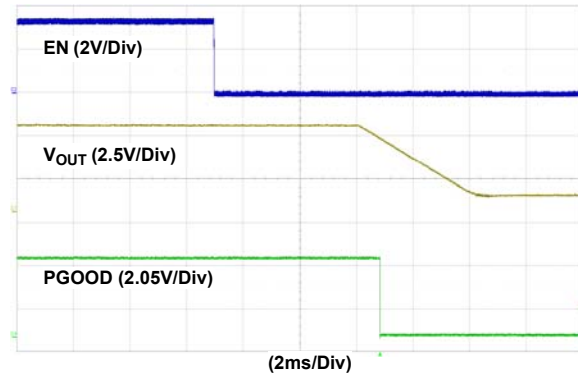


Figure 25. Soft-Stop at $V_{IN} = 12V$, $V_{OUT} = 5V$,
 $TOFF_DELAY = 5ms$, $TOFF_FALL = 5ms$,
 $POWER_GOOD_DELAY = 3ms$

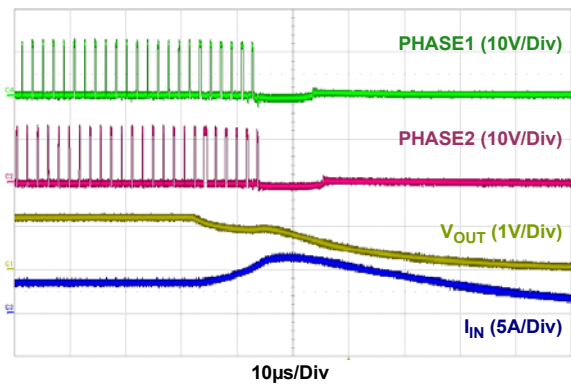


Figure 26. Output Short Circuit Protection at $V_{IN} = 12V$,
 $V_{OUT} = 1.2V$, $f_{SW} = 533kHz$

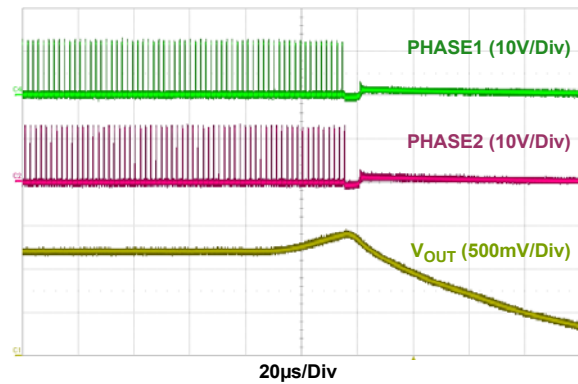


Figure 27. Output Overvoltage Protection at $V_{IN} = 12V$,
 $V_{OUT} = 1.2V$, $f_{SW} = 533kHz$,
 $V_{OUT_OV_FAULT_LIMIT} = 1.38V$

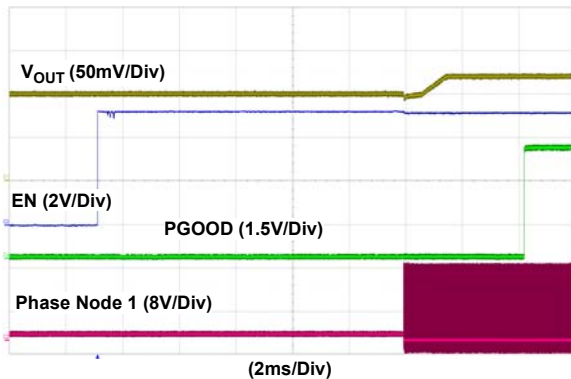


Figure 28. Pre-Bias Startup at $V_{IN} = 12V$, $V_{OUT} = 1.2V$,
Pre-Bias Voltage = 1V, $f_{SW} = 421kHz$

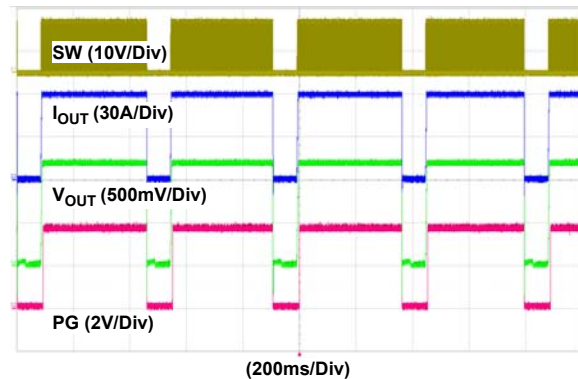


Figure 29. OCP 70ms Fault Retry at $V_{IN} = 12V$,
 $V_{OUT} = 1.2V$, $f_{SW} = 421kHz$,
Programmed I_{OUT} OC Fault Limit = 60A

6. Revision History

Rev.	Date	Description
0.00	Sept 11, 2018	Initial release

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
 2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
 3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
 4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
 5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
 6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
 7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
 8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
 9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
 10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
 11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
 12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

California Eastern Laboratories, Inc.
4590 Patrick Henry Drive, Santa Clara, California 95054-1817, U.S.A.
Tel: +1-408-919-2500, Fax: +1-408-988-0279

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

RTKA2108502H00000BU

