

# 16-Mbit (1M × 16/2M × 8) Static RAM

#### **Features**

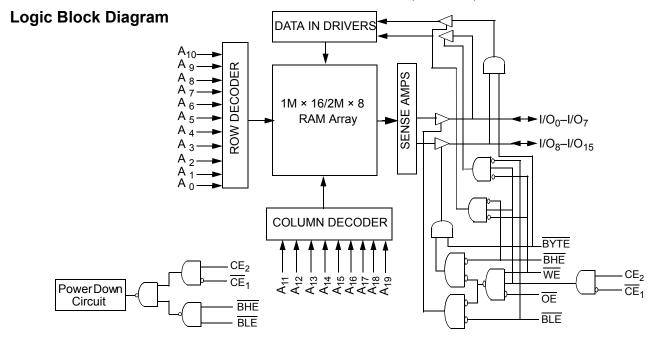
- Ultra-low standby power
  - Typical standby current: 5.5 μA
  - Maximum standby current: 16 μA
- TSOP I package configurable as 1M × 16 or 2M × 8 SRAM
- Very high speed: 45 ns
- Temperature ranges
  - □ Industrial: -40 °C to +85 °C
- Wide voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- Easy memory expansion with  $\overline{CE}_1$ ,  $CE_2$ , and  $\overline{OE}$  Features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Offered in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

### **Functional Description**

The CY62167GN is a high performance CMOS static RAM organized as 1M words by 16 bits or 2M words by 8 bits. This device features an advanced circuit design that provides an ultra low active current. Ultra low active current is ideal for providing More Battery Life  $^{\rm TM}$  (MoBL  $^{\rm (MoBL)}$ ) in portable applications such as cellular telephones. The device also has an automatic power down feature that reduces power consumption by 99 percent when addresses are not toggling. Place the device into standby mode when deselected ( $\overline{\rm CE_1}$  HIGH or  ${\rm CE_2}$  LOW or both BHE and BLE are HIGH). The input and output pins (I/O0 through I/O15) are placed in a high impedance state when: the device is deselected ( $\overline{\rm CE_1}$  HIGH or  ${\rm CE_2}$  LOW), outputs are disabled ( $\overline{\rm OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or a write operation is in progress ( $\overline{\rm CE_1}$  LOW,  ${\rm CE_2}$  HIGH and  $\overline{\rm WE}$  LOW).

To write to the device, take Chip Enables ( $\overline{\text{CE}}_1$  LOW and  $\text{CE}_2$   $\underline{\text{HIGH}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) input LOW. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from I/O pins (I/O $_0$  through I/O $_7$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ). If Byte High Enable ( $\overline{\text{BHE}}$ ) is LOW, then data from the I/O pins (I/O $_8$  through I/O $_15$ ) is written into the location specified on the address pins ( $A_0$  through  $A_{19}$ ).

To read from the device, take <u>Chip Enables</u> ( $\overline{\text{CE}}_1$  LOW and  $\text{CE}_2$  HIGH) <u>and Output Enable</u> ( $\overline{\text{OE}}$ ) LOW <u>while</u> forcing the Write Enable ( $\overline{\text{WE}}$ ) HIGH. If Byte Low Enable ( $\overline{\text{BLE}}$ ) is LOW, then data from the memory location specified <u>by the</u> address pins appears on I/O<sub>0</sub> to I/O<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory appears on I/O<sub>8</sub> to I/O<sub>15</sub>. See <u>Truth Table on page 13</u> for a complete description of read and write modes.



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### **Pin Configuration**

Figure 1. 48-ball VFBGA pinout (Top View) [1, 2]

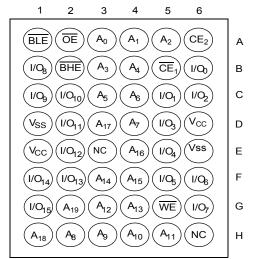
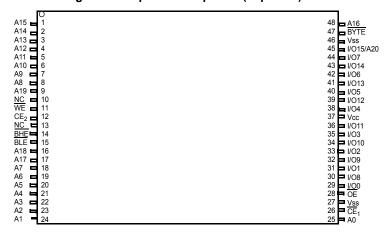


Figure 2. 48-pin TSOP I pinout (Top View) [2, 3]



### **Product Portfolio**

					Power Dissipation						
Product	Range	V <sub>CC</sub> Range (V)		Speed	Operating I <sub>CC</sub> (mA)				Standby I <sub>SB2</sub>		
Floudet	Kange			(ns)	f = 1	f = 1 MHz		f = f <sub>max</sub>		(μ <b>A</b> )	
		Min	Typ <sup>[4]</sup>	Max		Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max
CY62167GN18	Industrial	1.65	1.8	2.2	55	7	9	29	32	7	26
CY62167GN30		2.2	3.0	3.6	45			29	36	5.5	16
CY62167GN		4.5	5.0	5.5							

- Ball H6 for the VFBGA package can be used to upgrade to a 32M density.
- NC pins are not connected on the die.
- The BYTE pin in the 48-pin TSOP I package has to be tied to V<sub>CC</sub> to use the device as a 1M × 16 SRAM. The 48-pin TSOP I package can also be used as a 2M × 8 SRAM by tying the BYTE signal to V<sub>SS</sub>. In the 2M × 8 configuration, Pin 45 is A20, while BHE, BLE and I/O<sub>8</sub> to I/O<sub>14</sub> pins are not used.
   Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25 °C.



### **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ......-65 °C to + 150 °C Ambient temperature Supply voltage to ground potential<sup>[5, 6]</sup> ......–0.3 V to  $V_{CC(max)}$  + 0.3 V DC voltage applied to outputs in High Z state<sup>[5, 6]</sup> ......–0.3 V to  $V_{CC(max)}$  + 0.3 V DC input voltage<sup>[5, 6]</sup> .....-0.3 V to  $V_{CC(max)}$  + 0.3 V

Output current into outputs (LOW)20 mA	١
Static discharge voltage	
(MIL-STD-883, Method 3015)>2001 V	/
Latch-up current>200 mA	١

### **Operating Range**

Device Range	Ambient Temperature	<b>V</b> cc <sup>[7]</sup>
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

#### **Electrical Characteristics**

Over the Operating Range

D	Description	To al Count	141	45 ns/ 55 ns		5	11!4
Parameter	er Description Test Conditions		itions	Min	<b>Typ</b> <sup>[8]</sup>	Max	Unit
V <sub>OH</sub>	Output HIGH voltage	1.65 ≤ V <sub>CC</sub> ≤ 2.2	$I_{OH} = -0.1 \text{ mA}$	1.4	_	_	V
		2.2 ≤ V <sub>CC</sub> ≤ 2.7	$I_{OH} = -0.1 \text{ mA}$	2.0	_	_	
		$2.7 \le V_{CC} \le 3.6$	$I_{OH} = -1.0 \text{ mA}$	2.4	-	-	
		$4.5 \le V_{CC} \le 5.5$	$I_{OH} = -1.0 \text{ mA}$	2.4	_	-	
		$4.5 \le V_{CC} \le 5.5$	$I_{OH} = -0.1 \text{ mA}$	V <sub>OH</sub> – 0.5 <sup>[9]</sup>	_	_	
$V_{OL}$	Output LOW voltage	1.65 ≤ V <sub>CC</sub> ≤ 2.2	I <sub>OL</sub> = 0.1 mA	_	_	0.2	V
		2.2 ≤ V <sub>CC</sub> ≤ 2.7	I <sub>OL</sub> = 0.1 mA	_	_	0.4	
		$2.7 \le V_{CC} \le 3.6$	I <sub>OL</sub> = 2.1 mA	_	_	0.4	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5	I <sub>OL</sub> = 2.1 mA	_	_	0.4	
V <sub>IH</sub>	Input HIGH voltage	1.65 ≤ V <sub>CC</sub> ≤ 2.2		1.4	_	V <sub>CC</sub> + 0.2	V
		2.2 ≤ V <sub>CC</sub> ≤ 2.7		1.8	_	V <sub>CC</sub> + 0.3	
		2.7 ≤ V <sub>CC</sub> ≤ 3.6		2	-	V <sub>CC</sub> + 0.3	
		4.5 ≤ V <sub>CC</sub> ≤ 5.5		2.2	_	V <sub>CC</sub> + 0.5	
$V_{IL}$	Input LOW voltage	1.65 ≤ V <sub>CC</sub> ≤ 2.2		-0.2	-	0.4	V
		2.2 ≤ V <sub>CC</sub> ≤ 2.7		-0.3	_	0.6	
		$2.7 \le V_{CC} \le 3.6$		-0.3	_	0.8	
		$4.5 \le V_{CC} \le 5.5$		-0.5	_	0.8	
I <sub>IX</sub>	Input leakage current	$GND \le V_1 \le V_{CC}$		-1	_	+1	μА
I <sub>OZ</sub>	Output leakage current	$GND \le V_O \le V_{CC}$ , Ou		-1	-	+1	μΑ
I <sub>CC</sub>	V <sub>CC</sub> operating supply current	f = 22.22MHz (45 ns)	$V_{CC} = V_{CC(max)}$	-	29	36	mA
		f = 22.22MHz (45 ns) f = 18.18MHz (55 ns)	I <sub>OUT</sub> = 0 mA CMOS levels	_	29	32	mA
		f = 1 MHz		_	7	9	mA

- N<sub>IL(min)</sub> = -2.0 V for pulse durations less than 20 ns.
   V<sub>IH(max)</sub> = V<sub>CC</sub> + 2V for pulse durations less than 20 ns.
   Full Device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
   Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested
- 9. This parameter is guaranteed by design and not tested.



## **Electrical Characteristics** (continued)

Over the Operating Range

Downwoodow	Decembries	Took Condi	141		45 ns/ 55 ns		I I m!4
Parameter	Description	Test Conditions		Min	<b>Typ</b> <sup>[8]</sup>	Max	- Unit
I <sub>SB1</sub> <sup>[10]</sup>	Automatic power down current – CMOS inputs	$\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V or}$	CE <sub>2</sub> ≤ 0.2 V	_	5.5	16	μА
	ouncine owice inpute	or ( $\overline{BHE}$ and $\overline{BLE}$ ) $\geq V$	$V_{\rm CC} - 0.2 \text{ V},$				
	$V_{IN} \ge V_{CC} - 0.2 \text{ V}, V_{IN} \le 0.2 \text{ V},$						
		f = f <sub>max</sub> (address and	data only),				
		$f = 0$ ( $\overline{OE}$ , and $\overline{WE}$ ), V					
I <sub>SB2</sub> <sup>[10]</sup>	Automatic Power-down		25 °C <sup>[11]</sup>	-	5.5	6.5	μА
	Current – CMOS Inputs $V_{CC}$ = 2.2 V to 3.6 V and 4.5 V to 5.5 V		40 (1.1.)	_	6.3	8.0	
		or ( $\overline{BHE}$ and $\overline{BLE}$ ) $\geq$ $V_{CC} - 0.2 \text{ V}$ ,	70 °C <sup>[11]</sup>	_	8.4	12.0	
		$V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V,}$	85 °C	_	12.0	16.0	
		$f = 0$ , $V_{CC} = V_{CC(max)}$	05 1001/		7.0	00.0	
	Automatic Power-down Current – CMOS Inputs $V_{CC}$ = 1.65 V to 2.2 V		/ <sub>CC</sub> – 0.2 V,	_	7.0	26.0	

<sup>10.</sup> Chip enables ( $\overline{\text{CE}}_1$  and  $\text{CE}_2$ ), byte enables ( $\overline{\text{BHE}}$  and  $\overline{\text{BLE}}$ ) and  $\overline{\text{BYTE}}$  must be tied to CMOS levels to meet the I<sub>SB1</sub>/I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating. 11. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.



## Capacitance

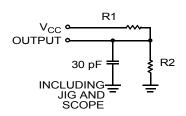
Parameter [12]	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 ^{\circ}\text{C}, f = 1 \text{MHz}, V_{CC} = V_{CC(typ)}$	10	pF
C <sub>OUT</sub>	Output capacitance		10	pF

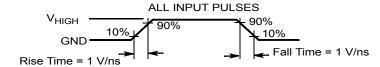
### **Thermal Resistance**

Parameter [12]	Description	Test Conditions	48-ball VFBGA	48-pin TSOP I	Unit
$\Theta_{JA}$		Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	31.50	57.99	°C/W
$\Theta_{\sf JC}$	Thermal resistance (junction to case)		15.75	13.42	°C/W

### **AC Test Loads and Waveforms**

Figure 3. AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT

Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R <sub>1</sub>	13500	16667	1103	1800	Ω
R <sub>2</sub>	10800	15385	1554	990	Ω
R <sub>TH</sub>	6000	8000	645	639	Ω
V <sub>TH</sub>	0.80	1.20	1.75	1.77	V
V <sub>HIGH</sub>	1.8	2.5	3.0	5.0	V

#### Note

<sup>12.</sup> Tested initially and after any design or process changes that may affect these parameters.



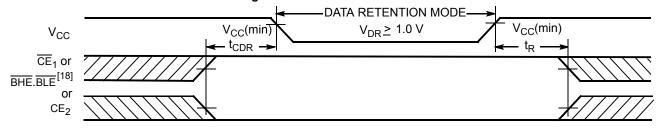
### **Data Retention Characteristics**

Over the Operating Range

Parameter	Description	Conditions	Min	<b>Typ</b> [13]	Max	Unit
$V_{DR}$	V <sub>CC</sub> for data retention		1.0	_	-	V
I <sub>CCDR</sub> [14, 15]	Data retention current	$V_{CC}$ = 2.2 V to 3.6 V, $\overline{CE}_1 \ge V_{CC} - 0.2 \text{ V or } CE_2 \le 0.2 \text{ V or}$ $(\overline{BHE} \text{ and } \overline{BLE}) \ge V_{CC} - 0.2 \text{ V},$	-	5.5	16	μА
		$V_{IN} \ge V_{CC} - 0.2 \text{ V or } V_{IN} \le 0.2 \text{ V}$ 1.2 V \le V_{CC} \le 2.2 V,	_	7.0	26.0	
		$\overline{\text{CE}}_1 \ge \text{V}_{\text{CC}} - 0.2 \text{ V or } \text{CE}_2 \le 0.2 \text{ V or}$ $(\overline{\text{BHE}} \text{ and } \overline{\text{BLE}}) \ge \text{V}_{\text{CC}} - 0.2 \text{ V},$ $\text{V}_{\text{IN}} \ge \text{V}_{\text{CC}} - 0.2 \text{ V or } \text{V}_{\text{IN}} \le 0.2 \text{ V}$				
t <sub>CDR</sub> <sup>[16]</sup>	Chip deselect to data retention time		0	_	_	_
t <sub>R</sub> <sup>[17, 19]</sup>	Operation recovery time		45/55	_	_	ns

#### **Data Retention Waveform**

Figure 4. Data Retention Waveform



- 13. Indicates the value for the center of distribution at 3.0 V, 25 °C and not 100% tested.

  14. Chip enables (CE<sub>1</sub> and CE<sub>2</sub>), byte enables (BHE and BLE) and BYTE must be tied to CMOS levels to meet the I<sub>SB1</sub> / I<sub>SB2</sub> / I<sub>CCDR</sub> spec. Other inputs can be left floating.

- 14. Chip enables (CE1 and CE2), byte enables (BTL2 and BTL2 into BTL2 into
- 19. These parameters are guaranteed by design and are not tested.



### **Switching Characteristics**

[20]	B	45	ns	55 ns		11!4
Parameter <sup>[20]</sup>	Description	Min	Max	Min	Max	Unit
Read Cycle						
t <sub>RC</sub>	Read cycle time	45.0	_	55.0	_	ns
t <sub>AA</sub>	Address to data valid	_	45.0	-	55.0	ns
t <sub>OHA</sub>	Data hold from address change	10.0	_	10.0	_	ns
t <sub>ACE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to data valid	_	45.0	-	55.0	ns
t <sub>DOE</sub>	OE LOW to data valid	_	22.0	-	25.0	ns
t <sub>LZOE</sub>	OE LOW to Low Z [21, 22]	5.0	_	5.0	_	ns
t <sub>HZOE</sub>	OE HIGH to High Z [21, 22, 23]	_	18.0	-	18.0	ns
t <sub>LZCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to Low Z [21, 22]	10.0	_	10.0	_	ns
t <sub>HZCE</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to High Z [21, 22, 23]	_	18.0	-	18.0	ns
t <sub>PU</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to power-up <sup>[24]</sup>	0	_	0	_	ns
t <sub>PD</sub>	CE <sub>1</sub> HIGH and CE <sub>2</sub> LOW to power-down <sup>[24]</sup>	_	45.0	-	55.0	ns
t <sub>DBE</sub>	BLE / BHE LOW to data valid	_	45.0	-	55.0	ns
t <sub>LZBE</sub>	BLE / BHE LOW to Low Z [21, 22]	5.0	_	5.0	_	ns
t <sub>HZBE</sub>	BLE / BHE HIGH to High Z [21, 22, 23]	_	18.0	-	18.0	ns
Write Cycle <sup>[25, 26]</sup>						
t <sub>WC</sub>	Write cycle time	45	_	55	_	ns
t <sub>SCE</sub>	CE <sub>1</sub> LOW and CE <sub>2</sub> HIGH to write end	35	_	40	_	ns
t <sub>AW</sub>	Address setup to write end	35	_	40	_	ns
t <sub>HA</sub>	Address hold from write end	0	_	0	_	ns
t <sub>SA</sub>	Address setup to write start	0	_	0	_	ns
t <sub>PWE</sub>	WE pulse width	35	_	40	_	ns
t <sub>BW</sub>	BLE / BHE LOW to write end	35	_	40	_	ns
t <sub>SD</sub>	Data setup to write end	25	_	25	_	ns
t <sub>HD</sub>	Data hold from write end	0	_	0	_	ns
t <sub>HZWE</sub>	WE LOW to High Z [21, 22, 23]	_	18	_	20	ns
t <sub>LZWE</sub>	WE HIGH to Low Z [21, 22]	10	-	10	_	ns

- 20. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1 V/ns, timing reference levels of V<sub>CC(typ)</sub>/2, input pulse levels of 0 to V<sub>CC(typ)</sub>, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> as shown in Figure 3 on page 6.
  21. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZDE</sub>, t<sub>HZOE</sub> is less than t<sub>LZOE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.
  22. Tested initially and after any design or process changes that may affect these parameters.
  23. t<sub>HZCE</sub>, t<sub>HZCE</sub>, t<sub>HZDE</sub>, and t<sub>HZWE</sub> transitions are measured when the outputs enter a high impedance state.

- 24. These parameters are guaranteed by design and are not tested.
- 24. These parameters are guaranteed by design and all this consider.

  25. The internal write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE or BLE or both = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write 26. The minimum write cycle pulse width for Write Cycle No. 3 (WE Controlled, OE LOW) should be equal to the sum of t<sub>HZWE</sub> and t<sub>SD</sub>.



## **Switching Waveforms**

Figure 5. Read Cycle No. 1 (Address Transition Controlled)<sup>[27, 28]</sup>

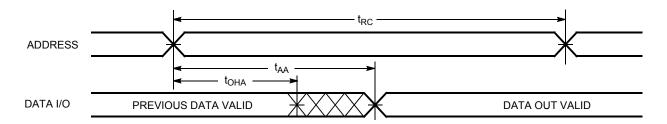
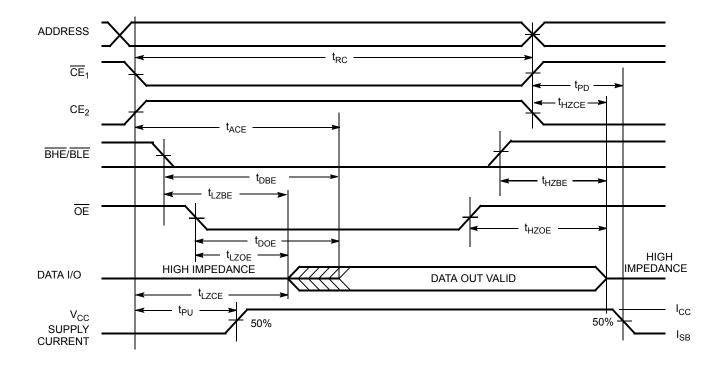


Figure 6. Read Cycle No. 2 ( $\overline{\text{OE}}$  Controlled)[28, 29]



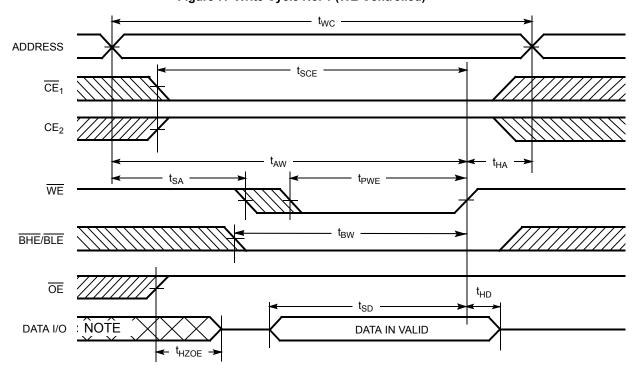
<sup>27.</sup> The device is continuously selected.  $\overline{OE}$ ,  $\overline{CE}_1 = V_{IL}$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  or both =  $V_{IL}$ , and  $CE_2 = V_{IH}$ .

<sup>28.</sup> WE is HIGH for read cycle.
29. Address valid before or similar to  $\overline{CE}_1$ ,  $\overline{BHE}$ ,  $\overline{BLE}$  transition LOW and  $\overline{CE}_2$  transition HIGH.



### Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 ( $\overline{\text{WE}}$  Controlled) $^{[30,\ 31,\ 32]}$ 



<sup>30.</sup> The internal write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE or BLE or both = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

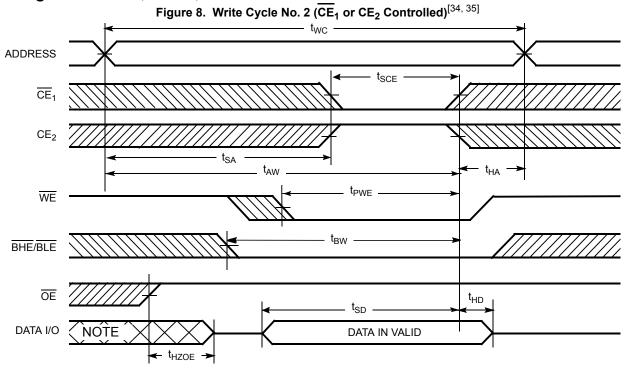
31. Data I/O is high impedance if OE = V<sub>IH</sub>.

<sup>32.</sup> If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}}$  =  $\text{V}_{\text{IH}}$ , the output remains in a high impedance state.

<sup>33.</sup> During this period the I/Os are in output state. Do not apply input signals.



### Switching Waveforms (continued)



<sup>34.</sup> The internal write time of the memory is defined by the overlap of WE, CE<sub>1</sub> = V<sub>IL</sub>, BHE or BLE or both = V<sub>IL</sub>, and CE<sub>2</sub> = V<sub>IH</sub>. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

35. If CE<sub>1</sub> goes HIGH and CE<sub>2</sub> goes LOW simultaneously with WE = V<sub>IH</sub>, the output remains in a high impedance state.

<sup>36.</sup> During this period the I/Os are in output state. Do not apply input signals.



### Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)[37, 38]

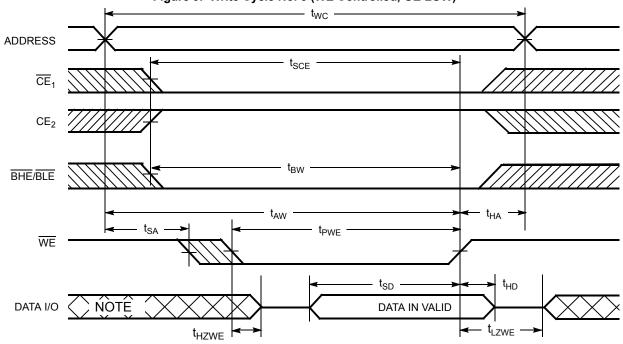
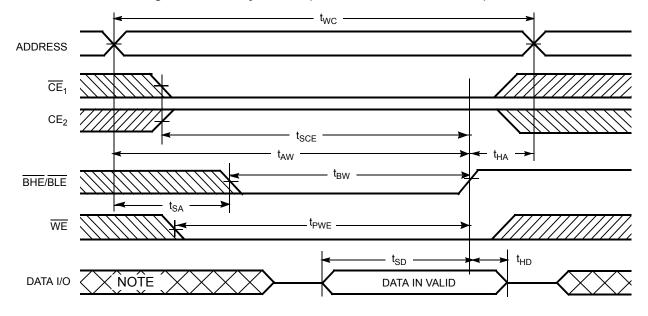


Figure 10. Write Cycle No. 4 (BHE/BLE Controlled, OE LOW)[37, 38]





### **Truth Table**

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
Н	X <sup>[40]</sup>	Х	Х	X <sup>[40]</sup>	X <sup>[40]</sup>	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
X <sup>[40]</sup>	L	Х	Х	X <sup>[40]</sup>	X <sup>[40]</sup>	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
X <sup>[40]</sup>	X <sup>[40]</sup>	Х	Х	Н	Н	High Z	Deselect/Power-down	Standby (I <sub>SB</sub> )
L	Н	Н	L	L	L	Data Out (I/O <sub>0</sub> -I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Η	Н	L	Н	L	Data Out (I/O <sub>0</sub> –I/O <sub>7</sub> ); High Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	L	L	Н	High Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data Out (I/O <sub>8</sub> –I/O <sub>15</sub> )	Read	Active (I <sub>CC</sub> )
L	Н	Н	Н	Х	Х	High Z	Output disabled	Active (I <sub>CC</sub> )
L	Н	L	Х	L	L	Data In (I/O <sub>0</sub> -I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	Η	L	Х	Н	L	Data In (I/O <sub>0</sub> –I/O <sub>7</sub> ); High Z (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )
L	Н	L	Х	L	Н	High Z (I/O <sub>0</sub> –I/O <sub>7</sub> ); Data In (I/O <sub>8</sub> –I/O <sub>15</sub> )	Write	Active (I <sub>CC</sub> )

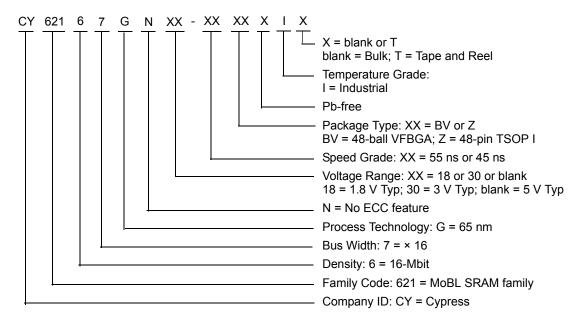
Note
40. The 'X' (Don't care) state for the chip enables and Byte enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.



## **Ordering Information**

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
55	1.65 V-2.2 V	CY62167GN18-55BVXI	51-85150	48-ball VFBGA (6 × 8 × 1 mm),	Industrial
		CY62167GN18-55BVXIT		Package Code: BV48	
45	2.2 V-3.6 V	CY62167GN30-45BVXI	51-85150	,,	
		CY62167GN30-45BVXIT		Package Code: BV48	
		CY62167GN30-45ZXI	51-85183	48-pin TSOP I (Pb-free)	
		CY62167GN30-45ZXIT			
	4.5 V–5.5 V	CY62167GN-45ZXI	51-85183	48-pin TSOP I (Pb-free)	
		CY62167GN-45ZXIT			

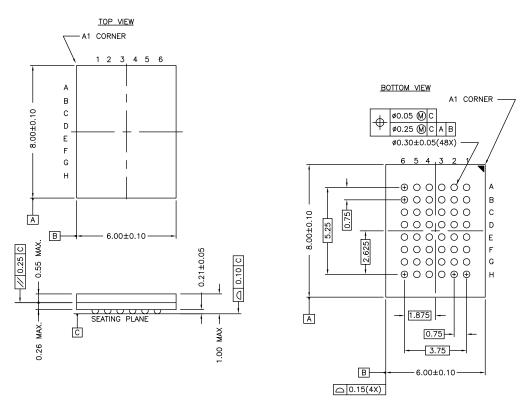
### **Ordering Code Definitions**





## **Package Diagrams**

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



NOTE:

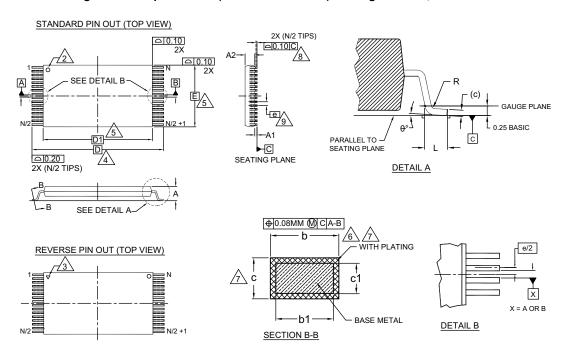
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H



### Package Diagrams (continued)

Figure 12. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Package Outline, 51-85183



SYMBOL	DIMENSIONS			
STIMBUL	MIN.	NOM.	MAX.	
Α	_	_	1.20	
A1	0.05	_	0.15	
A2	0.95	1.00	1.05	
b1	0.17	0.20	0.23	
b	0.17	0.22	0.27	
c1	0.10	_	0.16	
С	0.10	_	0.21	
D	20.00 BASIC			
D1	18.40 BASIC			
E	12.00 BASIC			
е	0.50 BASIC			
L	0.50	0.60	0.70	
θ	0°	_	8	
R	0.08	_	0.20	
N	48			

#### NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).

2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).

PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.

TO BE DETERMINED AT THE SEATING PLANE IS MADE WHICH THE PACKAGE.

DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.

DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.

DIMENSION 6 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF 6 DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm.

THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.

DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.

10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 \*F



## **Acronyms**

Acronym	Description			
BHE	Byte High Enable			
BLE	Byte Low Enable			
CE	Chip Enable			
CMOS	Complementary Metal Oxide Semiconductor			
I/O	Input/Output			
ŌĒ	Output Enable			
SRAM	Static Random Access Memory			
TSOP	Thin Small Outline Package			
VFBGA	Very Fine-Pitch Ball Grid Array			
WE	Write Enable			

## **Document Conventions**

### **Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μΑ	microampere
μS	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



# **Document History Page**

	Document Title: CY62167GN MoBL <sup>®</sup> , 16-Mbit (1M × 16/2M × 8) Static RAM Document Number: 001-93628				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change	
*B	5210733	NILE	07/04/2016	Changed status from Preliminary to Final.	
*C	5420388	VINI	09/08/2016	Updated Electrical Characteristics: Changed minimum value of $V_{OH}$ parameter corresponding to Test Condition "2.7 $\leq$ $V_{CC} \leq$ 3.6, $I_{OH} = -1.0$ mA" from 2.2 V to 2.4 V. Changed minimum value of $V_{IH}$ parameter corresponding to Test Condition "2.2 $\leq$ $V_{CC} \leq$ 2.7" from 2 V to 1.8 V. Updated Note 5 (Replaced 2 ns with 20 ns). Updated Note 6 (Replaced 2 ns with 20 ns). Updated Ordering Information: Updated part numbers. Added Tape and Reel parts. Updated to new template.	
*D	5783985	NILE	06/23/2017	Updated Data Retention Characteristics: Changed typical value of $I_{CCDR}$ parameter corresponding to Condition "1.2 V $\leq$ V $_{CC} \leq$ 2.2 V" from 5.5 $\mu A$ to 7.0 $\mu A$ . Changed maximum value of $I_{CCDR}$ parameter corresponding to Condition "1.2 V $\leq$ V $_{CC} \leq$ 2.2 V" from 16.0 $\mu A$ to 26.0 $\mu A$ . Updated Package Diagrams: spec 51-85183 – Changed revision from *D to *F. Updated to new template.	



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