EVALUATION KIT AVAILABLE

MAX2769

Universal GPS Receiver

General Description

The MAX2769 is the industry's first global navigation satellite system (GNSS) receiver covering GPS, GLONASS, and Galileo navigation satellite systems on a single chip. This single-conversion, low-IF GNSS receiver is designed to provide high performance for a wide range of consumer applications, including mobile handsets.

Designed on Maxim's advanced, low-power SiGe BiCMOS process technology, the MAX2769 offers the highest performance and integration at a low cost. Incorporated on the chip is the complete receiver chain, including a dual-input LNA and mixer, followed by the image-rejected filter, PGA, VCO, fractional-N frequency synthesizer, crystal oscillator, and a multibit ADC. The total cascaded noise figure of this receiver is as low as 1.4dB.

The MAX2769 completely eliminates the need for external IF filters by implementing on-chip monolithic filters and requires only a few external components to form a complete low-cost GPS receiver solution.

The MAX2769 is the most flexible receiver on the market. The integrated delta-sigma fractional-N frequency synthesizer allows programming of the IF frequency within a ±40Hz accuracy while operating with any reference or crystal frequencies that are available in the host system. The integrated ADC outputs 1 or 2 quantized bits for both I and Q channels, or up to 3 quantized bits for the I channel. Output data is available either at the CMOS logic or at the limited differential logic levels.

The MAX2769 is packaged in a compact 5mm x 5mm, 28-pin thin QFN package with an exposed paddle. The part is also available in die form. Contact the factory for further information.

Applications

- Location-Enabled Mobile Handsets
- PNDs (Personal Navigation Devices)
- PMPs (Personal Media Players)
- PDAs (Personal Digital Assistants)
- In-Vehicle Navigation Systems
- Telematics (Asset Tracking, Inventory Management)
- Recreational/Marine Navigation/Avionics
- Software GPS
- Laptops and Ultra-Mobile PCs
- Digital Still Cameras and Camcorders

Features

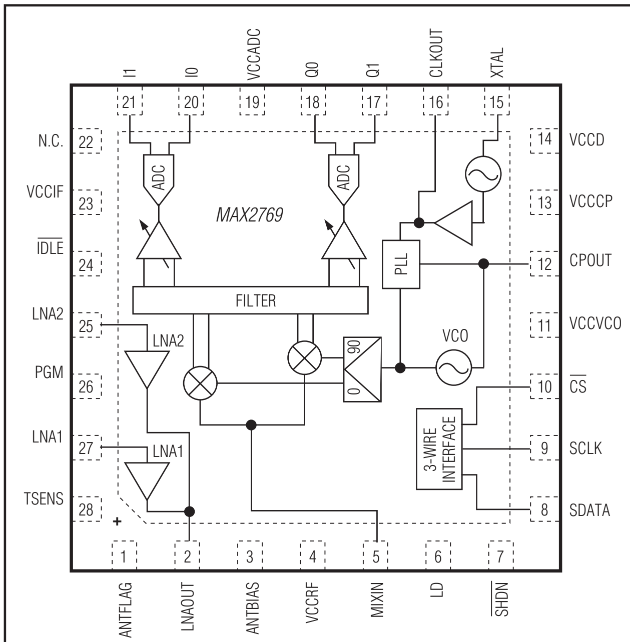
- ♦ **GPS/GLONASS/Galileo Receivers**
- ♦ **No External IF SAW or Discrete Filters Required**
- ♦ **Programmable IF Frequency**
- ♦ **Fractional-N Synthesizer with Integrated VCO Supports Wide Range of Reference Frequencies**
- ♦ **Dual-Input Uncommitted LNA for Separate Passive and Active Antenna Inputs**
- ♦ **1.4dB Cascade Noise Figure**
- ♦ **Integrated Crystal Oscillator**
- ♦ **Integrated Active Antenna Sensor**
- ♦ **10mA Supply Current in Low-Power Mode**
- ♦ **2.7V to 3.3V Supply Voltage**
- ♦ **Small, 28-Pin, RoHS-Compliant, Thin QFN Lead-Free Package (5mm x 5mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2769ETI+	-40°C to +85°C	28 Thin QFN-EP*
MAX2769E/W	-40°C to +85°C	Dice (In Wafer Form)

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed paddle.*

Pin Configuration/Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-0791; Rev 2; 6/10

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ....-0.3V to +4.2V
Other Pins to GND ....-0.3V to +(Operating V_{CC} + 0.3V)
Maximum RF Input Power ....+15dBm
Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derates 27mW/°C above +70°C)...2500mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (TQFN only, soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2769 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = GND. Registers are set to the default power-up states. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.7	2.85	3.3	V
Supply Current	Default mode, LNA1 is active (Note 2)	15	18	22	mA
	Default mode, LNA2 is active (Note 2)	12	15	19	
	Idle Mode™, $\overline{IDLE}$ = low		1.5		
	Shutdown mode, $\overline{SHDN}$ = low		20		µA
Voltage Drop at ANTBIAS from VCCRF	Sourcing 20mA at ANTBIAS		0.2		V
Short-Circuit Protection Current at ANTBIAS	ANTBIAS is shorted to ground		57		mA
Active Antenna Detection Current	To assert logic-high at ANTFLAG		1.1		mA
DIGITAL INPUT AND OUTPUT					
Digital Input Logic-High	Measure at the $\overline{SHDN}$ pin	1.5			V
Digital Input Logic-Low	Measure at the $\overline{SHDN}$ pin			0.4	V

Idle Mode is a trademark of Maxim Integrated Products, Inc.

AC ELECTRICAL CHARACTERISTICS

(MAX2769 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = GND. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ ll 7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CASCADED RF PERFORMANCE					
RF Frequency	L1 band		1575.42		MHz
Noise Figure	LNA1 input active, default mode (Note 3)		1.4		dB
	LNA2 input active, default mode (Note 3)		2.7		
	Measured at the mixer input		10.3		
Out-of-Band 3rd-Order Input Intercept Point	Measured at the mixer input (Note 4)		-7		dBm
In-Band Mixer Input Referred 1dB Compression Point	Measured at the mixer input		-85		dBm
Mixer Input Return Loss			10		dB
Image Rejection			25		dB
Spurs at LNA1 Input	LO leakage		-101		dBm
	Reference harmonics leakage		-103		
Maximum Voltage Gain	Measured from the mixer to the baseband analog output	91	96	103	dB
Variable Gain Range		55	59		dB
FILTER RESPONSE					
Passband Center Frequency			4		MHz
Passband 3dB Bandwidth	FBW = 00		2.5		MHz
	FBW = 10		4.2		
	FBW = 01		8		
Lowpass 3dB Bandwidth	FBW = 11		9		MHz
Stopband Attenuation	3rd-order filter, bandwidth = 2.5MHz, measured at 4MHz offset		30		dB
	5th-order filter, bandwidth = 2.5MHz, measured at 4MHz offset	41	49.5		
LNA					
LNA1 INPUT					
Power Gain			19		dB
Noise Figure			0.83		dB
Input IP3	(Note 5)		-1.1		dBm
Output Return Loss			10		dB
Intput Return Loss			8		dB
LNA2 INPUT					
Power Gain			13		dB
Noise Figure			1.14		dB
Input IP3	(Note 5)		1		dBm
Output Return Loss			19		dB
Input Return Loss			11		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2769 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = GND. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ ll 7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER					
LO Frequency Range	0.4V < V_{TUNE} < 2.4V	1550		1610	MHz
LO Tuning Gain			57		MHz/V
Reference Input Frequency		8		44	MHz
Main Divider Ratio		36		32,767	—
Reference Divider Ratio		1		1023	—
Charge-Pump Current	ICP = 0		0.5		mA
	ICP = 1		1		
TCXO INPUT BUFFER/OUTPUT CLOCK BUFFER					
Reference Input Level	Sine wave	0.4			V_{P-P}
Clock Output Multiply/Divide Range		÷4		x2	—
ADC					
ADC Differential Nonlinearity	AGC enabled, 3-bit output		±0.1		LSB
ADC Integral Nonlinearity	AGC enabled, 3-bit output		±0.1		LSB

Note 1: MAX2769 is production tested at T_A = +25°C. All min/max specifications are guaranteed by design and characterization from -40°C to +85°C, unless otherwise noted. Default register settings are not production tested or guaranteed. User must program the registers upon power-up.

Note 2: Default, low-NF mode of the IC. LNA choice is gated by the ANT_FLAG signal. In the normal mode of operation without an active antenna, LNA1 is active. If an active antenna is connected and ANT_FLAG switches to 1, LNA1 is automatically disabled and LNA2 becomes active. PLL is in an integer-N mode with $f_{COMP} = f_{TCXO}$ / 16 = 1.023MHz and I_{CP} = 0.5mA. The complex IF filter is configured as a 5th-order Butterworth filter with a center frequency of 4MHz and bandwidth of 2.5MHz. Output data is in a 2-bit sign/magnitude format at CMOS logic levels in the I channel only.

Note 3: The LNA output connects to the mixer input without a SAW filter between them.

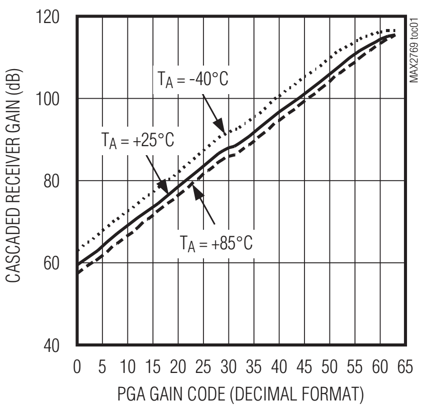
Note 4: Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz at -60dBm/tone. Passive pole at the mixer output is programmed to be 13MHz.

Note 5: Measured from the LNA input to the LNA output. Two tones are located at 12MHz and 24MHz offset frequencies from the GPS center frequency of 1575.42MHz at -60dBm per tone.

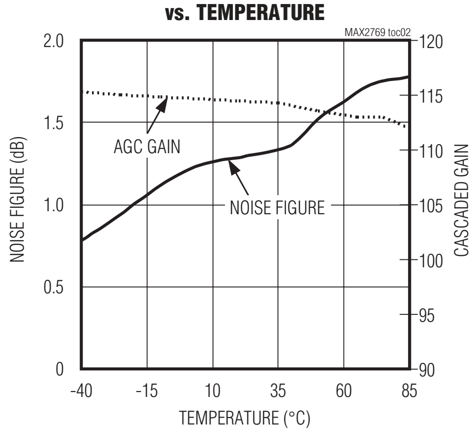
Typical Operating Characteristics

(MAX2769 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = GND. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ ll 7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

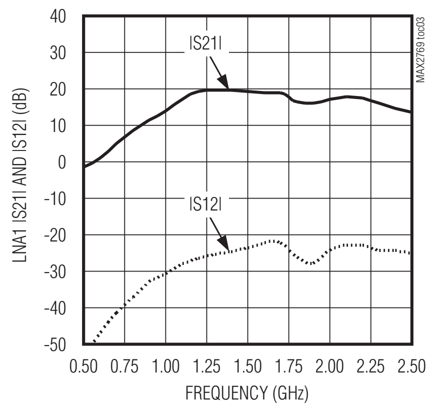
CASCADED RECEIVER GAIN vs. PGA GAIN CODE



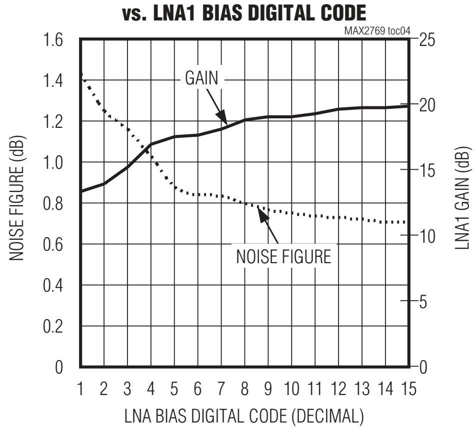
CASCADED GAIN AND NOISE FIGURE vs. TEMPERATURE



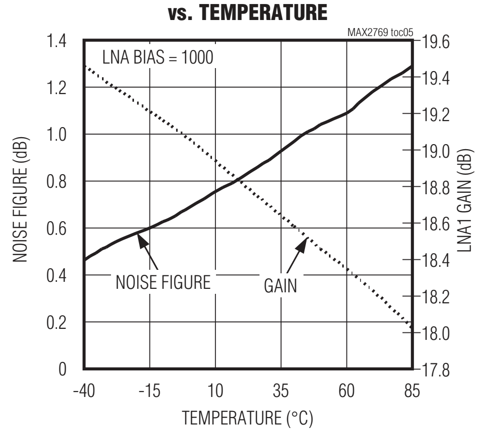
LNA1 |S21| AND |S12| vs. FREQUENCY



LNA1 GAIN AND NOISE FIGURE vs. LNA1 BIAS DIGITAL CODE



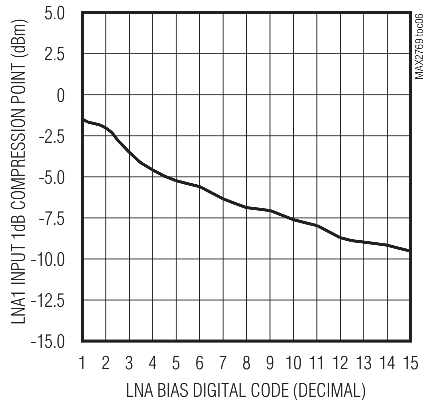
LNA1 GAIN AND NOISE FIGURE vs. TEMPERATURE



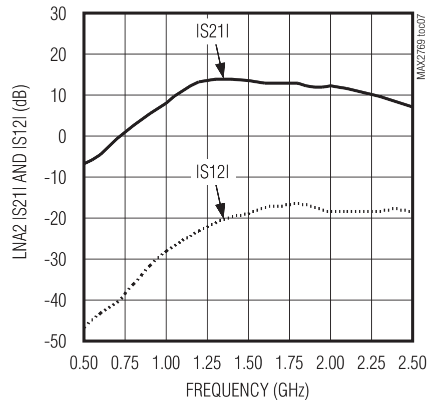
Typical Operating Characteristics (continued)

(MAX2769 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = GND. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ ll 7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

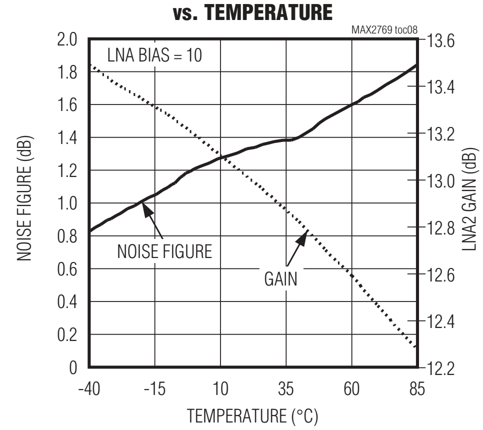
LNA1 INPUT 1dB COMPRESSION POINT vs. LNA1 BIAS DIGITAL CODE



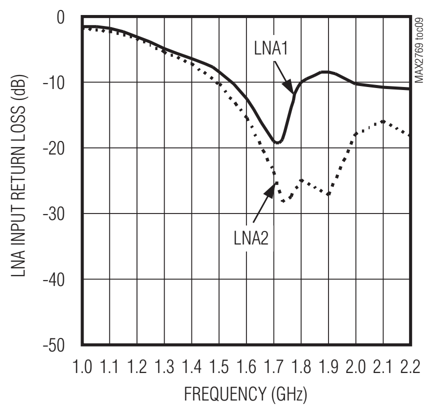
LNA2 |S21| AND |S12| vs. FREQUENCY



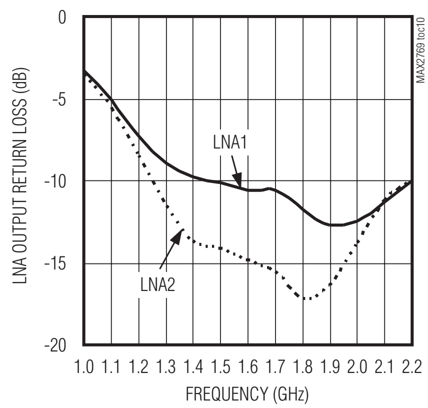
LNA2 GAIN AND NOISE FIGURE vs. TEMPERATURE



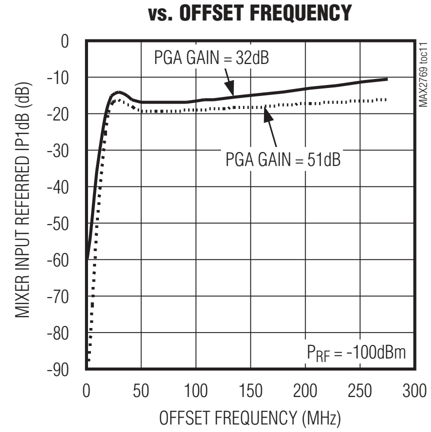
LNA INPUT RETURN LOSS vs. FREQUENCY



LNA OUTPUT RETURN LOSS vs. FREQUENCY



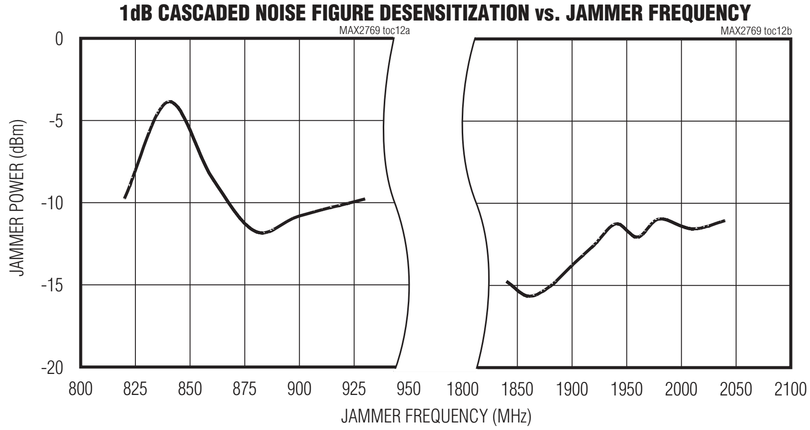
MIXER INPUT REFERRED IP1dB vs. OFFSET FREQUENCY



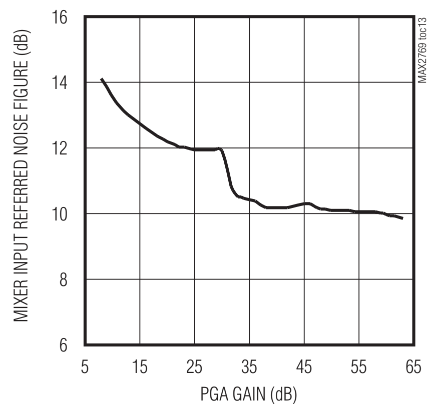
Typical Operating Characteristics (continued)

(MAX2769 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = GND. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ ll 7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

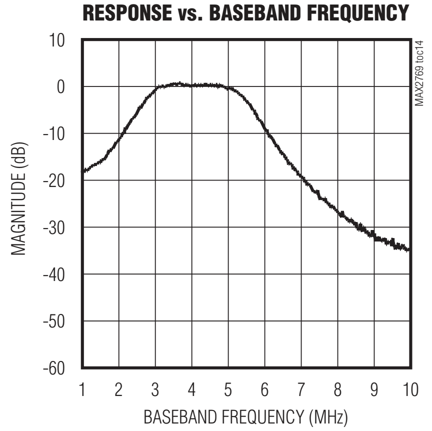
1dB CASCADED NOISE FIGURE DESENSITIZATION vs. JAMMER FREQUENCY



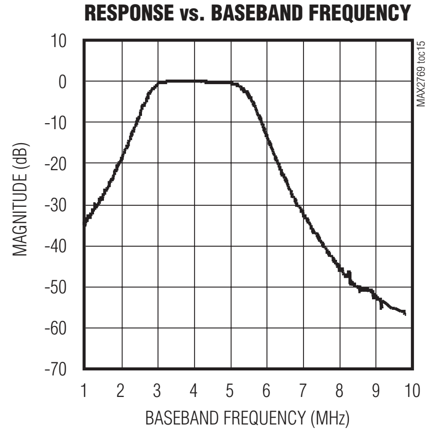
MIXER INPUT REFERRED NOISE FIGURE vs. PGA GAIN



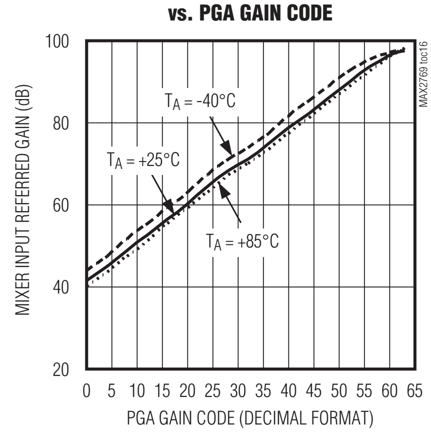
3RD-ORDER POLYPHASE FILTER MAGNITUDE RESPONSE vs. BASEBAND FREQUENCY



5TH-ORDER POLYPHASE FILTER MAGNITUDE RESPONSE vs. BASEBAND FREQUENCY



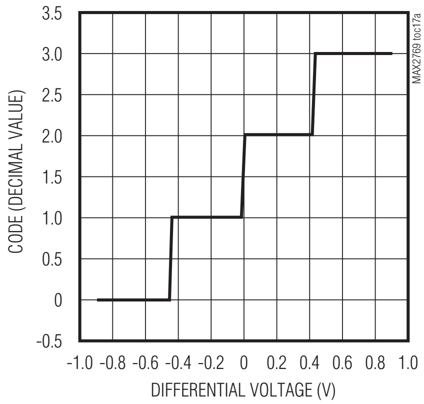
MIXER INPUT REFERRED GAIN vs. PGA GAIN CODE



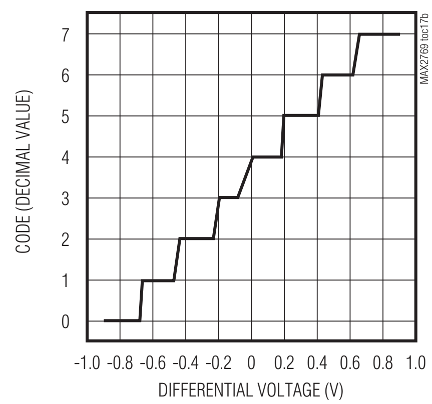
Typical Operating Characteristics (continued)

(MAX2769 EV kit, V_{CC} = 2.7V to 3.3V, T_A = -40°C to +85°C, PGM = GND. Registers are set to the default power-up states. LNA input is driven from a 50Ω source. All RF measurements are done in the analog output mode with ADC bypassed. PGA gain is set to 51dB gain by serial-interface word GAININ = 111010. Maximum IF output load is not to exceed 10kΩ ll 7.5pF on each pin. Typical values are at V_{CC} = 2.85V and T_A = +25°C, unless otherwise noted.)

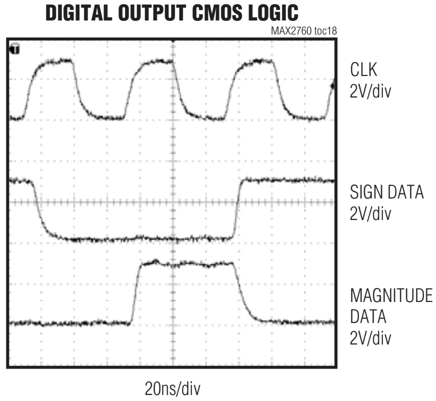
2-BIT ADC TRANSFER CURVE



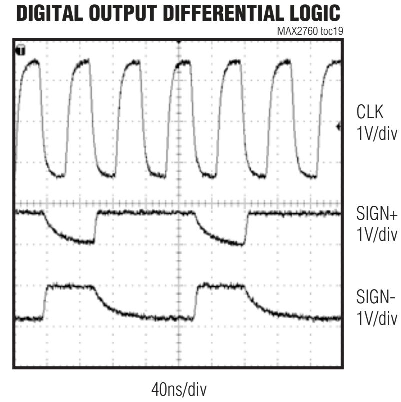
3-BIT ADC TRANSFER CURVE



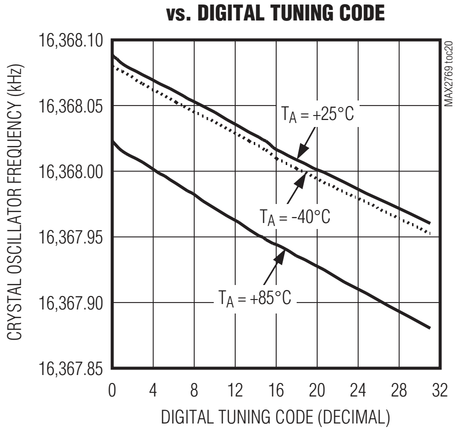
DIGITAL OUTPUT CMOS LOGIC



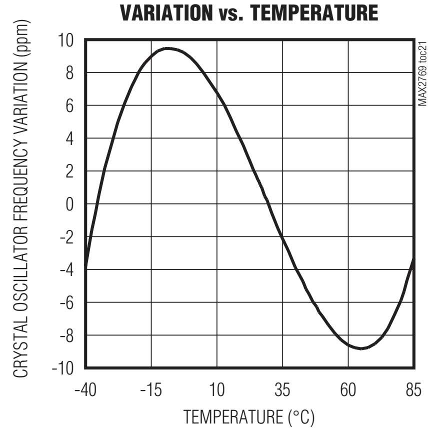
DIGITAL OUTPUT DIFFERENTIAL LOGIC



CRYSTAL OSCILLATOR FREQUENCY vs. DIGITAL TUNING CODE



CRYSTAL OSCILLATOR FREQUENCY VARIATION vs. TEMPERATURE



Typical Application Circuit

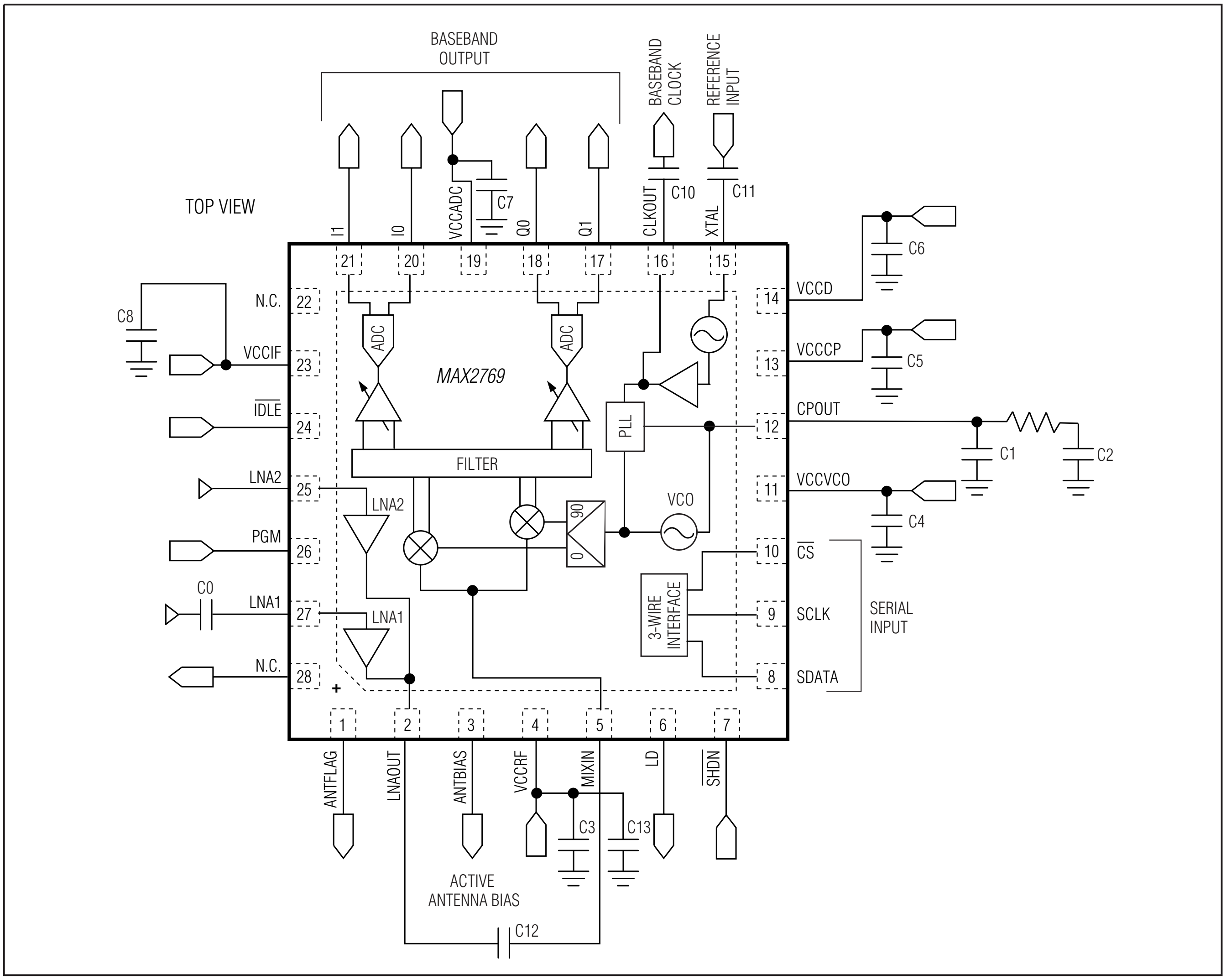


Table 1. Component List

DESIGNATION	QUANTITY	DESCRIPTION
C0	1	0.47nF AC-coupling capacitor
C1	1	27pF PLL loop filter capacitor
C2	1	0.47nF PLL loop filter capacitor
C3–C8	6	0.1µF supply voltage bypass capacitor
C10, C11	2	10nF AC-coupling capacitor
C12	1	0.47nF AC-coupling capacitor
C13	1	0.1nF supply voltage bypass capacitor
R1	1	20kΩ PLL loop filter resistor

Pin Description

PIN	NAME	FUNCTION
1	ANTFLAG	Active Antenna Flag Logic Output. A logic-high indicates that an active antenna is connected to the ANTBIAS pin.
2	LNAOUT	LNA Output. The LNA output is internally matched to 50Ω.
3	ANTBIAS	Buffered Supply Voltage Output. Provides a supply voltage bias for an external active antenna.
4	VCCRF	RF Section Supply Voltage. Bypass to GND with 100nF and 100pF capacitors in parallel as close as possible to the pin.
5	MIXIN	Mixer Input. The mixer input is internally matched to 50Ω.
6	LD	Lock-Detector CMOS Logic Output. A logic-high indicates the PLL is locked.
7	$\overline{\text{SHDN}}$	Operation Control Logic Input. A logic-low shuts off the entire device.
8	SDATA	Data Digital Input of 3-Wire Serial Interface
9	SCLK	Clock Digital Input of 3-Wire Serial Interface. Active when $\overline{\text{CS}}$ is low. Data is clocked in on the rising edge of the SCLK.
10	$\overline{\text{CS}}$	Chip-Select Logic Input of 3-Wire Serial Interface. Set $\overline{\text{CS}}$ low to allow serial data to shift in. Set $\overline{\text{CS}}$ high when the loading action is completed.
11	VCCVCO	VCO Supply Voltage. Bypass to GND with a 100nF capacitor as close as possible to the pin.
12	CPOUT	Charge-Pump Output. Connect a PLL loop filter as a shunt C and a shunt combination of series R and C (see the *Typical Application Circuit*).
13	VCCCP	PLL Charge-Pump Supply Voltage. Bypass to GND with a 100nF capacitor as close as possible to the pin.
14	VCCD	Digital Circuitry Supply Voltage. Bypass to GND with a 100nF capacitor as close as possible to the pin.
15	XTAL	XTAL or Reference Oscillator Input. Connect to XTAL or a DC-blocking capacitor if TCXO is used.
16	CLKOUT	Reference Clock Output
17	Q1	Q-Channel Voltage Outputs. Bits 0 and 1 of the Q-channel ADC output or 1-bit limited differential logic output or analog differential voltage output.
18	Q0	
19	VCCADC	ADC Supply Voltage. Bypass to GND with a 100nF capacitor as close as possible to the pin.
20	I0	I-Channel Voltage Outputs. Bits 0 and 1 of the I-channel ADC output or 1-bit limited differential logic output or analog differential voltage output.
21	I1	
22	N.C.	No Connection. Leave this pin unconnected.
23	VCCIF	IF Section Supply Voltage. Bypass to GND with a 100nF capacitor as close as possible to the pin.
24	$\overline{\text{IDLE}}$	Operation Control Logic Input. A logic-low enables the idle mode, in which the XTAL oscillator is active, and all other blocks are off.
25	LNA2	LNA Input Port 2. This port is typically used with an active antenna. Internally matched to 50Ω.
26	PGM	Logic Input. Connect to GND to use the serial interface. A logic-high allows programming to 8 hard-coded by device states connecting SDATA, $\overline{\text{CS}}$, and SCLK to supply or ground according to Table 3.
27	LNA1	LNA Input Port 1. This port is typically used with a passive antenna. Internally matched to 50Ω (see the *Typical Application Circuit*).
28	N.C.	No connection. Leave this pin open.
—	EP	Exposed Paddle. Ultra-low-inductance connection to ground. Place several vias to the PCB ground plane.

Detailed Description

Integrated Active Antenna Sensor

The MAX2769 includes a low-dropout switch to bias an external active antenna. To activate the antenna switch output, set ANTEN in the Configuration 1 register to logic 1. This closes the switch that connects the antenna bias pin to VCCRF to achieve a low 200mV dropout for a 20mA load current. A logic-low in ANTEN disables the antenna bias. The active antenna circuit also features short-circuit protection to prevent the output from being shorted to ground.

Low-Noise Amplifier (LNA)

The MAX2769 integrates two low-noise amplifiers. LNA1 is typically used with a passive antenna. This LNA requires an AC-coupling capacitor. In the default mode, the bias current is set to 4mA, the typical noise figure and IIP3 are approximately 0.8dB and -1.1dBm, respectively. LNA1 current can be programmed through ILNA in Configuration 1 register. In the low-current mode of 1mA, the typical noise figure is degraded to 1.2dB and the IIP3 is lowered to -15dBm. LNA2 is typically used with an active antenna. The LNA2 is internally matched to 50Ω and requires a DC-blocking capacitor. Bits LNAMODE in the Configuration 1 register control the modes of the two LNAs. See Table 6 for the LNA mode settings and current selections.

Mixer

The MAX2769 includes a quadrature mixer to output low-IF or zero IF I and Q signals. The quadrature mixer is internally matched to 50Ω and requires a low-side LO injection. The output of the LNA and the input of the mixer are brought off-chip to facilitate the use of a SAW filter.

Programmable Gain Amplifier (PGA)

The MAX2769 integrates a baseband programmable gain amplifier that provides 59dB of gain control range. The PGA gain can be programmed through the serial interface by setting bits GAININ in the Configuration 3 register. Set bits 12 and 11 (AGCMODE) in the Configuration 2 register to 10 to control the gain of the PGA directly from the 3-wire interface.

Automatic Gain Control (AGC)

The MAX2769 provides a control loop that automatically programs PGA gain to provide the ADC with an input power that optimally fills the converter and establishes a desired magnitude bit density at its output. An algorithm operates by counting the number of magnitude bits over 512 ADC clock cycles and comparing the magnitude bit count to the reference value provided through a control word (GAINREF). The desired magnitude bit density is expressed as a value of GAINREF in a decimal format divided by the counter length of 512. For example, to achieve the magnitude bit density of 33%, which is optimal for a 2-bit converter, program the GAINREF to 170, so that 170 / 512 = 33%.

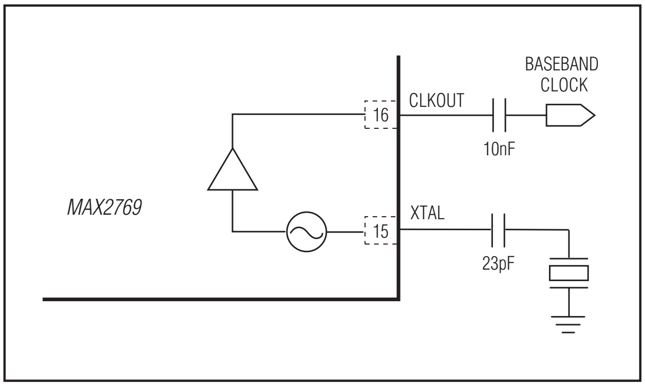


Figure 1. Schematic of the Crystal Oscillator in the MAX2679 EV Kit

Baseband Filter

The baseband filter of the receiver can be programmed to be a lowpass filter or a complex bandpass filter. The lowpass filter can be configured as a 3rd-order Butterworth filter for a reduced group delay by setting bit F3OR5 in the Configuration 1 register to be 1 or a 5th-order Butterworth filter for a steeper out-of-band rejection by setting the same bit to be 0. The two-sided 3dB corner bandwidth can be selected to be 2.5MHz, 4.2MHz, 8MHz, or 18MHz (only to be used as a lowpass filter) by programming bits FBW in the Configuration 1 register. When the complex filter is enabled by changing bit FCENX in the Configuration 1 register to 1, the lowpass filter becomes a bandpass filter and the center frequency can be programmed by bits FCEN in the Configuration 1 register.

Synthesizer

The MAX2769 integrates a 20-bit sigma-delta fractional-N synthesizer allowing the device to tune to a required VCO frequency with an accuracy of approximately ±40Hz. The synthesizer includes a 10-bit reference divider with a divisor range programmable from 1 to 1023, a 15-bit integer portion main divider with a divisor range programmable from 36 to 32767, and also a 20-bit fractional portion main divider. The reference divider is programmable by bits RDIV in the PLL integer division ratio register (see Table 10), and can accommodate reference frequencies from 8MHz to 44MHz. The reference divider needs to be set so the comparison frequency falls between 0.05MHz to 32MHz.

Table 2. Output Data Format

INTEGER VALUE	SIGN/MAGNITUDE					UNSIGNED BINARY					TWO'S COMPLEMENT BINARY				
	1b	1.5b	2b	2.5b	3b	1b	1.5b	2b	2.5b	3b	1b	1.5b	2b	2.5b	3b
7	0	01	01	011	011	1	10	11	101	111	0	01	01	101	011
5	0	01	01	001	010	1	10	11	100	110	0	01	01	100	010
3	0	01	00	001	001	1	10	10	100	101	0	01	00	100	001
1	0	00	00	000	000	1	11	10	011	110	0	00	00	011	000
-1	1	00	10	000	100	0	11	01	011	011	1	00	11	011	111
-3	1	10	10	101	101	0	01	01	001	010	1	11	11	111	110
-5	1	10	11	101	110	0	01	00	001	001	1	11	10	111	101
-7	1	10	11	111	111	0	01	00	000	000	1	11	10	110	100

The PLL loop filter is the only external block of the synthesizer. A typical PLL filter is a classic C-R-C network at the charge-pump output. The charge-pump output sink and source current is 0.5mA by default, and the LO tuning gain is 57MHz/V. As an example, see the *Typical Application Circuit* for the recommended loop-filter component values for f_{COMP} = 1.023MHz and loop bandwidth = 50kHz.

The desired integer and fractional divider ratios can be calculated by dividing the LO frequency (f_{LO}) by f_{COMP}. f_{COMP} can be calculated by dividing the TCXO frequency (f_{TCXO}) by the reference division ratio (RDIV). For example, let the TCXO frequency be 20MHz, RDIV be 1, and the nominal LO frequency be 1575.42MHz. The following method can be used when calculating divider ratios supporting various reference and comparison frequencies:

$$\text{Comparison Frequency} = \frac{f_{TCXO}}{RDIV} = \frac{20MHz}{1} = 20MHz$$

$$\text{LO Frequency Divider} = \frac{f_{LO}}{f_{COMP}} = \frac{1575.42MHz}{20MHz} = 78.771$$

Integer Divider = 78(d) = 000 000 0100 1110 (binary)

Fractional Divider = 0.771 x 2^{20} = 808452 (decimal) = 1100 0101 0110 0000 0100

In the fractional mode, the synthesizer should not be operated with integer division ratios greater than 251.

Crystal Oscillator

The MAX2769 includes an on-chip crystal oscillator. A parallel mode crystal is required when the crystal oscillator is being used. It is recommended that an AC-coupling capacitor be used in series with the crystal and the XTAL pin to optimize the desired load capacitance and to center the crystal-oscillator frequency. Take the parasitic loss of interconnect traces on the PCB into account when optimizing the load capacitance. For example, the MAX2769 EV kit utilizes a 16.368MHz crystal that is designed for a 12pF load capacitance. A series capacitor of 23pF is used to center the crystal oscillator frequency, see Figure 1. In addition, the 5-bit serial-interface word, XTALCAP in the PLL Configuration register, can be used to vary the crystal-oscillator frequency electronically. The range of the electronic adjustment depends on how much the chosen crystal frequency can be pulled by the varying capacitor. The frequency of the crystal oscillator used on the MAX2769 EV kit has a range of approximately 200Hz.

The MAX2769 provides a reference clock output. The frequency of the clock can be adjusted to crystal-oscillator frequency, a quarter of the oscillator frequency, a half of the oscillator frequency, or twice the oscillator frequency, by programming bits REFDIV in the PLL Configuration register.

ADC

The MAX2769 features an on-chip ADC to digitize the downconverted GPS signal. The maximum sampling rate of the ADC is approximately 50Msps. The sampled output is provided in a 2-bit format (1-bit magnitude and 1-bit sign) by default and also can be configured as a 1-bit, 1.5-bit, or 2-bit in both I and Q channels, or 1-bit, 1.5-bit, 2-bit, 2.5-bit, or 3-bit in the I channel only. The ADC supports the digital outputs in three different formats: the unsigned binary, the sign and magnitude, or the two's complement format by setting bits FORMAT in Configuration register 2. MSB bits are output at I1 or Q1 pins and LSB bits are output at I0 or Q0 pins, for I or Q channel, respectively. In the case of 2.5-bit or 3-bit, output data format is selected in the I channel only, the

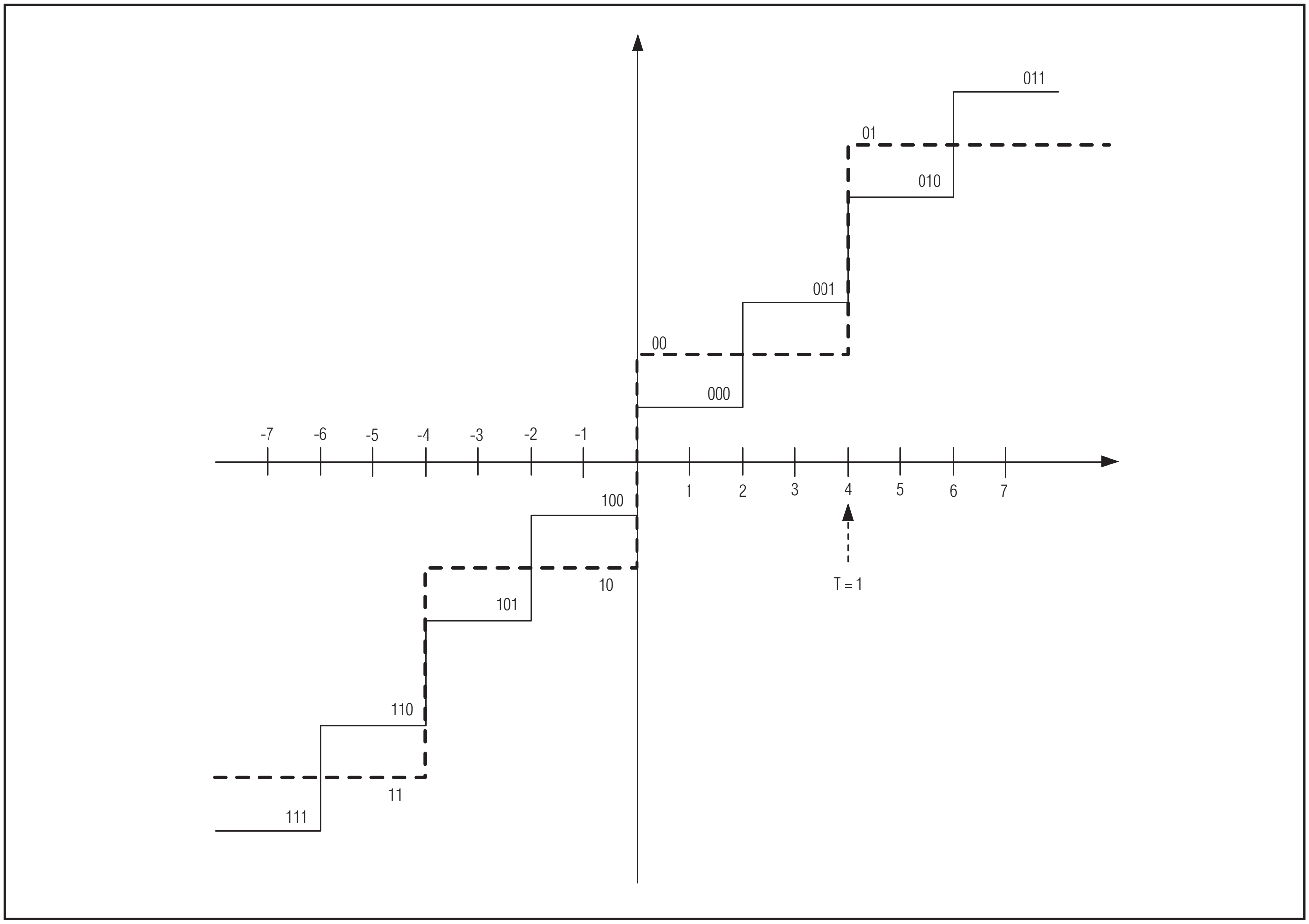


Figure 2. ADC Quantization Levels for 2- and 3-Bit Cases

MSB is output at I1, the second bit is at I0, and the LSB is at Q1.

Figure 2 illustrates the ADC quantization levels for 2- and 3-bit cases and also describes the sign/magnitude data mapping. The variable T = 1 designates the location of the magnitude threshold for the 2-bit case.

Fractional Clock Divider

A 12-bit fractional clock divider is located in the clock path prior to the ADC and can be used to generate the ADC clock that is a fraction of the reference input clock. In a fractional divider mode, the instantaneous division ratio alternates between integer division ratios to achieve the required fraction. For example, if the fractional output clock is 4.5 times slower than the input clock, an average division ratio of 4.5 is achieved through an equal series of alternating divide-by-4 and divide-by-5 periods. The fractional division ratio is given by:

$$f_{OUT} / f_{IN} = L_{COUNT} / (4096 - M_{COUNT} + L_{COUNT})$$

where L_{COUNT} and M_{COUNT} are the 12-bit counter values programmed through the serial interface.

DSP Interface

GPS data is output from the ADC as the four logic signals (bit_0, bit_1, bit_2, and bit_3) that represent sign/magnitude, unsigned binary, or two's complement binary data in the I (bit_0 and bit_1) and Q (bit_2 and bit_3) channels. The resolution of the ADC can be set up to 3 bits per channel. For example, the 2-bit I and Q data in sign/magnitude format is mapped as follows: $bit_0 = I_{SIGN}$, $bit_1 = I_{MAG}$, $bit_2 = Q_{SIGN}$, and $bit_3 = Q_{MAG}$. The data can be serialized in 16-bit segments of bit_0, followed by bit_1, bit_2, and bit_3. The number of bits to be serialized is controlled by the bits STRMBITS in the Configuration 3 regis-

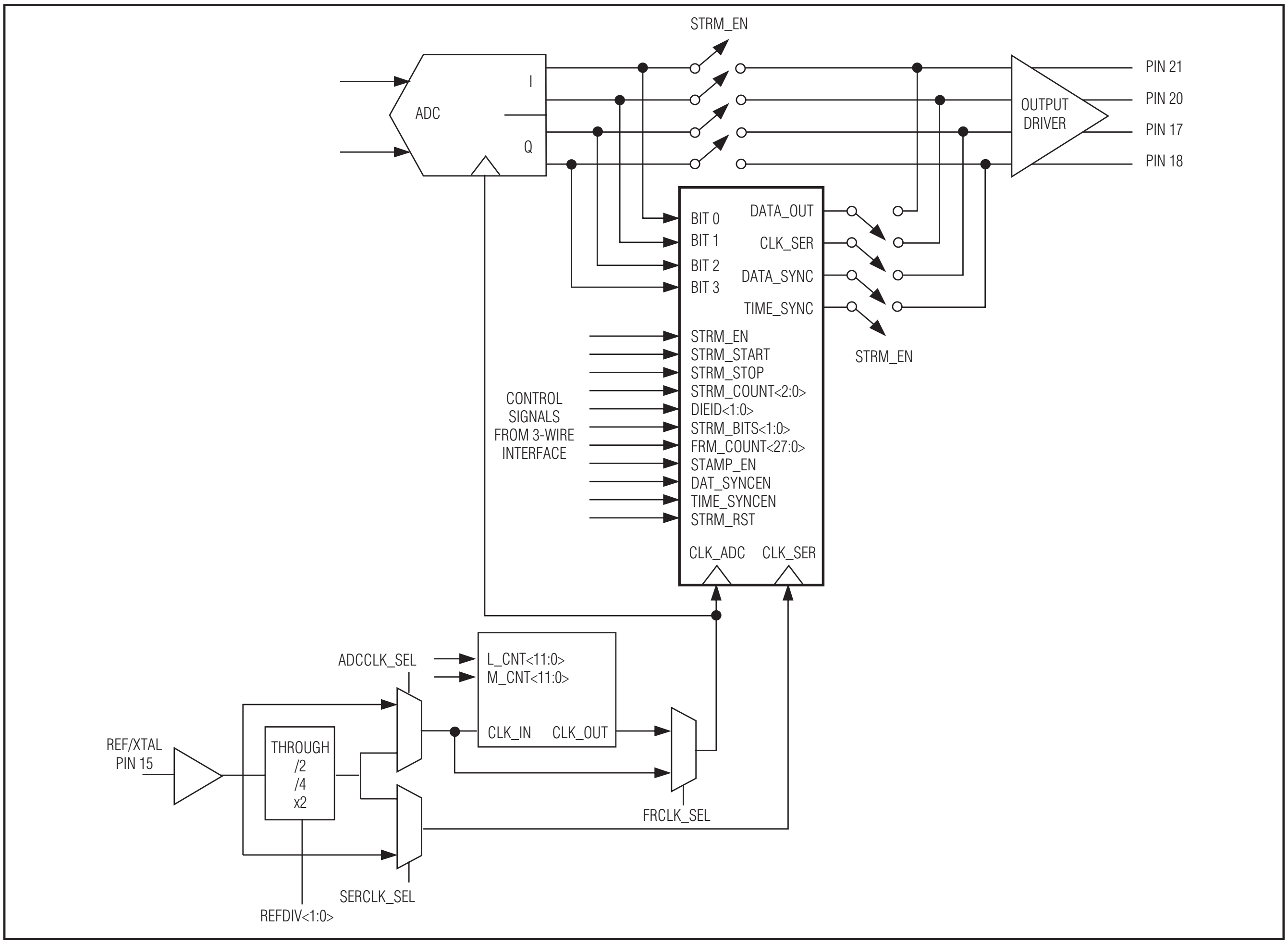


Figure 3. DSP Interface Top-Level Connectivity and Control Signals

ter. This selects between bit_0; bit_0 and bit_1; bit_0 and bit_2; and bit_0, bit_1, bit_2, and bit_3 cases. If only bit_0 is serialized, the data stream consists of bit_0 data only. If a serialization of bit_0 and bit_1 (or bit_2) is selected, the stream data pattern consists of 16 bits of bit_0 data followed by 16 bits of bit_1 (or bit_2) data, which, in turn, is followed by 16 bits of bit_0 data, and so on. In this case, the serial clock must be at least twice as fast as the ADC clock. If a 4-bit serialization of bit_0, bit_1, bit_2, and bit_3 is chosen, the serial clock must be at least four times faster than the ADC clock.

The ADC data is loaded in parallel into four holding registers that correspond to four ADC outputs. Holding registers are 16 bits long and are clocked by the ADC clock. At the end of the 16-bit ADC cycle, the data is transferred into four shift registers and shifted serially to the output during the next 16-bit ADC cycle. Shift registers are clocked by a serial clock that must be chosen fast enough so that all data is shifted out before the next set of data is loaded from the ADC. An all-zero pattern follows the data after all valid ADC data are streamed to the output. A DATASYNC signal is used to signal the beginning of each valid 16-bit data slice. In addition, there is a TIME_SYNC signal that is output every 128 to 16,384 cycles of the ADC clock.

Preconfigured Device States

When a serial interface is not available, the device can be used in preconfigured states that don't require programming through the serial interface. Connecting the PGM pin to logic-high and SCLK, SDATA, and $\overline{CS}$ pins to either logic-high or low sets the device in one of the preconfigured states according to Table 3.

Serial Interface, Address, and Bit Assignments

A serial interface is used to program the MAX2769 for configuring the different operating modes.

The serial interface is controlled by three signals: SCLK (serial clock), $\overline{CS}$ (chip select), and SDATA (serial data). The control of the PLL, AGC, test, and block selection is performed through the serial-interface bus from the baseband controller. A 32-bit word, with the MSB (D27) being sent first, is clocked into a serial shift register when the chip-select signal is asserted low. The timing of the interface signals is shown in Figure 4 and Table 4 along with typical values for setup and hold time requirements.

Table 3. Preconfigured Device States

DEVICE STATE	DEVICE ELECTRICAL CHARACTERISTICS								3-WIRE CONTROL PINS		
	REFERENCE FREQUENCY (MHz)	REFERENCE DIVISION RATIO	MAIN DIVISION RATIO	I AND Q OR I ONLY	NUMBER OF I Q BITS	I AND Q LOGIC LEVEL	IF CENTER FREQUENCY (MHz)	IF FILTER ORDER	SCLK	DATA	$\overline{CS}$
0	16.368	16	1536	I	1	Differential	4.092	5th	0	0	0
1	16.368	16	1536	I	1	Differential	4.092	3rd	0	0	1
2	16.368	16	1536	I	2	CMOS	4.092	5th	0	1	0
3	32.736	32	1536	I	2	CMOS	4.092	5th	0	1	1
4	19.2	96	7857	I	2	CMOS	4.092	5th	1	0	0
5	18.414	18	1539	I	2	CMOS	1.023*	5th	1	0	1
6	13	65	7857	I	2	CMOS	4.092	5th	1	1	0
7	16.368	16	1536	I	1	CMOS	4.092	5th	1	1	1

**If the IF center frequency is programmed to 1.023MHz, the filter passband extends from 0.1MHz to 2.6MHz.*

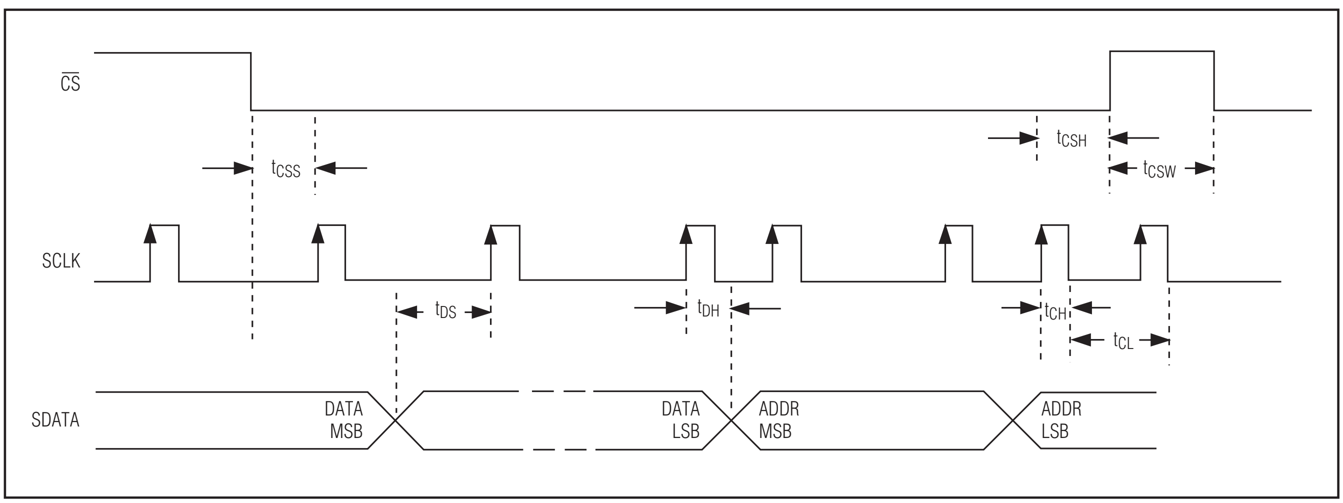


Figure 4. 3-Wire Timing Diagram

Table 4. Serial-Interface Timing Requirements

SYMBOL	PARAMETER	TYP VALUE	UNITS
t_{CSS}	Falling edge of $\overline{CS}$ to rising edge of the first SCLK time.	10	ns
t_{DS}	Data to serial-clock setup time.	10	ns
t_{DH}	Data to clock hold time.	10	ns
t_{CH}	Serial clock pulse-width high.	25	ns
t_{CL}	Clock pulse-width low.	25	ns
t_{CSH}	Last SCLK rising edge to rising edge of $\overline{CS}$.	10	ns
t_{CSW}	$\overline{CS}$ high pulse width.	1	clock

Table 5. Default Register Setting

REGISTER NAME	ADDRESS (A3:A0)	DATA	DEFAULT (D27:D0)
CONF1	0000	Configures RX and IF sections, bias settings for individual blocks.	A2919A3
CONF2	0001	Configures AGC and output sections.	0550288
CONF3	0010	Configures support and test functions for IF filter and AGC.	EAFF1DC
PLLCONF	0011	PLL, VCO, and CLK settings.	9EC0008
DIV	0100	PLL main and reference division ratios, other controls.	0C00080
FDIV	0101	PLL fractional division ratio, other controls.	8000070
STRM	0110	DSP interface number of frames to stream.	8000000
CLK	0111	Fractional clock-divider values.	10061B2
TEST1	1000	Reserved for test mode.	1E0F401
TEST2	1001	Reserved for test mode.	14C0402

Detailed Register Definitions

Table 6. Configuration 1 (Address: 0000)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
CHIPEN	27	1	Chip enable. Set 1 to enable the device and 0 to disable the entire device except the serial bus.
IDLE	26	0	Idle enable. Set 1 to put the chip in the idle mode and 0 for operating mode.
ILNA1	25:22	1000	LNA1 current programming.
ILNA2	21:20	10	LNA2 current programming.
ILO	19:18	10	LO buffer current programming.
IMIX	17:16	01	Mixer current programming.
MIXPOLE	15	0	Mixer pole selection. Set 1 to program the passive filter pole at mixer output at 36MHz, or set 0 to program the pole at 13MHz.
LNAMODE	14:13	00	LNA mode selection, D14:D13 = 00: LNA selection gated by the antenna bias circuit, 01: LNA2 is active; 10: LNA1 is active; 11: both LNA1 and LNA2 are off.
MIXEN	12	1	Mixer enable. Set 1 to enable the mixer and 0 to shut down the mixer.
ANTEN	11	1	Antenna bias enable. Set 1 to enable the antenna bias and 0 to shut down the antenna bias.
FCEN	10:5	001101	IF center frequency programming. Default for f_{CENTER} = 4MHz, BW = 2.5MHz.
FBW	4:3	00	IF filter center bandwidth selection. D4:D3 = 00: 2.5MHz; 10: 4.2MHz; 01: 8MHz; 11: 18MHz (only used as a lowpass filter).
F3OR5	2	0	Filter order selection. Set 0 to select the 5th-order Butterworth filter. Set 1 to select the 3rd-order Butterworth filter.
FCENX	1	1	Polyphase filter selection. Set 1 to select complex bandpass filter mode. Set 0 to select lowpass filter mode.
FGAIN	0	1	IF filter gain setting. Set 0 to reduce the filter gain by 6dB.

Table 7. Configuration 2 (Address: 0001)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
IQEN	27	0	I and Q channels enable. Set 1 to enable both I and Q channels and 0 to enable I channel only.
GAINREF	26:15	170d	AGC gain reference value expressed by the number of MSB counts (magnitude bit density).
—	14:13	00	Reserved.
AGCMODE	12:11	00	AGC mode control. Set D12:D11 = 00: independent I and Q; 01: I and Q gains are locked to each other; 10: gain is set directly from the serial interface by GAININ; 11: disallowed state.
FORMAT	10:9	01	Output data format. Set D10:D9 = 00: unsigned binary; 01: sign and magnitude; 1X: two's complement binary.
BITS	8:6	010	Number of bits in the ADC. Set D8:D6 = 000: 1 bit, 001: 1.5 bits; 010: 2 bits; 011: 2.5 bits, 100: 3 bits.
DRVCFG	5:4	00	Output driver configuration. Set D5:D4 = 00: CMOS logic, 01: limited differential logic; 1X: analog outputs.
LOEN	3	1	LO buffer enable. Set 1 to enable LO buffer or 0 to disable the buffer.
RESERVED	2	0	Reserved.
DIEID	1:0	00	Identifies a version of the IC.

Table 8. Configuration 3 (Address: 0010)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
GAININ	27:22	111010	PGA gain value programming from the serial interface in steps of dB per LSB.
FSLOWEN	21	1	Low value of the ADC full-scale enable. Set 1 to enable or 0 to disable.
HILOADEN	20	0	Set 1 to enable the output driver to drive high loads.
ADCEN	19	1	ADC enable. Set 1 to enable ADC or 0 to disable.
DRVEN	18	1	Output driver enable. Set 1 to enable the driver or 0 to disable.
FOFSTEN	17	1	Filter DC offset cancellation circuitry enable. Set 1 to enable the circuitry or 0 to
FILTEN	16	1	IF filter enable. Set 1 to enable the filter or 0 to disable.
FHIPEN	15	1	Highpass coupling enable. Set 1 to enable the highpass coupling between the filter and PGA, or 0 to disable the coupling.
—	14	1	Reserved.
PGAIEN	13	1	I-channel PGA enable. Set 1 to enable PGA in the I channel or 0 to disable.
PGAQEN	12	0	Q-channel PGA enable. Set 1 to enable PGA in the Q channel or 0 to disable.
STRMEN	11	0	DSP interface for serial streaming of data enable. This bit configures the IC such that the DSP interface is inserted in the signal path. Set 1 to enable the interface or 0 to disable the interface.
STRMSTART	10	0	The positive edge of this command enables data streaming to the output. It also enables clock, data sync, and frame sync outputs.
STRMSTOP	9	0	The positive edge of this command disables data streaming to the output. It also disables clock, data sync, and frame sync outputs.
STRMCOUNT	8:6	111	Sets the length of the data counter from 128 (000) to 16,394 (111) bits per frame.
STRMBITS	5:4	01	Number of bits streamed. D5:D4 = 00: I MSB; 01: I MSB, I LSB; 10: I MSB, Q MSB; 11: I MSB, I LSB, Q MSB, Q LSB.
STAMPEN	3	1	The signal enables the insertion of the frame number at the beginning of each frame. If disabled, only the ADC data is streamed to the output.
TIMESYNCEN	2	1	This signal enables the output of the time sync pulses at all times when streaming is enabled by the STRMEN command. Otherwise, the time sync pulses are available only when data streaming is active at the output, for example, in the time intervals bound by the STRMSTART and STRMSTOP commands.
DATSYNCEN	1	0	This control signal enables the sync pulses at the DATASYNC output. Each pulse is coincident with the beginning of the 16-bit data word that corresponds to a given output bit.
STRMRST	0	0	This command resets all the counters irrespective of the timing within the stream cycle.

Table 9. PLL Configuration (Address: 0011)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
VCOEN	27	1	VCO enable. Set 1 to enable the VCO or 0 to disable VCO.
IVCO	26	0	VCO current-mode selection. Set 1 to program the VCO in the low-current mode or 0 to program in the normal mode.
—	25	0	Reserved.
REFOUTEN	24	1	Clock buffer enable. Set 1 to enable the clock buffer or 0 to disable the clock buffer.
—	23	1	Reserved.
REFDIV	22:21	11	Clock output divider ratio. Set D22:D21 = 00: clock frequency = XTAL frequency x 2; 01: clock frequency = XTAL frequency / 4; 10: clock frequency = XTAL frequency / 2; 11: clock frequency = XTAL.
IXTAL	20:19	01	Current programming for XTAL oscillator/buffer. Set D20:D19 = 00: oscillator normal current; 01: buffer normal current; 10: oscillator medium current; 11: oscillator high current.
XTALCAP	18:14	10000	Digital XTAL load cap programming.
LDMUX	13:10	0000	LD pin output selection. Set D13:D10 = 0000: PLL lock-detect signal.
ICP	9	0	Charge-pump current selection. Set 1 for 1mA and 0 for 0.5mA.
PFDEN	8	0	Set 0 for normal operation or 1 to disable the PLL phase frequency detector.
—	7	0	Reserved.
CPTEST	6:4	000	Charge-pump test. Set D6:D4 = 000: normal operation; X10: pump up; X01 = pump down; 100 = high impedance; 111: both up and down on.
INT_PLL	3	1	PLL mode control. Set 1 to enable the integer-N PLL or 0 to enable the fractional-N PLL.
PWRSAV	2	0	PLL power-save mode. Set 1 to enable the power-save mode or 0 to disable.
—	1	0	Reserved.
—	0	0	Reserved.

Table 10. PLL Integer Division Ratio (Address 0100)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
NDIV	27:13	1536d	PLL integer division ratio.
RDIV	12:3	16d	PLL reference division ratio.
—	2:0	000	Reserved.

Table 11. PLL Division Ratio (Address 0101)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
FDIV	27:8	80000h	PLL fractional divider ratio.
—	7:0	01110000	Reserved.

Table 12. DSP Interface (Address 0110)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
FRAMECOUNT	27:0	8000000h	This word defines the frame number at which to start streaming. This mode is active when streaming mode is enabled by a command STRMEN, but a command STRMSTART is not received. In this case, the frame counter is reset upon the assertion of STRMEN, and it begins its count. When the frame number reaches the value defined by FRMCOUNT, the streaming begins.

Table 13. Clock Fractional Division Ratio (Address 0111)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
L_CNT	27:16	256d	Sets the value for the L counter.
M_CNT	15:4	1563d	Sets the value for the M counter.
FCLKIN	3	0	Fractional clock divider. Set 1 to select the ADC clock to come from the fractional clock divider, or 0 to bypass the ADC clock from the fractional clock divider.
ADCCLK	2	0	ADC clock selection. Set 0 to select the ADC and fractional divider clocks to come from the reference divider/multiplier.
SERCLK	1	1	Serializer clock selection. Set 0 to select the serializer clock output to come from the reference divider/multiplier.
MODE	0	0	DSP interface mode selection.

Table 14. Test Mode 1 (Address 1000)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
—	27:0	1E0F401	Reserved.

Table 15. Test Mode 2 (Address 1001)

DATA BIT	LOCATION	DEFAULT VALUE	DESCRIPTION
—	27:0	14C0402	Reserved.

Applications Information

The LNA and mixer inputs require careful consideration in matching to 50Ω lines. Proper supply bypassing, grounding, and layout are required for reliable performance from any RF circuit.

Low-Power Operation

The MAX2769 can be operated in a low-power mode by programming the bias current values of individual blocks to their minimum recommended values. The list below summarizes the recommended changes to serial interface registers from their default states to achieve a low-power operation:

ILNA1 = 0010

ILNA2 = 00

ILO = 00

IMIX = 00

F3OR5 = 1

ANTEN = 0

BITS = 000

IVCO = 0

REFOUTEN = 0

PLLPWRSAV = 1

In this mode, LNA, mixer, LO, and VCO currents are reduced to their minimum recommended values. The IF filter is configured as a 3rd-order filter. The output data is in a 1-bit CMOS mode in the I channel only. PLL is in an integer-N power-saving mode, which can be used if the main division ratio is divisible by 32. The antenna bias circuitry is disabled.

In the low-power mode, the total current consumption reduces to 10mA, while the total cascaded noise figure increases to 3.8dB.

Operation in Wideband Galileo and GLONASS Applications

The use of the wideband receiver options is recommended for Galileo and GLONASS applications. The frequency synthesizer is used to tune LO to a desired frequency, which, in turn, determines the choice of the IF center frequency. Either a fractional-N or an integer-N mode of the frequency synthesizer can be used depending on the choice of the reference frequency.

For Galileo reception, set the IF filter bandwidth to 4.2MHz (FBW = 10) and adjust the IF center frequency through a control word FCEN to the middle of the down-converted signal band. Alternatively, use wideband settings of 8MHz and 18MHz when the receiver is in a zero-IF mode.

For GLONASS as well as GPS P-code reception, a zero-IF receiver configuration is used in which the IF filter is used in a lowpass filter mode (FCENX = 1) with a two-sided bandwidth of 18MHz.

It is recommended that an active antenna LNA be used in wide-bandwidth applications such that the PGA is operated at lower gain levels for a maximum bandwidth. If a PGA gain is programmed directly from a serial interface, GAININ values between 32 and 38 are recommended. Set the filter pole at the mixer output to 36MHz through MIXPOLE = 1.

Layout Issues

The MAX2769 EV kit can be used as a starting point for layout. For best performance, take into consideration grounding and routing of RF, baseband, and power-supply PCB proper line. Make connections from vias to the ground plane as short as possible. On the high-impedance ports, keep traces short to minimize shunt capacitance. EV kit Gerber files can be requested at www.maxim-ic.com.

Power-Supply Layout

To minimize coupling between different sections of the IC, a star power-supply routing configuration with a large decoupling capacitor at a central V_{CC} node is recommended. The V_{CC} traces branch out from this node, each going to a separate V_{CC} node in the circuit. Place a bypass capacitor as close as possible to each supply pin This arrangement provides local decoupling at each V_{CC} pin. Use at least one via per bypass capacitor for a low-inductance ground connection. Do not share the capacitor ground vias with any other branch.

Chip Information

PROCESS: SiGe BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2855+3	21-0140
WAFER	WDICE8	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/07	Initial release	—
1	1/09	Added MAX2769E/W, updated specifications	1, 4, 12, 16, 22
2	6/10	Removed references to temperature sensor function, changed four specifications for SPF, and added soldering temperature	1–4, 8, 9, 10, 14–18, 22

Maxim Integrated 160 Rio Robles, San Jose, CA 95134 USA 1-408-601-1000