CY14C064I
CY14B064I
CY14E064I

64-Kbit (8 K × 8) Serial (I^2C) nvSRAM with Real Time Clock

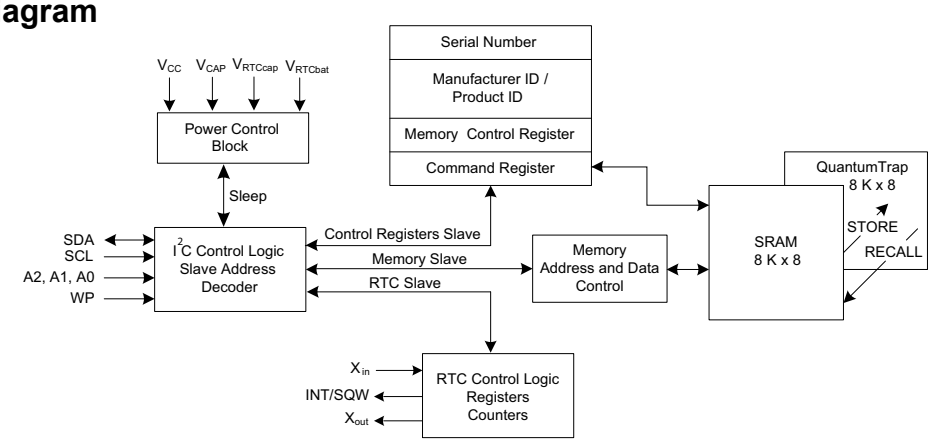
Features

- 64-Kbit nonvolatile static random access memory (nvSRAM)
  - Internally organized as 8 K × 8
  - STORE to QuantumTrap nonvolatile elements initiated automatically on power-down (AutoStore) or by using I^2C command (Software STORE) or HSB pin (Hardware STORE)
  - RECALL to SRAM initiated on power-up (Power-Up RECALL) or by I^2C command (Software RECALL)
  - Automatic STORE on power-down with a small capacitor
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years at 85 °C
- Real Time Clock (RTC)
  - Full-featured RTC
  - Watchdog timer
  - Clock alarm with programmable interrupts
  - Backup power fail indication
  - Square wave output with programmable frequency (1 Hz, 512 Hz, 4096 Hz, 32.768 kHz)
  - Capacitor or battery backup for RTC
  - Backup current of 0.45 µA (typical)
- High-speed I^2C interface [1]
  - Industry standard 100 kHz and 400 kHz speed
  - Fast mode Plus 1 MHz speed
  - High speed: 3.4 MHz
  - Zero cycle delay reads and writes
- Write protection
  - Hardware protection using Write Protect (WP) pin
  - Software block protection for one-quarter, one-half, or entire array
- I^2C access to special functions
  - Nonvolatile STORE/RECALL
  - 8-byte serial number
  - Manufacturer ID and Product ID
  - Sleep mode
- Low power consumption
  - Average active current of 1 mA at 3.4 MHz operation
  - Average standby mode current of 250 µA
  - Sleep mode current of 8 µA
- Industry standard configurations
  - Operating voltages:
    - CY14C064I: V_{CC} = 2.4 V to 2.6 V
    - CY14B064I: V_{CC} = 2.7 V to 3.6 V
    - CY14E064I: V_{CC} = 4.5 V to 5.5 V
  - Industrial temperature
  - 16-pin small outline integrated circuit (SOIC) package
  - Restriction of hazardous substances (RoHS) compliant

Overview

The Cypress CY14C064I/CY14B064I/CY14E064I combines a 64-Kbit nvSRAM[2] with a full-featured RTC in a monolithic integrated circuit with serial I^2C interface. The memory is organized as 8 K words of 8 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, creating the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while the QuantumTrap cells provide highly reliable nonvolatile storage of data. Data transfers from SRAM to the nonvolatile elements (STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM from the nonvolatile memory (RECALL operation). The STORE and RECALL operations can also be initiated by the user through I^2C commands.

Logic Block Diagram

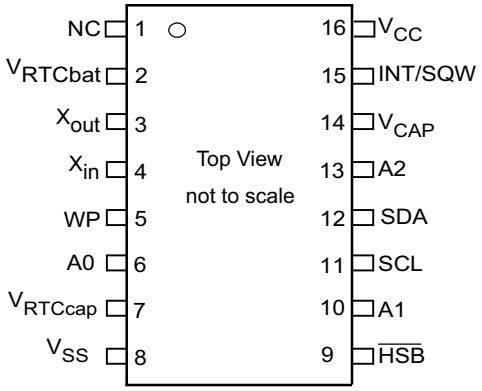


Notes
1. The I^2C nvSRAM is a single solution which is usable for all four speed modes of operation. As a result, some I/O parameters are slightly different than those on chips which support only one mode of operation. Refer to AN87209 for more details.
2. Serial (I^2C) nvSRAM will be referred to as nvSRAM throughout the datasheet.

Contents

Pinout

Figure 1. 16-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
SCL	Input	Clock: Runs at speeds up to a maximum of f_{SCL}.
SDA	Input/Output	I/O: Input/output of data through I^2C interface. Output: Is open-drain and requires an external pull-up resistor.
WP	Input	Write Protect: Protects the memory from all writes. This pin is internally pulled LOW and hence can be left open if not connected.
A2–A0	Input	Slave Address: Defines the slave address for I^2C. These pins are internally pulled LOW and hence can be left open if not connected.
$\overline{HSB}$	Input/Output	Hardware STORE Busy: Output: Indicates busy status of nvSRAM when LOW. After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (External pull-up resistor connection optional). Input: Hardware STORE implemented by pulling this pin LOW externally.
V_{CAP}	Power supply	AutoStore capacitor: Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If not required, AutoStore must be disabled and this pin left as No Connect. It must never be connected to ground.
V_{RTCcap}[3]	Power supply	Capacitor backup for RTC: Left unconnected if V_{RTCbat} is used.
V_{RTCbat}[3]	Power supply	Battery backup for RTC: Left unconnected if V_{RTCcap} is used.
X_{out}[3]	Output	Crystal output connection
X_{in}[3]	Input	Crystal input connection
INT/SQW[3]	Output	Interrupt output/calibration/square wave. Programmable to respond to the clock alarm, the watchdog timer, and the power monitor. Also programmable to either active HIGH (push or pull) or LOW (open drain). In Calibration mode, a 512 Hz square wave is driven out. In Square Wave mode, the user may select a frequency of 1 Hz, 512 Hz, 4096 Hz, or 32768 Hz to be used as a continuous output.
NC	No connect	No connect. This pin is not connected to the die.
V_{SS}	Power supply	Ground
V_{CC}	Power supply	Power supply

Note
3. Left unconnected if RTC feature is not used.

I²C Interface

I²C bus consists of two lines – serial clock line (SCL) and serial data line (SDA) – that carry information between multiple devices on the bus. I²C supports multi-master and multi-slave configurations. The data is transmitted from the transmitter to the receiver on the SDA line and is synchronized with the clock SCL generated by the master.

The SCL and SDA lines are open-drain lines and are pulled up to V_{CC} using resistors. The choice of a pull-up resistor on the system depends on the bus capacitance and the intended speed of operation. The master generates the clock, and all the data I/Os are transmitted in synchronization with this clock. The CY14X064I supports up to 3.4 MHz clock speed on SCL line.

Protocol Overview

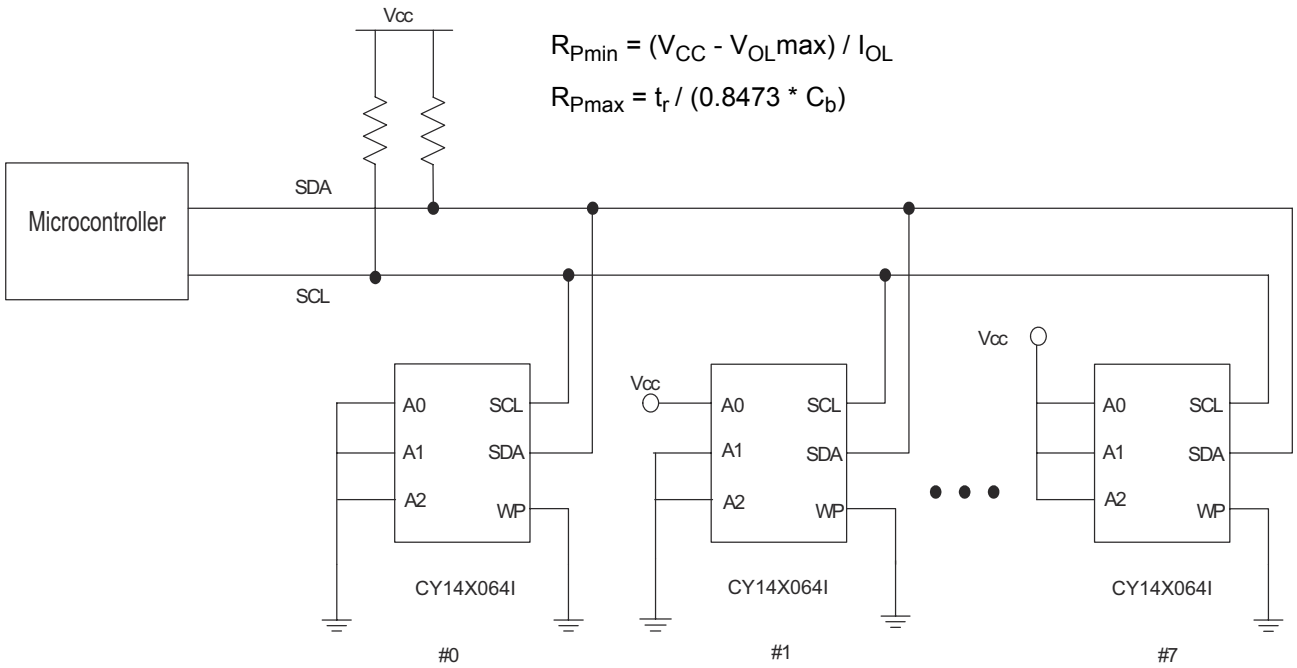
This device supports only a 7-bit addressable scheme. The master generates a START condition to initiate the communication followed by broadcasting a slave select byte. The slave select byte consists of a 7-bit slave address that the master intends to communicate with and R/$\overline{W}$ bit indicating a read or a write operation. The selected slave responds to this with an acknowledgement (ACK). After a slave is selected, the remaining part of the communication takes place between the master and the selected slave device. The other devices on the bus ignore the signals on the SDA line until a STOP or Repeated START condition is detected. The data transfer is done between the master and the selected slave device through the SDA pin synchronized with the SCL clock generated by the master.

I²C Protocol – Data Transfer

Each transaction in I²C protocol starts with the master generating a START condition on the bus, followed by a 7-bit slave address and eighth bit (R/$\overline{W}$) indicating a read (1) or a write (0) operation. All signals are transmitted on the open-drain SDA line and are synchronized with the clock on SCL line. Each byte of data transmitted on the I²C bus is acknowledged by the receiver by holding the SDA line LOW on the ninth clock pulse. The request for write by the master is followed by the memory address and data bytes on the SDA line. The writes can be performed in burst-mode by sending multiple bytes of data. The memory address increments automatically after the receive/transmit of each byte on the falling edge of the ninth clock cycle. The new address is latched just prior to sending/receiving the acknowledgment bit. This allows the next sequential byte to be accessed with no additional addressing. On reaching the last memory location, the address rolls back to 0x0000 and writes continue. The slave responds to each byte sent by the master during a write operation with an ACK. A write sequence can be terminated by the master generating a STOP or Repeated START condition.

A read request is performed at the current address location (address next to the last location accessed for read or write). The memory slave device responds to a read request by transmitting the data on the current address location to the master. A random address read may also be performed by first sending a write request with the intended address of read. The master must abort the write immediately after the last address byte and issue a Repeated START or STOP signal to prevent any write operation. The following read operation starts from this address. The master acknowledges the receipt of one byte of data by holding the SDA pin LOW for the ninth clock pulse. The reads can be terminated by the master sending a no-acknowledge (NACK) signal on the SDA line after the last data byte. The NACK signal causes the CY14X064I to release the SDA line and the master can then generate a STOP or a Repeated START condition to initiate a new operation.

Figure 2. System Configuration using Serial (I²C) nvSRAM



Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The state of the data line can only change when the clock on the SCL line is LOW for the data to be valid. There are only two conditions under which the SDA line may change state with SCL line held HIGH: START and STOP condition. The START and STOP conditions are generated by the master to signal the beginning and end of a communication sequence on the I^2C bus.

START Condition (S)

A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. Every transaction in I^2C begins with the master generating a START condition.

STOP Condition (P)

A LOW to HIGH transition on the SDA line while SCL is HIGH indicates a STOP condition. This condition indicates the end of the ongoing transaction.

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again after the STOP condition.

Repeated START (Sr)

If a Repeated START condition is generated instead of a STOP condition, the bus continues to be busy. The ongoing transaction on the I^2C lines is stopped and the bus waits for the master to send a slave ID for communication to restart.

Figure 3. START and STOP Conditions

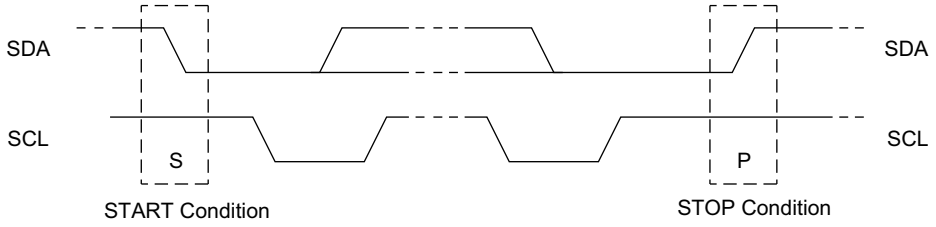
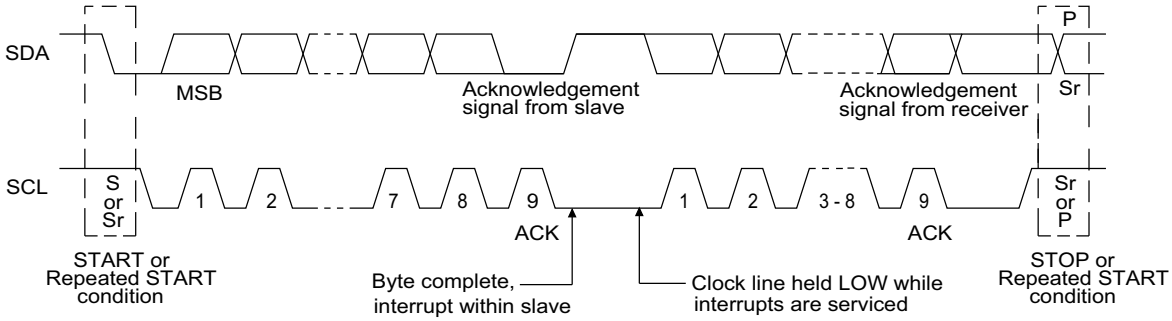


Figure 4. Data Transfer on the I^2C Bus



Byte Format

Each operation in I^2C is done using 8-bit words. The bits are sent in MSB first format on SDA line and each byte is followed by an ACK signal by the receiver.

An operation continues till a NACK is sent by the receiver or STOP or Repeated START condition is generated by the master The SDA line must remain stable when the clock (SCL) is HIGH except for a START or STOP condition.

Acknowledge / No-acknowledge

After transmitting one byte of data or address, the transmitter releases the SDA line. The receiver pulls the SDA line LOW to acknowledge the receipt of the byte. Every byte of data transferred on the I^2C bus needs a response with an ACK signal by the receiver to continue the operation. Failing to do so is considered as a NACK state. NACK is the state where receiver does not acknowledge the receipt of data and the operation is aborted.

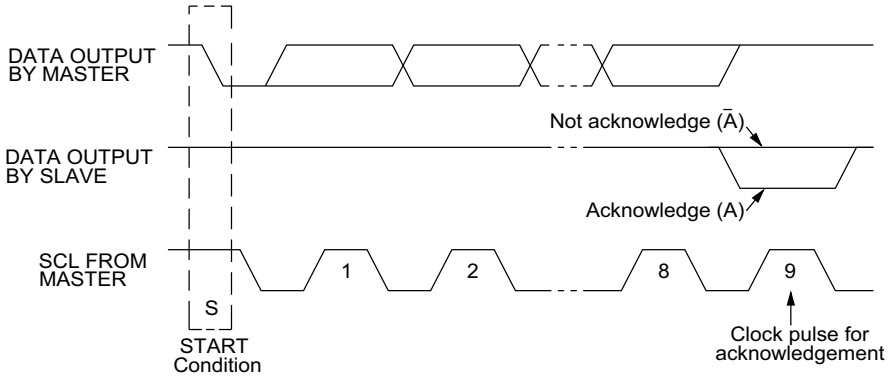
NACK can be generated by master during a READ operation in following cases:

- The master did not receive valid data due to noise.
- The master generates a NACK to abort the READ sequence. After a NACK is issued by the master, nvSRAM slave releases control of the SDA pin and the master is free to generate a Repeated START or STOP condition.

NACK can be generated by nvSRAM slave during a WRITE operation in these cases:

- nvSRAM did not receive valid data due to noise.
- The master tries to access write protected locations on the nvSRAM. Master must restart the communication by generating a STOP or Repeated START condition.

Figure 5. Acknowledge on the I²C Bus



High-Speed Mode (Hs-mode)

In Hs-mode, nvSRAM can transfer data at bit rates of up to 3.4 Mbit/s. A master code (0000 1XXXb) must be issued to place the device into high-speed mode. This enables master/slave communication for speed up to 3.4 MHz. A stop condition will exit Hs-mode.

Serial Data Format in Hs-mode

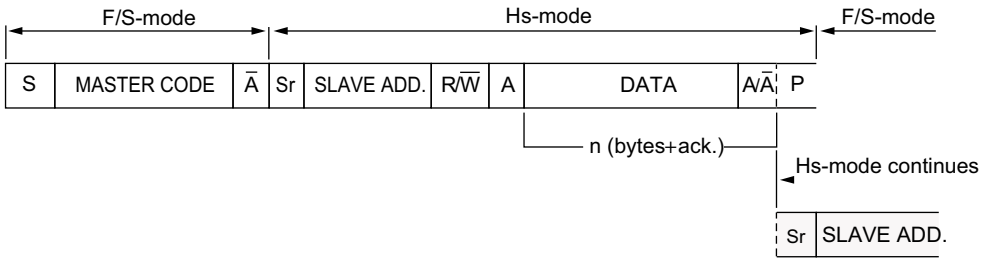
Serial data transfer format in Hs-mode meets the standard-mode I²C-bus specification. Hs-mode can only commence after the following conditions (all of which are in F/S-modes):

1. START condition (S)
2. 8-bit master code (0000 1XXXb)
3. No-acknowledge bit (Ā)

Single and multiple-byte reads and writes are supported. After the device enters into Hs-mode, data transfer continues in Hs-mode until stop condition is sent by master device. The slave switches back to F/S-mode after a STOP condition (P). To continue data transfer in Hs-mode, the master sends Repeated START (Sr).

See Figure 13 on page 11 and Figure 16 on page 12 for Hs-mode timings for read and write operation.

Figure 6. Data Transfer Format in Hs-mode



Slave Device Address

Every slave device on an I^2C bus has a device select address. The first byte after START condition contains the slave device address with which the master intends to communicate. The seven MSBs are the device address and the LSB (R/$\overline{W}$ bit) is used for indicating Read or Write operation. The CY14X064I reserves three sets of upper 4 MSBs [7:4] in the slave device address field for accessing the Memory, RTC Registers, and Control Registers. The accessing mechanism is described in the following section.

The nvSRAM product provides three different functionalities: Memory, RTC Registers and Control Registers functions (such as serial number and product ID). The three functions of the device are accessed through different slave device addresses.

The first four most significant bits [7:4] in the device address register are used to select between the nvSRAM functions.

Table 1. Slave Device Addressing

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	nvSRAM Function Select
1	0	1	0	Device select ID			R/$\overline{W}$	Selects Memory
1	1	0	1	Device select ID			R/$\overline{W}$	Selects RTC Registers
0	0	1	1	Device select ID			R/$\overline{W}$	Selects Control Registers

CY14X064I Slave Devices

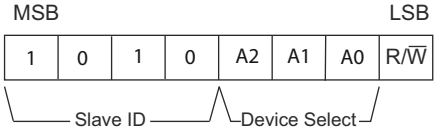
- Memory, 8 K × 8
- RTC Registers, 16 × 8
- Control Registers
  - Memory Control Register, 1 × 8
  - Serial Number, 8 × 8
  - Device ID, 4 × 8
  - Command Register, 1 × 8

Memory Slave Device

The nvSRAM device is selected for read/write if the master issues the slave address as 1010b followed by three bits of device select. If the slave address sent by the master matches with the Memory Slave device address then depending on the R/$\overline{W}$ bit of the slave address, the data will be either read from (R/$\overline{W}$ = '1') or written to (R/$\overline{W}$ = '0') the nvSRAM.

The address length for CY14X064I is 13 bits and thus it requires 2 address bytes to map the entire memory address location. The dedicated two address bytes represent bit A0 to A12. However, since the address is only 13-bits, it implies that the first three MSB bits that is fed in is ignored by the device. Although these bits are 'don't care', Cypress recommends that this bit is treated as 0 to enable seamless transition to higher memory densities.

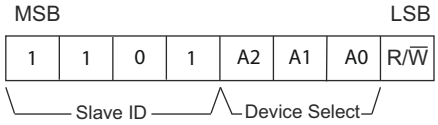
Figure 7. Memory Slave Device Address



RTC Registers Slave Device

The RTC Registers is selected for read/write if the master issues the slave address as 1101b followed by three bits of device select. Then, depending on the R/$\overline{W}$ bit of the slave address, data is either read from (R/$\overline{W}$ = '1') or written to (R/$\overline{W}$ = '0') the RTC Registers. The RTC Registers slave address is followed by one byte address of RTC Register for read/write operation. The RTC Registers map is explained in the Table 10.

Figure 8. RTC Registers Slave Device Address



Control Registers Slave Device

The Control Registers Slave device includes the serial number, product ID, Memory Control, and Command Register.

The nvSRAM Control Register Slave device is selected for read/write if the master issues the slave address as 0011b followed by three bits of device select. Then, depending on the R/$\overline{W}$ bit of the slave address, data is either read from (R/$\overline{W}$ = '1') or written to (R/$\overline{W}$ = '0') the device.

Figure 9. Control Registers Slave Device Address

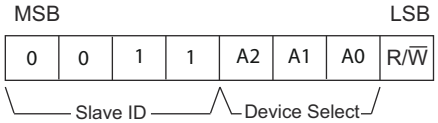


Table 2. Control Registers Map

Address	Description	Read/Write	Details
0x00	Memory Control Register	Read/Write	Contains Block Protect bits and Serial Number lock bit
0x01	Serial Number 8 bytes	Read/Write (Read only when SNL is set)	Programmable Serial Number. Locked by setting the Serial Number lock bit in the Memory Control Register to '1'.
0x02			
0x03			
0x04			
0x05			
0x06			
0x07			
0x08			
0x09	Device ID	Read only	Device ID is factory programmed
0x0A			
0x0B			
0x0C			
0x0D	Reserved	Reserved	Reserved
0xAA	Command Register	Write only	Allows commands for STORE, RECALL, AutoStore Enable/Disable, SLEEP Mode

Memory Control Register

The Memory Control Register contains the following bits:

Table 3. Memory Control Register Bits

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SNL (0)	0	0	BP1 (0)	BP0 (0)	0	0

- **BP1:BP0**: Block protect bits are used to protect 1/4, 1/2 or full memory array. These bits can be written through a write instruction to the 0x00 location of the Control Register Slave device. However, any STORE cycle transfers SRAM data into a nonvolatile cell regardless of whether or not the block is protected. The default value shipped from the factory for BP0 and BP1 is '0'.

Table 4. Block Protection

Level	BP1:BP0	Block Protection
0	00	None
1/4	01	0x1800–0x1FFF
1/2	10	0x1000–0x1FFF
1	11	0x0000–0x1FFF

- **S/N Lock (SNL) Bit**: Serial Number Lock bit (SNL) is used to lock the serial number. After the bit is set to '1', the serial number registers are locked and no modification is allowed. This bit cannot be cleared to '0'. The serial number is secured on the next STORE operation (Software STORE or AutoStore). If AutoStore is not enabled, user must perform the Software STORE operation to secure the lock bit status. If a STORE was not performed, the serial number lock bit will not survive the power cycle. The default value shipped from the factory for SNL is '0'.

Command Register

The Command Register resides at address 'AA' of the Control Registers Slave device. This is a write only register. The byte written to this register initiates a STORE, RECALL, AutoStore Enable, AutoStore Disable, and Sleep mode operation as listed in Table 5. The section Executing Commands Using Command Register on page 19 explains how you can execute Command Register bytes.

Table 5. Command Register Bytes

Data Byte [7:0]	Command	Description
0011 1100	STORE	STORE SRAM data to nonvolatile memory
0110 0000	RECALL	RECALL data from nonvolatile memory to SRAM
0101 1001	ASENB	Enable AutoStore
0001 1001	ASDISB	Disable AutoStore
1011 1001	SLEEP	Enter Sleep Mode for low power consumption

- **STORE**: Initiates nvSRAM Software STORE. The nvSRAM cannot be accessed for t_{STORE} time after this instruction has been executed. When initiated, the device performs a STORE operation regardless of whether or not a write has been performed since the last NV operation. After the t_{STORE} cycle time is completed, the SRAM is activated again for read/write operations.
- **RECALL**: Initiates nvSRAM Software RECALL. The nvSRAM cannot be accessed for t_{RECALL} time after this instruction has been executed. The RECALL operation does not alter the data in the nonvolatile elements. A RECALL may be initiated in two ways: Hardware RECALL, initiated on power-up; and Software RECALL, initiated by a I^2C RECALL instruction.
- **ASENB**: Enables nvSRAM AutoStore. The nvSRAM cannot be accessed for t_{SS} time after this instruction has been executed. This setting is not nonvolatile and needs to be followed by a manual STORE sequence if this is desired to survive the power cycle. The part comes from the factory with AutoStore Enabled and 0x00 written in all cells.
- **ASDISB**: Disables nvSRAM AutoStore. The nvSRAM cannot be accessed for t_{SS} time after this instruction has been executed. This setting is not nonvolatile and needs to be followed by a manual STORE sequence if this is desired to survive the power cycle.

Note If AutoStore is disabled and V_{CAP} is not required, it is required that the V_{CAP} pin is left open. V_{CAP} pin must never be

connected to ground. Power Up RECALL operation cannot be disabled in any case.

- **SLEEP**: SLEEP instruction puts the nvSRAM in a sleep mode. When the SLEEP instruction is registered, the nvSRAM takes t_{SS} time to process the SLEEP request. Once the SLEEP command is successfully registered and processed, the nvSRAM toggles HSB LOW, performs a STORE operation to secure the data to nonvolatile memory and then enters into SLEEP mode. Whenever nvSRAM enters into sleep mode, it initiates non volatile STORE cycle which results in losing an endurance cycle per sleep command execution. A STORE cycle starts only if a write to the SRAM has been performed since the last STORE or RECALL cycle.

The nvSRAM enters into sleep mode in this manner:

1. The master sends a START command.
2. The master sends Control Registers Slave device ID with I^2C write bit set (R/W = '0').
3. The slave (nvSRAM) sends an ACK back to the master.
4. The master sends Command Register address (0xAA).
5. The slave (nvSRAM) sends an ACK back to the master.
6. The master sends Command Register byte for entering into sleep mode.
7. The slave (nvSRAM) sends an ACK back to the master.
8. The master generates a STOP condition.

Once in sleep mode, the device starts consuming I_{ZZ} current t_{SLEEP} time after SLEEP instruction is registered. The device is not accessible for normal operations until it is out of sleep mode. The nvSRAM wakes up after t_{WAKE} duration after the device slave address is transmitted by the master.

Transmitting any of the three slave addresses wakes the nvSRAM from sleep mode. The nvSRAM device is not accessible during t_{SLEEP} and t_{WAKE} interval and any attempt to access the nvSRAM device by the master is ignored and nvSRAM sends NACK to the master. An alternate method of determining when the device is ready is for the master can send read or write commands and look for an ACK.

Write Protection (WP)

The Write Protect (WP) pin is an active HIGH pin and protects the entire memory and all registers from write operations. To inhibit all the write operations, this pin must be held HIGH. When this pin is HIGH, all memory and register writes are prohibited and the address counter is not incremented. This pin is internally pulled LOW and, therefore, can be left open if not used.

AutoStore Operation

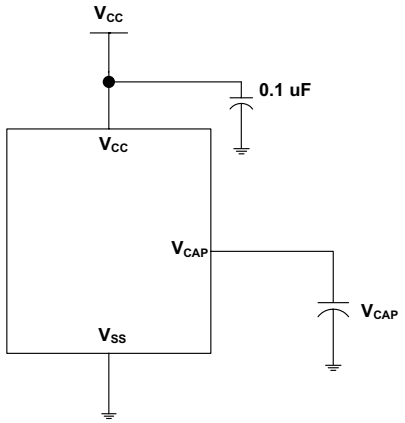
The AutoStore operation is a unique feature of nvSRAM that automatically stores the SRAM data to QuantumTrap cells during power-down. This STORE makes use of an external capacitor (V_{CAP}) and enables the device to safely STORE the data in the nonvolatile memory when power goes down.

During normal operation, the device draws current from V_{CC} to charge the capacitor connected to the V_{CAP} pin. When the voltage on the V_{CC} pin drops below V_{SWITCH} during power-down, the device inhibits all memory accesses to nvSRAM and automatically performs a conditional STORE operation using the charge from the V_{CAP} capacitor. The AutoStore operation is not initiated if no write cycle has been performed since the last STORE or RECALL.

Note If a capacitor is not connected to V_{CAP} pin, AutoStore must be disabled by issuing the AutoStore Disable instruction specified in Command Register on page 8. If AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the Store. This will corrupt the data stored in nvSRAM as well as the serial number and it will unlock the SNL bit.

Figure 10 shows the proper connection of the storage capacitor (V_{CAP}) for AutoStore operation. See the DC Electrical Characteristics on page 29 for the size of the V_{CAP}.

Figure 10. AutoStore Mode



Hardware STORE and $\overline{HSB}$ pin Operation

The $\overline{HSB}$ pin in CY14X064I is used to control and acknowledge STORE operations. If no STORE or RECALL is in progress, this pin can be used to request a Hardware STORE cycle. When the $\overline{HSB}$ pin is driven LOW, the device conditionally initiates a STORE operation after t_{DELAY} duration. An actual STORE cycle starts only if a write to the SRAM has been performed since the last STORE or RECALL cycle. Reads and Writes to the memory are inhibited for t_{STORE} duration or as long as HSB pin is LOW.

The $\overline{HSB}$ pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

Note For successful last data byte STORE, a hardware STORE should be initiated at least one clock cycle after the last data bit D0 is received.

Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ pin unconnected if not used.

Hardware RECALL (Power Up)

During power-up, when V_{CC} crosses V_{SWITCH}, an automatic RECALL sequence is initiated that transfers the content of nonvolatile memory to the SRAM. The data may have been

previously stored on the nonvolatile memory through a STORE sequence.

A Power Up RECALL cycle takes t_{FA} time to complete and the memory access is disabled during this time. HSB pin can be used to detect the ready status of the device.

Write Operation

The last bit of the slave device address indicates a read or a write operation. In case of a write operation, the slave device address is followed by the memory or register address and data. A write operation continues as long as a STOP or Repeated START condition is generated by the master or if a NACK is issued by the nvSRAM.

A NACK is issued from the nvSRAM under the following conditions:

1. A valid Device ID is not received.
2. A write (burst write) access to a protected memory block address returns a NACK from nvSRAM after the data byte is received. However, the address counter is set to this address and the following current read operation starts from this address.
3. A write/random read access to an invalid or out-of-bound memory address returns a NACK from the nvSRAM after the address is received. The address counter remains unchanged in such a case.

After a NACK is sent out from the nvSRAM, the write operation is terminated and any data on the SDA line is ignored till a STOP or a Repeated START condition is generated by the master.

For example, consider a case where the burst write access is performed on Control Register Slave address 0x01 for writing the serial number and continued to the address 0x09, which is a read-only register. The device returns a NACK and address counter is not incremented. A following read operation is started from the address 0x09. Further, any write operation which starts from a write protected address (say, 0x09) is responded by the nvSRAM with a NACK after the data byte is sent and set the address counter to this address. A following read operation starts from the address 0x09 in this case also.

Note In case user tries to read/write access an address that does not exist (for example 0x0D in Control Register Slave or 0x3F in RTC registers), nvSRAM responds with a NACK immediately after the out-of-bound address is transmitted. The address counter remains unchanged and holds the previous successful read or write operation address.

A write operation is performed internally with no delay after the eighth bit of data is transmitted. If a write operation is not intended, the master must terminate the write operation before the eighth clock cycle by generating a STOP or Repeated START condition.

More details on write instructions are provided in the section Memory Slave Access on page 10.

Read Operation

If the last bit of the slave device address is ‘1’, a read operation is assumed and the nvSRAM takes control of the SDA line immediately after the slave device address byte is sent out by the master. The read operation starts from the current address location (the location following the previous successful write or read operation). When the last address is reached, the address counter loops back to the first address.

In case of the Control Register Slave, whenever a burst read is performed such that it flows to a non-existent address, the reads operation loops back to 0x00. This is applicable, in particular, for the Command Register.

Read operation can be ended using the following methods:

1. The master issues a NACK on the ninth clock cycle followed by a STOP or a Repeated START condition on the tenth clock cycle.
2. The master generates a STOP or Repeated START condition on the ninth clock cycle.

More details on write instruction are provided in the section Memory Slave Access on page 10.

Memory Slave Access

The following sections describe the data transfer sequence required to perform read or write operations from nvSRAM.

Write nvSRAM

Each write operation consists of a slave address being transmitted after the start condition. The last bit of slave address must be set as ‘0’ to indicate a Write operation. The master may write one byte of data or continue writing multiple consecutive address locations while the internal address counter keeps incrementing automatically. The address register is reset to 0x0000 after the last address in memory is accessed. The write operation continues till a STOP or Repeated START condition is generated by the master or a NACK is issued by the nvSRAM.

A write operation is executed only after nvSRAM receives all the eight data bits. The nvSRAM sends an ACK signal after a successful write operation. A write operation may be terminated by the master by generating a STOP condition or a Repeated START operation. If the master desires to abort the current write operation without altering the memory contents, this should be done using a START/STOP condition prior to the eighth data bit.

If the master tries to access a write protected memory address on the nvSRAM, a NACK is returned after the data byte intended to write the protected address is transmitted and address counter will not be incremented. Similarly, in a burst mode write operation, a NACK is returned when the data byte that attempts to write a protected memory location and the address counter is not incremented.

Figure 11. Single-Byte Write into nvSRAM (except Hs-mode)

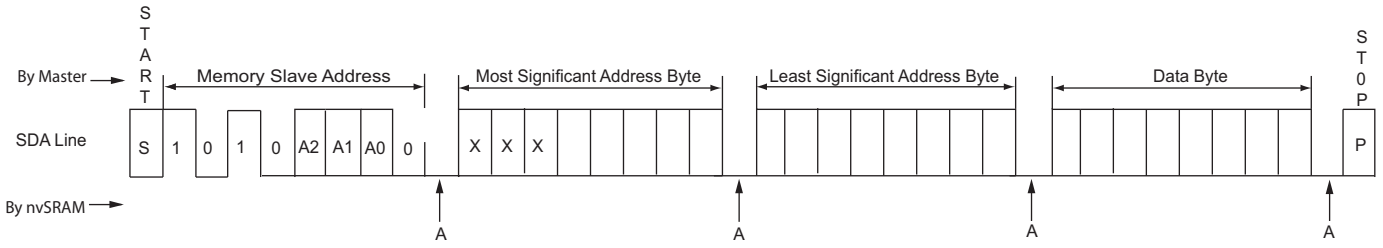


Figure 12. Multi-Byte Write into nvSRAM (except Hs-mode)

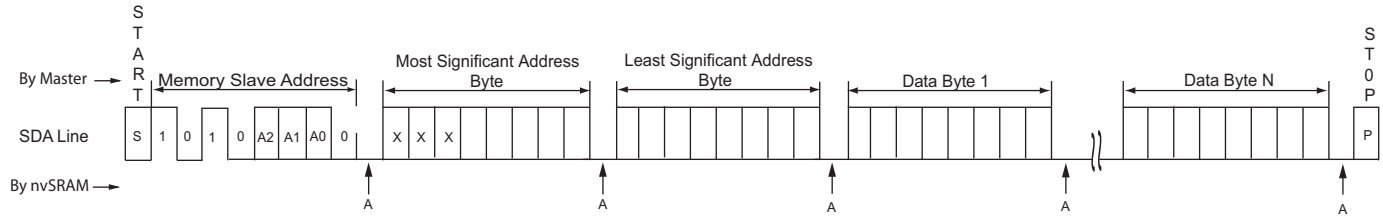


Figure 13. Single-Byte Write into nvSRAM (Hs-mode)

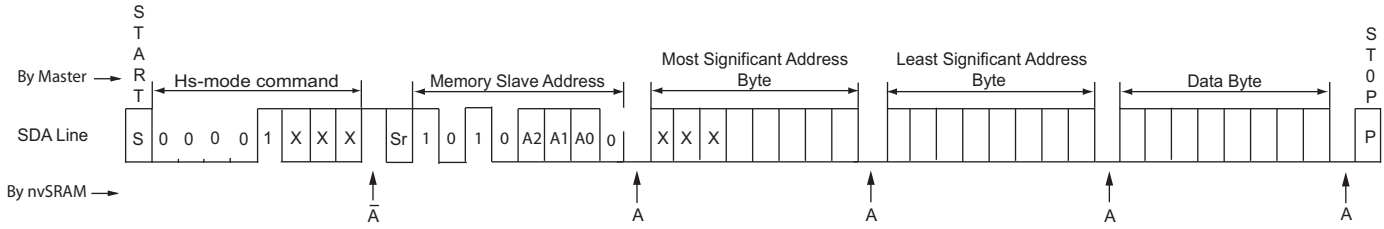
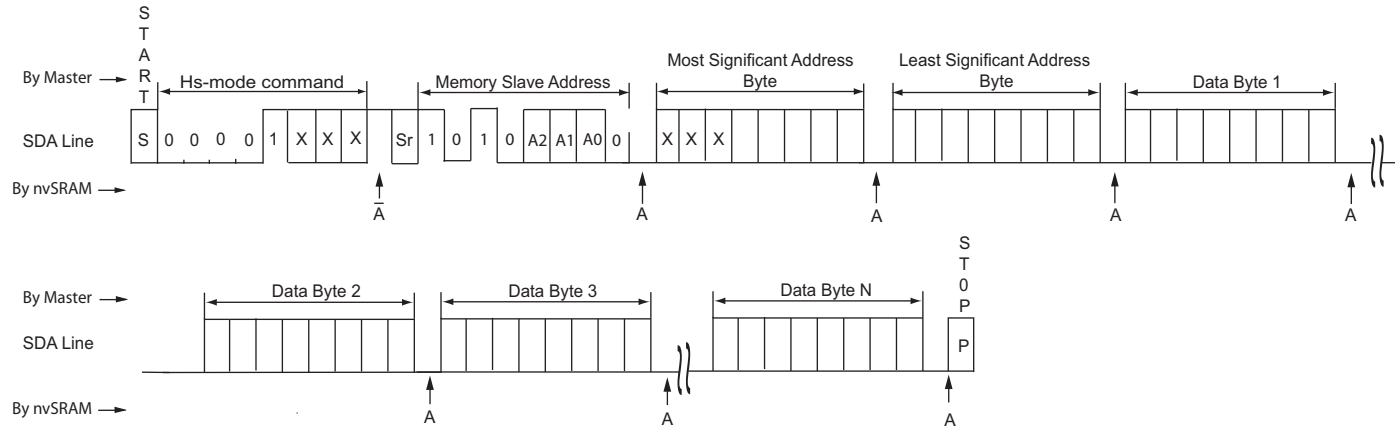


Figure 14. Multi-Byte Write into nvSRAM (Hs-mode)



Current nvSRAM Read

Each read operation starts with the master transmitting the nvSRAM slave address with the LSB set to '1' to indicate 'Read'. The reads start from the address on the address counter. The address counter is set to the address location next to the last accessed with a 'Write' or 'Read' operation. The master may terminate a read operation after reading 1 byte or continue reading addresses sequentially till the last address in the memory after which the address counter rolls back to the address 0x0000. The valid methods of terminating read access are described in the section Read Operation on page 10.

Figure 15. Current Location Single-Byte nvSRAM Read (except Hs-mode)

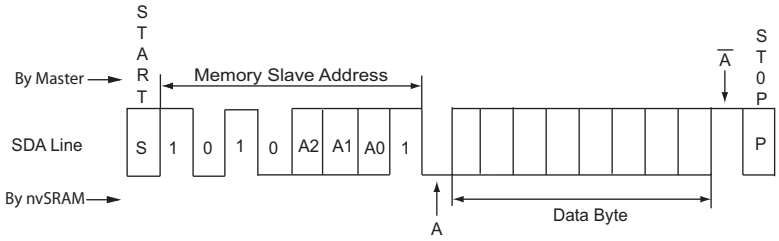


Figure 16. Current Location Multi-Byte nvSRAM Read (except Hs-mode)

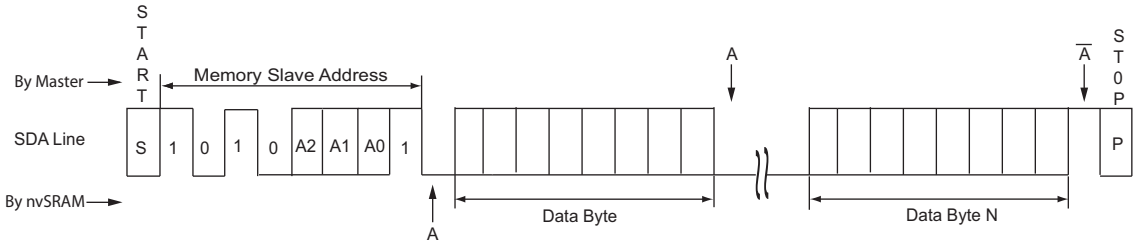


Figure 17. Current Location Single-Byte nvSRAM Read (Hs-mode)

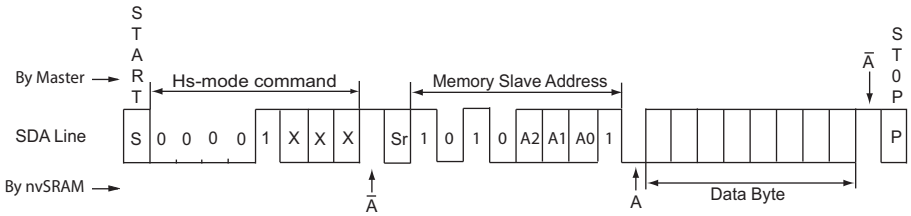
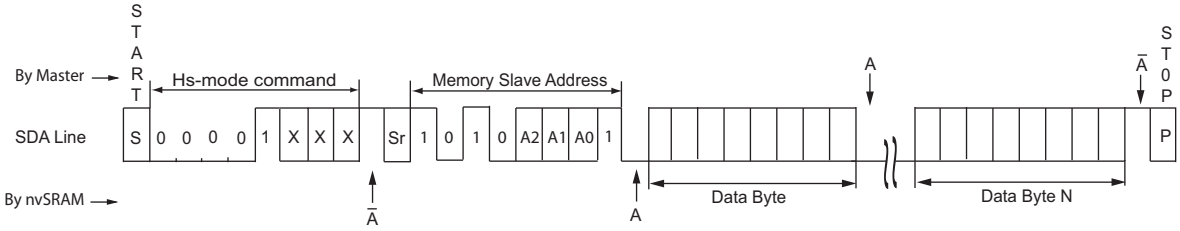


Figure 18. Current Location Multi-Byte nvSRAM Read (Hs-mode)



Random Address Read

A random address read is performed by first initiating a write operation and generating a Repeated START immediately after the last address byte is acknowledged. The address counter is set to this address and the next read access to this slave initiates read operation from here. The master may terminate a read operation after reading 1 byte or continue reading addresses sequentially till the last address in the memory after which the address counter rolls back to the start address 0x0000.

Figure 19. Random Address Single-Byte Read (except Hs-mode)

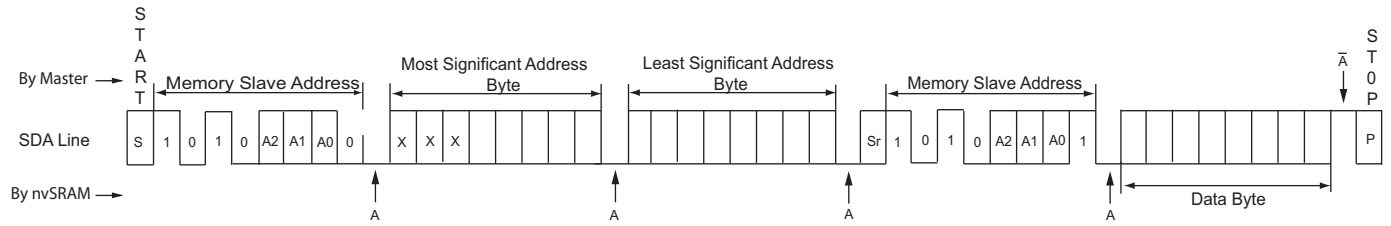


Figure 20. Random Address Multi-Byte Read (except Hs-mode)

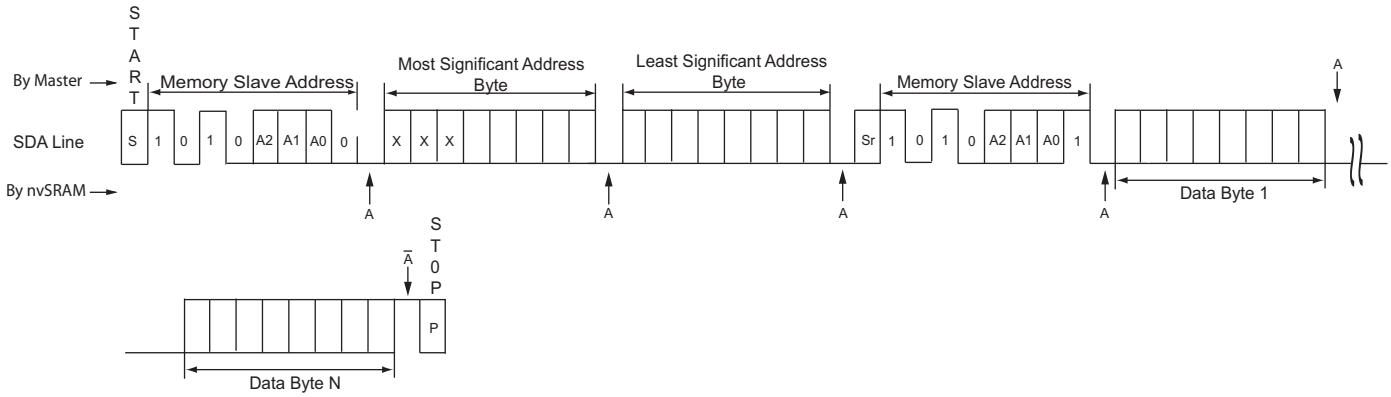


Figure 21. Random Address Single-Byte Read (Hs-mode)

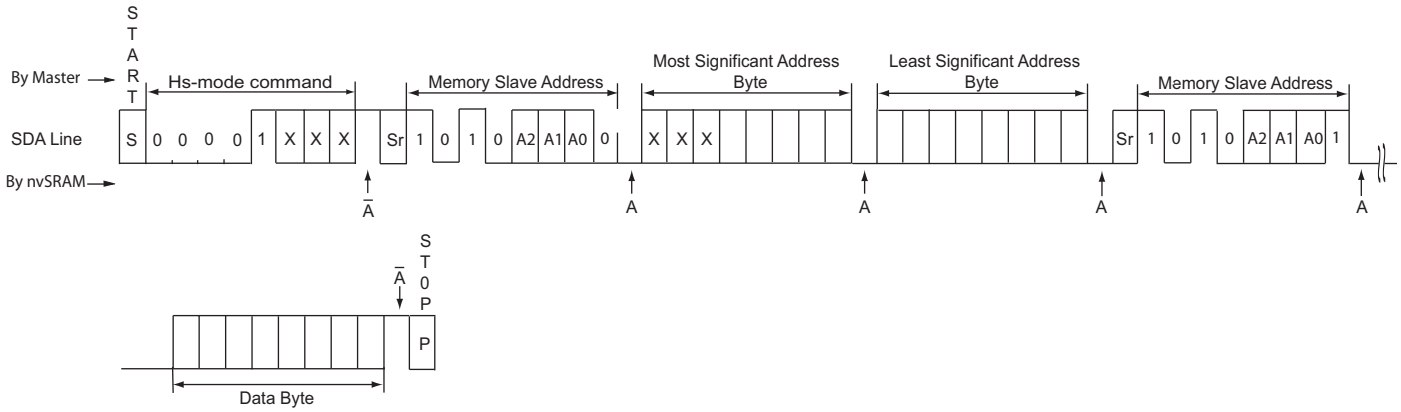
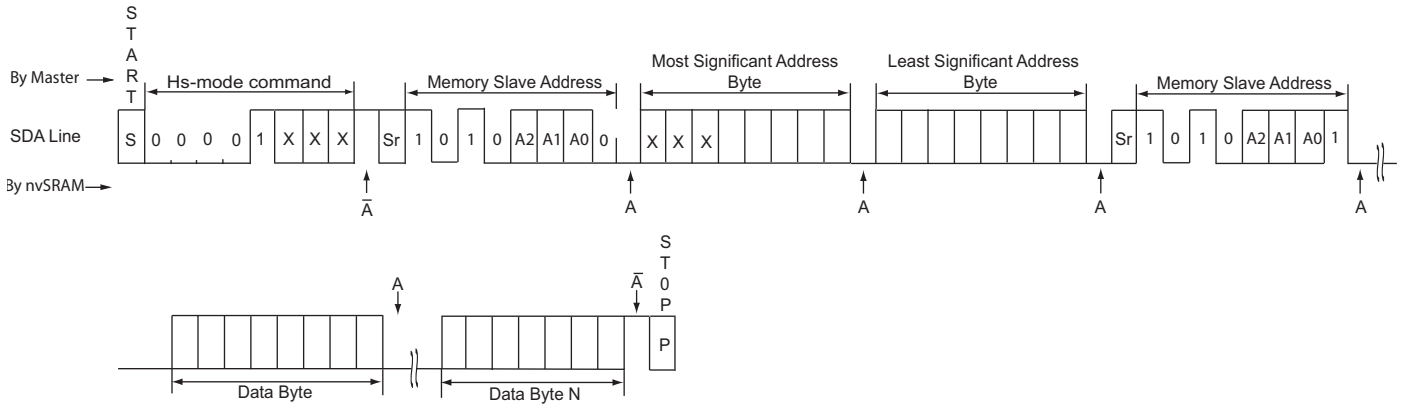


Figure 22. Random Address Multi-Byte Read (Hs-mode)



RTC Registers Slave Access

The following sections describe the data transfer sequence required to perform read or write operations from RTC registers.

Write RTC Registers

A write to RTC registers is initiated with the RTC Registers Slave address followed by one byte of address and data. The master may write one byte of data or continue writing multiple consecutive address locations while the internal address counter keeps incrementing automatically. The address register is reset to 0x00 after the last RTC register is accessed. The write operation continues till a STOP or Repeated START condition is generated by the master or a NACK is issued by the nvSRAM RTC Registers Slave.

A write operation is executed only after all the eight data bits have been received by the nvSRAM. The nvSRAM sends an ACK signal after the successful operation of the write instruction A write operation may be terminated by the master by generating a STOP condition or a Repeated START operation before the last data bit is sent.

If the master tries to access an out of bound memory address on the RTC Registers Slave, a NACK is returned after the address byte is transmitted. The address counter remains unaffected and the following current read operation starts from the address value held in the address counter.

Figure 23. Single-Byte Write into RTC Registers

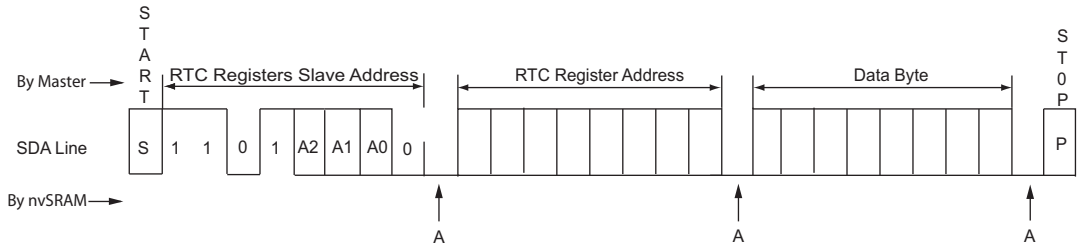
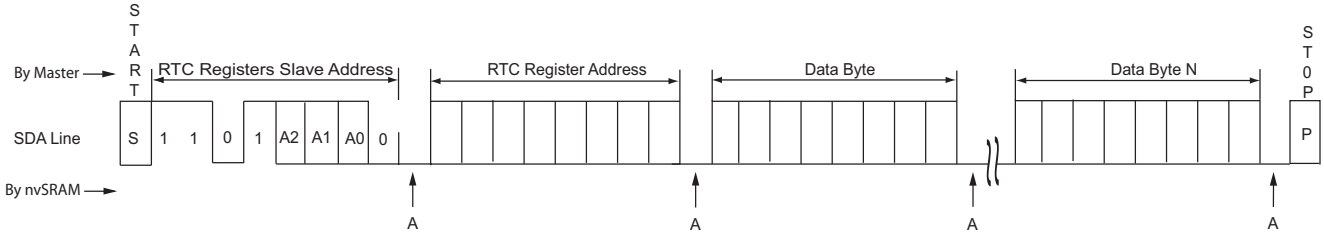


Figure 24. Multi-Byte Write into RTC Registers



Current Address RTC Registers Read

A current read of RTC registers starts with the master sending the RTC Registers Slave address after the START condition. All read operations begin from the current address (the address next to previously accessed address location). After the last address is read sequentially, the address latch loops back to the first location (0x00) and read operation continues. The master may terminate a read operation after reading one byte or continue reading addresses sequentially till the last address in the memory after which the address counter rolls back to the address 0x00. A read operation may be terminated by the master by generating a STOP condition or a Repeated START operation or a NACK.

Figure 25. Current Address RTC Registers Single-Byte Read

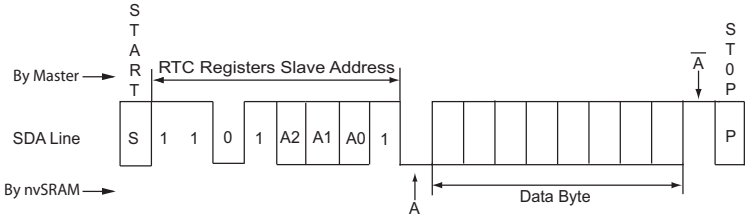
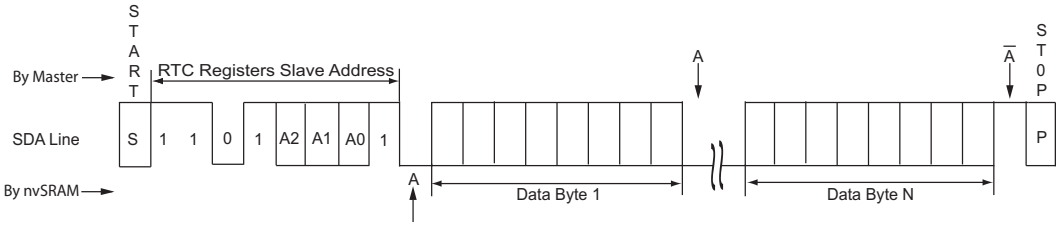


Figure 26. Current Address RTC Registers Multi-Byte Read



Random Address RTC Registers Read

A random address read is performed by first initiating a write operation and generating a Repeated START immediately after the last address byte is acknowledged. The address counter is set to this address and the next read access to this slave initiates the read operation from here. The master may terminate a read operation after reading one byte or continue reading addresses sequentially till the last address in the memory after which the address counter rolls back to the start address location of RTC (0x00).

A random address read attempt on an out of bound memory address on the RTC Registers Slave is responded back with a NACK from the nvSRAM after the address byte is transmitted. The address counter remains unaffected and the following current read operation starts from the address value held in the address counter.

Figure 27. Random Address RTC Registers Single-Byte Read

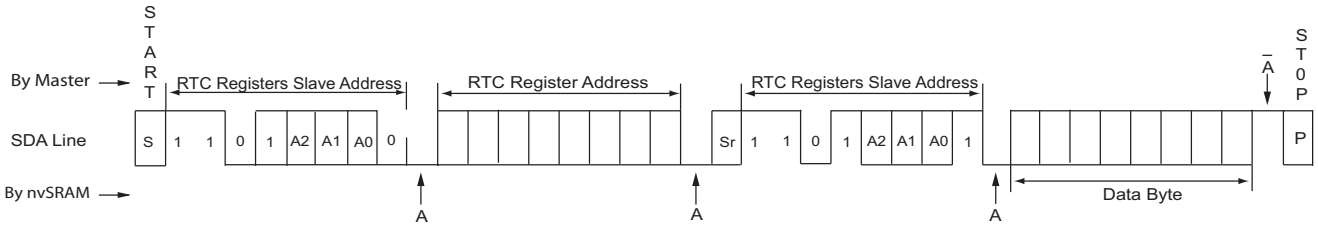
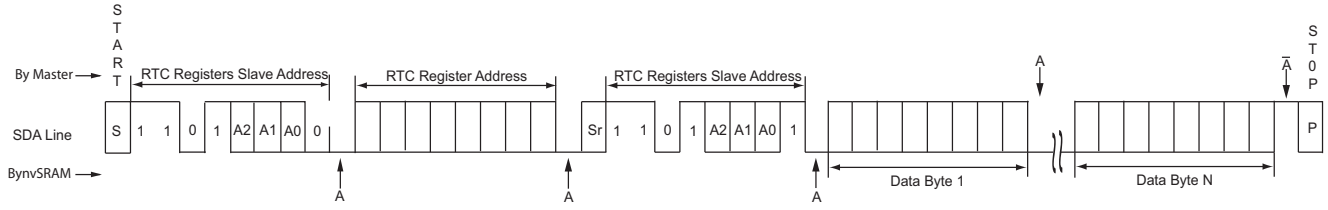


Figure 28. Random Address RTC Registers Multi-Byte Read



Control Registers Slave

The following sections describe the data transfer sequence required to perform read or write operations from Control Registers Slave.

Write Control Registers

To write the Control Registers Slave, the master transmits the Control Registers Slave address after generating the START condition. The write sequence continues from the address location specified by the master till the master generates a STOP condition or the last writable address location.

If a non-writable address location is accessed for write operation during a normal write or a burst, the slave generates a NACK after the data byte is sent and the write sequence terminates. Any following data bytes are ignored and the address counter is not incremented.

If a write operation is performed on the Command Register (0xAA), the following current read operation also begins from the first address (0x00) as in this case, the current address is an out-of-bound address. The address is not incremented and the next current read operation begins from this address location. If a write operation is attempted on an out-of-bound address location, the nvSRAM sends a NACK immediately after the address byte is sent.

Further, if the serial number is locked, only two addresses (0xAA or Command Register, and 0x00 or Memory Control Register) are writable in the Control Registers Slave. On a write operation to any other address location, the device will acknowledge command byte and address bytes but it returns a NACK from the control Registers Slave for data bytes. In this case, the address will not be incremented and a current read will happen from the last acknowledged address.

The nvSRAM Control Registers Slave sends a NACK when an out of bound memory address is accessed for write operation, by the master. In such a case, a following current read operation begins from the last acknowledged address.

Figure 29. Single-Byte Write into Control Registers

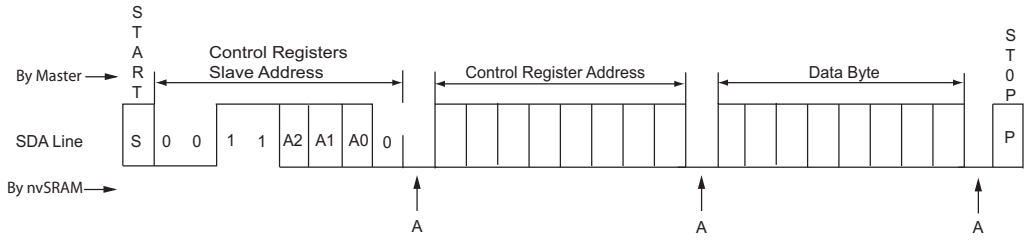
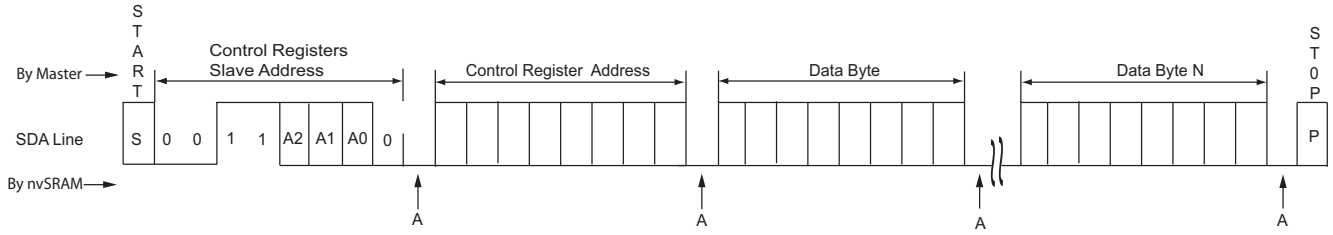


Figure 30. Multi-Byte Write into Control Registers



Current Control Registers Read

A read of Control Registers Slave is started with master sending the Control Registers Slave address after the START condition with the LSB set to '1'. The reads begin from the current address which is the next address to the last accessed location. The reads to Control Registers Slave continues until the last readable address location and loops back to the first location (0x00). Note that the Command Register is a write only register and is not accessible through the sequential read operations. If a burst read operation begins from the Command Register (0xAA), the address counter wraps around to the first address in the register map (0x00).

Figure 31. Control Registers Single-Byte Read

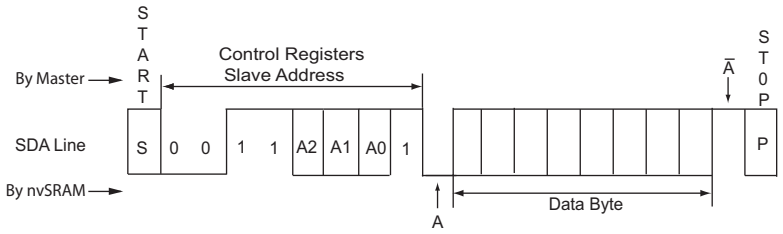
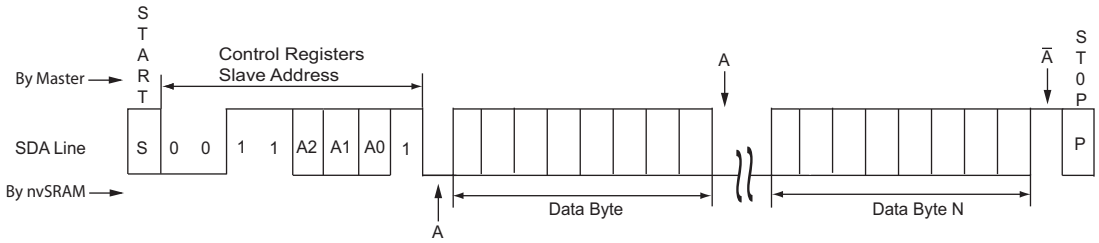


Figure 32. Current Control Registers Multi-Byte Read



Random Control Registers Read

A read of random address may be performed by initiating a write operation to the intended location of read and immediately following with a Repeated START operation. The reads to Control Registers Slave continues till the last readable address location and loops back to the first location (0x00). Note that the Command Register is a write only register and is not accessible through the sequential read operations. A random read starting at the Command Register (0xAA) loops back to the first address in the Control Register register map (0x00). If a random read operation is initiated from an out-of-bound memory address, the nvSRAM sends a NACK after the address byte is sent.

Figure 33. Random Control Registers Single-Byte Read

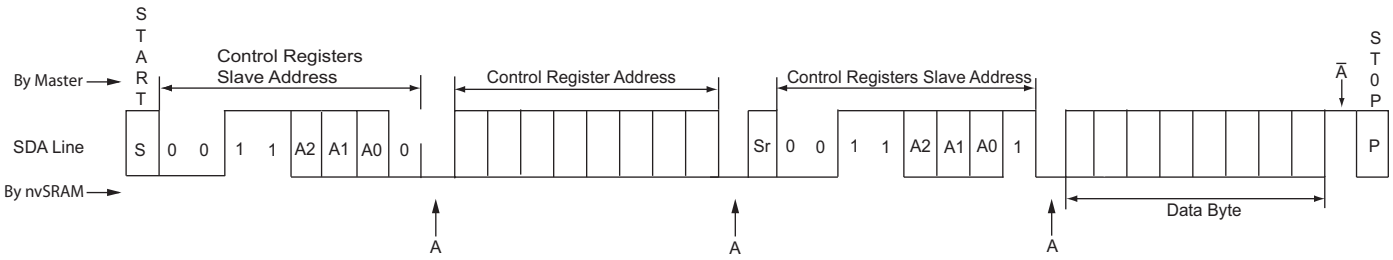
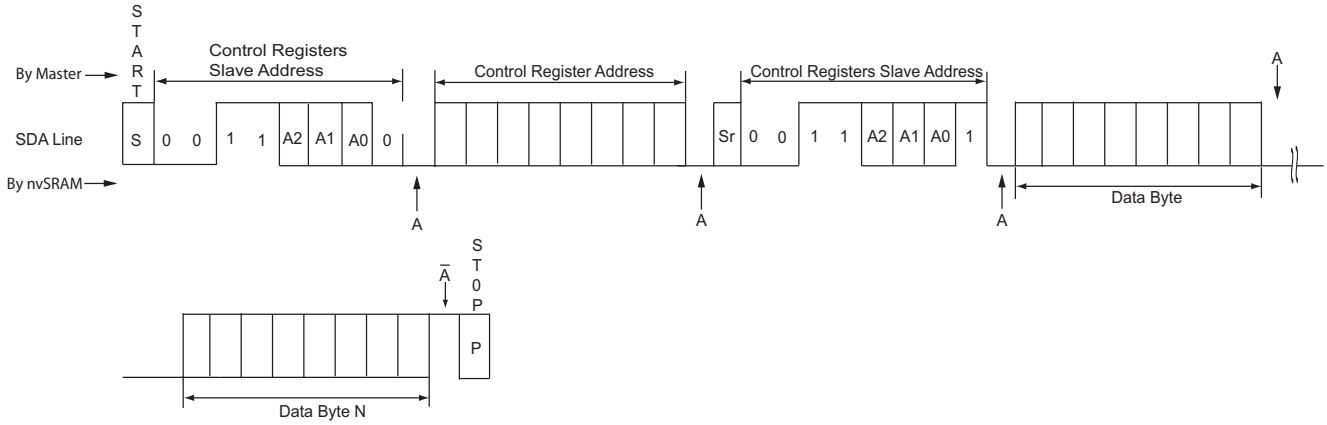


Figure 34. Random Control Registers Multi-Byte Read



Serial Number

Serial number is an 8 byte memory space provided to the user to uniquely identify this device. It typically consists of a two byte customer ID, followed by five bytes of unique serial number and one byte of CRC check. However, nvSRAM does not calculate the CRC and it is up to the user to utilize the eight byte memory space in the desired format. The default values for the eight byte locations are set to '0x00'.

Serial Number Write

The serial number can be accessed through the Control Registers Slave Device. To write the serial number, master transmits the Control Registers Slave address after the START condition and writes to the address location from 0x01 to 0x08. The content of Serial Number registers is secured to nonvolatile memory on the next STORE operation. If AutoStore is enabled, nvSRAM automatically stores the serial number in the nonvolatile memory on power-down. However, if AutoStore is disabled, user must perform a STORE operation to secure the contents of Serial Number registers.

Note If the serial number lock (SNL) bit is not set, the serial number registers can be re-written regardless of whether or not a STORE has happened. After the serial number lock bit is set, no writes to the serial number registers are allowed. If the master tries to perform a write operation to the serial number registers when the lock bit is set, a NACK is returned and write is not performed.

Serial Number Lock

After writes to serial number registers is complete, the master is responsible for locking the serial number by setting the serial number lock bit to '1' in the Memory Control Register (0x00). The content of Memory Control Register and serial number are secured on the next STORE operation (STORE or AutoStore). If AutoStore is not enabled, user must perform the STORE operation to secure the lock bit status.

If a STORE was not performed, the serial number lock bit will not survive the power cycle. The serial number lock bit and 8-byte serial number is defaults to '0' at power-up.

Serial Number Read

Serial number can be read back by a read operation of the intended address of the Control Registers Slave. The Control Registers Device loops back from the last address (excluding the Command Register) to 0x00 address location while performing burst read operation. The serial number resides in the locations from 0x01 to 0x08. Even if the serial number is not locked, a serial number read operation returns the current values written to the serial number registers. The master may perform a serial number read operation to confirm if the correct serial number is written to the registers before setting the lock bit.

Device ID

Device ID is a 4-byte code consisting of JEDEC assigned manufacturer ID, product ID, density ID, and die revision. These registers are set in the factory and are read only registers for the user.

Table 6. Device ID

Device	Device ID (4 bytes)	Device ID Description			
		31–21 (11 bits)	20–7 (14 bits)	6–3 (4 bits)	2–0 (3 bits)
		Manufacturer ID	Product ID	Density ID	Die Rev
CY14C064I	0x0681E088	00000110100	00001111000001	0001	000
CY14B064I	0x0681E888	00000110100	00001111010001	0001	000
CY14E064I	0x0681F288	00000110100	00001111100101	0001	000

The device ID is divided into four parts as shown in Table 6:

1. Manufacturer ID (11 bits)

This is the JEDEC assigned manufacturer ID for Cypress. JEDEC assigns the manufacturer ID in different banks. The first three bits of the manufacturer ID represent the bank in which ID is assigned. The next eight bits represent the manufacturer ID.

Cypress manufacturer ID is 0x34 in bank 0. Therefore the manufacturer ID for all Cypress nvSRAM products is as given below:

Cypress ID - 000_0011_0100

2. Product ID (14 bits)

The product ID for device is shown in the Table 6.

3. Density ID (4 bits)

The 4-bit density ID is used as shown in Table 6 for indicating the 64Kb density of the product.

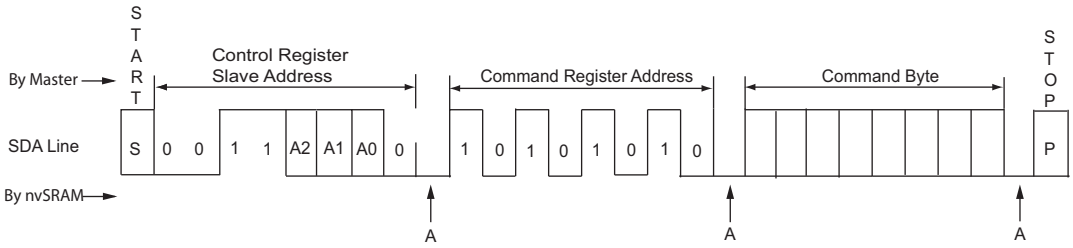
4. Die Rev (3 bits)

This is used to represent any major change in the design of the product. The initial setting of this is always 0x0.

Executing Commands Using Command Register

The Control Registers Slave allows different commands to be executed by writing the specific command byte in the Command Register (0xAA). The command byte codes for each command are specified in Table 5 on page 8. During the execution of these commands the device is not accessible and returns a NACK if any of the three slave devices is selected. If an invalid command is sent by the master, the nvSRAM responds with an ACK indicating that the command has been acknowledged with NOP (No Operation). The address will rollover to 0x00 location.

Figure 35. Command Execution using Command Register



Real Time Clock Operation

nvTIME Operation

The CY14X064I offers internal registers that contain clock, alarm, watchdog, interrupt, and control functions. The RTC registers occupy a separate address space from nvSRAM and are accessible through the Read RTC register and Write RTC register sequence on register addresses 0x00 to 0x0F. Internal double buffering of the clock and the timer information registers prevents accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or the clock accuracy of the internal clock when accessing clock data. Clock and alarm registers store data in BCD format.

Clock Operations

The clock registers maintain time up to 9,999 years in one-second increments. The time can be set to any calendar time and the clock automatically keeps track of days of the week and month, leap years, and century transitions. There are eight registers dedicated to the clock functions, which are used to set time with a write cycle and to read time with a read cycle. These registers contain the time of day in BCD format. Bits defined as '0' are currently not used and are reserved for future use by Cypress.

Reading the Clock

The double buffered RTC register structure reduces the chance of reading incorrect data from the clock. Internal updates to the CY14X064I time keeping registers are stopped when the read bit 'R' (in the flags register at 0x00) is set to '1' before reading clock data to prevent reading of data in transition. Stopping the register updates does not affect clock accuracy.

When a read sequence of RTC device is initiated, the update of the user timekeeping registers stops and does not restart until a STOP or a Repeated START condition is generated. The RTC registers are read while the internal clock continues to run. After the end of read sequence, all the RTC registers are simultaneously updated within 20 ms.

Setting the Clock

A write access to the RTC device stops updates to the time keeping registers and enables the time to be set when the write bit 'W' (in the flags register at 0x00) is set to '1'. The correct day, date, and time is then written into the registers and must be in 24 hour BCD format. The time written is referred to as the "Base Time". This value is stored in nonvolatile registers and used in the calculation of the current time. When the write bit 'W' is cleared by writing '0' to it and a STOP or Repeated START condition is encountered, the values of timekeeping registers are transferred to the actual clock counters after which the clock resumes normal operation. If a valid STOP or Repeated START condition is not generated by the master, the time written to the RTC registers is never transferred to the actual clock counters.

If the time written to the timekeeping registers is not in the correct BCD format, each invalid nibble of the RTC registers continue counting to 0xF before rolling over to 0x0 after which RTC resumes normal operation.

Note After 'W' bit is set to '0', values written into the timekeeping, alarm, calibration, and interrupt registers are transferred to the RTC time keeping counters in t_{RTCp} time. These counter values must be saved to nonvolatile memory either by initiating a Software/Hardware STORE or AutoStore operation. While working in AutoStore disabled mode, perform a STORE operation after t_{RTCp} time while writing into the RTC registers for the modifications to be correctly recorded.

Backup Power

The RTC in the CY14X064I is intended for permanently powered operation. The V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When the primary power, V_{CC}, fails and drops below V_{SWITCH} the device switches to the backup power supply.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of the clock operation with the primary source removed, the data stored in the nvSRAM is secure, having been stored in the nonvolatile elements when power was lost.

During backup operation, the CY14X064I consumes a 0.45 µA (Typ) at room temperature. The user must choose capacitor or battery values according to the application.

Backup time values based on maximum current specifications are shown in the following table. Nominal backup times are approximately two times longer.

Table 7. RTC Backup Time

Capacitor Value	Backup Time (CY14B064I)
0.1 F	60 hours
0.47 F	12 days
1.0 F	25 days

Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up. If a battery backup is used, a 3-V lithium battery is recommended and the CY14X064I sources current only from the battery when the primary power is removed. However, the battery is not recharged at any time by the CY14X064I. The battery capacity must be chosen for total anticipated cumulative down time required over the life of the system.

Stopping and Starting the Oscillator

The OSCEN bit in the calibration register at 0x08 controls the enable and disable of the oscillator. This bit is nonvolatile and is shipped to customers in the "enabled" (set to '0') state. To preserve the battery life when the system is in storage, OSCEN must be set to '1'. This turns off the oscillator circuit, extending the battery life. If the OSCEN bit goes from disabled to enabled, it takes approximately one second (two seconds maximum) for the oscillator to start.

While system power is off, if the voltage on the backup supply (V_{RTCcap} or V_{RTCbat}) falls below their respective minimum level, the oscillator may fail.The CY14X064I has the ability to detect oscillator failure when system power is restored. This is recorded in the Oscillator Fail Flag (OSCF) of the flags register at the address 0x00. When the device is powered on (V_{CC} goes above V_{SWITCH}) the OSCEN bit is checked for the 'enabled' status. If the OSCEN bit is enabled and the oscillator is not active within

the first 5 ms, the OSCF bit is set to ‘1’. The system must check for this condition and then write ‘0’ to clear the flag.

Note that in addition to setting the OSCF flag bit, the time registers are reset to the ‘Base Time’, which is the value last written to the timekeeping registers. The control or calibration registers and the OSCEN bit are not affected by the ‘oscillator failed’ condition.

The value of OSCF must be reset to ‘0’ when the time registers are written for the first time. This initializes the state of this bit which may have become set when the system was first powered on.

To reset OSCF, set the write bit ‘W’ (in the flags register at 0x00) to a ‘1’ to enable writes to the flags register. Write a ‘0’ to the OSCF bit and then reset the write bit to ‘0’ to disable writes.

Calibrating the Clock

The RTC is driven by a quartz-controlled crystal with a nominal frequency of 32.768 kHz. Clock accuracy depends on the quality of the crystal and calibration. The crystals available in the market typically have an error of $\pm$20 ppm to $\pm$35 ppm. However, CY14X064I employs a calibration circuit that improves the accuracy to +1/–2 ppm at 25 °C. This implies an error of +2.5 seconds to -5 seconds per month.

The calibration circuit adds or subtracts counts from the oscillator divider circuit to achieve this accuracy. The number of pulses that are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the calibration register at 0x08. The calibration bits occupy the five lower order bits in the calibration register. These bits are set to represent any value between ‘0’ and 31 in binary form. Bit D5 is a sign bit, where a ‘1’ indicates positive calibration and a ‘0’ indicates negative calibration. Adding counts speeds the clock up and subtracting counts slows the clock down. If a binary ‘1’ is loaded into the register, it corresponds to an adjustment of 4.068 or –2.034 ppm offset in oscillator error, depending on the sign.

Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once per minute, have one second shortened by 128 or lengthened by 256 oscillator cycles. If a binary ‘1’ is loaded into the register, only the first two minutes of the 64-minute cycle are modified. If a binary 6 is loaded, the first 12 are affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is, 4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

To determine the required calibration, the CAL bit in the flags register (0x00) must be set to ‘1’. This causes the INT pin to toggle at a nominal frequency of 512 Hz. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.01024 Hz indicates a +20 ppm error. Hence, a decimal value of –10 (001010b) must be loaded into the Calibration register to offset this error.

Note Setting or changing the calibration register does not affect the test output frequency.

To set or clear CAL, set the write bit ‘W’ (in the flags register at 0x00) to ‘1’ to enable writes to the flags register. Write a value to CAL, and then reset the write bit to ‘0’ to disable writes.

Alarm

The alarm function compares user programmed values of alarm time and date (stored in the registers 0x01-5) with the corresponding time of day and date values. When a match occurs, the alarm internal flag (AF) is set and an interrupt is generated on INT pin if alarm interrupt enable (AIE) bit is set.

There are four alarm match fields - date, hours, minutes, and seconds. Each of these fields has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to ‘0’ indicates that the corresponding field is used in the match process. Depending on the match bits, the alarm occurs as specifically as once a month or as frequently as once every minute. Selecting none of the match bits (all 1s) indicates that no match is required and therefore, alarm is disabled. Selecting all match bits (all 0s) causes an exact time and date match.

There are two ways to detect an alarm event: by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0x00 indicates that a date or time match has occurred. The AF bit is set to ‘1’ when a match occurs. Reading the flags register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

To set, clear or enable an alarm, set the ‘W’ bit (in flags register - 0x00) to ‘1’ to enable writes to alarm registers. After writing the alarm value, clear the ‘W’ bit back to ‘0’ for the changes to take effect.

Note CY14X064I requires the alarm match bit for seconds (bit ‘D7’ in Alarm-Seconds register 0x02) to be set to ‘0’ for proper operation of Alarm Flag and Interrupt.

Watchdog Timer

The watchdog timer is a free running down counter that uses the 32 Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the watchdog timer register.

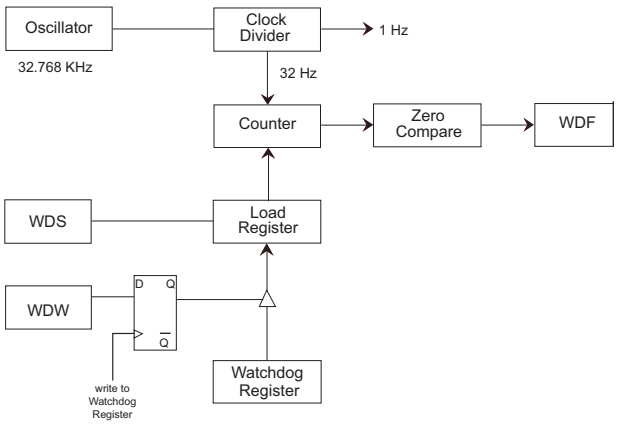
The timer consists of a loadable register and a free running counter. On power-up, the watchdog time out value in register 0x07 is loaded into the Counter Load register. Counting begins on power-up and restarts from the loadable value any time the Watchdog Strobe (WDS) bit is set to ‘1’. The counter is compared to the terminal value of ‘0’. If the counter reaches this value, it causes an internal flag and an optional interrupt output. You can prevent the time out interrupt by setting WDS bit to ‘1’ prior to the counter reaching ‘0’. This causes the counter to reload with the watchdog time out value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt and WDT flag never occur.

New time out values are written by setting the watchdog write bit to ‘0’. When the WDW is ‘0’, new writes to the watchdog time out value bits D5-D0 are enabled to modify the time out value. When WDW is ‘1’, writes to bits D5-D0 are ignored. The WDW function enables a user to set the WDS bit without concern that the watchdog timer value is modified. A logical diagram of the watchdog timer is shown in Figure 36 on page 22. Note that setting the watchdog time out value to ‘0’ disables the watchdog function.

The output of the watchdog timer is the flag bit WDF that is set if the watchdog is allowed to time out. If the watchdog interrupt

enable (WIE) bit in the Interrupt register is set, a hardware interrupt on INT pin is also generated on watchdog timeout. The flag and the hardware interrupt are both cleared when user reads the flag registers.

Figure 36. Watchdog Timer Block Diagram



Programmable Square Wave Generator

The square wave generator block uses the crystal output to generate a desired frequency on the INT pin of the device. The output frequency can be programmed to be one of the following:

1. 1 Hz
2. 512 Hz
3. 4096 Hz
4. 32768 Hz

The square wave output is not generated while the device is running on backup power.

Power Monitor

The CY14X064I provides a power management scheme with power fail interrupt capability. It also controls the internal switch to back up power for the clock and protects the memory from low V_{CC} access. The power monitor is based on an internal band gap reference circuit that compares the V_{CC} voltage to V_{SWITCH} threshold.

When V_{SWITCH} is reached, as V_{CC} decays from power loss, a data store operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source, read and write operations to nvSRAM are inhibited and the RTC functions are not available to the user. The RTC clock continues to operate in the background. The updated RTC time keeping registers are available to the user after V_{CC} is restored to the device (see nvSRAM Specifications on page 33).

Backup Power Monitor

The CY14X064I provides a backup power monitoring system that detects the backup power (either battery or capacitor backup) failure. The backup power fail flag (BPF) is issued on the next power-up in case of backup power failure. The BPF flag is set in the event of backup voltage falling lower than $V_{BAKFAIL}$. The backup power is monitored even while the RTC is running in backup mode. Low voltage detected during backup mode is flagged through the BPF flag. BPF can hold the data only until a defined low level of the back up voltage (V_{DR}).

Interrupts

The CY14X064I has a flags register, interrupt register, and interrupt logic that can signal interrupt to the microcontroller. There are three potential sources for interrupt: watchdog timer, power monitor, and alarm timer. Each of these can be individually enabled to drive the INT pin by appropriate setting in the interrupt register (0x06). In addition, each has an associated flag bit in the flags register (0x00) that the host processor uses to determine the cause of the interrupt. The INT pin driver has two bits that specify its behavior when an interrupt occurs.

An interrupt is raised only if both a flag is raised by one of the three sources and the respective interrupt enable bit in interrupts register is enabled (set to ‘1’). After an interrupt source is active, two programmable bits, H/L and P/L, determine the behavior of the output pin driver on INT pin. These two bits are located in the Interrupt register and can be used to drive level or pulse mode output from the INT pin. In pulse mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In the level mode, the pin goes to its active polarity until the flags register is read by the user. This mode is used as an interrupt to a host microcontroller. The control bits are summarized in the following section.

Interrupts are only generated while working on normal power and are not triggered when system is running in backup power mode.

Note CY14X064I generates valid interrupts only after the Powerup RECALL sequence is completed. All events on INT pin must be ignored for t_{FA} duration after powerup.

Interrupt Register

Watchdog Interrupt Enable (WIE): When set to ‘1’, the watchdog timer drives the INT pin and an internal flag when a watchdog time out occurs. When WIE is set to ‘0’, the watchdog timer only affects the WDF flag in flags register.

Alarm Interrupt Enable (AIE): When set to ‘1’, the alarm match drives the INT pin and an internal flag. When AIE is set to ‘0’, the alarm match only affects the AF flag in the flags register.

Power Fail Interrupt Enable (PFE): When set to ‘1’, the power fail monitor drives the pin and an internal flag. When PFE is set to ‘0’, the power fail monitor only affects the PF flag in the flags register.

Square Wave Enable (SQWE): When set to ‘1’, a square wave of programmable frequency is generated on the INT pin. The frequency is decided by the SQ1 and SQ0 bits of the interrupts register. This bit is nonvolatile and survives power cycle. The SQWE bit overrides all other interrupts. However, CAL bit will take precedence over the square wave generator. This bit defaults to ‘0’ from the factory.

High/Low (H/L): When set to a ‘1’, the INT pin is active HIGH and the driver mode is push pull. The INT pin drives HIGH only when V_{CC} is greater than V_{SWITCH}. When set to a ‘0’, the INT pin is active LOW and the drive mode is open drain. The INT pin must be pulled up to Vcc by a 10 k resistor while using the interrupt in active LOW mode.

Pulse/Level (P/L): When set to a '1' and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a '0', the INT pin is driven HIGH or LOW (determined by H/L) until the flags register is read.

SQ1 and SQ0. These bits are used together to fix the frequency of square wave on INT pin output when SQWE bit is set to '1'. These bits are nonvolatile and survive power cycle. The output frequency is decided as illustrated in this table.

Table 8. SQW Output Selection

SQ1	SQ0	Frequency	Comment
0	0	1 Hz	1 Hz signal
0	1	512 Hz	512 Hz clock output
1	0	4096 Hz	4 kHz clock output
1	1	32768 Hz	Oscillator output frequency

When an enabled interrupt source activates the INT pin, an external host reads the flag registers to determine the cause. Remember that all flags are cleared when the register is read. If the INT pin is programmed for Level mode, then the condition clears and the INT pin returns to its inactive state. If the pin is programmed for Pulse mode, then reading the flag also clears the flag and the pin. The pulse does not complete its specified duration if the flags register is read. If the INT pin is used as a host reset, the flags register is not read during a reset.

Following is a summary table that shows the state of the INT pin,

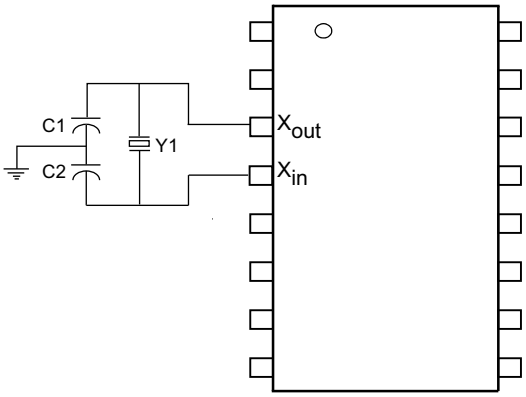
Table 9. State of the INT pin

CAL	SQWE	WIE/AIE/ PFE	INT Pin Output
1	X	X	512 Hz
0	1	X	Square wave output
0	0	1	Alarm
0	0	0	HI-Z

Flags Register

The flags register has three flag bits: WDF, AF, and PF, which can be used to generate an interrupt. These flags are set by the watchdog timeout, alarm match, or power fail monitor respectively. The processor can either poll this register or enable interrupts to be informed when a flag is set. These flags are automatically reset after the register is read. The flags register is automatically loaded with the value 0x00 on power-up (except for the OSCF bit. See Stopping and Starting the Oscillator on page 20).

Figure 37. RTC Recommended Component Configuration [4]

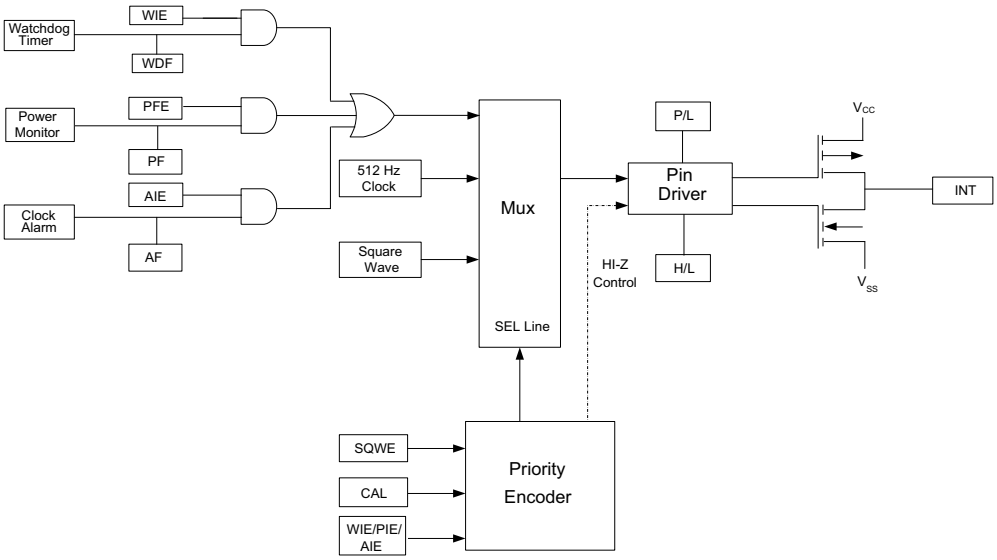


Recommended Values

Y1 = 32.768 kHz (12.5 pF)
C_1 = 12 pF
C_2 = 69 pF

Note: The recommended values for C1 and C2 include board trace capacitance.

Figure 38. Interrupt Block Diagram



WDF - Watchdog timer flag
WIE - Watchdog interrupt enable
PF - Power fail flag
PFE - Power Fail Enable
AF - Alarm fag
AIE - Alarm interrupt enable
P/L - Pulse level
H/L - High/Low
SQWE - Square wave enable

Note
4. For nonvolatile static random access memory (nvSRAM) real time clock (RTC) design guidelines and best practices, refer application note AN61546.

Table 10. RTC Register Map [5, 6]

Register	BCD Format Data								Function/Range
	D7	D6	D5	D4	D3	D2	D1	D0	
0x0F	10s years				Years				Years: 00–99
0x0E	0	0	0	10s months	Months				Months: 01–12
0x0D	0	0	10s day of month		Day of month				Day of month: 01–31
0x0C	0	0	0	0	0	Day of week			Day of week: 01–07
0x0B	0	0	10s hours		Hours				Hours: 00–23
0x0A	0	10s minutes			Minutes				Minutes: 00–59
0x09	0	10s seconds			Seconds				Seconds: 00–59
0x08	OSCEN (0)	0	Cal Sign (0)	Calibration (00000)					Calibration Values [7]
0x07	WDS (0)	WDW (0)	WDT (000000)						Watchdog [7]
0x06	WIE (0)	AIE (0)	PFE (0)	SQWE (0)	H/L (1)	P/L (0)	SQ1 (0)	SQ0 (0)	Interrupts [7]
0x05	M (1)	0	10s alarm date		Alarm day				Alarm, day of month: 01–31
0x04	M (1)	0	10s alarm hours		Alarm hours				Alarm, hours: 00–23
0x03	M (1)	10s alarm minutes			Alarm minutes				Alarm, minutes: 00–59
0x02	M (1)	10s alarm seconds			Alarm seconds				Alarm, seconds: 00–59
0x01	10s centuries				Centuries				Centuries: 00–99
0x00	WDF	AF	PF	OSCF[8]	BPF[8]	CAL (0)	W (0)	R (0)	Flags [7]

Notes
5. ( ) designates values shipped from the factory.
6. The unused bits of RTC registers are reserved for future use and should be set to '0'.
7. This is a binary value, not a BCD value.
8. When user resets OSCF and BPF flag bits, the flags register will be updated after t_{RTCp} time.

Table 11. Register Map Detail

Register	Description							
0x0F	**Time Keeping - Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10s years				Years			
	Contains the lower two BCD digits of the year. Lower nibble (four bits) contains the value for years; upper nibble (four bits) contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99.							
0x0E	**Time Keeping - Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10s month	Months			
	Contains the BCD digits of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12.							
0x0D	**Time Keeping - Date**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s day of month		Day of month			
	Contains the BCD digits for the date of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the 10s digit and operates from 0 to 3. The range for the register is 1–31. Leap years are automatically adjusted for.							
0x0C	**Time Keeping - Day**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day of week		
	Lower nibble (three bits) contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, because the day is not integrated with the date.							
0x0B	**Time Keeping - Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s hours		Hours			
	Contains the BCD value of hours in 24 hour format. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23.							
0x0A	**Time Keeping - Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s minutes			Minutes			
	Contains the BCD value of minutes. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59.							
0x09	**Time Keeping - Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s seconds			Seconds			
	Contains the BCD value of seconds. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper digit and operates from 0 to 5. The range for the register is 0–59.							
0X08	**Calibration/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	OSCEN	0	Calibration sign	Calibration				
OSCEN	Oscillator Enable. When set to ‘1’, the oscillator is stopped. When set to ‘0’, the oscillator runs. Disabling the oscillator saves battery or capacitor power during storage.							
Calibration Sign	Determines if the calibration adjustment is applied as an addition (1) to or as a subtraction (0) from the time-base.							

Table 11. Register Map Detail (continued)

Register	Description							
Calibration	These five bits control the calibration of the clock.							
0x07	**Watchdog Timer**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDS	WDW	WDT					
WDS	Watchdog Strobe. Setting this bit to ‘1’ reloads and restarts the watchdog timer. Setting the bit to ‘0’ has no effect. The bit is cleared automatically after the watchdog timer is reset. The WDS bit is write only. Reading it always returns a 0.							
WDW	Watchdog Write Enable. Setting this bit to ‘1’ disables any WRITE to the watchdog timeout value (D5–D0). This enables the user to set the watchdog strobe bit without disturbing the timeout value. Setting this bit to ‘0’ allows bits D5–D0 to be written to the watchdog register when the next write cycle is complete. This function is explained in more detail in Watchdog Timer on page 21.							
WDT	Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The range of timeout value is 31.25 ms (a setting of 1) to 2 seconds (setting of 3 Fh). Setting the watchdog timer register to ‘0’ disables the timer. These bits can be written only if the WDW bit was set to 0 on a previous cycle.							
0x06	**Interrupt Status/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WIE	AIE	PFE	SQWE	H/L	P/L	SQ1	SQ0
WIE	Watchdog Interrupt Enable. When set to ‘1’ and a watchdog timeout occurs, the watchdog timer drives the INT pin and the WDF flag. When set to ‘0’, the watchdog timeout affects only the WDF flag.							
AIE	Alarm Interrupt Enable. When set to ‘1’, the alarm match drives the INT pin and the AF flag. When set to ‘0’, the alarm match only affects the AF flag.							
PFE	Power Fail Enable. When set to ‘1’, the alarm match drives the INT pin and the PF flag. When set to ‘0’, the power fail monitor affects only the PF flag.							
SQWE	Square Wave Enable. When set to ‘1’, a square wave is driven on the INT pin with frequency programmed using SQ1 and SQ0 bits. The square wave output takes precedence over interrupt logic. If the SQWE bit is set to ‘1’. when an enabled interrupt source becomes active, only the corresponding flag is raised and the INT pin continues to drive the square wave.							
H/L	High/Low. When set to ‘1’, the INT pin is driven active HIGH. When set to ‘0’, the INT pin is open drain, active LOW.							
P/L	Pulse/Level. When set to ‘1’, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to ‘0’, the INT pin is driven to an active level (as set by H/L) until the flags register is read.							
SQ1, SQ0	SQ1, SQ0. These bits are used to decide the frequency of the Square wave on the INT pin output when SQWE bit is set to ‘1’. The following is the frequency output for each combination of (SQ1, SQ0): (0, 0) - 1 Hz (0, 1) - 512 Hz (1, 0) - 4096 Hz (1, 1) - 32768 Hz							
0x05	**Alarm - Day**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	0	10s alarm date		Alarm date			
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
M	Match. When this bit is set to ‘0’, the date value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the date value.							
0x04	**Alarm - Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	0	10s alarm hours		Alarm hours			
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
M	Match. When this bit is set to ‘0’, the hours value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the hours value.							

Table 11. Register Map Detail (continued)

Register	Description							
0x03	**Alarm - Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	10s alarm minutes			Alarm minutes			
	Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.							
M	Match. When this bit is set to ‘0’, the minutes value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the minutes value.							
0x02	**Alarm - Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	10s alarm seconds			Alarm seconds			
	Contains the alarm value for the seconds and the mask bit to select or deselect the seconds’ value.							
M	Match. When this bit is set to ‘0’, the seconds value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the seconds value.							
0x01	**Time Keeping - Centuries**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10s centuries				Centuries			
	Contains the BCD value of centuries. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 9. The range for the register is 0-99 centuries.							
0x00	**Flags**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDF	AF	PF	OSCF	BPF	CAL	W	R
WDF	Watchdog Timer Flag. This read only bit is set to ‘1’ when the watchdog timer is allowed to reach ‘0’ without being reset by the user. It is cleared to ‘0’ when the flags register is read or on power-up							
AF	Alarm Flag. This read only bit is set to ‘1’ when the time and date match the values stored in the alarm registers with the match bits = ‘0’. It is cleared when the flags register is read or on power-up.							
PF	Power Fail Flag. This read only bit is set to ‘1’ when power falls below the power fail threshold V_{SWITCH}. It is cleared when the flags register is read.							
OSCF	Oscillator Fail Flag. Set to ‘1’ on power-up if the oscillator is enabled and not running in the first 5 ms of operation. This indicates that RTC backup power failed and clock value is no longer valid. This bit survives power cycle and is never cleared internally by the chip. The user must check for this condition and write '0' to clear this flag. When user resets OSCF flag bit, the bit will be updated after t_{RTCp} time.							
BPF	Backup Power Fail Flag. Set to ‘1’ on power-up if the backup power (battery or capacitor) failed. The backup power fail condition is determined by the voltage falling below their respective minimum specified voltage. BPF can hold the data only till a defined low level of the back up voltage (V_{DR}). User must reset this bit to clear this flag. When user resets BPF flag bit, the bit will be updated after t_{RTCp} time.							
CAL	Calibration Mode. When set to ‘1’, a 512 Hz square wave is output on the INT pin. When set to ‘0’, the INT pin resumes normal operation. This bit takes priority than SQ0/SQ1 and other functions. This bit defaults to ‘0’ (disabled) on power-up.							
W	Write Enable: Setting the ‘W’ bit to ‘1’ freezes updates of the RTC registers. The user can then write to RTC registers, alarm registers, calibration register, interrupt register and flags register. Setting the ‘W’ bit to ‘0’ causes the contents of the RTC registers to be transferred to the time keeping counters if the time has changed. This transfer process takes t_{RTCp} time to complete. This bit defaults to 0 on power-up.							
R	Read Enable: Setting ‘R’ bit to ‘1’, stops clock updates to user RTC registers so that clock updates are not seen during the reading process. Set ‘R’ bit to ‘0’ to resume clock updates to the holding register. Setting this bit does not require ‘W’ bit to be set to ‘1’. This bit defaults to ‘0’ on power-up.							

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature 1000h

At 85 °C ambient temperature ..... 20 Years

Maximum junction temperature ..... 150 °C

Supply voltage on V_{CC} relative to V_{SS}

CY14C064I: .....–0.5 V to +3.1 V

CY14B064I: .....–0.5 V to +4.1 V

CY14E064I: .....–0.5 V to +7.0 V

DC voltage applied to outputs in high Z state .....–0.5 V to V_{CC} + 0.5 V

Input voltage .....–0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential .....–2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 seconds) ..... +260 °C

DC output current (1 output at a time, 1s duration). .... 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 140 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC}
CY14C064I	Industrial	–40 °C to +85 °C	2.4 V to 2.6 V
CY14B064I			2.7 V to 3.6 V
CY14E064I			4.5 V to 5.5 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [9]	Max	Unit
V_{CC}	Power supply		CY14C064I	2.4	2.5	2.6	V
			CY14B064I	2.7	3.0	3.6	V
			CY14E064I	4.5	5.0	5.5	V
I_{CC1}	Average V_{CC} current	f_{SCL} = 3.4 MHz; Values obtained without output loads (I_{OUT} = 0 mA)		–	–	1	mA
		f_{SCL} = 1 MHz; Values obtained without output loads (I_{OUT} = 0 mA)	CY14C064I CY14B064I	–	–	400	µA
			CY14E064I	–	–	450	µA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = max Average current for duration t_{STORE}		–	–	3	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}		–	–	3	mA
I_{SB}	V_{CC} standby current	SCL ≥ (V_{CC} – 0.2 V). V_{IN} ≤ 0.2 V or ≥ (V_{CC} – 0.2 V). 'W' bit set to '0'. Standby current level after nonvolatile cycle is complete. Inputs are static. f_{SCL} = 0 MHz.		–	–	250	µA
I_{ZZ}	Sleep mode current	t_{SLEEP} time after SLEEP Instruction is registered. All inputs are static and configured at CMOS logic level.		–	–	8	µA
I_{IX}[10]	Input current in each I/O pin (except $\overline{HSB}$)	0.1 V_{CC} < V_i < 0.9 $V_{CC(max)}$		–1	–	+1	µA
	Input current in each I/O pin (for $\overline{HSB}$)			–100	–	+1	µA
I_{OZ}	Output leakage current			–1	–	+1	µA

Note

9. Typical values are at 25 °C, V_{CC} = $V_{CC(typ)}$. Not 100% tested.
10. Not applicable to WP, A2, A1 and A0 pins.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [9]	Max	Unit
C_i	Capacitance for each I/O pin	Capacitance measured across all input and output signal pin and V_{SS}.		–	–	7	pF
V_{IH}	Input HIGH voltage			0.7 × Vcc	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage			–0.5	–	0.3 × V_{CC}	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA		0	–	0.4	V
		I_{OL} = 6 mA		0	–	0.6	V
R_{in} [11]	Input resistance (WP, A2, A1, A0)	For V_{IN} = $V_{IL(max)}$		50	–	–	KΩ
		For V_{IN} = $V_{IH(min)}$		1	–	–	MΩ
V_{hys}	Hysteresis of Schmitt trigger inputs			0.05 × V_{CC}	–	–	V
V_{CAP} [12]	Storage capacitor	Between V_{CAP} pin and V_{SS}	CY14C064I	170	220	270	µF
			CY14B064I CY14E064I	42	47	180	µF
V_{VCAP} [13, 14]	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} = Max	CY14C064I CY14B064I	–	–	V_{CC}	V
			CY14E064I	–	–	V_{CC}– 0.5	V

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

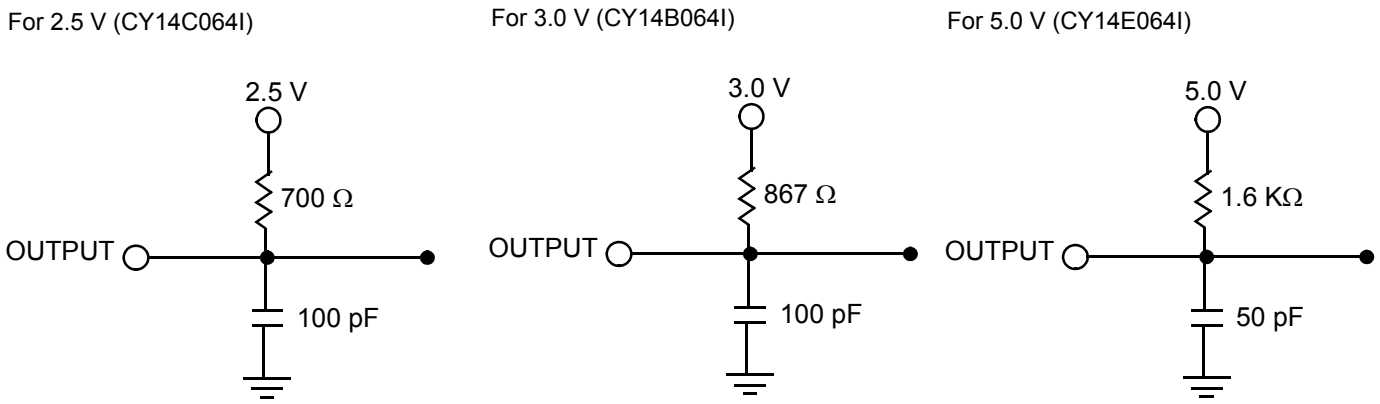
Thermal Resistance

Parameter [14]	Description	Test Conditions	16-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, according to EIA / JESD51.	56.68	°C/W
Θ_{JC}	Thermal resistance (junction to case)		32.11	°C/W

Notes
11. The input pull-down circuit is stronger (50 KΩ) when the input voltage is below V_{IL} and weak (1 MΩ) when the input voltage is above V_{IH}.
12. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note AN43593 for more details on V_{CAP} options.
13. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
14. These parameters are guaranteed by design and are not tested.

AC Test Loads and Waveforms

Figure 39. AC Test Loads and Waveforms



AC Test Conditions

Description	CY14C064I	CY14B064I	CY14E064I
Input pulse levels	0 V to 2.5 V	0 V to 3 V	0 V to 5 V
Input rise and fall times (10%–90%)	10 ns	10 ns	10 ns
Input and output timing reference levels	1.25 V	1.5 V	2.5 V

RTC Characteristics

Over the Operating Range

Parameter	Description		Min	Typ	Max	Units
V_{RTCbat}	RTC battery pin voltage		1.8	–	3.6	V
I_{BAK}[15]	RTC backup current	T_A (Min)	–	–	0.45	µA
		25 °C	–	0.45	–	µA
		T_A (Max)	–	–	0.60	µA
V_{RTCcap}[16]	RTC capacitor pin voltage	T_A (Min)	1.6	–	3.6	V
		25 °C	1.5	3.0	3.6	V
		T_A (Max)	1.4	–	3.6	V
$V_{BAKFAIL}$	Backup failure threshold		1.8	–	2.2	V
V_{DR}	BPF flag retention voltage		1.6	–	–	V
t_{OCS}	RTC oscillator time to start		–	1	2	sec
t_{RTCp}	RTC processing time from end of ‘W’ bit set to ‘0’		–	–	1	ms
R_{BKCHG}	RTC backup capacitor charge current-limiting resistor		350	–	850	Ω

Notes
15. Current drawn from either V_{RTCcap} or V_{RTCbat} when $V_{CC} < V_{SWITCH}$.
16. If $V_{RTCcap} > 0.5$ V or if no capacitor is connected to V_{RTCcap} pin, the oscillator will start in t_{OCS} time. If a backup capacitor is connected and $V_{RTCcap} < 0.5$ V, the capacitor must be allowed to charge to 0.5 V for oscillator to start.

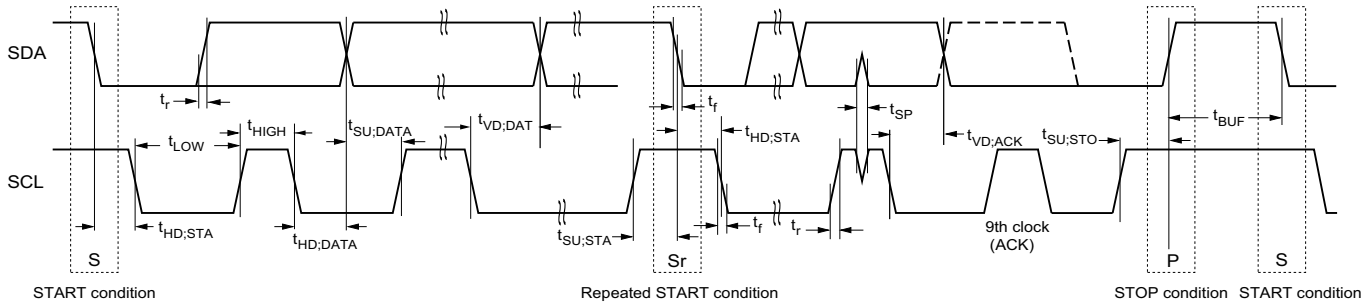
AC Switching Characteristics

Over the Operating Range

Parameter [17]	Description	3.4 MHz [18]		1 MHz [18]		400 kHz [18]		Unit
		Min	Max	Min	Max	Min	Max	
f_{SCL}	Clock frequency, SCL	–	3400	–	1000	–	400	kHz
$t_{SU;\ STA}$	Setup time for Repeated START condition	160	–	250	–	600	–	ns
$t_{HD;STA}$	Hold time for START condition	160	–	250	–	600	–	ns
t_{LOW}	LOW period of the SCL	160	–	500	–	1300	–	ns
t_{HIGH}	HIGH period of the SCL	60	–	260	–	600	–	ns
$t_{SU;DATA}$	Data in setup time	10	–	100		100		ns
$t_{HD;DATA}$	Data hold time (In/Out)	0	–	0	–	0	–	ns
t_{DH}	Data out hold time	0	–	0	–	0	–	ns
t_r [19]	Rise time of SDA and SCL	–	80	–	120	–	300	ns
t_f [19]	Fall time of SDA and SCL	–	80	–	120	–	300	ns
$t_{SU;STO}$	Setup time for STOP condition	160	–	250	–	600	–	ns
$t_{VD;DATA}$	Data output valid time	–	130	–	400	–	900	ns
$t_{VD;ACK}$	ACK output valid time	–	130	–	400	–	900	ns
t_{OF} [19]	Output fall time from V_{IH} min to V_{IL} max	–	80	–	120	–	250	ns
t_{BUF}	Bus free time between STOP and next START condition	0.3		0.5	–	1.3	–	us
t_{SP}	Pulse width of spikes that must be suppressed by input filter	–	10	–	50	–	50	ns

Switching Waveforms

Figure 40. Timing Diagram



Note

17. Test conditions assume signal transition time of 10 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL} and load capacitance shown in Figure 39 on page 31.
18. Bus Load (Cb) considerations; Cb < 500 pF for I^2C clock frequency (SCL) 100/400 KHz; Cb < 550 pF for SCL at 1000 kHz; Cb < 100 pF for SCL at 3.4 MHz.
19. These parameters are guaranteed by design and are not tested.

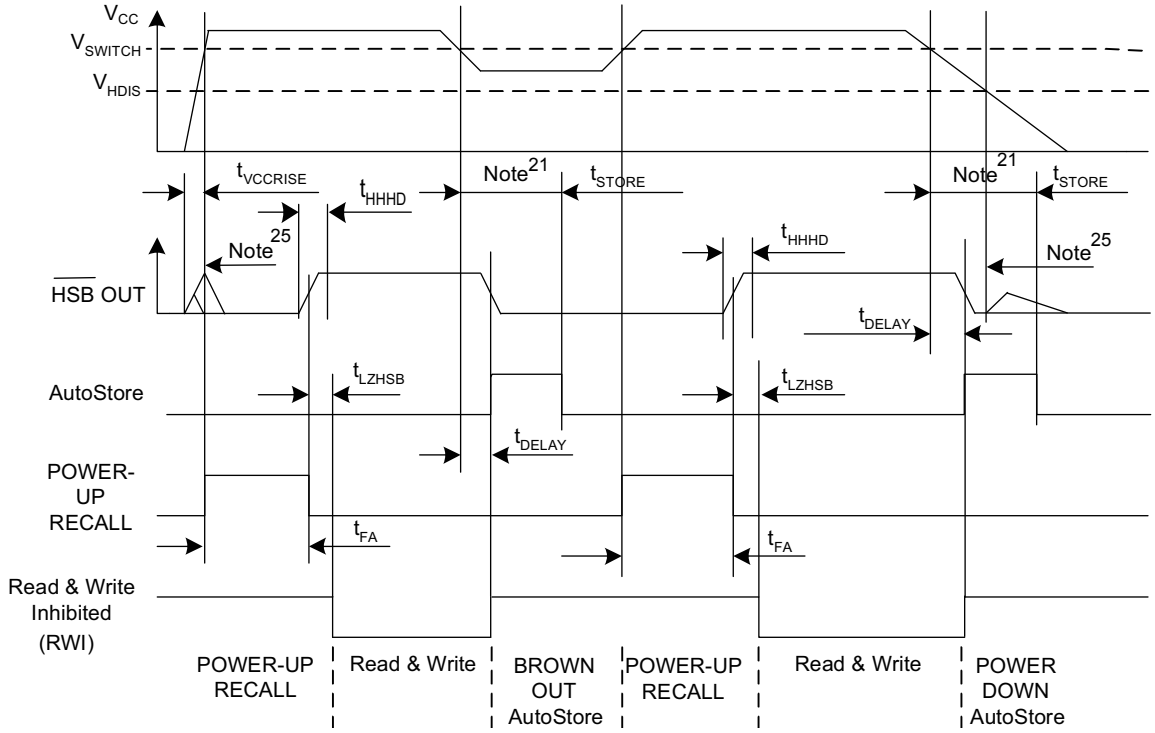
nvSRAM Specifications

Over the Operating Range

Parameter	Description		Min	Max	Unit
t_{FA} [20]	Power-up RECALL duration	CY14C064I	–	40	ms
		CY14B064I	–	20	ms
		CY14E064I	–	20	ms
t_{STORE} [21]	STORE cycle duration		–	8	ms
t_{DELAY} [22]	Time allowed to complete SRAM write cycle		–	25	ns
$t_{VCCRISE}$ [23]	V_{CC} rise time		150	–	µs
V_{SWITCH}	Low voltage trigger level	CY14C064I	–	2.35	V
		CY14B064I	–	2.65	V
		CY14E064I	–	4.40	V
t_{LZHSB} [23]	$\overline{HSB}$ high to nvSRAM active time		–	5	µs
V_{HDIS} [23]	$\overline{HSB}$ output disable voltage		–	1.9	V
t_{HHHD} [23]	$\overline{HSB}$ HIGH active time		–	500	ns
t_{WAKE}	Time for nvSRAM to wake up from SLEEP mode	CY14C064I	–	40	ms
		CY14B064I	–	20	ms
		CY14E064I	–	20	ms
t_{SLEEP}	Time to enter low power mode after issuing SLEEP instruction		–	8	ms
t_{SB} [23]	Time to enter into standby mode after issuing STOP condition		–	100	µs

Switching Waveforms

Figure 41. AutoStore or Power-Up RECALL [24]



Notes
20. t_{FA} starts from the time V_{CC} rises above V_{SWITCH}.
21. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
22. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
23. These parameters are guaranteed by design and are not tested.
24. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
25. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Software Controlled STORE/RECALL Cycles

Over the Operating Range

Parameter	Description	CY14X064I		Unit
		Min	Max	
t_{RECALL}	RECALL duration	–	600	µs
t_{SS}[26, 27]	Software sequence processing time	–	500	µs

Switching Waveforms

Figure 42. Software STORE/RECALL Cycle

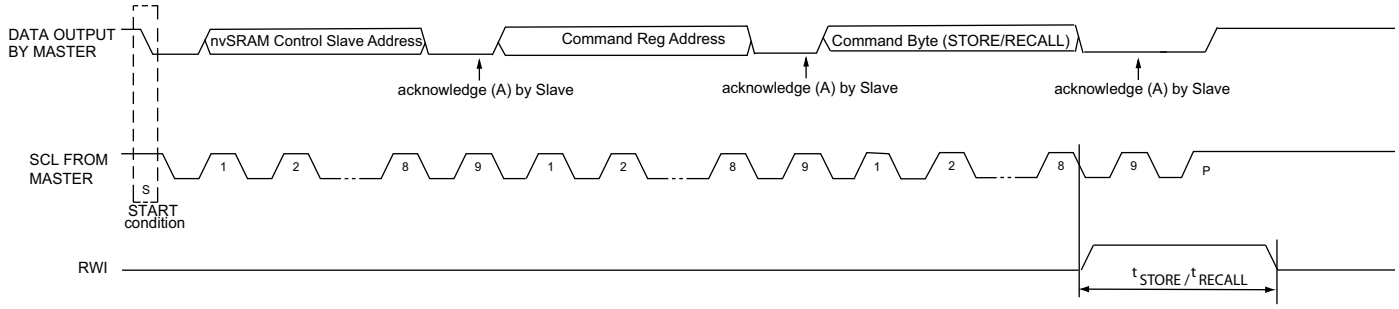
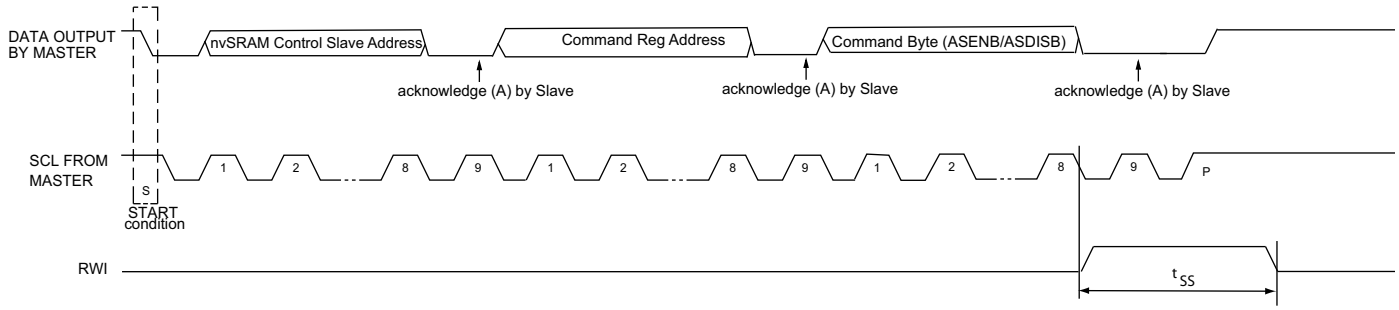


Figure 43. AutoStore Enable/Disable Cycle



Notes
26. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
27. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

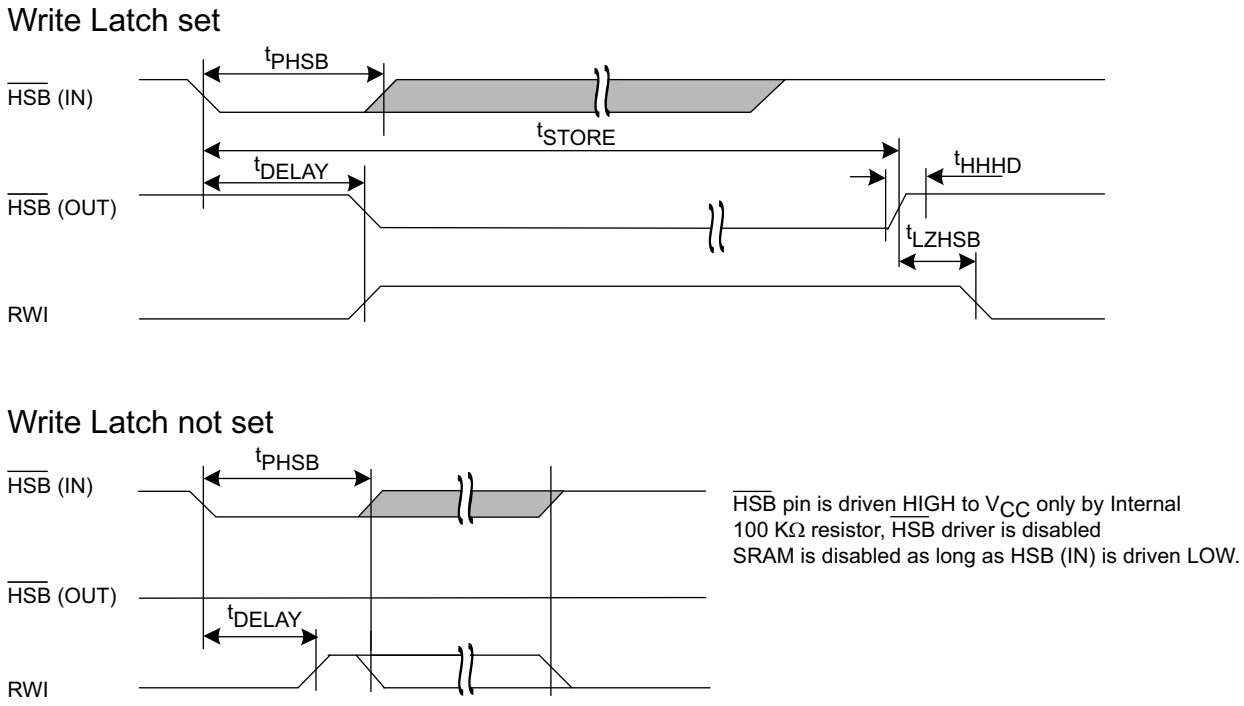
Hardware STORE Cycle

Over the Operating Range

Parameter	Description	CY14X064I		Unit
		Min	Max	
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Switching Waveforms

Figure 44. Hardware STORE Cycle [28]



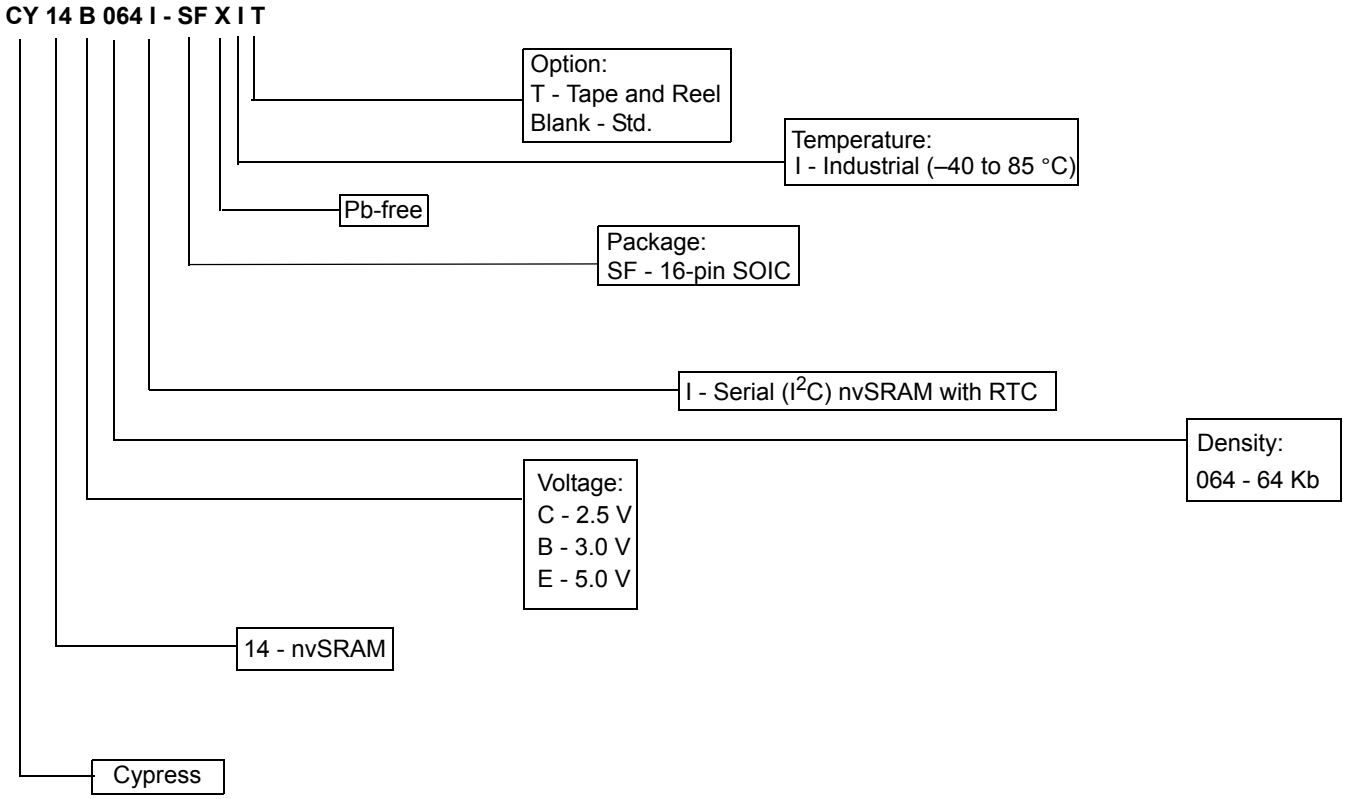
Note
28. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY14B064I-SFXI	51-85022	16-pin SOIC	Industrial
CY14B064I-SFXIT			

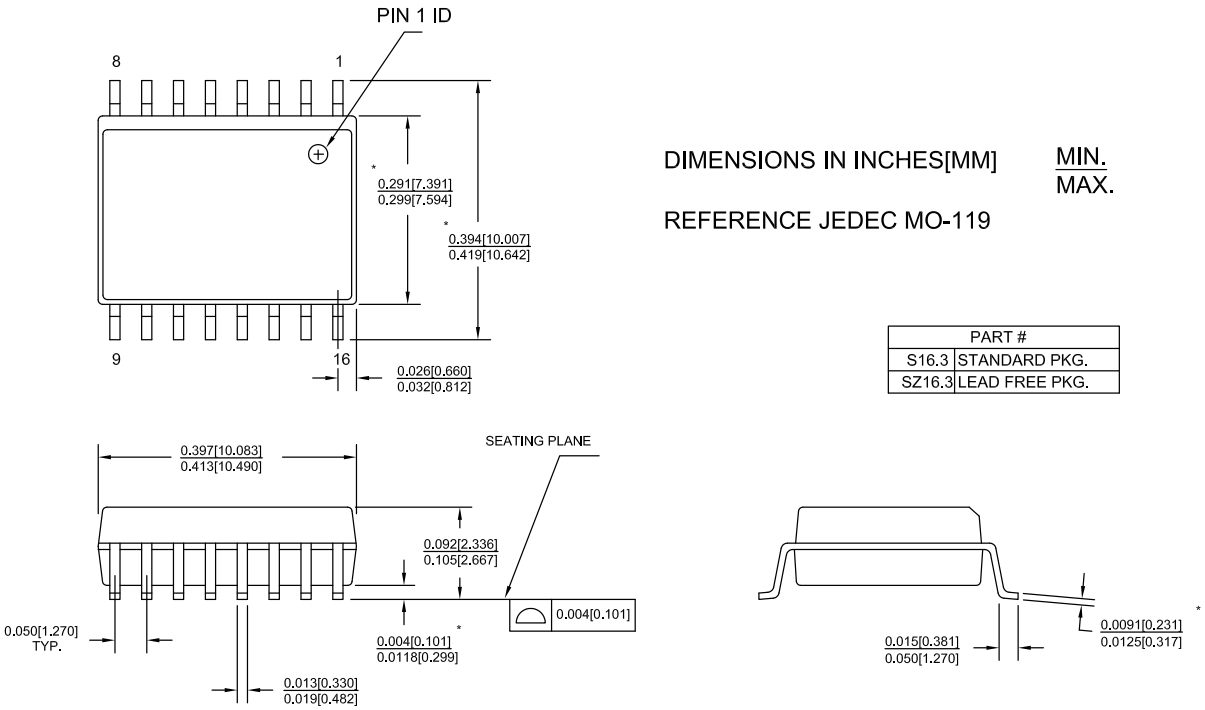
The above part is Pb-free. This table contains Preliminary information. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagram

Figure 45. 16-pin SOIC (0.413 × 0.299 × 0.0932 Inches) Package Outline, 51-85022



51-85022 *E

Acronyms

Acronym	Description
ACK	Acknowledge
BCD	Binary Coded Decimal
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
EIA	Electronic Industries Alliance
I^2C	Inter-Integrated Circuit Bus
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
nvSRAM	Non-volatile Static Random Access Memory
OSCF	Oscillator Fail Flag
RoHS	Restriction of Hazardous Substances
$R/\overline{W}$	Read/Write
RTC	Real Time Clock
RWI	Read and Write Inhibited
SCL	Serial Clock Line
SDA	Serial Data Line
SNL	Serial Number Lock
SOIC	Small Outline Integrated Circuit
SRAM	Static Random Access Memory
WP	Write Protect

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
F	farad
Hz	hertz
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
V	volt
W	watt

Document History Page

Document Title: CY14C064I, CY14B064I, CY14E064I, 64-Kbit (8 K × 8) Serial (I^2C) nvSRAM with Real Time Clock Document Number: 001-68169				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3201504	GVCH	03/21/2011	New data sheet.
*A	3389965	GVCH	12/05/2011	Updated Pin Definitions (Updated SDA pin description, added Note 3 and referred the same note in V_{RTCcap}, V_{RTCbat}, X_{out}, X_{in} pins). Updated Command Register (SLEEP description on page 9). Updated Device ID (Added device ID (4 bytes) column in Table 6). Updated Executing Commands Using Command Register (description). Added Note 4 and referred the same note in Figure 37. Updated DC Electrical Characteristics (Added I_{CC1} parameter value for 1 MHz frequency, changed maximum value of I_{CC2} parameter from 2 mA to 3 mA, removed I_{CC3} parameter, Added Note 12 and referred the note in the V_{CAP} parameter). Updated RTC Characteristics (Updated values of I_{BAK} and V_{RTCcap} parameters). Updated AC Switching Characteristics (Added Note 17 and referred the note in the Parameter column, and updated maximum value of t_{SP} parameter from 5 ns to 10 ns for 3.4 MHz). Updated Software Controlled STORE/RECALL Cycles (Updated Figure 42 and Figure 43). Updated Package Diagram.
*B	3580269	GVCH	04/12/2012	Updated nvSRAM Specifications (Referred Note 23 in the t_{SB} parameter).
*C	3680853	GVCH	07/25/2012	Updated DC Electrical Characteristics (Added V_{VCAP} parameter and its details, added Note 13 and referred the same note in V_{VCAP} parameter, also referred Note 14 in V_{VCAP} parameter).
*D	3762644	GVCH	10/01/2012	Updated Maximum Ratings (Removed “Ambient temperature with power applied” and included “Maximum junction temperature”).
*E	3909913	GVCH	02/21/2013	Changed status from “Preliminary” to “Final”. Updated Features: Added Note 1 and referred the same note in “High speed I^2C interface”.
*F	3985389	GVCH	04/30/2013	Updated Features: Updated Note 1. Updated DC Electrical Characteristics: Added one more condition “I_{OL} = 6 mA” for V_{OL} parameter and added respective values. Updated RTC Characteristics: Changed maximum value of $V_{BAKFAIL}$ parameter from 2 V to 2.2 V. Updated AC Switching Characteristics: Updated Note 18. Changed value of t_{OF} parameter from 300 ns to 250 ns for 400 kHz frequency. Updated Package Diagram: spec 51-85022 – Changed revision from *D to *E.

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