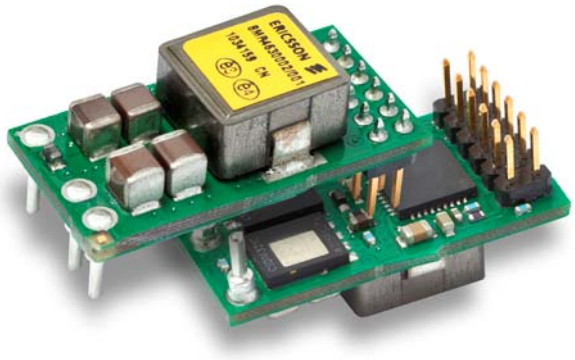
ERICSSON

Technical Specification

| **BMR 463 series** POL Regulators<br>Input 4.5-14 V, Output up to 20 A / 66 W | EN/LZT 146 434 R1A January 2011 |
|---|---|
| |  |

## Key Features

- Small package
  25.65 x 13.8 x 8.2 mm (1.01 x 0.543 x 0.323 in)
- 0.6 V - 3.3 V output voltage range
- High efficiency, typ. 97.1% at 5Vin, 3.3Vout half load
- Configuration and Monitoring via PMBus
- Synchonization & phase spreading
- Current sharing, Voltage Tracking & Voltage margining
- MTBF 20 Mh



## General Characteristics

- Fully regulated
- For narrow board pitch applications (15 mm/0.6 in)
- Non-Linear Response for reduction of decoupling cap.
- Input under voltage shutdown
- Over temperature protection
- Output short-circuit & Output over voltage protection
- Remote Control & Power Good
- Voltage setting via pin-strap or PMBus
- Advanced Configurable via Graphical Used Interface
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality

**Safety Approvals**

**Design for Environment**

Meets requirements in high-temperature lead-free soldering processes.

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**BMR 463 series** POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

EN/LZT 146 434 R1A January 2011



## Ordering Information

| Product program | Output |
|---|---|
| BMR 463 | 0.6-3.3 V, 20 A/ 66 W |

Product number and Packaging

| BMR 463 $n_1n_2n_3n_4/n_5n_6n_7n_8$ | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Options | $n_1$ | $n_2$ | $n_3$ | $n_4$ | / | $n_5$ | $n_6$ | $n_7$ | $n_8$ |
| Mounting | o | | | | / | | | | |
| Mechanical | | o | | | / | | | | |
| Interface | | | o | o | / | | | | |
| Configuration | | | | | / | o | o | o | |
| Packaging | | | | | / | | | | o |

| Options | Description | |
|---|---|---|
| $n_1$ | 0 | Through hole mount version (TH) |
| | 1 | Surface mount version (SMD) |
| $n_2$ | 0 | Open frame |
| $n_3$ $n_4$ | 02 | PMBus and analog pin strap |
| $n_5$ $n_6$ $n_7$ | 001 | Basic configuration |
| $n_8$ | C | Antistatic tape & reel of 200 products (1 full reel/box =200 products) |

Example: A through-hole mounted, open frame, PMBus and analog pin strap, basic configuration with antistatic tape & reel packaging would be BMR 463 0002/001C

## General Information

### Reliability

The failure rate ($\lambda$) and mean time between failures (MTBF) is calculated at max output power and an operating ambient temperature ($T_A$) of +40°C. Different calculations methods could be used which may give different results. Ericsson Power Modules uses Telcordia SR-332 Issue 2 Method 1 (parts count method) to calculate the mean steady-state failure rate and standard deviation ($\sigma$). MTBF = 1/$\lambda$

MTBF for the BMR 463 series = 20 Mh and $\sigma$ = 12 Mh

Telcordia SR-332 Issue 2 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

MTBF at 90% confidence level = 15 Mh

### Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2002/95/EC and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Ericsson Power Modules products include:

- Lead in glass of electronics components [5]
- Lead as an alloying element in copper alloy containing up to 4% lead by weight [6 c]
- Lead in high melting temperature type solder [7a]
- Lead in electronic ceramic parts [7c]
- Lead in solders to complete a viable connection between semiconductor die and carrier within integrated circuit flip chip packages [15]

### Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of our products.

### Warranty

Warranty period and conditions are defined in Ericsson Power Modules General Terms and Conditions of Sale.

### Limitation of Liability

Ericsson Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person's health or life).

## Safety Specification

### General information

Ericsson Power Modules DC/DC converters and DC/DC regulators are designed in accordance with safety standards IEC/EN/UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without "Conditions of Acceptability". Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

Component power supplies for general use should comply with the requirements in IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment.* There are other more product related standards, e.g. IEEE 802.3 *CSMA/CD (Ethernet) Access Method*, and ETS-300132-2 *Power supply interface at the input to telecommunications equipment, operated by direct current (dc)*, but all of these standards are based on IEC/EN/UL 60950-1 with regards to safety.

Ericsson Power Modules DC/DC converters and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1.

The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

The products should be installed in the end-use equipment, in accordance with the requirements of the ultimate application. Normally the output of the DC/DC converter is considered as SELV (Safety Extra Low Voltage) and the input source must be isolated by minimum Double or Reinforced Insulation from the primary circuit (AC mains) in accordance with IEC/EN/UL 60950-1.

### Isolated DC/DC converters

It is recommended that a slow blow fuse is to be used at the input of each DC/DC converter. If an input filter is used in the circuit the fuse should be placed in front of the input filter.
In the rare event of a component problem that imposes a short circuit on the input source, this fuse will provide the following functions:

- Isolate the fault from the input power source so as not to affect the operation of other parts of the system.
- Protect the distribution wiring from excessive current and power loss thus preventing hazardous overheating.

The galvanic isolation is verified in an electric strength test. The test voltage ($V_{iso}$) between input and output is 1500 Vdc or 2250 Vdc (refer to product specification).

### 24 V DC systems

The input voltage to the DC/DC converter is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

### 48 and 60 V DC systems

If the input voltage to the DC/DC converter is 75 Vdc or less, then the output remains SELV (Safety Extra Low Voltage) under normal and abnormal operating conditions.

Single fault testing in the input power supply circuit should be performed with the DC/DC converter connected to demonstrate that the input voltage does not exceed 75 Vdc.

If the input power source circuit is a DC power system, the source may be treated as a TNV-2 circuit and testing has demonstrated compliance with SELV limits in accordance with IEC/EN/UL60950-1.

### Non-isolated DC/DC regulators

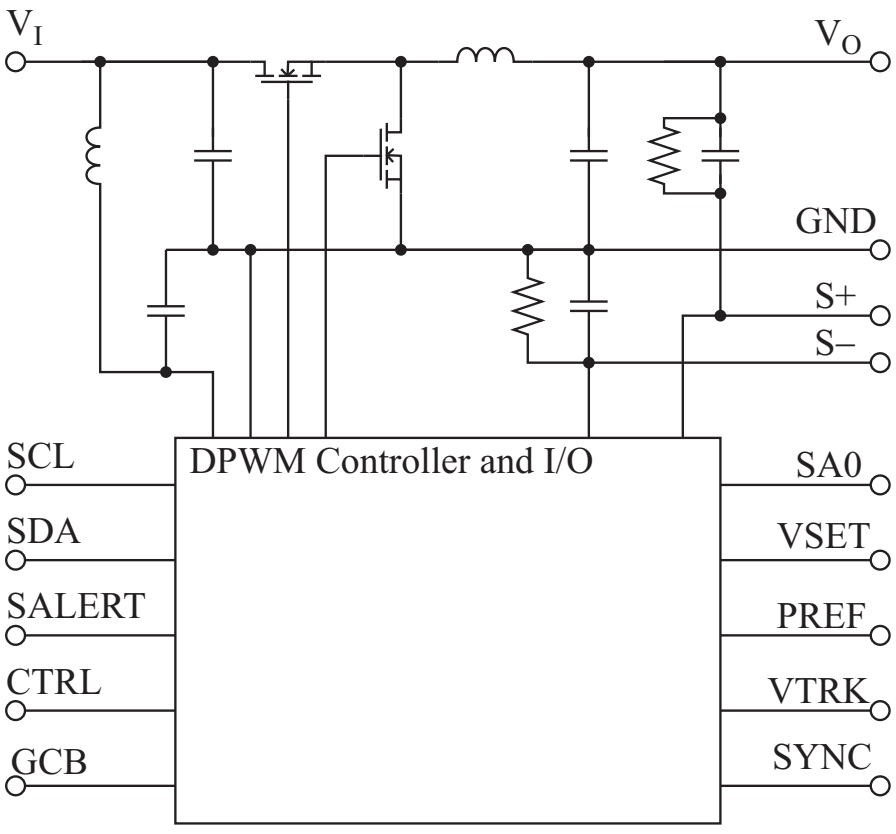
The input voltage to the DC/DC regulator is SELV (Safety Extra Low Voltage) and the output remains SELV under normal and abnormal operating conditions.

### Absolute Maximum Ratings

| Characteristics | | min | typ | max | Unit |
|---|---|---|---|---|---|
| $T_{P1}$ | Operating temperature (see Thermal Consideration section) | -40 | | 120 | °C |
| $T_S$ | Storage temperature | -40 | | 125 | °C |
| $V_I$ | Input voltage (See Operating Information Section for input and output voltage relations) | -0.3 | | 16 | V |
| Logic I/O voltage | CTRL, SA0, SALERT, SCL, SDA, VSET, SYNC, GCB | -0.3 | | 6.5 | V |
| Ground voltage differential | S-, PREF, GND | -0.3 | | 0.3 | V |
| Analog pin voltage | $V_O$, S+, VTRK | -0.3 | | 6.5 | V |

Stress in excess of Absolute Maximum Ratings may cause permanent damage. Absolute Maximum Ratings, sometimes referred to as no destruction limits, are normally tested with one parameter at a time exceeding the limits in the Electrical Specification. If exposed to stress above these limits, function and performance may degrade in an unspecified manner.

### Fundamental Circuit Diagram



## Electrical Specification

**BMR 463**

$T_{P1}$ = -30 to +85ºC, $V_I$ = 4.5 to 14 V
Typical values given at: $T_{P1}$ = +25°C, $V_I$ = 12.0 V, max $I_O$, unless otherwise specified under Conditions.
Basic configuration (configuration file: 190 10-CDA 102 0175/001)
Additional $C_I$ = 470 µF, $C_O$ = 470 µF. See Operating Information section for selection of capacitor types.
Sense pins are connected to the output pins.

| Characteristics | | | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input voltage rise time | | monotonic | 5 | | | ms |
| $V_O$ | Output voltage without pin stap | | | | 1.2 | | V |
| | Output voltage adjustment range | | $V_I > V_O + 1.0$ V | 0.60 | | 3.30 | V |
| | Output voltage adjustment including margining | | $V_I > V_O + 1.0$ V | 0.54 | | 3.63 | V |
| | Output voltage set-point resolution | | | | ±0.025 | | % $V_O$ |
| | Output voltage accuracy | | Includes, line, load, temp. | -1 | | 1 | % |
| | Line regulation | | $V_O$ = 0.6 V | | 2 | | mV |
| | | | $V_O$ = 1.0 V | | 2 | | |
| | | | $V_O$ = 1.8 V | | 2 | | |
| | | | $V_O$ = 3.3 V | | 3 | | |
| | Load regulation; Iout = 0 - 100% | | $V_O$ = 0.6 V | | 3 | | mV |
| | | | $V_O$ = 1.0 V | | 2 | | |
| | | | $V_O$ = 1.8 V | | 2 | | |
| | | | $V_O$ = 3.3 V | | 2 | | |
| $V_{Oac}$ | Output ripple & noise | | $V_O$ = 0.6 V | | 20 | | mVp-p |
| | | | $V_O$ = 1.0 V | | 30 | | |
| | | | $V_O$ = 1.8 V | | 40 | | |
| | | | $V_O$ = 3.3 V | | 60 | | |
| $I_O$ | Output current | | | | | 20 | A |
| $I_S$ | Static input current | | $V_O$ = 0.6 V | | 1.26 | | A |
| | | | $V_O$ = 1.0 V | | 1.94 | | |
| | | | $V_O$ = 1.8 V | | 3.31 | | |
| | | | $V_O$ = 3.3 V | | 5.89 | | |
| $I_{lim}$ | Current limit threshold | | Full working range | 22 | 25 | 30 | A |
| $I_{sc}$ | Short circuit current | RMS, hiccup mode, See Note 3 | $V_O$ = 0.6 V | | 8 | | A |
| | | | $V_O$ = 1.0 V | | 6 | | |
| | | | $V_O$ = 1.8 V | | 5 | | |
| | | | $V_O$ = 3.3 V | | 4 | | |
| η | Efficiency | 50% of max $I_O$ | $V_O$ = 0.6 V | | 84.0 | | % |
| | | | $V_O$ = 1.0 V | | 89.3 | | |
| | | | $V_O$ = 1.8 V | | 92.8 | | |
| | | | $V_O$ = 3.3 V | | 94.8 | | |
| | | max $I_O$ | $V_O$ = 0.6 V | | 79.3 | | % |
| | | | $V_O$ = 1.0 V | | 86.0 | | |
| | | | $V_O$ = 1.8 V | | 90.7 | | |
| | | | $V_O$ = 3.3 V | | 93.6 | | |
| $P_d$ | Power dissipation | | $V_O$ = 0.6 V | | 3.12 | | W |
| | | | $V_O$ = 1.0 V | | 3.25 | | |
| | | | $V_O$ = 1.8 V | | 3.68 | | |
| | | | $V_O$ = 3.3 V | | 4.52 | | |
| $P_{li}$ | Input idling power | Factory default: Continues Conduction Mode, CCM | $V_O$ = 0.6 V | | 0.56 | | W |
| | | | $V_O$ = 1.0 V | | 0.57 | | |
| | | | $V_O$ = 1.8 V | | 0.68 | | |
| | | | $V_O$ = 3.3 V | | 0.99 | | |
| | | DCM, Discontinues Conduction Mode (diode emulation) | $V_O$ = 0.6 V | | 0.36 | | W |
| | | | $V_O$ = 1.0 V | | 0.30 | | |
| | | | $V_O$ = 1.8 V | | 0.20 | | |
| | | | $V_O$ = 3.3 V | | 0.21 | | |

| | | | | | |
|---|---|---|---|---|---|
| | | DCM with Adaptive Frequency and Minimum Pulse Enabled | $V_O$ = 0.6 V | 0.26 | W |
| | | | $V_O$ = 1.0 V | 0.27 | |
| | | | $V_O$ = 1.8 V | 0.34 | |
| | | | $V_O$ = 3.3 V | 0.43 | |
| | | DCM with Adaptive Frequency and Minimum Pulse Disabled | $V_O$ = 0.6 V | 0.25 | W |
| | | | $V_O$ = 1.0 V | 0.20 | |
| | | | $V_O$ = 1.8 V | 0.20 | |
| | | | $V_O$ = 3.3 V | 0.20 | |
| $P_{CTRL}$ | Input standby power | Turned off with CTRL-pin | Factory default: Monitoring enabled, Precise timing enabled | 180 | mW |
| | | | Monitoring enabled, Precise timing disabled | 120 | |
| | | | Low power mode: Monitoring disabled, Precise timing disabled | 85 | mW |

| | | | | | |
|---|---|---|---|---|---|
| $C_I$ | Internal input capacitance | | | 70 | µF |
| $C_{OI}$ | Internal output capacitance | | | 200 | µF |
| $C_O$ | Total external output capacitance | | 300 | 15 000 | µF |
| | ESR range of capacitors (per single capacitor) | | 5 | 30 | mΩ |

| | | | | | |
|---|---|---|---|---|---|
| $V_{tr1}$ | Load transient peak voltage deviation<br>Load step 25-75-25% of max $I_O$ | Factory default configuration di/dt = 2 A/µs | $V_O$ = 0.6 V | 210 | mV |
| | | | $V_O$ = 1.0 V | 220 | |
| | | | $V_O$ = 1.8 V | 220 | |
| | | | $V_O$ = 3.3 V | 240 | |
| | | Optimized PID and NLR configuration di/dt = 2 A/µs | $V_O$ = 0.6 V | 60 | |
| | | | $V_O$ = 1.0 V | 70 | |
| | | | $V_O$ = 1.8 V | 70 | |
| | | | $V_O$ = 3.3 V | 80 | |
| $t_{tr1}$ | Load transient recovery time, Note 5<br>Load step 25-75-25% of max $I_O$ | Factory default configuration di/dt = 2 A/µs | $V_O$ = 0.6 V | 120 | µs |
| | | | $V_O$ = 1.0 V | 100 | |
| | | | $V_O$ = 1.8 V | 100 | |
| | | | $V_O$ = 3.3 V | 50 | |
| | | Optimized PID and NLR configuration di/dt = 2 A/µs | $V_O$ = 0.6 V | 30 | |
| | | | $V_O$ = 1.0 V | 25 | |
| | | | $V_O$ = 1.8 V | 25 | |
| | | | $V_O$ = 3.3 V | 20 | |

| | | | | | |
|---|---|---|---|---|---|
| $f_s$ | Switching frequency | Factory default | | 320 | kHz |
| | Switching frequency range | See Note 7 | 200 | 640 | kHz |
| | Switching frequency set-point accuracy | | | ±5 | % |
| | Maximum PWM Duty Cycle | | 5 | 95 | % |
| | Minimum Sync Pulse Width | | 150 | | ns |
| | Synchronization Frequency Tolerance | External clock source | | ±13 | % |

| | | | | | |
|---|---|---|---|---|---|
| Input Under Voltage Lockout, UVLO | UVLO Threshold | Factory default | | 3.85 | V |
| | UVLO Threshold range | | 3.85 | 14 | V |
| | Set point accuracy | | -200 | 200 | mV |
| | Hysteresis | Factory default | | 0.35 | V |
| | Hysteresis range | | 0 | 10.15 | V |
| | Delay | | | 2.5 | µs |
| | Fault response | Factory default, See Note 3 | | Automatic restart, 70ms | |
| Input Over Voltage Protection | IOVP Threshold | Factory default | | 16 | V |
| | IOVP Threshold range | | 4.2 | 16 | V |
| | Set point accuracy | | | ±200 | mV |
| | Hysteresis | Factory default | | 1 | V |
| | Hysteresis range | | 0 | 11.8 | V |
| | Delay | | | 2.5 | µs |

| | | | | | |
|---|---|---|---|---|---|
| | Fault response | Factory default, See Note 3 | Automatic restart, 70ms | | |
| Power Good, PG, See Note 2 | PG threshold | Factory default | 90 | | % $V_O$ |
| | PG hysteresis | Factory default | 5 | | % $V_O$ |
| | PG delay | Factory default | 10 | | ms |
| | PG delay range | | 0 | 500 | s |
| Output voltage Over/Under Voltage Protection, OVP/UVP | UVP threshold | Factory default | 85 | | % $V_O$ |
| | UVP range | | 0 | 110 | % $V_O$ |
| | UVP hysteresis | | 5 | | % $V_O$ |
| | OVP threshold | Factory default | 115 | | % $V_O$ |
| | OVP range | | 0 | 115 | % $V_O$ |
| | UVP/OVP Response time | Factory default | 25 | | µs |
| | UVP/OVP Response time range | | 5 | 60 | µs |
| | Fault response | Factory default, See Note 3 | Automatic restart, 70ms | | |
| Over Current Protection, OCP | Threshold | Factory default | 25 | | A |
| | Threshold range | | 0 | 25 | A |
| | Set-point accuracy | | ±10 | | % of Full Scale |
| | Protection delay, See Note 4 | Factory default | 5 | | $T_{sw}$ |
| | Protection delay range | | 1 | 32 | $T_{sw}$ |
| | Fault response | Factory default, See Note 3 | Automatic restart, 70ms | | |
| Over Temperature Protection, OTP at P1 | Threshold | Factory default | 120 | | °C |
| | Threshold range | | -40 | 120 | °C |
| | Hysteresis | Factory default | 15 | | °C |
| | Hysteresis range | | 0 | 160 | °C |
| | Fault response | Factory default, See Note 3 | Automatic restart, 70ms | | |

| | | | | | |
|---|---|---|---|---|---|
| $V_{IL}$ | Logic input low threshold | SALERT, SCL, SDA, VSET, GCB | | 0.8 | V |
| $V_{IH}$ | Logic input high threshold | | 2 | | V |
| $V_{OL}$ | Logic output low (sinking) | SALERT, SCL, SDA, VSET, GCB $I_{OL} \leq 4$ mA | | 0.4 | V |
| $V_{OH}$ | Logic output high (sourcing) | SALERT, SCL, SDA, VSET, GCB $I_{OL} \leq 2$ mA | 2.25 | | V |
| $t_{set}$ | Setup time, SMBus | See Note 1 | 300 | | ns |
| $t_{hold}$ | Hold time, SMBus | See Note 1 | 250 | | ns |
| $C_p$ | Internal capacitance on pins | SCL,SDA, SALERT,GCB | | 10 | pF |

| | | | | | |
|---|---|---|---|---|---|
| Delay Time | Delay duration, Note 6 | Factory default | 10 | | ms |
| | Delay duration range | | 2 | 500 000 | |
| | Delay accuracy | CTRL controlled Precise timing enabled Factory default | ±0.25 | | ms |
| | | PMBus controlled Precise timing disabled | -0.25/+4 | | ms |
| Ramp Time | Ramp duration | Factory default | 10 | | ms |
| | Ramp duration range | | 0 | 200 | |
| | Ramp time accuracy | | 100 | | µs |

| | | | | |
|---|---|---|---|---|
| VTRK Input Bias Current | VTRK = 5.5 V | 110 | 200 | µA |
| VTRK Tracking Static Accuracy, Note 8 | 100% Tracking ($V_{OUT}$-VTRK) | -100 | 100 | mV |
| VTRK Regulation Accuracy | 100% Tracking ($V_{OUT}$-VTRK) | -1 | 1 | % |

| | | | |
|---|---|---|---|
| Current share accuracy | | 20 | % of Full Sscale |
| Number of modules in current sharing group | | 1 | 8 | |

| | | | | |
|---|---|---|---|---|
| VIN_READ, 0x88h | Accuracy vs. $V_I$ | | 3 | % |

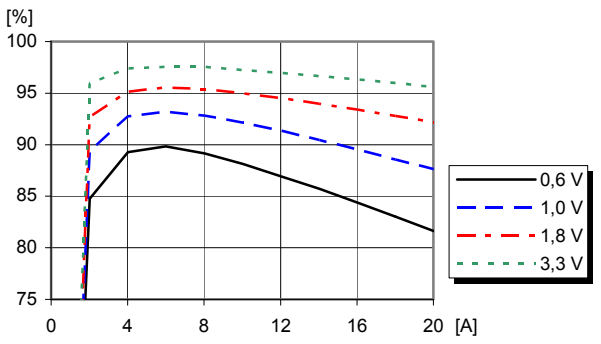
| | | | | |
|---|---|---|---|---|
| VOUT_READ, 0x8Bh | Accuracy vs. $V_O$ | | 1 | % |
| IOUT_READ, 0x8Ch | Accuracy vs. $I_O$ | $V_I$ = 12 V, $V_O$ = 1 V, $T_{P1}$ = 0 to +85°C | ±1.4 | A |
| IOUT_READ, 0x8Ch | Accuracy vs. $I_O$ | $V_I$ = 4.5-14 V, $V_O$ = 1 V, $T_{P1}$ = 0 to +85°C | ±2.6 | A |

Note 1: See Power Management section for I2C/SMBus Setup and Hold Times – Definitions.
Note 2: Monitorable over PMBus Interface.
Note 3: Continuous re-starts with 70 ms between each start. See Power Management section for additional fault response types.
Note 4: $T_{sw}$ is the switching period.
Note 5: Within +/-3% of $V_O$
Note 6: See Soft-start Power Up section.
Note 7: The product is not fully verified outside default switching frequency.
Note 8: In a dynamical case accuracy will depend on VTRK slewrate and the regulator bandwidth.

## Typical Characteristics
## Efficiency and Power Dissipation

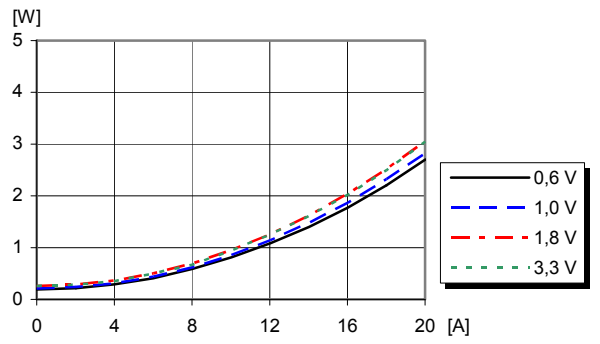
**BMR 463**

### Efficiency vs. Output Current at $V_I$ = 5 V



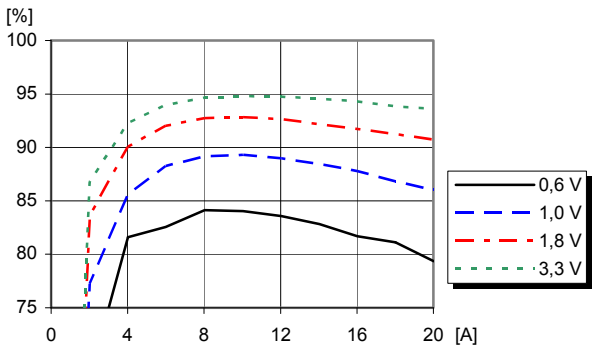

Efficiency vs. load current and output voltage:
$T_{P1}$ = +25°C. $V_I$=5 V, $f_{sw}$=320 kHz, $C_O$ = 470 µF. Default Configuration.

### Power Dissipation vs. Output Current at $V_I$ = 5 V



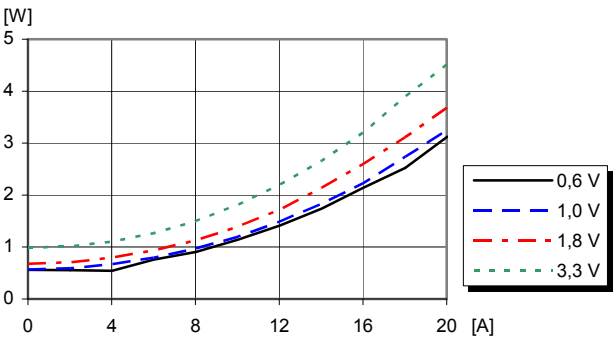

Dissipated power vs. load current and output voltage:
$T_{P1}$ = +25°C. $V_I$=5 V, $f_{sw}$=320 kHz, $C_O$ = 470 µF. Default Configuration.

### Efficiency vs. Output Current at $V_I$ = 12 V



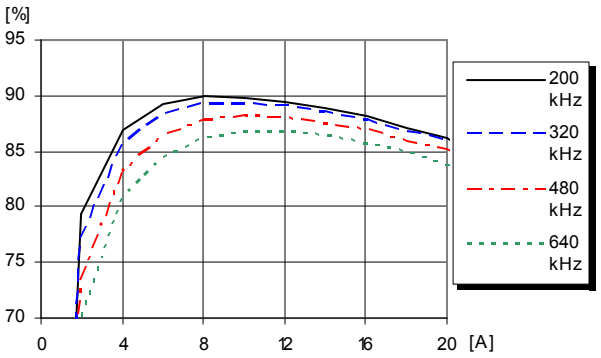

Efficiency vs. load current and output voltage at
$T_{P1}$ = +25°C. $V_I$=12 V, $f_{sw}$=320 kHz, $C_O$ = 470 µF. Default Configuration.

### Power Dissipation vs. Output Current at $V_I$ = 12 V



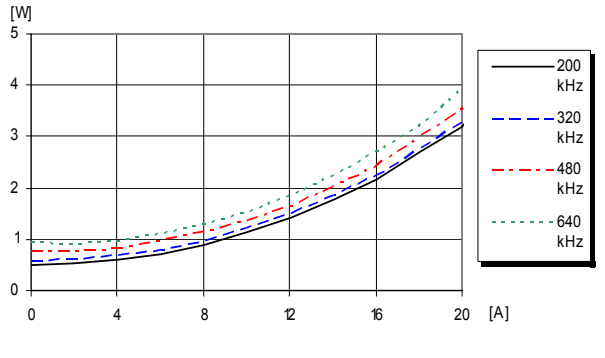

Dissipated power vs. load current and output voltage:
$T_{P1}$ = +25°C. $V_I$=12 V, $f_{sw}$=320 kHz, $C_O$ = 470 µF. Default Configuration.

### Efficiency vs. Output Current and Switch Frequency




Efficiency vs. load current and switch frequency at
$T_{P1}$ = +25°C. $V_I$=12 V, $V_O$=1.0 V, $C_O$ = 470 µF.

### Power Dissipation vs. Output Current and Switch Frequency

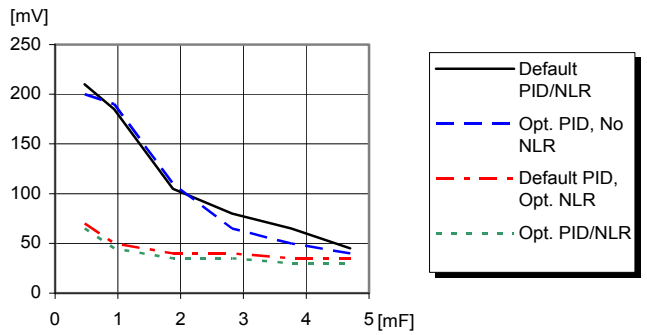



Dissipated power vs. load current and switch frequency at
$T_{P1}$ = +25°C. $V_I$=12 V, $V_O$=1.0 V, $C_O$ = 470 µF.

## Typical Characteristics
## Load Transient

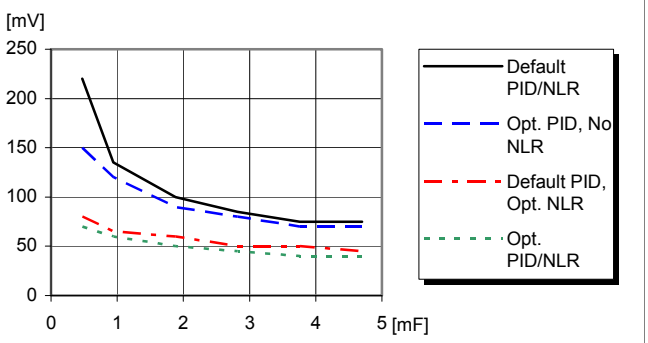
**BMR 463**

### Load Transient vs. Decoupling Capacitance, $V_O$ = 1.0 V



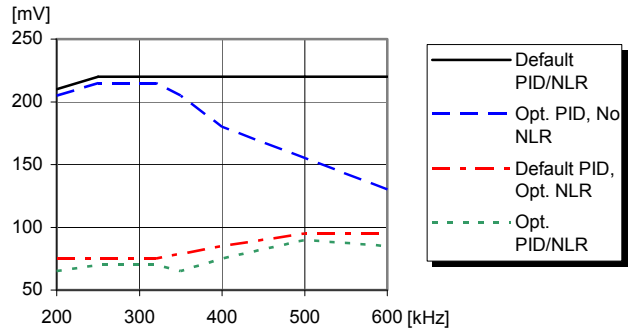

Load transient peak voltage deviation vs. decoupling capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 µF/ 10 mΩ,
$T_{P1}$ = +25°C. $V_I$=12 V, $V_O$=1.0 V, $f_{sw}$=320 kHz, di/dt=2 A/µs

### Load Transient vs. Decoupling Capacitance, $V_O$ = 3.3 V



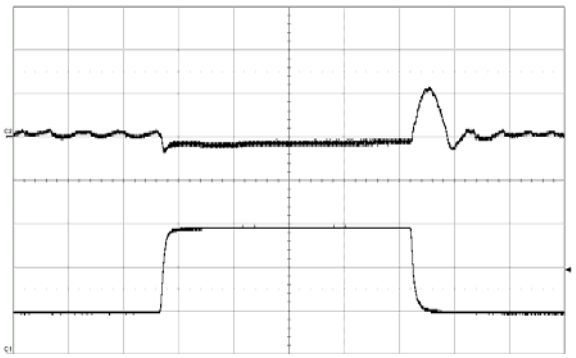

Load transient peak voltage deviation vs. decoupling capacitance.
Step-change (5-15-5 A). Parallel coupling of capacitors with 470 µF/ 10 mΩ
$T_{P1}$ = +25°C. $V_I$=12 V, $V_O$=3.3 V, $f_{sw}$=320 kHz, di/dt=2 A/µs

### Load transient vs. Switch Frequency




Load transient peak voltage deviation vs. frequency. Step-change (5-15-5 A).
$T_{P1}$ = +25°C. $V_I$=12 V, $V_O$=1.0 V, $C_O$ = 470 µF.

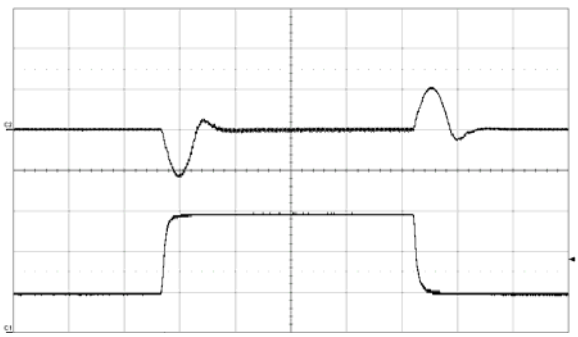
### Output Load Transient Response, Default



Output voltage response to load current step-change (5-15-5 A) at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $V_O$ =1.0 V
di/dt=2 A/µs, $f_{sw}$=320 kHz, $C_O$ = 470 µF.
Default PID Control Loop and NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

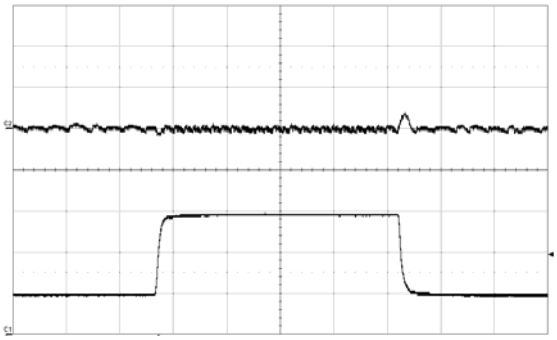
### Output Load Transient Response, Optimized PID, no NLR



Output voltage response to load current step-change (5-15-5 A) at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $V_O$ =1.0 V
di/dt=2 A/µs, $f_{sw}$=320 kHz, $C_O$ = 470 µF.
Optimized PID Control Loop and no NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

### Output Load Transient Response, Optimized NLR



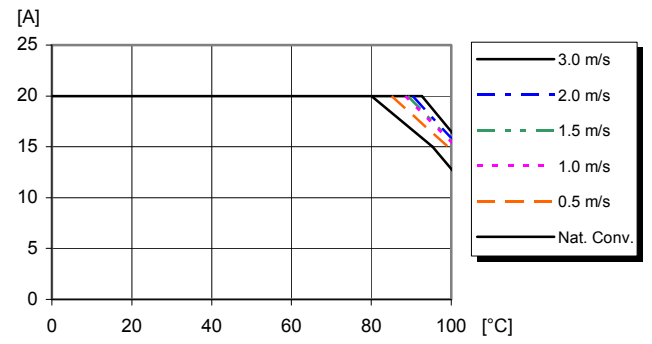
Output voltage response to load current step-change (5-15-5 A) at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $V_O$ =1.0 V
di/dt=2 A/µs, $f_{sw}$=320 kHz, $C_O$ = 470 µF.
Default PID Control Loop and optimized NLR

Top trace: output voltage (200 mV/div.).
Bottom trace: load current (5 A/div.).
Time scale: (0.1 ms/div.).

## Typical Characteristics
## Output Current Characteristic

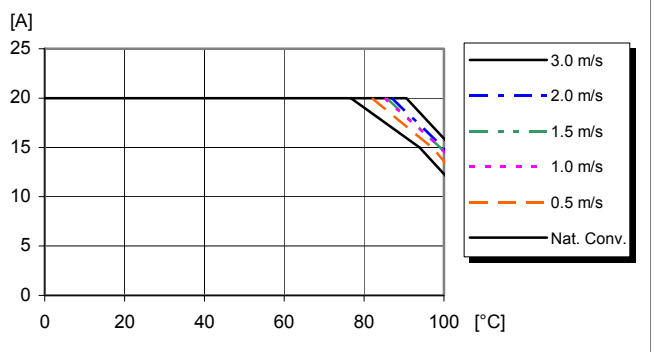
**BMR 463**

### Output Current Derating, $V_O$ = 0.6 V



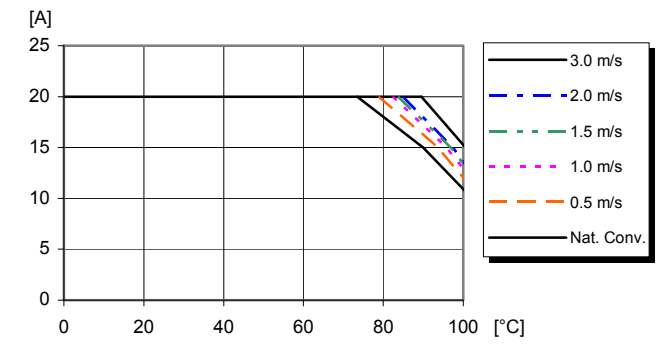

Available load current vs. ambient air temperature and airflow at $V_O$ = 0.6 V, $V_I$ = 12 V. See Thermal Consideration section.

### Output Current Derating, $V_O$ = 1.0 V



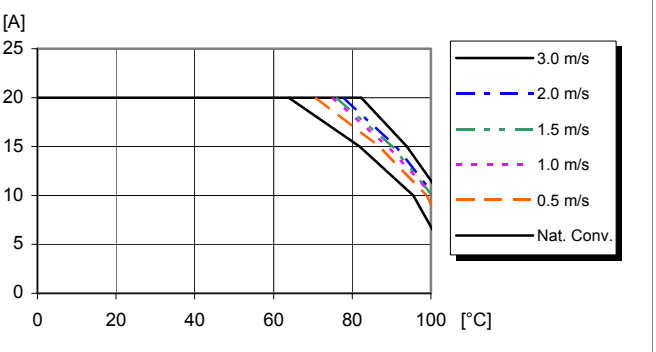

Available load current vs. ambient air temperature and airflow at $V_O$ = 1.0 V, $V_I$ = 12 V. See Thermal Consideration section.

### Output Current Derating, $V_O$ = 1.8 V



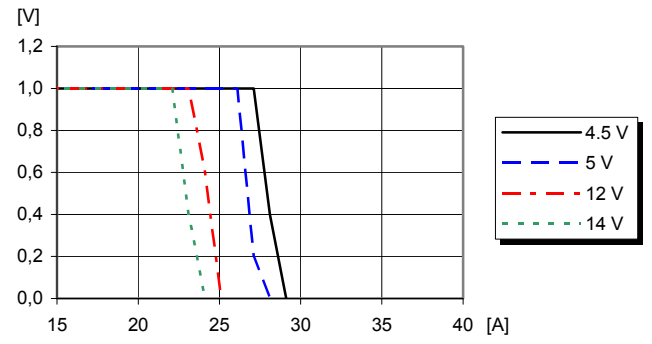

Available load current vs. ambient air temperature and airflow at $V_O$ = 1.8 V, $V_I$ = 12 V. See Thermal Consideration section.

### Output Current Derating, $V_O$ = 3.3 V



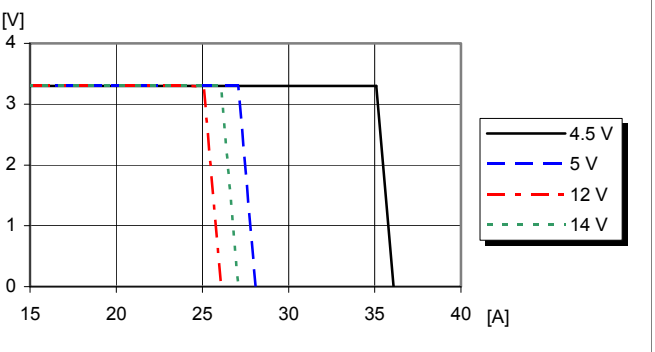

Available load current vs. ambient air temperature and airflow at $V_O$ = 3.3 V, $V_I$ = 12 V. See Thermal Consideration section.

### Current Limit Characteristics, $V_O$ = 1.0 V




Output voltage vs. load current at $T_{P1}$ = +25°C.

### Current Limit Characteristics, $V_O$ = 3.3 V

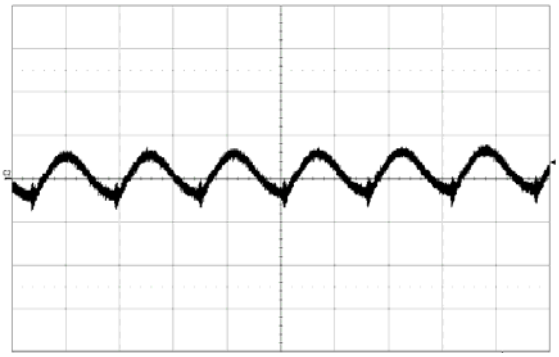



Output voltage vs. load current at $T_{P1}$ = +25°C.

## Typical Characteristics
## Output Voltage

**BMR 463**

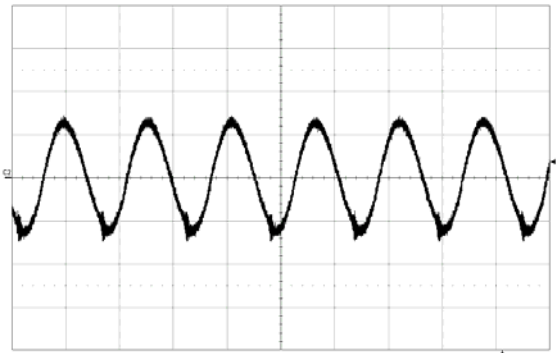
### Output Ripple & Noise, $V_O$ = 1.0 V



Output voltage ripple at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $C_O$ = 470 µF,
$I_O$ = 20 A resistive load.
Default Configuration.

Trace: output voltage (20 mV/div.).
Time scale: (2 µs/div.).

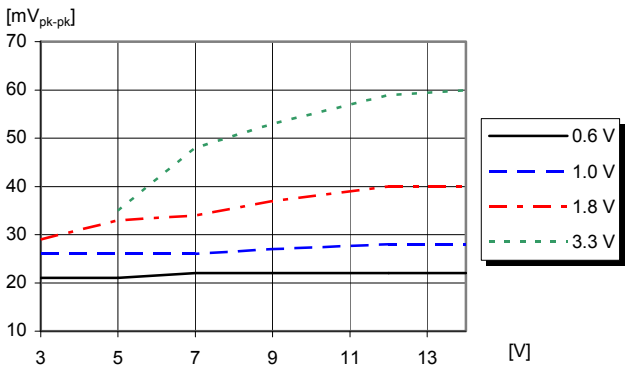
### Output Ripple & Noise, $V_O$ = 3.3 V



Output voltage ripple at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $C_O$ = 470 µF,
$I_O$ = 20 A resistive load.
Default Configuration.

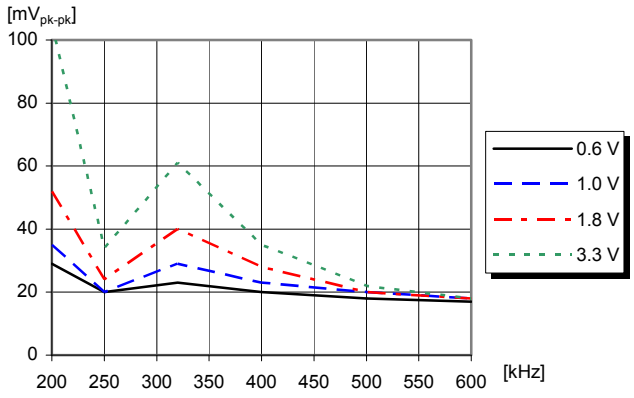
Trace: output voltage (20 mV/div.).
Time scale: (2 µs/div.).

### Output Ripple vs. Input Voltage



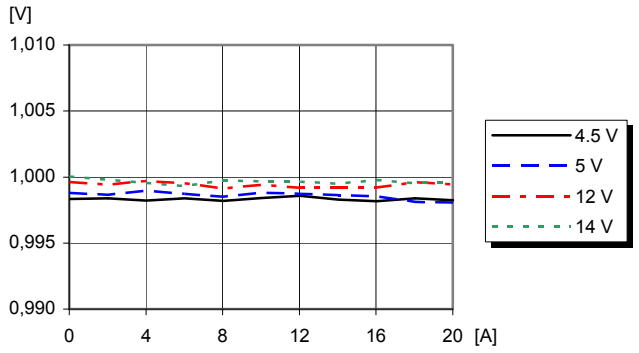

Output voltage ripple $V_{pk-pk}$ at: $T_{P1}$ = +25°C, $C_O$ = 470 µF, $I_O$ = 20 A resistive load.
Default Configuration.

### Output Ripple vs. Frequency



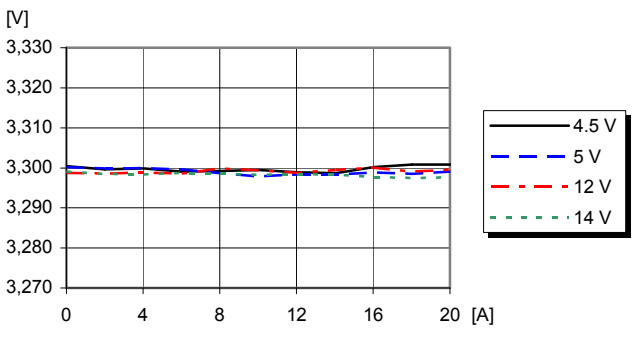

Output voltage ripple $V_{pk-pk}$ at: $T_{P1}$ = +25°C, $V_I$ = 12 V, $C_O$ = 470 µF, $I_O$ = 20 A resistive load.
Default Configuration.

### Load regulation, $V_O$ = 1.0 V




Load regulation at $V_o$=1.0 V at: $T_{P1}$ = +25°C, $C_O$ = 470 µF.

### Load regulation, $V_O$ = 3.3 V

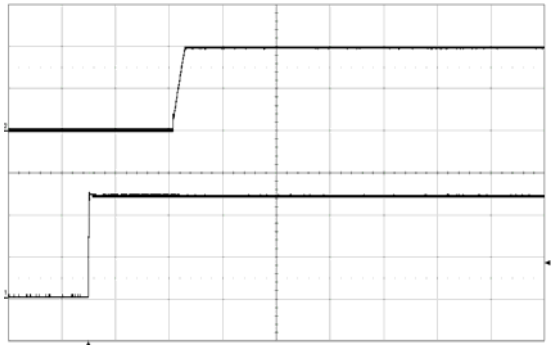



Load regulation at $V_o$=3.3 V at: $T_{P1}$ = +25°C, $C_O$ = 470 µF.

## Typical Characteristics
## Start-up and shut-down

**BMR 463**

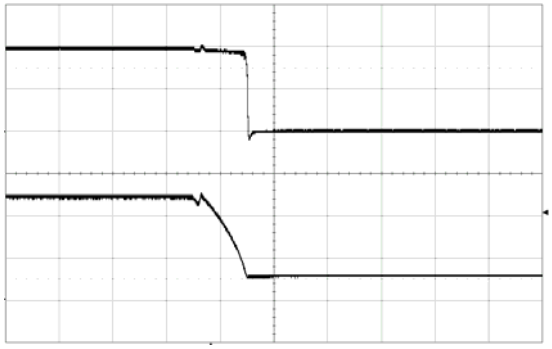
### Start-up by input source



Start-up enabled by connecting $V_I$ at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $V_O$ = 1.0 V
$C_O$ = 470 µF, $I_O$ = 20 A resistive load.
Default Configuration

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

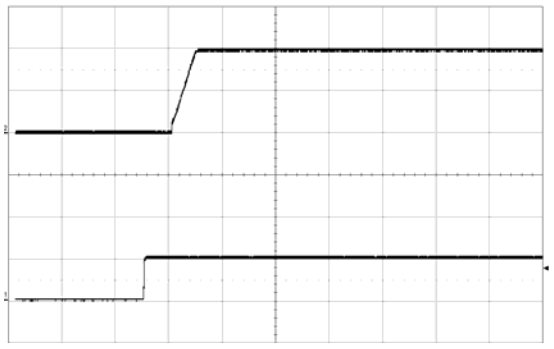
### Shut-down by input source



Shut-down enabled by disconnecting $V_I$ at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $V_O$ = 1.0 V
$C_O$ = 470 µF, $I_O$ = 20 A resistive load.
Default Configuration

Top trace: output voltage (0.5 V/div).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

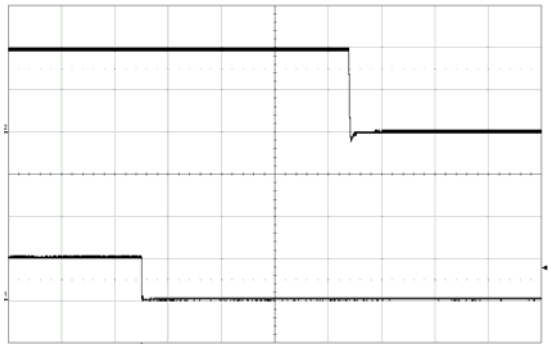
### Start-up by CTRL signal



Start-up by enabling CTRL signal at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $V_O$ = 1.0 V
$C_O$ = 470 µF, $I_O$ = 20 A resistive load.
Default Configuration

Top trace: output voltage (0.5 V/div.).
Bottom trace: input voltage (5 V/div.).
Time scale: (20 ms/div.).

### Shut-down by CTRL signal



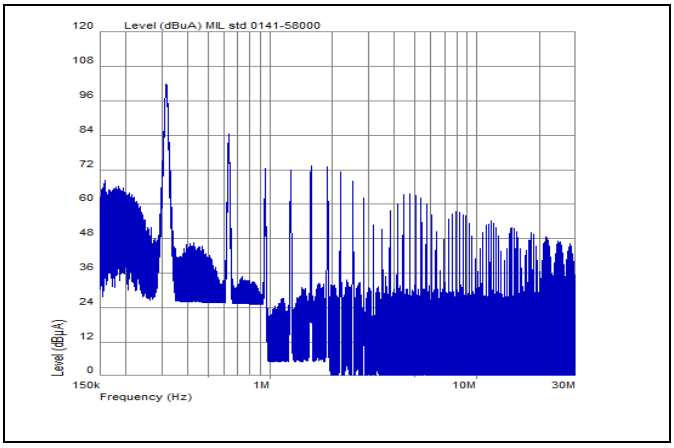
Shut-down enabled by disconnecting $V_I$ at:
$T_{P1}$ = +25°C, $V_I$ = 12 V, $V_O$ = 1.0 V
$C_O$ = 470 µF, $I_O$ = 20 A resistive load.
Default Configuration.

Top trace: output voltage (0.5 V/div).
Bottom trace: input voltage (5 V/div.).
Time scale: (2 ms/div.).

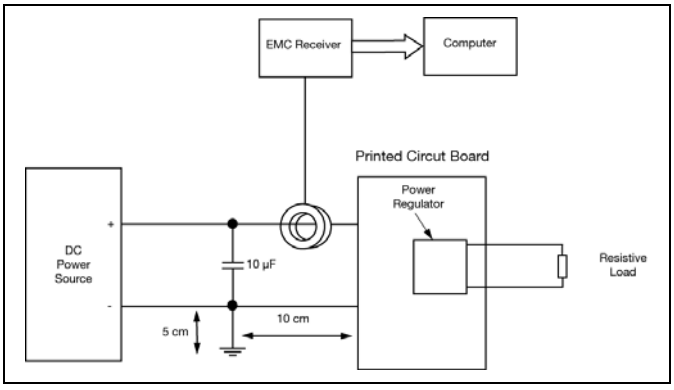
## EMC Specification

Conducted EMI measured according to test set-up and standard MIL std 0141 - 58000.
The fundamental switching frequency is 320 kHz for BMR463 at $V_I$ = 12.0 V, max $I_O$.

**Conducted EMI** Input terminal value (typ)




*EMI without filter*



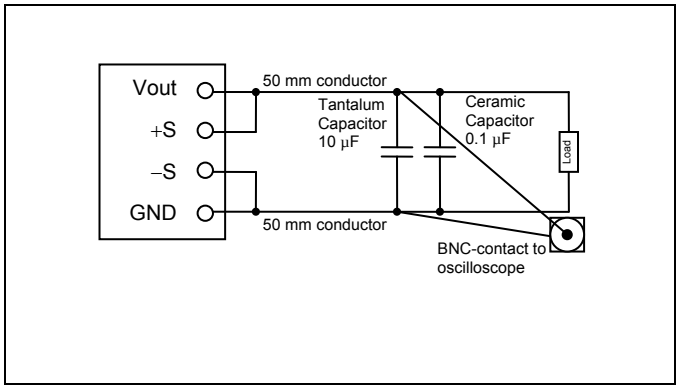

*Test set-up*

### Layout Recommendations

The radiated EMI performance of the product will depend on the PWB layout and ground layer design. It is also important to consider the stand-off of the product. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.
A ground layer will increase the stray capacitance in the PWB and improve the high frequency EMC performance.

### Output Ripple and Noise

Output ripple and noise measured according to figure below.
A 50 mm conductor works as a small inductor forming together with the two capacitances a damped filter.




*Output ripple and noise test set-up. Additional $C_O$ = 470 µF was added close to the output pins.*

## Operating information

### Power Management Overview

This product is equipped with a PMBus interface. The product incorporates a wide range of readable and configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults. A fault is also shown as an alert on the SALERT pin. The following product parameters can continuously be monitored by a host: Input voltage, output voltage/current, and internal temperature. If the monitoring is not needed it can be disabled and the product enters a low power mode reducing the power consumption. The protection features are not affected.

The product is delivered with a default configuration suitable for a wide range operation in terms of input voltage, output voltage, and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface. Please contact your local Ericsson Power Modules representative for design support of custom configurations or appropriate SW tools for design and down-load of your own configurations.

### Input Voltage

The input voltage range, 4.5 - 14 V, makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter. See Ordering Information for input voltage range.

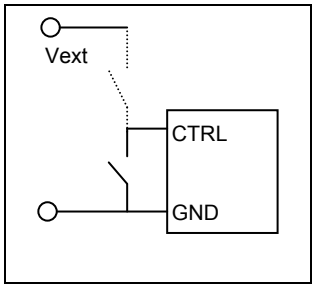
**Input Under Voltage Lockout, UVLO**

The product monitors the input voltage and will turn-on and turn-off at configured levels. The default turn-on input voltage level setting is 4.20 V, whereas the corresponding turn-off input voltage level is 3.85 V. Hence, the default hysteresis between turn-on and turn-off input voltage is 0.35 V. Once an input turn-off condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption. The unit will continue to operate as long as the input voltage can be supported. If the input voltage continues to fall, there will come a point where the unit will cease to operate.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a turn-off is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the product will be re-enabled. The turn-on and turn-off levels and response can be reconfigured using the PMBus interface.

**Remote Control**




The product is equipped with a remote control function, i.e., the CTRL pin. The remote control can be connected to either the primary negative input connection (GND) or an external voltage (Vext), which is a 3 - 5 V positive supply voltage in accordance to the SMBus Specification version 2.0.

The CTRL function allows the product to be turned on/off by an external device like a semiconductor or mechanical switch. By default the product will turn on when the CTRL pin is left open and turn off when the CTRL pin is applied to GND. The CTRL pin has an internal pull-up resistor. The maximum required sink current is 0.5 mA. When the CTRL pin is left open, the voltage generated on the CTRL pin is max 6 V.
The product can also be configured using the PMBus interface to be “Always on”, i.e., starts immediately when an appropriate input voltage is applied, or turn on/off can be performed with PMBus commands.

**Input and Output Impedance**

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. The performance in some applications can be enhanced by addition of external capacitance as described under External Decoupling Capacitors. If the input voltage source contains significant inductance, the addition a capacitor with low ESR at the input of the product will ensure stable operation.

**External Decoupling Capacitors**

Input capacitors:
The input ripple RMS current in a buck converter is equal to

Eq. 1. $I_{inputRMS} = I_{load}\sqrt{D(1-D)}$ ,

where $I_{load}$ is the output load current and $D$ is the duty cycle. The maximum load ripple current becomes $I_{load}/2$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor, and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors. A minimum capacitance of 300 µF with low ESR is recommended. The ripple current rating of the capacitors must follow Eq. 1. For high-performance/transient applications or wherever the input source performance is degraded, additional low ESR ceramic type capacitors at the input is recommended. The additional input low ESR capacitance above the minimum level insures an optimized performance.

Output capacitors:
When powering loads with significant dynamic current requirements, the voltage regulation at the point of load can be improved by addition of decoupling capacitors at the load. The most effective technique is to locate low ESR ceramic and electrolytic capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. The ceramic capacitors will handle high-frequency dynamic load changes while the electrolytic capacitors are used to handle low frequency dynamic load changes. Ceramic capacitors will also reduce high frequency noise at the load.
It is equally important to use low resistance and low inductance PWB layouts and cabling.
External decoupling capacitors are a part of the control loop of the product and may affect the stability margins.
Stable operation is guaranteed for the following total capacitance $C_O$ in the output decoupling capacitor bank where

Eq. 2. $C_O = [C_{\min}, C_{\max}] = [300, 15000]$ µF.

The decoupling capacitor bank should consist of capacitors which has a capacitance value larger than $C \geq C_{\min}$ and has an $ESR$ range of

Eq. 3. $ESR = [ESR_{\min}, ESR_{\max}] = [5, 30]$ mΩ

The control loop stability margins are limited by the minimum time constant $\tau_{\min}$ of the capacitors. Hence, the time constant of the capacitors should follow Eq. 4.

Eq. 4. $\tau \geq \tau_{min} = C_{min} ESR_{min} = 1.5\ \mu s$

This relation can be used if your preferred capacitors have parameters outside the above stated ranges in Eq. 2 and Eq.3.

- If the capacitors capacitance value is $C < C_{min}$ one must use at least $N$ capacitors where
  $N \geq \left\lceil \frac{C_{min}}{C} \right\rceil$ and $ESR \geq ESR_{min} \frac{C_{min}}{C}$.
- If the ESR value is $ESR > ESR_{max}$ one must use at least $N$ capacitors of that type where
  $N \geq \left\lceil \frac{ESR}{ESR_{max}} \right\rceil$ and $C \geq \frac{C_{min}}{N}$.
- If the $ESR$ value is $ESR < ESR_{min}$ the capacitance value should be
  $C \geq C_{min} \frac{ESR_{min}}{ESR}$.

For a total capacitance outside the above stated range or capacitors that do not follow the stated above requirements above a re-design of the control loop parameters will be necessary for robust dynamic operation and stability.

### Control Loop Compensation

The product is configured with a robust control loop compensation which allows for a wide range operation of input and output voltages and capacitive loads as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the control loop can be optimized for a robust and stable operation and with an improved load transient response. This optimization will minimize the amount of required output decoupling capacitors for a given load transient requirement yielding an optimized cost and minimized board space. The control loop parameters can be reconfigured using the PMBus interface.

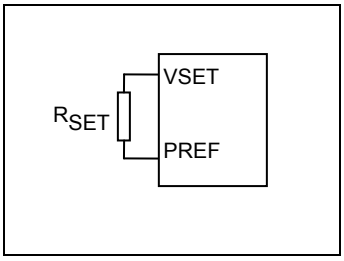
### Load Transient Response Optimization

The product incorporates a Non-Linear transient Response, NLR, loop that decreases the response time and the output voltage deviation during a load transient. The NLR results in a higher equivalent loop bandwidth than is possible using a traditional linear control loop. The product is pre-configured with appropriate NLR settings for robust and stable operation for a wide range of input voltage and a capacitive load range as defined in the section External Decoupling Capacitors. For an application with a specific input voltage, output voltage, and capacitive load, the NLR configuration can be optimized for a robust and stable operation and with an improved load transient response. This will also reduce the amount of output decoupling capacitors and yield a reduced cost. However, the NLR reduces the energy efficiency. In order to obtain maximal energy efficiency the load transient requirement has to be met by the standard control loop compensation and the decoupling capacitors. The NLR settings can be reconfigured using the PMBus interface.

### Remote Sense

The product has remote sense that can be used to compensate for voltage drops between the output and the point of load. The sense traces should be located close to the PWB ground layer to reduce noise susceptibility. The remote sense circuitry will compensate for up to 0.3 V voltage drop between output pins and the point of load. If the remote sense is not needed +S should be connected to VOUT and −S should be connected to GND.

### Output Voltage Adjust using Pin-strap Resistor




Using an external Pin-strap resistor, $R_{SET}$, the output voltage can be set in the range 0.6 V to 3.3 V at 28 different levels shown in the table below. The resistor should be applied between the VSET pin and the PREF pin.

$R_{SET}$ also sets the maximum output voltage, see section Limiting the maximum output voltage. The resistor is sensed only during product boot-up. Changing the resistor value during normal operation will not change the output voltage. The input voltage must be at least 1 V larger than the output voltage in order to deliver the correct output voltage. See Ordering Information for output voltage range.

The following table shows recommended resistor values for $R_{SET}$ (1% tolerance resistors suggested).

| $V_{OUT}$ [V] | $R_{SET}$[kΩ] | $V_{OUT}$ [V] | $R_{SET}$[kΩ] |
|---|---|---|---|
| 0.60 | 10 | 1.50 | 46.4 |
| 0.65 | 11 | 1.60 | 51.1 |
| 0.70 | 12.1 | 1.70 | 56.2 |
| 0.75 | 13.3 | 1.80 | 61.9 |
| 0.80 | 14.7 | 1.90 | 68.1 |
| 0.85 | 16.2 | 2.00 | 75 |
| 0.90 | 17.8 | 2.10 | 82.5 |
| 0.95 | 19.6 | 2.20 | 90.9 |
| 1.00 | 21.5 | 2.30 | 100 |
| 1.05 | 23.7 | 2.50 | 110 |
| 1.10 | 26.1 | 3.00 | 121 |
| 1.15 | 28.7 | 3.30 | 133 |
| 1.20 | 31.6 | | |
| 1.25 | 34.8 | | |
| 1.30 | 38.3 | | |
| 1.40 | 42.2 | | |

The output voltage and the maximum output voltage can be pin strapped to three fixed values by connecting the VSET pin according to the table below.

| $V_{OUT}$ [V] | VSET |
|---|---|
| 0.60 | Shorted to PREF |
| 1.2 | Open "high impedance" |
| 2.5 | Logic High, GND as reference |

### Output Voltage Adjust using PMBus

The output voltage of the product can be configured using the PMBus interface in the range 0.54 to 3.63. See Ordering Information for output voltage range.

### Limiting the maximum output voltage

The product can be configured for maximum output voltage protection. The output voltage pin-strap resistor $R_{SET}$ also sets the maximum output voltage equal to 110% of the nominal output value, $V_{OUTMAX} = 1.1 \times V_{OUT}$. A PMBus command can not set the nominal output voltage higher than $V_{OUTMAX}$. This protects the load from an over voltage due to an accidental wrong PMBus command.

### Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. If the output voltage exceeds the OVP limit, the product can respond in different ways:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart, i.e. the output voltage is pulled to ground level (crowbar function).

The default response from an overvoltage fault is to immediately shut down as in 2. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled. For continuous OVP when operating from an external clock for synchronization, the only allowed response is an immediate shutdown. The OVP limit and fault response can be reconfigured using the PMBus interface.

### Under Voltage Protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. The UVP limit can be reconfigured using the PMBus interface.

### Power Good

The product provides a Power Good (PG) signal as a flag in the Status Word register that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG signal will be asserted if the output is within -10%/+15% of the target voltage. These limits may be changed via the PMBus interface. A PG delay period is defined as the time from when all conditions within the product for asserting PG are met to when the PG signal is actually asserted. By default, the PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10 ms, the PG delay will be set to 10 ms. The PG delay may be set independently of the soft-start ramp using the PMBus interface.

### Switching Frequency

The fundamental switching frequency $f_{PROG}$ is 320 kHz, which yields optimal power efficiency. The switching frequency can be set to any value between 200 kHz and 640 kHz using the PMBus interface. The switching frequency will change the efficiency/power dissipation, load transient response and output ripple. For optimal control loop performance the control loop must be re-designed when changing the switching frequency.

### Synchronization

Synchronization is a feature that allows multiple products to be synchronized to a common frequency. Synchronized products powered from the same bus eliminate beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. Eliminating the slow beat frequencies (usually <10 kHz) allows the EMI filter to be designed to attenuate only the synchronization frequency. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.
The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC Output working as a master driving the synchronization. All others on the same synchronization bus should be configured with SYNC Input or SYNC Auto Detect (Default configuration) for correct operation. When the SYNC pin is configured in auto detect mode the product will automatically check for a clock signal on the SYNC pin.

### Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and efficiency losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized. Up to 16 different phases can be used.
The phase spreading of the product can be configured using the PMBus interface.

### Parallel Operation (Current Sharing)

Paralleling multiple products can be used to increase the output current capability of a single power rail. By connecting the GCB pins of each device and configuring the devices as a current sharing rail, the units will share the current equally within a few percent. Enabling up to 100% utilization of the current capability for each device in the current sharing rail. The product uses a low-bandwidth, first-order digital current sharing technique to balance the unequal device output

loading by aligning the load lines of slave devices to a master device. Artificial droop resistance is added to the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PWB layout. Up to 8 devices can be configured in a given current sharing group.

During periods of light loading, it may be beneficial to disable one or more phases in order to eliminate the current drain and switching losses associated with those phases, resulting in higher efficiency. The product offers the ability to add and drop phases using a PMBus command in response to an observed load current change. All phases in a current share rail are considered active prior to the current sharing rail ramp to power-good. Phases can be dropped after power-good is reached. Any member of the current sharing rail can be dropped. If the reference device is dropped, the remaining active device with the lowest member position will become the new reference. Additionally, any change to the number of members of a current sharing rail will precipitate autonomous phase distribution within the rail where all active phases realign their phase position based on their order within the number of active members. If the members of a current sharing rail are forced to shut down due to an observed fault, all members of the rail will attempt to re-start simultaneously after the fault has cleared.

**Adaptive Diode Emulation**

Most power converters use synchronous rectification to optimize efficiency over a wide range of input and output conditions. However, at light loads the synchronous MOSFET will typically sink current and introduce additional energy losses associated with higher peak inductor currents, resulting in reduced efficiency. Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is not available for current sharing groups. Note: the overall bandwidth of the product may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps. The diode emulation mode can be configured using the PMBus interface.

**Adaptive Frequency and Pulse Skip Control**

Since switching losses contribute to the efficiency of the power converter, reducing the switching frequency will reduce the switching losses and increase efficiency. The product includes an Adaptive Frequency Control mode, which effectively reduces the observed switching frequency as the load decreases. Adaptive frequency mode is only available while the device is operating within Adaptive Diode Emulation Mode. As the load current is decreased, diode emulation mode decreases the Synch-FET on-time to prevent negative inductor current from flowing. As the load is decreased further, the Switch-FET pulse width will begin to decrease while maintaining the programmed frequency, $f_{PROG}$ (set by the FREQ_SWITCH command). Once the Switch-FET pulse width (D) reaches 50% of the nominal duty cycle, $D_{NOM}$ (determined by $V_I$ and $V_O$), the switching frequency will start to decrease according to the following equation:

Eq. 5. $$f_{sw} = D\left(\frac{2(f_{PROG} - f_{MIN})}{D_{NOM}}\right) + f_{MIN}\ .$$

Disabling a minimum Synch-FET makes the product also pulse skip which reduces the power loss further.
It should be noted that adaptive frequency mode is not available for current sharing groups and is not allowed when the device is placed in auto-detect mode and a clock source is present on the SYNC pin, or if the device is outputting a clock signal on its SYNC pin. The adaptive frequency and pulse skip modes can be configured using the PMBus interface.

**Efficiency Optimized Dead Time Control**

The product utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the switch and synch FETs. The algorithm constantly adjusts the deadtime non-overlap to minimize the duty cycle, thus maximizing efficiency. This algorithm will null out deadtime differences due to component variation, temperature and loading effects. The algorithm can be configured via the PMBus interface.

**Over Current Protection (OCP)**

The product includes current limiting circuitry for protection at continuous overload. The following OCP response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the product).
5. Initiate an immediate shutdown.

The default response from an over current fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled.The load distribution should be designed for the maximum output short circuit current specified. The OCP limit and response of the product can be reconfigured using the PMBus interface.

Note.
When the ratioVo/Vi is higher than 0.66 (e.g. Vi = 4.5 V and Vo = 3.3 V), and with the current sense configuration according to factory default, the current limit threshold will be above specified maximum value. To achieve the specified current limit threshold, the current sense configuration should be changed to "up slope sensing". This is configured by using the PMBus interface.

**Soft-start Power Up**

The soft-start control introduces a time-delay (default setting 10 ms) before allowing the output voltage to rise. The default rise time of the ramp up is 10 ms. Power-up is hence completed within 20 ms in default configuration using remote control. When starting by applying input voltage the control circuit boot-up time adds an additional ~25 ms delay. The soft-start power up of the product can be reconfigured using the PMBus interface.

**Output Voltage Sequencing**

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another. Multi-product sequencing can be achieved by configuring the start delay and rise time of each device through the PMBus interface and by using the CTRL start signal.

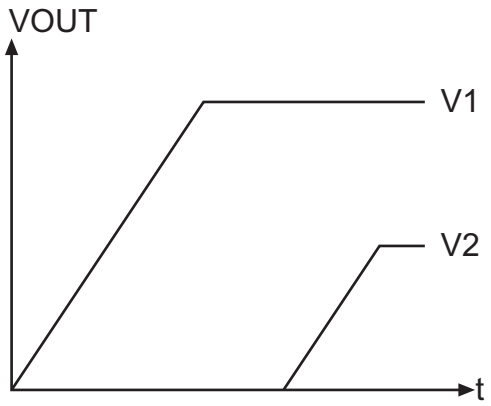



*Illustration of Output Voltage Sequencing.*

**Voltage Tracking**

The product integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. During ramp-up, the output voltage follows the VTRK voltage until the preset output voltage level is met. The product offers two modes of tracking as follows:

1. Coincident. This mode configures the product to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

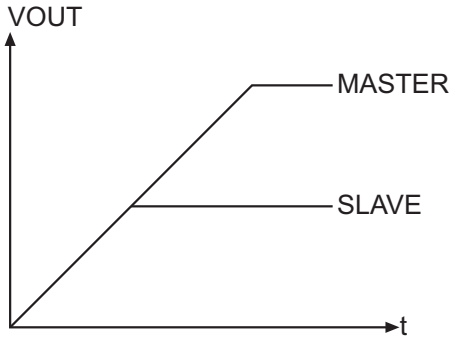



*Illustration of Coincident Voltage Tracking.*

2. Ratiometric. This mode configures the product to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but a different tracking ratio may be set by an external resistive voltage divider or through the PMBus interface.

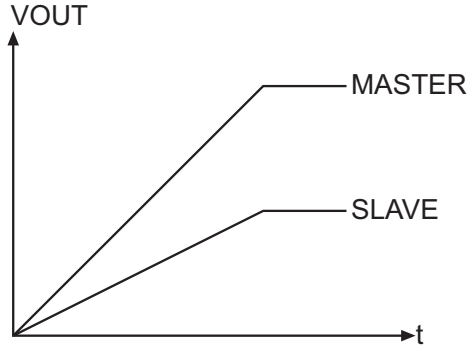



*Illustration of Ratiometric Voltage Tracking*

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. All of the CTRL pins in the tracking group must be connected and driven by a single logic source. It should be noted that current sharing groups that are also configured to track another voltage do not offer pre-bias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside force.

**Voltage Margining Up/Down**

The product can adjust its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit over its supply margin or range. It can also be used to verify the function of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus interface to as high as 10% or as low as 0 V.

**Pre-Bias Startup Capability**

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. The BMR463 product family incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition. Pre-bias protection is not offered for current sharing groups that also have voltage tracking enabled.

**Group Communication Bus**

The Group Communication Bus, GCB bus, is used to communicate between products. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The GCB bus solves the PMBus data rate limitation. The GCB pin on all devices in an application should be connected. A pull-up resistor is required on the GCB bus order to guarantee the rise time as follows:

Eq. 6 $\tau = R_{GCB} C_{GCB} = 1\mu s$ ,

where $R_{GCB}$ is the pull up resistor value and $C_{GCB}$ is the bus loading. The pull-up resistor should be tied to to an external 3.3 V or 5 V supply voltage, which should be present prior to or during power-up.

**Fault spreading**

The product can be configured to broadcast a fault event over the GCB bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the GCB bus. The other devices on the GCB bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

**Over Temperature Protection (OTP)**

The products are protected from thermal overload by an internal over temperature shutdown circuit. When $T_{P1}$ as defined in thermal consideration section exceeds 120°C the product will shut down. The product will make continuous attempts to start up and resume normal operation automatically when the temperature has dropped >15°C below the temperature threshold. The OTP level, hysteresis, and fault response of the product can be reconfigured using the PMBus interface. The fault response can be configured as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts (default configuration).
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

## Thermal Consideration

**General**

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation.
Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependant on the airflow across the product. Increased airflow enhances the cooling of the product.
The Output Current Derating graph found in the Output section for each model provides the available output current vs. ambient air temperature and air velocity at specified $V_I$.

The products with an output power $\geq 100$ W are tested on a 254 x 254 mm, 35 µm (1 oz), 16-layer test board, and for output power $< 100$ W a 254 x 254 mm, 35 µm (1 oz), 8-layer test board is used. The test board is mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm.

Proper cooling of the product can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions should not exceed the max values provided in the table below.

Note that the max value is the absolute maximum rating (non destruction) and that the electrical Output data is guaranteed up to $T_{P1}$ +85°C.

See Design Note 019 for further information.

**BMR 463 series** POL Regulators
Input 4.5-14 V, Output up to 20 A / 66 W

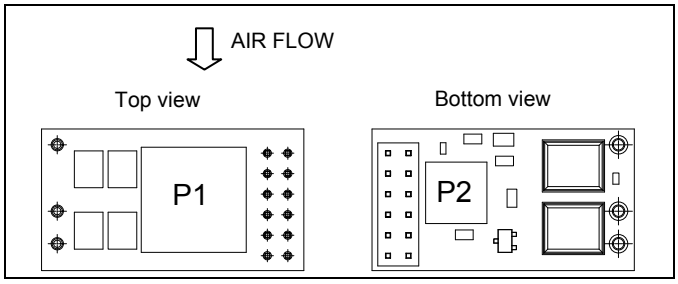
EN/LZT 146 434 R1A January 2011



### Definition of product operating temperature

The product operating temperatures are used to monitor the temperature of the product, and proper thermal conditions can be verified by measuring the temperature at positions P1 and P2. The temperature at these positions ($T_{P1}$, $T_{P2}$) should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperatures above maximum $T_{P1}$, measured at the reference point P1 are not allowed and may cause permanent damage.

| Position | Description | Max Temp. |
|---|---|---|
| P1 | Reference point, L1, inductor | 120º C |
| P2 | N1, control circuit | 120º C |

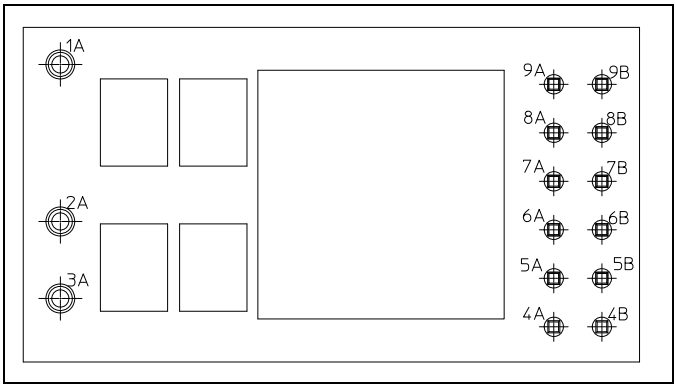



*Temperature positions and air flow direction.*

### Definition of reference temperature $T_{P1}$

The reference temperature is used to monitor the temperature limits of the product. Temperature above maximum $T_{P1}$, measured at the reference point P1 is not allowed and may cause degradation or permanent damage to the product. $T_{P1}$ is also used to define the temperature range for normal operating conditions. $T_{P1}$ is defined by the design and used to guarantee safety margins, proper operation and high reliability ot the product.

### Connections



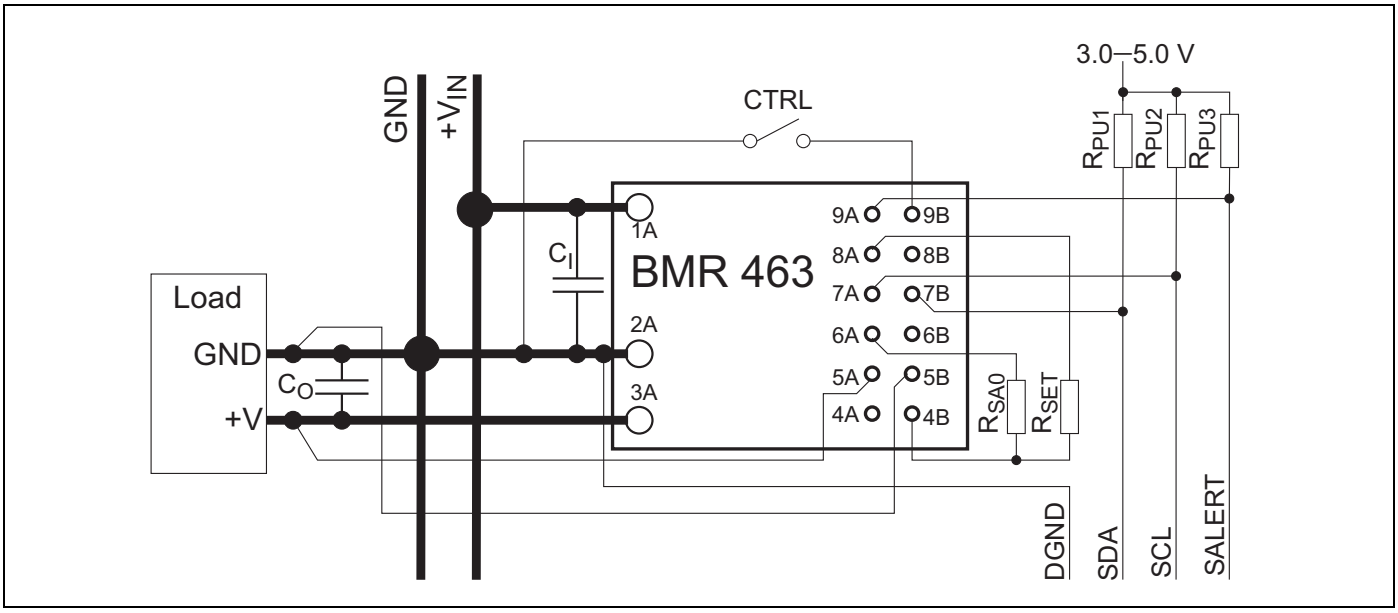

*Pin layout, top view.*

| Pin | Designation | Function |
|---|---|---|
| 1A | VIN | Input Voltage |
| 2A | GND | Power Ground |
| 3A | VOUT | Output Voltage |
| 4A | VTRK | Voltage Tracking input |
| 4B | PREF | Pin-strap reference |
| 5A | +S | Positive sense |
| 5B | −S | Negative sense |
| 6A | SA0 | PMBus address pinstrap |
| 6B | GCB | Group Communication Bus |
| 7A | SCL | PMBus Clock |
| 7B | SDA | PMBus Data |
| 8A | VSET | Output voltage pinstrap |
| 8B | SYNC | Synchronization I/O |
| 9A | SALERT | PMBus Alert |
| 9B | CTRL | Remote Control |

### PWB layout considerations

The pinstrap resistors, Rset, and $R_{SA0}$ should be placed as close to the product as possible to minimize loops that may pick up noise.
Avoid current carrying planes under the pinstrap resistors and the PMBus signals.
The capacitor $C_I$ (or capacitors implementing it) should be placed as close to the input pins as possible.
Capacitor $C_O$ (or capacitors implementing it) should be placed close to the load.

**Typical Application Circuit**




*Standalone with PMBus communication*

### PMBus Interface

This product provides a PMBus digital interface that enables the user to configure many aspects of the device operation as well as to monitor the input and output voltages, output current and device temperature. The product can be used with any standard two-wire $I^2C$ or SMBus host device. In addition, the module is compatible with PMBus version 1.1 and includes an SALERT line to help mitigate bandwidth limitations related to continuous fault monitoring. The product supports both 100 kHz and 400 kHz bus clock frequency. The PMBus signals, SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors is required to guarantee the rise time as follows:

Eq. 7 $\tau = R_P C_p = 1\mu s$

where $R_p$ is the pull-up resistor value and $C_p$ is the bus loading, the maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external 3.0 to 5.0 V ±10% supply voltage, which should be present prior to or during power-up.

### Monitoring via PMBus

It is possible to monitor a wide variety of different parameters through the PMBus interface. Fault conditions can be monitored using the SALERT pin, which will be asserted when any number of pre-configured fault or warning conditions occur. It is also possible to continuously monitor one or more of the power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle

### Snap Shot Parameter Capture

This product offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The following parameters are stored:

- Input voltage
- Output voltage
- Output current
- Internal junction temperature
- Switching frequency
- Duty cycle
- Status registers

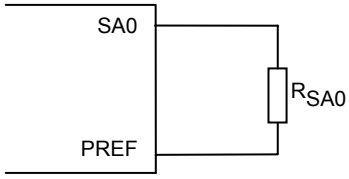
The Snapshot feature enables the user to read the parameters via the PMBus interface during normal operation, although it should be noted that reading the 22 bytes will occupy the bus for some time. The Snapshot enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Automatic store to Flash memory following a fault is triggered when any fault threshold level is exceeded, provided that the specific fault response is to shut down. Writing to Flash memory is not allowed if the device is configured to re-try following the specific fault condition. It should also be noted that the device supply voltage must be maintained during the time the device is writing data to Flash memory; a process that requires between 700-1400 µs depending on whether the data is set up for a block write. Undesirable results may be observed if the input voltage of the modules drops below 3.0 V during this process

### Software Tools for Design and Production

Ericsson provides software for configuration and monitoring of this product via the PMBus interface.
For more information please contact your local Ericsson sales representative.

### PMBus addressing

The PMBus address should be configured with a resistor connected between the SA0 pin and the PREF pin, as shown in the figure below. Recommended resistor values for hard-wiring PMBus addresses (series E96, 1% tolerance resistors suggested) are shown in the table.




*Schematic of connection of address resistor.*

| Index | $R_{SA0}$ [kΩ] | Index | $R_{SA0}$ [kΩ] |
|---|---|---|---|
| 0 | 10 | 13 | 34.8 |
| 1 | 11 | 14 | 38.3 |
| 2 | 12.1 | 15 | 42.2 |
| 3 | 13.3 | 16 | 46.4 |
| 4 | 14.7 | 17 | 51.1 |
| 5 | 16.2 | 18 | 56.2 |
| 6 | 17.8 | 19 | 61.9 |
| 7 | 19.6 | 20 | 68.1 |
| 8 | 21.5 | 21 | 75 |
| 9 | 23.7 | 22 | 82.5 |
| 10 | 26.1 | 23 | 90.9 |
| 11 | 28.7 | 24 | 100 |
| 12 | 31.6 | | |

The PMBus address follows the equation below:

Eq. 8 PMBus Address (decimal) = 75 + Index

This allows the use of 25 different PMBus addresses, yielding the decimal address range of 0d$[75,K,99]$. However, the address 0d75 is allocated for production needs and can not be used. If more than 24 devices of this type are required on the same PMBus another adress range is required. See Ordering Information for different PMBus address ranges. The user shall also be aware of further limitations of the address space as stated in the SMBus Specification.

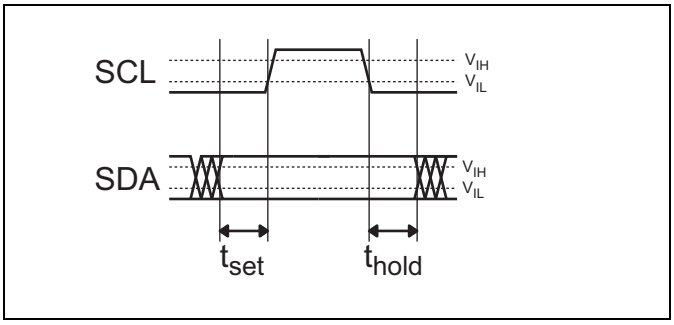
**Optional PMBus Addressing**

The address space is increased by connecting the SA0 pin according to the following table.

| SA0 $R_{SA0}$ [kΩ] | Address |
|---|---|
| Shorted to PREF | 0d33 |
| Open “high impedance” | 0d36 |
| Logic High, GND as reference | 0d39 |

*Logic High definitions see Electrical Specification*

**I²C/SMBus Setup and Hold Times – Definitions**




*SMBus timing diagram*

The setup time, $t_{set}$, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time $t_{hold}$, is the time data must be stable after the rising edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail.

### PMBus Commands

The product is PMBus compliant. The following table lists the implemented PMBus commands. For more detailed information see PMBus Power System Management Protocol Specification; Part I – General Requirements, Transport and Electrical Interface and PMBus Power System Management Protocol; Part II – Command Language.

| Designation | Cmd | Impl |
|---|---|---|
| **Standard PMBus Commands** | | |
| Control Commands | | |
| PAGE | 00h | No |
| OPERATION | 01h | Yes |
| ON_OFF_CONFIG | 02h | Yes |
| WRITE_PROTECT | 10h | No |
| Output Commands | | |
| VOUT_MODE (Read Only) | 20h | Yes |
| VOUT_COMMAND | 21h | Yes |
| VOUT_TRIM | 22h | Yes |
| VOUT_CAL_OFFSET | 23h | Yes |
| VOUT_MAX | 24h | Yes |
| VOUT_MARGIN_HIGH | 25h | Yes |
| VOUT_MARGIN_LOW | 26h | Yes |
| VOUT_TRANSITION_RATE | 27h | Yes |
| VOUT_DROOP | 28h | Yes |
| MAX_DUTY | 32h | Yes |
| FREQUENCY_SWITCH | 33h | Yes |
| IOUT_CAL_GAIN | 38h | Yes |
| IOUT_CAL_OFFSET | 39h | Yes |
| VOUT_SCALE_LOOP | 29h | No |
| VOUT_SCALE_MONITOR | 2Ah | No |
| COEFFICIENTS | 30h | No |
| Fault Limit Commands | | |
| POWER_GOOD_ON | 5Eh | Yes |
| VOUT_OV_FAULT_LIMIT | 40h | Yes |
| VOUT_UV_FAULT_LIMIT | 44h | Yes |
| IOUT_OC_FAULT_LIMIT | 46h | Yes |
| IOUT_UC_FAULT_LIMIT | 4Bh | Yes |
| OT_FAULT_LIMIT | 4Fh | Yes |
| OT_WARN_LIMIT | 51h | Yes |
| UT_WARN_LIMIT | 52h | Yes |
| UT_FAULT_LIMIT | 53h | Yes |
| VIN_OV_FAULT_LIMIT | 55h | Yes |
| VIN_OV_WARN_LIMIT | 57h | Yes |
| VIN_UV_WARN_LIMIT | 58h | Yes |
| VIN_UV_FAULT_LIMIT | 59h | Yes |
| VOUT_OV_WARN_LIMIT | 42h | No |
| VOUT_UV_WARN_LIMIT | 43h | No |
| IOUT_OC_WARN_LIMIT | 4Ah | No |
| Fault Response Commands | | |
| VOUT_OV_FAULT_RESPONSE | 41h | Yes |
| VOUT_UV_FAULT_RESPONSE | 45h | Yes |
| OT_FAULT_RESPONSE | 50h | Yes |
| UT_FAULT_RESPONSE | 54h | Yes |
| VIN_OV_FAULT_RESPONSE | 56h | Yes |
| VIN_UV_FAULT_RESPONSE | 5Ah | Yes |
| IOUT_OC_FAULT_RESPONSE | 47h | No |
| IOUT_UC_FAULT_RESPONSE | 4Ch | No |
| Time setting Commands | | |
| TON_DELAY | 60h | Yes |
| TON_RISE | 61h | Yes |
| TOFF_DELAY | 64h | Yes |
| TOFF_FALL | 65h | Yes |
| TON_MAX_FAULT_LIMIT | 62h | No |
| Status Commands (Read Only) | | |
| CLEAR_FAULTS | 03h | Yes |
| STATUS_BYTE | 78h | Yes |
| STATUS_WORD | 79h | Yes |
| STATUS_VOUT | 7Ah | Yes |
| STATUS_IOUT | 7Bh | Yes |
| STATUS_INPUT | 7Ch | Yes |
| STATUS_TEMPERATURE | 7Dh | Yes |
| STATUS_CML | 7Eh | Yes |
| Monitor Commands (Read Only) | | |
| READ_VIN | 88h | Yes |
| READ_VOUT | 8Bh | Yes |
| READ_IOUT | 8Ch | Yes |
| READ_TEMPERATURE_1 | 8Dh | Yes |
| READ_TEMPERATURE_2 | 8Eh | No |
| READ_FAN_SPEED_1 | 90h | No |
| READ_DUTY_CYCLE | 94h | Yes |
| READ_FREQUENCY | 95h | Yes |
| Identification Commands (Read Only) | | |
| PMBUS_REVISION | 98h | Yes |
| MFR_ID | 99h | Yes |

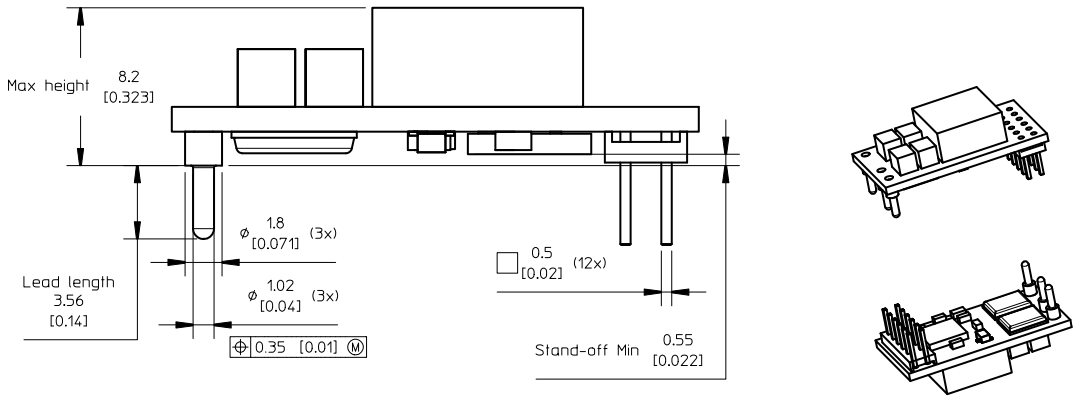
| Designation | Cmd | Impl |
|---|---|---|
| MFR_MODEL | 9Ah | Yes |
| MFR_REVISION | 9Bh | Yes |
| MFR_LOCATION | 9Ch | Yes |
| MFR_DATE | 9Dh | Yes |
| MFR_SERIAL | 9Eh | Yes |
| Group Commands | | |
| INTERLEAVE | 37h | Yes |
| Supervisory Commands | | |
| STORE_DEFAULT_ALL | 11h | Yes |
| RESTORE_DEFAULT_ALL | 12h | Yes |
| STORE_USER_ALL | 15h | No |
| RESTORE_USER_ALL | 16h | No |
| | | |
| **Product Specific Commands** | | |
| Time Setting Commands | | |
| POWER_GOOD_DELAY | D4h | Yes |
| Fault limit Commands | | |
| IOUT_AVG_OC_FAULT_LIMIT | E7h | Yes |
| IOUT_AVG_UC_FAULT_LIMIT | E8h | Yes |
| Fault Response Commands | | |
| MFR_IOUT_OC_FAULT_RESPONSE | E5h | Yes |
| MFR_IOUT_UC_FAULT_RESPONSE | E6h | Yes |
| OVUV_CONFIG | D8h | Yes |
| Configuration and Control Commands | | |
| MFR_CONFIG | D0h | Yes |
| USER_CONFIG | D1h | Yes |
| MISC_CONFIG | E9h | Yes |
| PID_TAPS | D5h | Yes |
| PID_TAPS_ADAPT | F2h | Yes |
| INDUCTOR | D6h | Yes |
| NLR_CONFIG | D7h | Yes |
| TEMPCO_CONFIG | DCh | Yes |
| DEADTIME | DDh | Yes |
| DEADTIME_CONFIG | DEh | Yes |
| DEADTIME_MAX | BFh | Yes |
| SNAPSHOT | EAh | Yes |
| SNAPSHOT_CONTROL | F3h | Yes |
| DEVICE_ID | E4h | Yes |
| USER_DATA_00 | B0h | Yes |
| Group Commands | | |
| SEQUENCE | E0h | Yes |
| GCB_GROUP | E2h | Yes |

| Designation | Cmd | Impl |
|---|---|---|
| ISHARE_CONFIG | D2h | Yes |
| PHASE_CONTROL | F0h | Yes |
| Supervisory Commands | | |
| PRIVATE_PASSWORD | FBh | Yes |
| PUBLIC_PASSWORD | FCh | Yes |
| UNPROTECT | FDh | Yes |
| SECURITY_LEVEL | FAh | Yes |

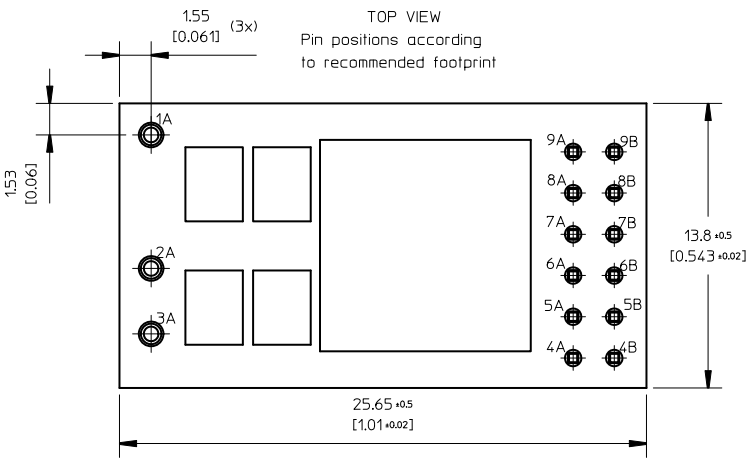
Notes:
Cmd is short for Command.
Impl is short for Implemented.

| **BMR 463 series** POL Regulators<br>Input 4.5-14 V, Output up to 20 A / 66 W | EN/LZT 146 434 R1A January 2011 |
|---|---|
| |  |

## Mechanical Information – Through hole mount version

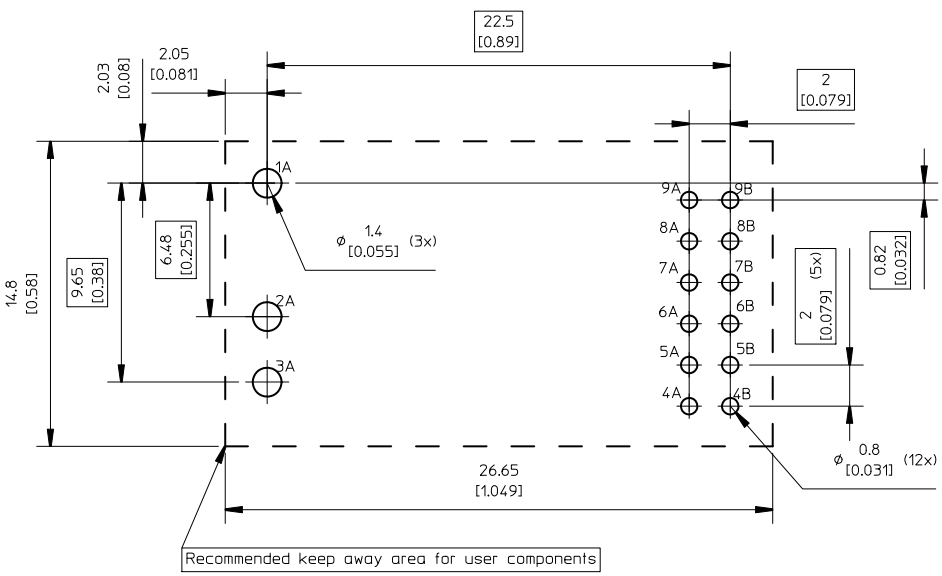




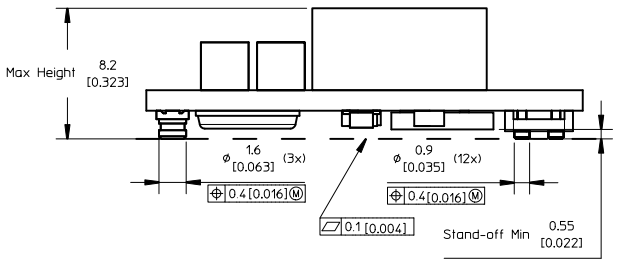

PIN SPECIFICATIONS
Pin 1A-3A Material: Copper alloy
Plating: Min Matte tin 8-13 µm over 2.5-5 µm Ni.
Pin 4A-9B Material: Brass
Plating: Min Au 0.2 µm over 1.27 µm Ni.

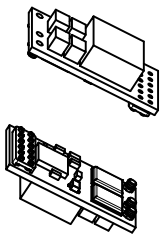
RECOMMENDED FOOTPRINT - TOP VIEW

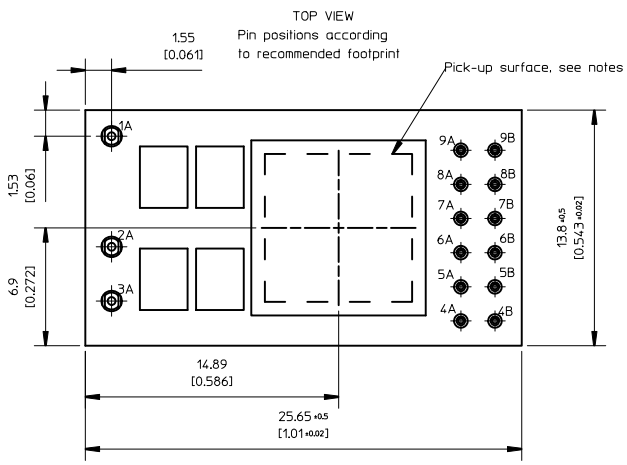



Weight: Typical 5.6 g
All dimensions in mm [inch].
Tolerances unless specified:
x.x ±0.50 mm [0.02],
x.xx ±0.25 mm [0.01]
(not applied on footprint or typical values)

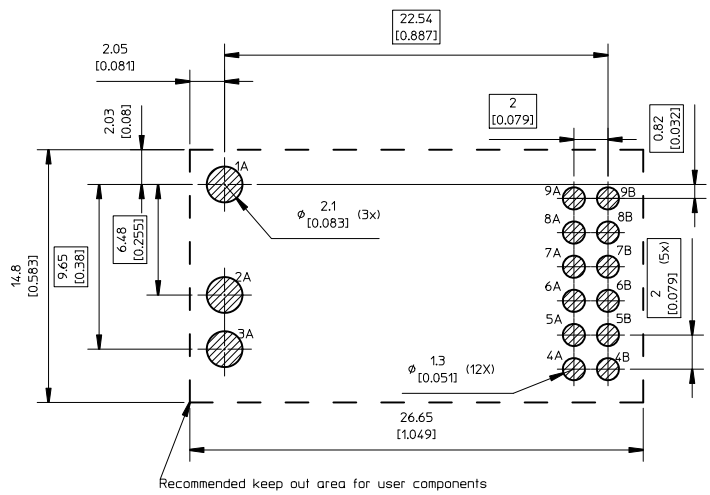
## Mechanical Information – Surface Mount Version






RECOMMENDED FOOTPRINT - TOP VIEW




NOTES

PIN SPECIFICATIONS
Pin 1A-3A Material: Copper alloy
Plating: Au 0.1 µm over 1-3 µm Ni.
Pin 4A-9B Material: Brass
Plating: Au 0.1 µm over 2 µm Ni.

PICK-UP SURFACE
Recommended pick-up nozzle size for assigned pick-up area is maximum Ø8 [0.315].

Weight: Typical 5.6 g
All dimensions in mm [inch].
Tolerances unless specified:
x.x ±0.50 [0.02]
x.xx±0.25 [0.01]
(not applied on footprint or typical values)

### Soldering Information - Surface Mounting

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PCB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

### Minimum Pin Temperature Recommendations

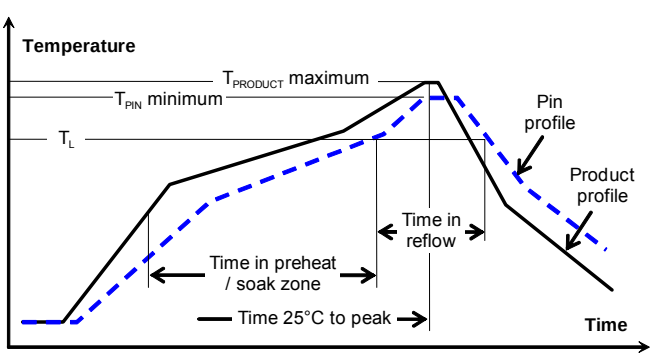
Pin number 2A chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

### SnPb solder processes

For SnPb solder processes, a pin temperature ($T_{PIN}$) in excess of the solder melting temperature, ($T_L$, 183°C for Sn63Pb37) for more than 30 seconds and a peak temperature of 210°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

| General reflow process specifications | | SnPb eutectic | Pb-free |
|---|---|---|---|
| Average ramp-up ($T_{PRODUCT}$) | | 3°C/s max | 3°C/s max |
| Typical solder melting (liquidus) temperature | $T_L$ | 183°C | 221°C |
| Minimum reflow time above $T_L$ | | 30 s | 30 s |
| Minimum pin temperature | $T_{PIN}$ | 210°C | 235°C |
| Peak product temperature | $T_{PRODUCT}$ | 225°C | 260°C |
| Average ramp-down ($T_{PRODUCT}$) | | 6°C/s max | 6°C/s max |
| Maximum time 25°C to peak | | 6 minutes | 8 minutes |




### Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature ($T_{PIN}$) in excess of the solder melting temperature ($T_L$, 217 to 221°C for SnAgCu solder alloys) for more than 30 seconds and a peak temperature of 235°C on all solder joints is recommended to ensure a reliable solder joint.

### Maximum Product Temperature Requirements

Top of the product PCB near pin 4B is chosen as reference location for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since this will likely be the warmest part of the product during the reflow process.

### SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

### Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

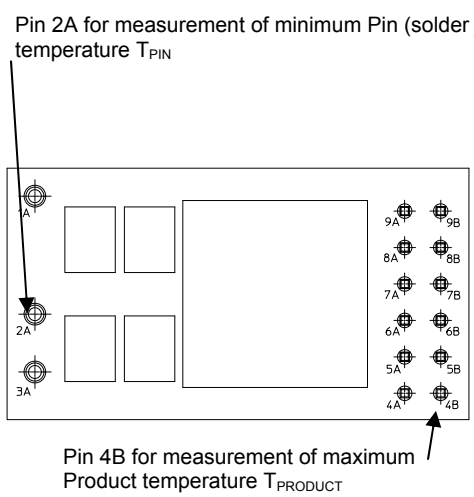
During reflow $T_{PRODUCT}$ must not exceed 260 °C at any time.

### Dry Pack Information

Surface mounted versions of the products are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

### Thermocoupler Attachment



**Soldering Information - Hole Mounting**

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

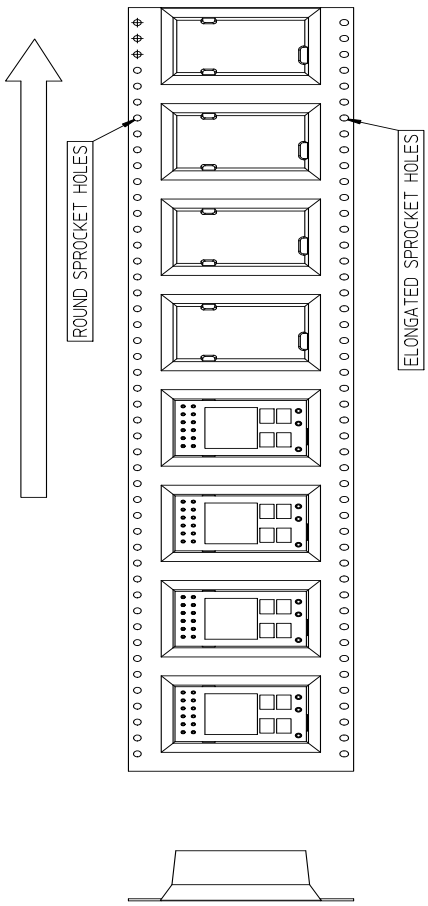
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

**Delivery Package Information**

The products are delivered in antistatic carrier tape (EIA 481 standard).

| Carrier Tape Specifications | |
|---|---|
| **Material** | PS, antistatic |
| **Surface resistance** | < $10^7$ Ohm/square |
| **Bakeability** | The tape is not bakable |
| **Tape width, W** | 44 mm [1.73 inch] |
| **Pocket pitch, $P_1$** | 24 mm [0.95 inch] |
| **Pocket depth, $K_0$** | 12.4 mm [0.488 inch] |
| **Reel diameter** | 381 mm [15 inch] |
| **Reel capacity** | 200 products /reel |
| **Reel weight** | TBD kg/full reel |



**Product Qualification Specification**

| Characteristics | | | |
|---|---|---|---|
| External visual inspection | IPC-A-610 | | |
| Change of temperature (Temperature cycling) | IEC 60068-2-14 Na | Temperature range<br>Number of cycles<br>Dwell/transfer time | -40 to 100°C<br>1000<br>15 min/0-1 min |
| Cold (in operation) | IEC 60068-2-1 Ad | Temperature $T_A$<br>Duration | -45°C<br>72 h |
| Damp heat | IEC 60068-2-67 Cy | Temperature<br>Humidity<br>Duration | 85°C<br>85 % RH<br>1000 hours |
| Dry heat | IEC 60068-2-2 Bd | Temperature<br>Duration | 125°C<br>1000 h |
| Electrostatic discharge susceptibility | IEC 61340-3-1, JESD 22-A114<br>IEC 61340-3-2, JESD 22-A115 | Human body model (HBM)<br>Machine Model (MM) | Class 2, 2000 V<br>Class 3, 200 V |
| Immersion in cleaning solvents | IEC 60068-2-45 XA, method 2 | Water<br>Glycol ether<br>Isopropyl alcohol | 55°C<br>35°C<br>35°C |
| Mechanical shock | IEC 60068-2-27 Ea | Peak acceleration<br>Duration | 100 g<br>6 ms |
| Moisture reflow sensitivity [1] | J-STD-020C | Level 1 (SnPb-eutectic)<br>Level 3 (Pb Free) | 225°C<br>260°C |
| Operational life test | MIL-STD-202G, method 108A | Duration | 1000 h |
| Resistance to soldering heat [2] | IEC 60068-2-20 Tb, method 1A | Solder temperature<br>Duration | 270°C<br>10-13 s |
| Robustness of terminations | IEC 60068-2-21 Test Ua1<br>IEC 60068-2-21 Test Ue1 | Through hole mount products<br>Surface mount products | All leads<br>All leads |
| Solderability | IEC 60068-2-58 test Td [1]<br><br>IEC 60068-2-20 test Ta [2] | Preconditioning<br>Temperature, SnPb Eutectic<br>Temperature, Pb-free<br><br>Preconditioning<br>Temperature, SnPb Eutectic<br>Temperature, Pb-free | 150°C dry bake 16 h<br>215°C<br>235°C<br><br>Steam ageing<br>235°C<br>260°C |
| Vibration, broad band random | IEC 60068-2-64 Fh, method 1 | Frequency<br>Spectral density<br>Duration | 10 to 500 Hz<br>0.07 $g^2$/Hz<br>10 min in each 3 perpendicular directions |

Notes
[1] Only for products intended for reflow soldering (surface mount products)
[2] Only for products intended for wave soldering (plated through hole products)