

74LVC32A

Quad 2-input OR gate

Rev. 7 — 27 May 2020

Product data sheet

1. General description

The 74LVC32A is a quad 2-input OR gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- CMOS low power dissipation
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74LVC32AD | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74LVC32ADB | -40 °C to +125 °C | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74LVC32APW | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74LVC32ABQ | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

4. Functional diagram

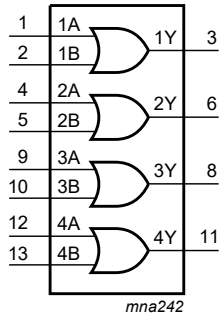


Fig. 1. Logic symbol

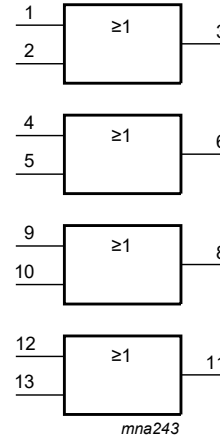


Fig. 2. IEC logic symbol

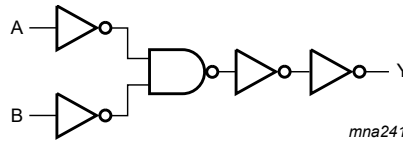


Fig. 3. Logic diagram for one gate

5. Pinning information

5.1. Pinning

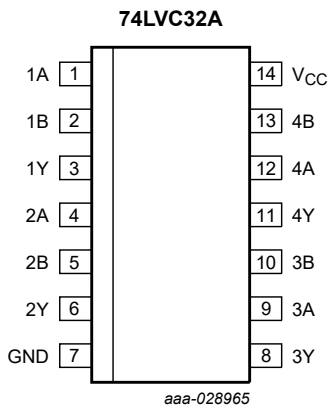


Fig. 4. Pin configuration SOT108-1 (SO14)

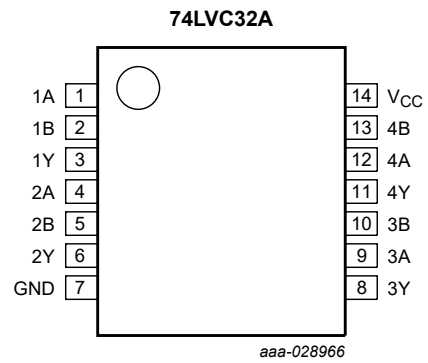
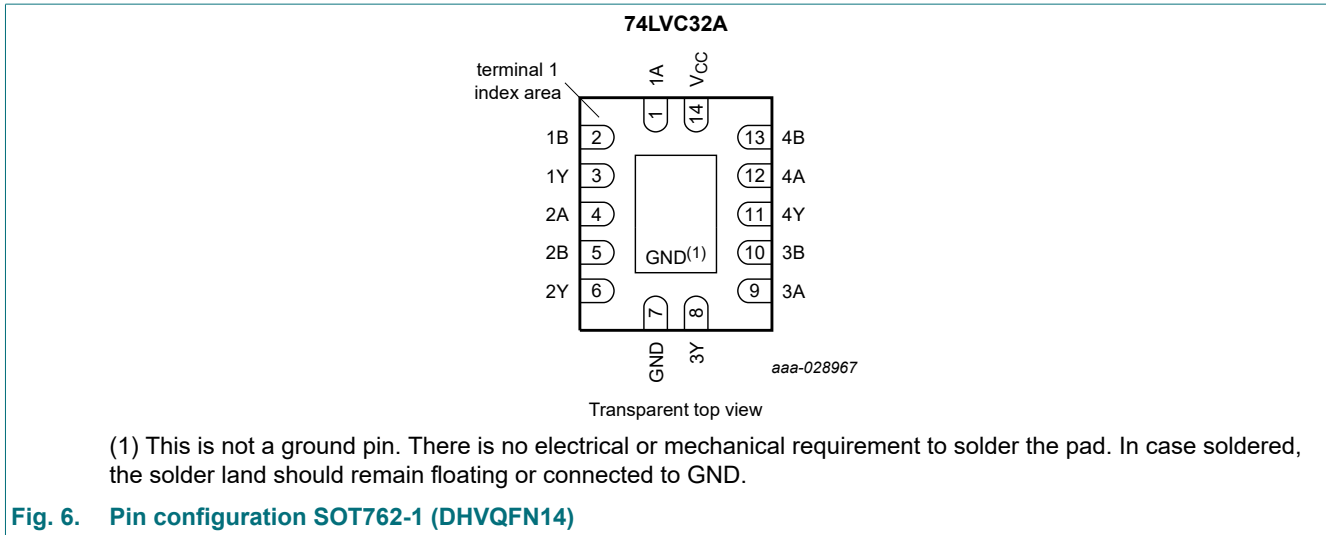


Fig. 5. Pin configuration SOT337-1 (SSOP14) and SOT402-1 (TSSOP14)



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|----------------|
| 1A, 2A, 3A, 4A | 1, 4, 9, 12 | data input |
| 1B, 2B, 3B, 4B | 2, 5, 10, 13 | data input |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care

| Input | | Output |
|-------|----|--------|
| nA | nB | nY |
| L | L | L |
| X | H | H |
| H | X | H |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|-------------------------------|----------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ | -50 | - | mA |
| V_I | input voltage | | [1] -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ | - | ± 50 | mA |
| V_O | output voltage | | [2] -0.5 | $V_{CC} + 0.5$ | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ± 50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C | [3] - | 500 | mW |

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT337-1 (SSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|----------------------------|------|-----|----------|------|
| V_{CC} | supply voltage | | 1.65 | - | 3.6 | V |
| | | functional | 1.2 | - | - | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | 0 | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 3.6 V | 0 | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-----------------------|---------|---------------------|-----------------------|---------------------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | 1.08 | - | - | 1.08 | - | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65V _{CC} | - | - | 0.65V _{CC} | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | 0.12 | - | 0.12 | V |
| | | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35V _{CC} | - | 0.35V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V | V _{CC} - 0.2 | - | - | V _{CC} - 0.3 | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 1.2 | - | - | 1.05 | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.8 | - | - | 1.65 | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 2.2 | - | - | 2.05 | - | V |
| | | I _O = -18 mA; V _{CC} = 3.0 V | 2.4 | - | - | 2.25 | - | V |
| | | I _O = -24 mA; V _{CC} = 3.0 V | 2.2 | - | - | 2.0 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | |
| | | I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V | - | - | 0.2 | - | 0.3 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.45 | - | 0.65 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.6 | - | 0.8 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.4 | - | 0.6 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.55 | - | 0.8 | V |
| I _I | input leakage current | V _{CC} = 3.6 V; V _I = 5.5 V or GND | - | ±0.1 | ±5 | - | ±20 | µA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A | - | 0.1 | 10 | - | 40 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A | - | 5 | 500 | - | 5000 | µA |
| C _I | input capacitance | V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC} | - | 4.0 | - | - | - | pF |

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|-------------|-------------------------------|---|------------------|---------|-----|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t_{pd} | propagation delay | nA, nB to nY; see Fig. 7 [2] | | | | | | |
| | | $V_{CC} = 1.2\text{ V}$ | - | 10 | - | - | - | ns |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | 0.5 | 4.2 | 9.0 | 0.5 | 10.4 | ns |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.5 | 2.4 | 4.9 | 1.5 | 5.7 | ns |
| | | $V_{CC} = 2.7\text{ V}$ | 1.5 | 2.5 | 4.4 | 1.5 | 5.5 | ns |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 1.0 | 2.2 | 3.8 | 1.0 | 5.0 | ns |
| $t_{sk(o)}$ | output skew time | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [3] | - | - | 1.0 | - | 1.5 | ns |
| C_{PD} | power dissipation capacitance | per gate; $V_I = \text{GND to } V_{CC}$ [4] | | | | | | |
| | | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | - | 4.7 | - | - | - | pF |
| | | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | - | 8.0 | - | - | - | pF |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | - | 11.0 | - | - | - | pF |

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 1.2\text{ V}, 1.8\text{ V}, 2.5\text{ V}, 2.7\text{ V},$ and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

10.1. Waveforms and test circuit

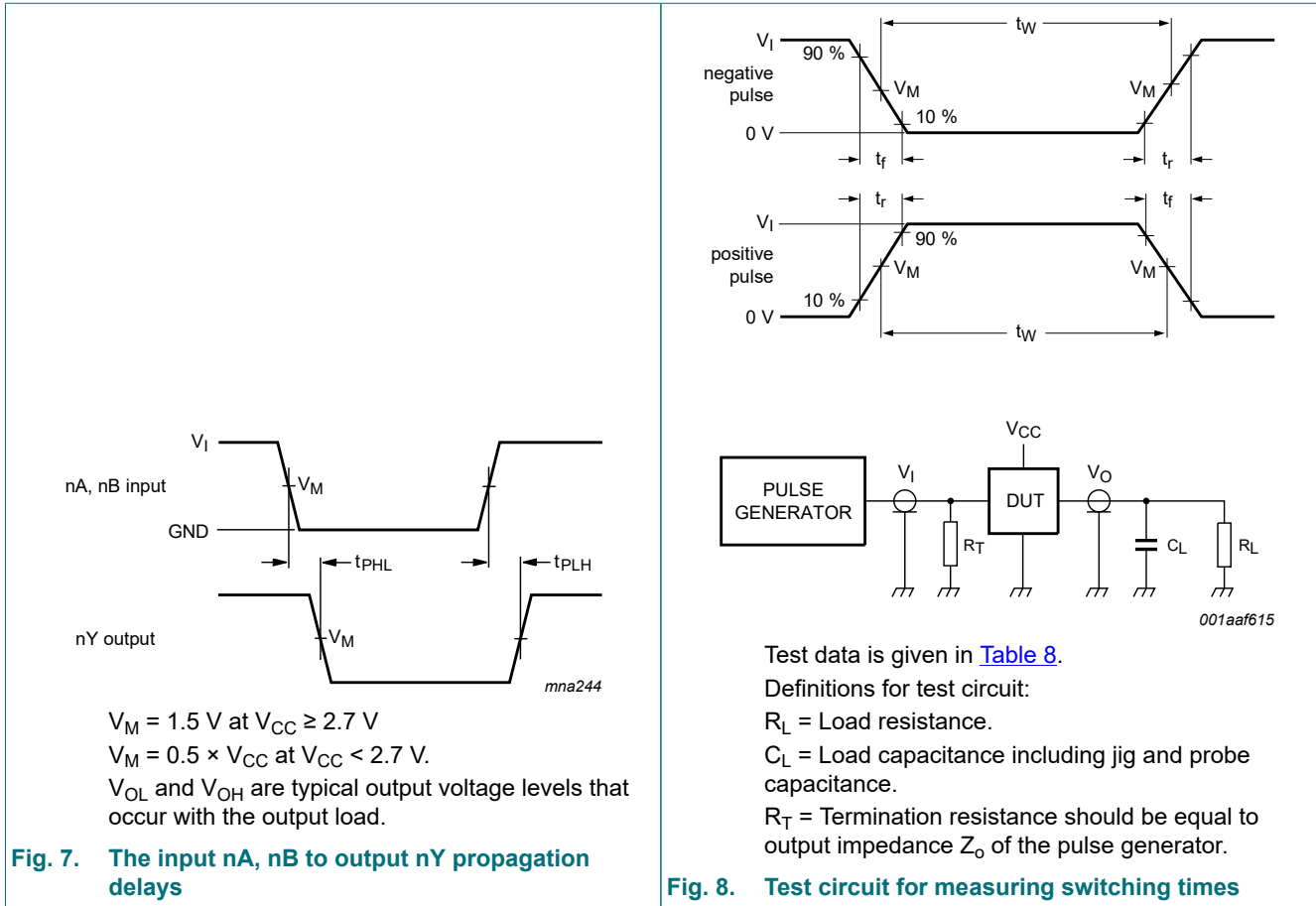


Table 8. Test data

| Supply voltage | Input | | Load | |
|------------------|----------|----------------------|-------|--------------|
| | V_I | t_r, t_f | C_L | R_L |
| 1.2 V | V_{CC} | $\leq 2\text{ ns}$ | 30 pF | 1 k Ω |
| 1.65 V to 1.95 V | V_{CC} | $\leq 2\text{ ns}$ | 30 pF | 1 k Ω |
| 2.3 V to 2.7 V | V_{CC} | $\leq 2\text{ ns}$ | 30 pF | 500 Ω |
| 2.7 V | 2.7 V | $\leq 2.5\text{ ns}$ | 50 pF | 500 Ω |
| 3.0 V to 3.6 V | 2.7 V | $\leq 2.5\text{ ns}$ | 50 pF | 500 Ω |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

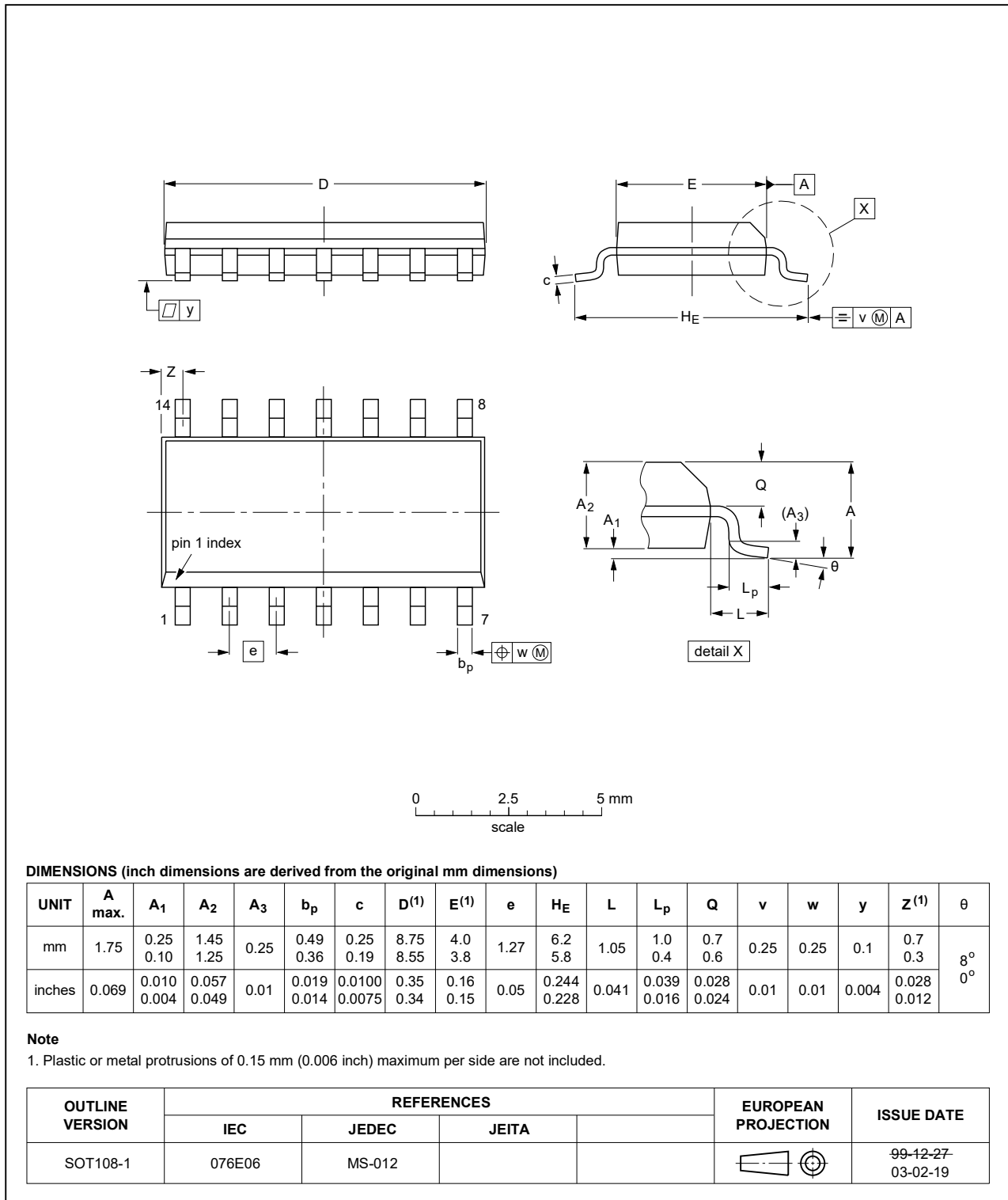


Fig. 9. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

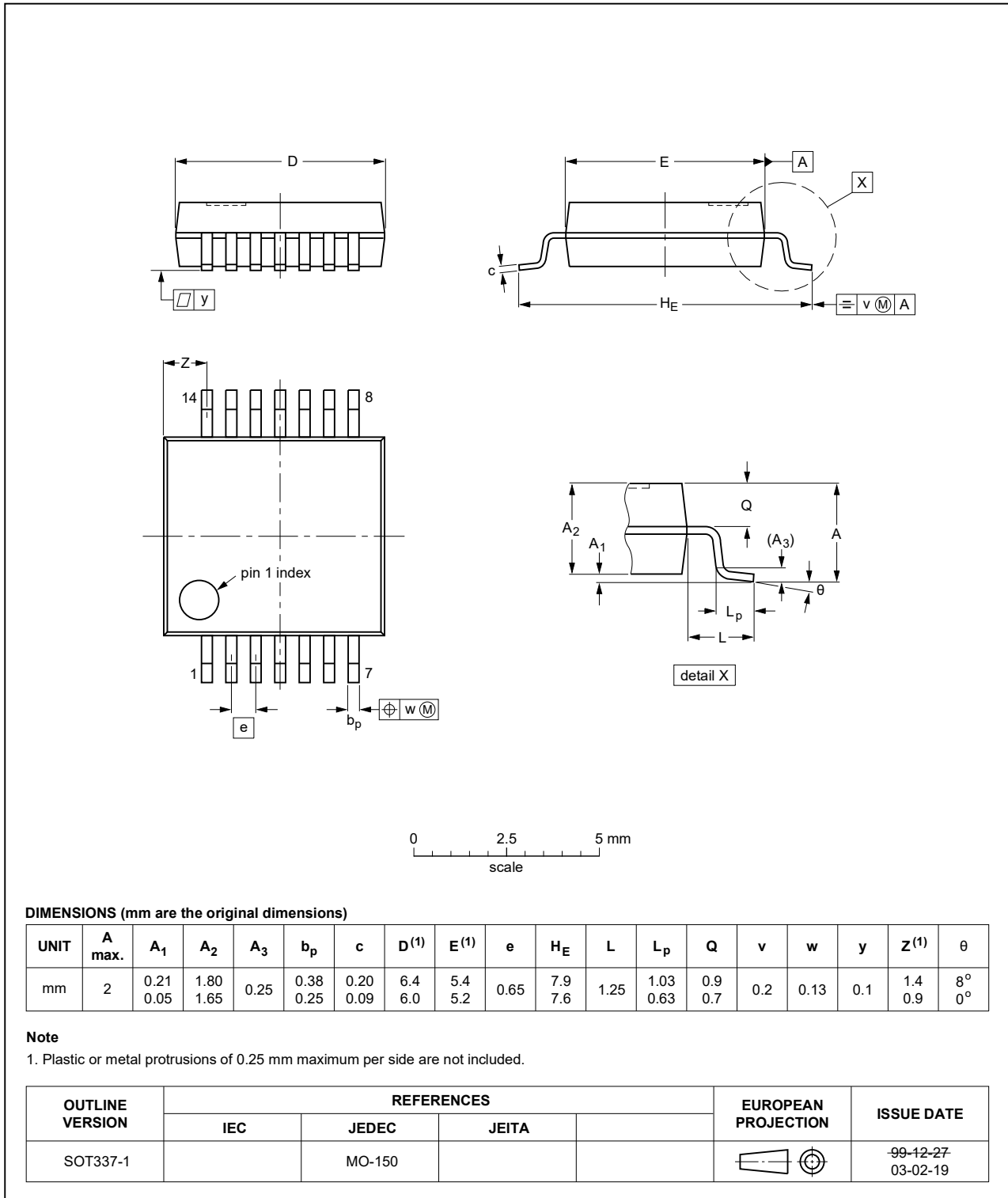


Fig. 10. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

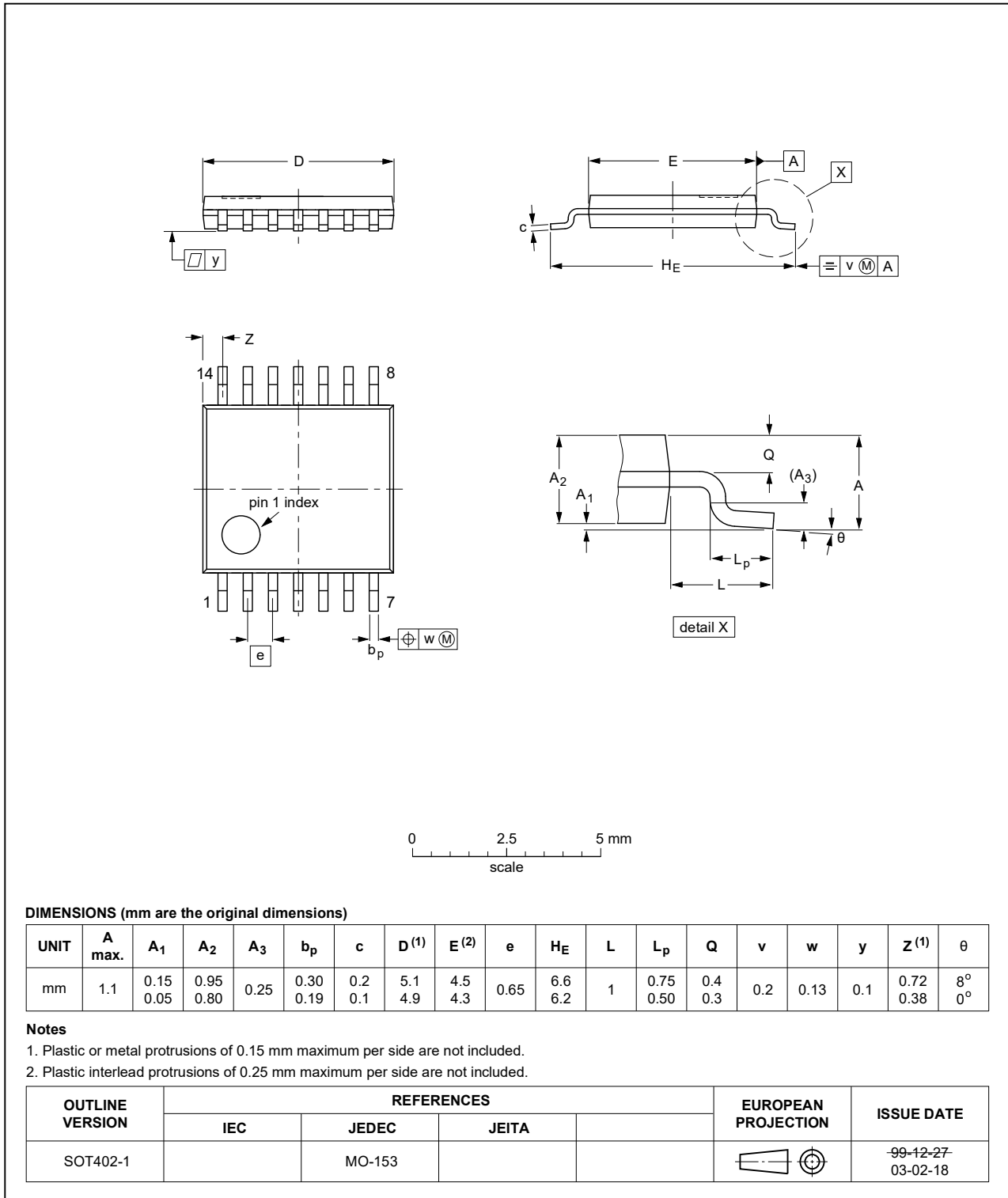


Fig. 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

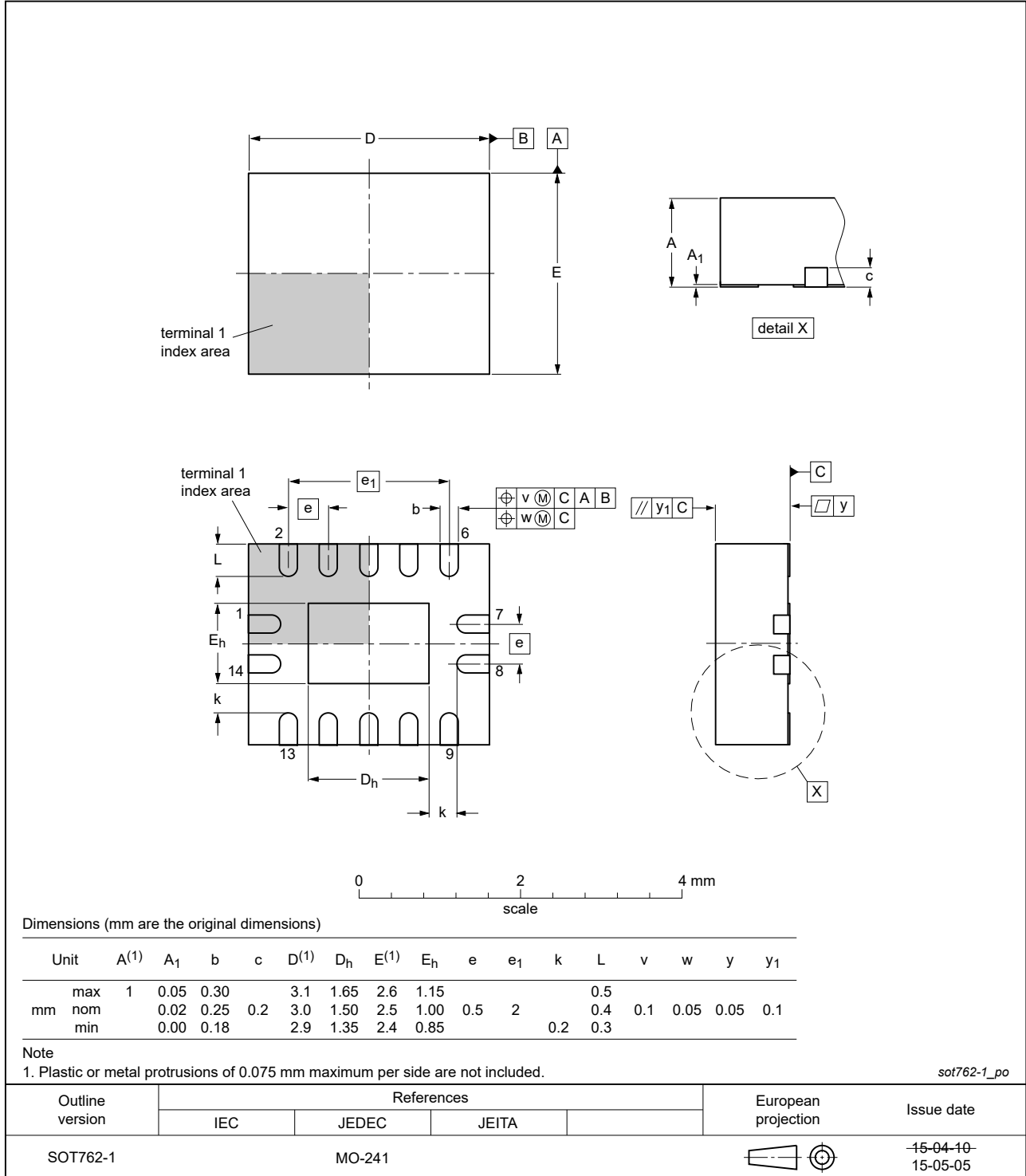


Fig. 12. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|-----------------------|---------------|--------------|
| 74LVC32A v.7 | 20200527 | Product data sheet | - | 74LVC32A v.6 |
| Modifications: | <ul style="list-style-type: none"> • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation updated. | | | |
| 74LVC32A v.6 | 20180912 | Product data sheet | - | 74LVC32A v.5 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Package outline drawing SOT762-1 updated. • Typo corrected in t_{pd} value: 1.05 ns to 1.5 ns. | | | |
| 74LVC32A v.5 | 20111117 | Product data sheet | - | 74LVC32A v.4 |
| Modifications: | <ul style="list-style-type: none"> • Legal pages updated. • Table 6, ΔI_{CC}: condition V_{CC} changed. | | | |
| 74LVC32A v.4 | 20111019 | Product data sheet | - | 74LVC32A v.3 |
| 74LVC32A v.3 | 20030716 | Product specification | - | 74LVC32A v.2 |
| 74LVC32A v.2 | 19970630 | Product specification | - | 74LVC32A v.1 |
| 74LVC32A v.1 | 19970630 | Product specification | - | - |

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|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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