81 GHz to 86 GHz, E-Band Variable Gain Amplifier

Data Sheet **HMC8121**

FEATURES

Gain: 22 dB typical
Wide gain control range: 17 dB typical
Output third-order intercept (OIP3): 27.5 dBm typical
Output power for 1 dB compression (P1dB): 20 dBm typical
Saturated output power (P_{SAT}): 21 dBm typical
DC supply: 4 V at 265 mA
No external matching required
Die size: 3.599 mm × 1.369 mm × 0.05 mm

APPLICATIONS

E-band communication systems
High capacity wireless backhaul radio systems
Test and measurement

GENERAL DESCRIPTION

The HMC8121 is an integrated E-band, gallium arsenide (GaAs), pseudomorphic (pHEMT), monolithic microwave integrated circuit (MMIC), variable gain amplifier and/or driver amplifier that operates from 81 GHz to 86 GHz. The HMC8121 provides up to 22 dB of gain, 20 dBm output P1dB, 27.5 dBm of OIP3, and 21 dBm of P_{SAT} while requiring only 265 mA from a 4 V power supply. Two gain control voltages (V_{CTL1} and V_{CTL2}) are provided to allow up to 17 dB of variable gain control. The HMC8121 exhibits excellent linearity and is optimized for E-band communications and high capacity wireless backhaul radio systems. All data is taken with the chip in a 50 Ω test fixture connected via a 3 mil wide × 0.5 mil thick × 7 mil long ribbon on each port.

FUNCTIONAL BLOCK DIAGRAM

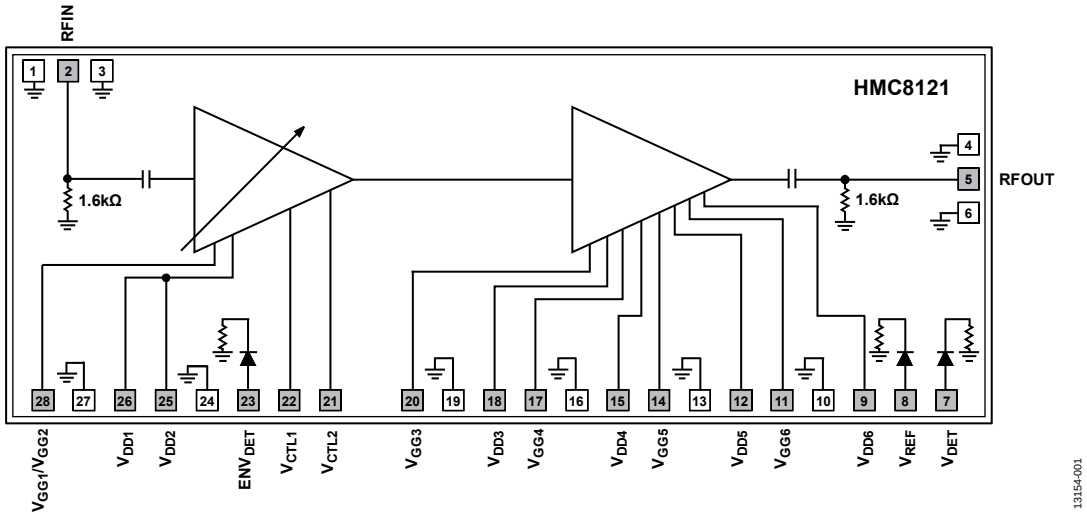

Figure 1.

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Technical Support www.analog.com

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REVISION HISTORY

2/16—Revision A: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{DDx} = 4 V, V_{CTLx} = −5 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
RF Frequency Range	81		86	GHz
PERFORMANCE				
Gain	19	22		dB
Gain Variation over Temperature		0.03		dB/°C
Gain Control Range	12	17		dB
Output Power for 1 dB Compression (P1dB)	16	20		dBm
Saturated Output Power (P_{SAT})		21		dBm
Output Third-Order Intercept (OIP3) at Maximum Gain[1]		27.5		dBm
Input Return Loss		12		dB
Output Return Loss		10		dB
POWER SUPPLY				
Total Supply Current (I_{DD})[2]		265		mA

[1] Data taken at power input (P_{IN}) = −10 dBm/tone, 1 MHz spacing.
[2] Set V_{CTL1}/V_{CTL2} = −5 V and then adjust V_{GG1}/V_{GG2}, V_{GG3}, V_{GG4}, V_{GG5}, and V_{GG6} from −2 V to 0 V to achieve a total drain current (I_{DD}) = 265 mA.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (V_{DD1} to V_{DD6})	4.5 V
Gate Bias Voltage (V_{GG1}/V_{GG2}, V_{GG3} to V_{GG6})	−3 V to 0 V
Gain Control Voltage (V_{CTL1} and V_{CTL2})	−6 V to 0 V
Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
28-Pad Bare Die [CHIP]	69.5	°C/W

[1] Based on ABLEBOND® 84-1LMIT as die attach epoxy with thermal conductivity of 3.6 W/mK.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

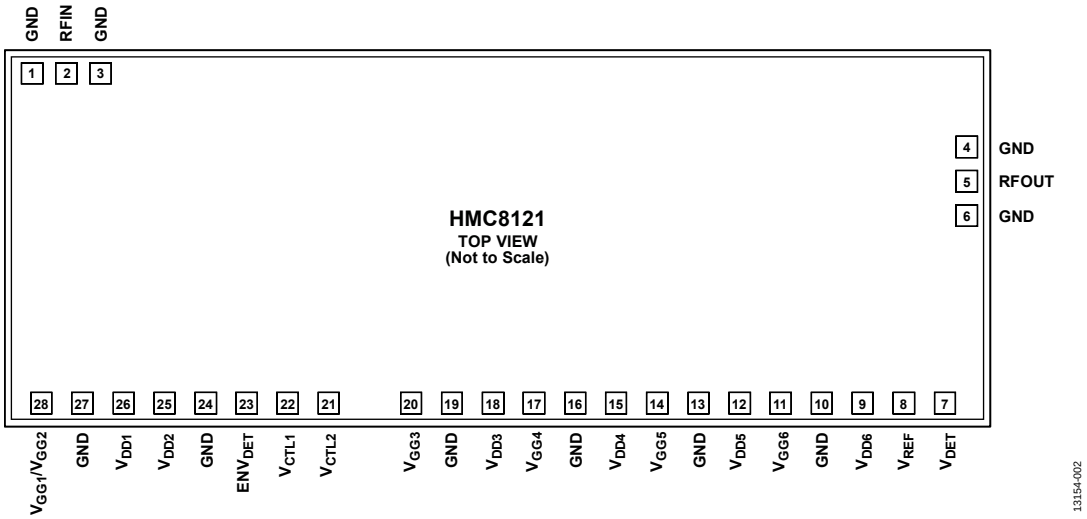

Figure 2. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 4, 6, 10, 13, 16, 19, 24, 27	GND	Ground Connection (See Figure 3).
2	RFIN	RF Input. DC couple RFIN and match it to 50 Ω (see Figure 4).
5	RFOUT	RF Output. DC couple RFOUT and match it to 50 Ω (see Figure 5).
7	V_{DET}	Detector Voltage for the Power Detector (See Figure 6). V_{DET} is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor. Refer to the typical application circuit for the required external components (see Figure 38).
8	V_{REF}	Reference Voltage for the Power Detector (See Figure 6). V_{REF} is the dc bias of the diode biased through an external resistor used for the temperature compensation of V_{DET}. Refer to the typical application circuit for the required external components (see Figure 38).
9, 12, 15, 18, 25, 26	V_{DD6} to V_{DD1}	Drain Bias Voltage for the Variable Gain Amplifier (See Figure 7). For the required external components, see Figure 38.
11, 14, 17, 20, 28	V_{GG6} to V_{GG3}, V_{GG1}/V_{GG2}	Gate Bias Voltage for the Variable Gain Amplifier (See Figure 8). For the required external components, see Figure 38.
21, 22	V_{CTL2}, V_{CTL1}	Gain Control Voltage for the Variable Gain Amplifier (See Figure 9). For the required external components, see Figure 38.
23	ENV_{DET}	Envelope Detector (See Figure 10). For the required external components, see Figure 38.
Die Bottom	GND	Ground. Die bottom must be connected to the RF/dc ground (see Figure 3).

INTERFACE SCHEMATICS

Figure 3. GND Interface

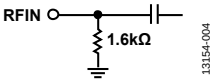

Figure 4. RFIN Interface

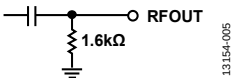

Figure 5. RFOUT Interface

Figure 6. V_{DET}, V_{REF} Interface

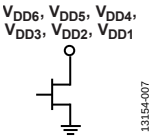

Figure 7. V_{DD6} to V_{DD1} Interface

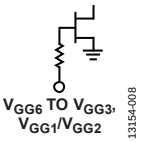

Figure 8. V_{GG6} to V_{GG3}, V_{GG1}/V_{GG2} Interface

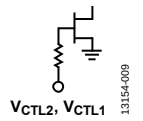

Figure 9. V_{CTL2}, V_{CTL1} Interface

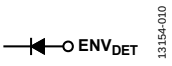

Figure 10. ENV_{DET} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

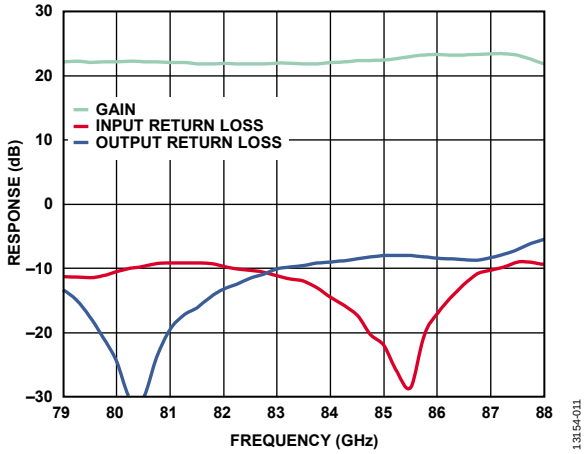

Figure 11. Broadband Gain and Return Loss Response vs. Frequency, $V_{CTL1}/V_{CTL2} = -5$ V

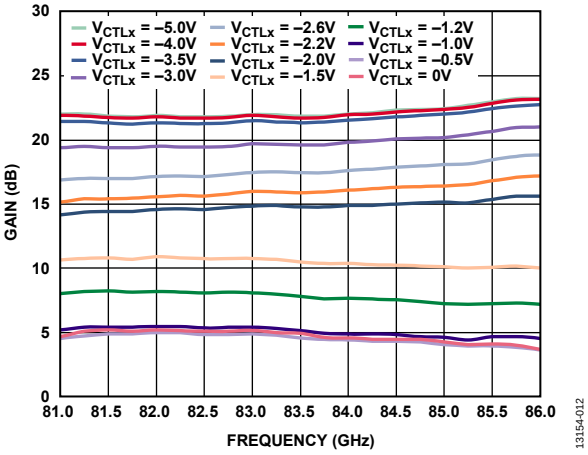

Figure 12. Gain vs. Frequency at Various Control Voltages

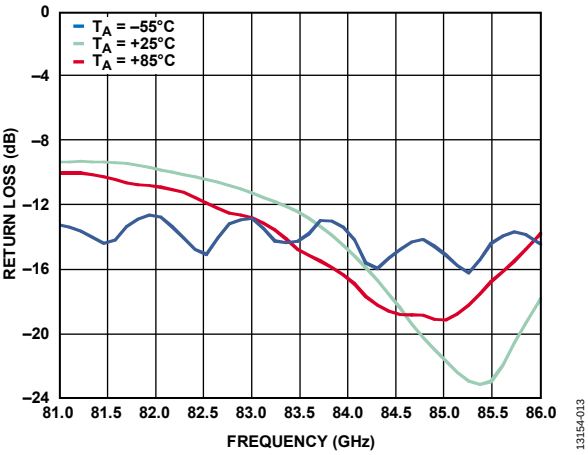

Figure 13. Input Return Loss vs. Frequency at Various Temperatures, $V_{CTL1}/V_{CTL2} = -5$ V

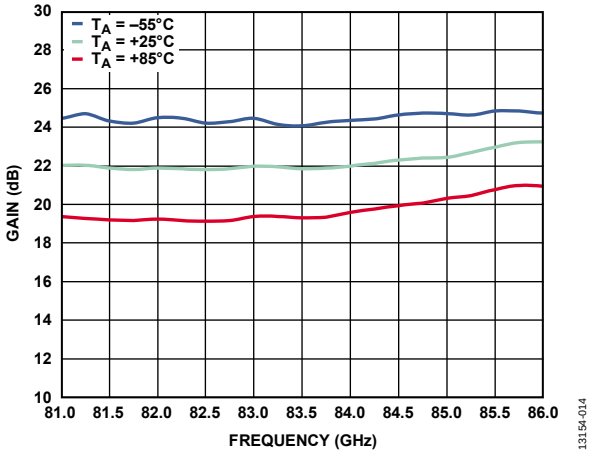

Figure 14. Gain vs. Frequency at Various Temperatures, $V_{CTL1}/V_{CTL2} = -5$ V

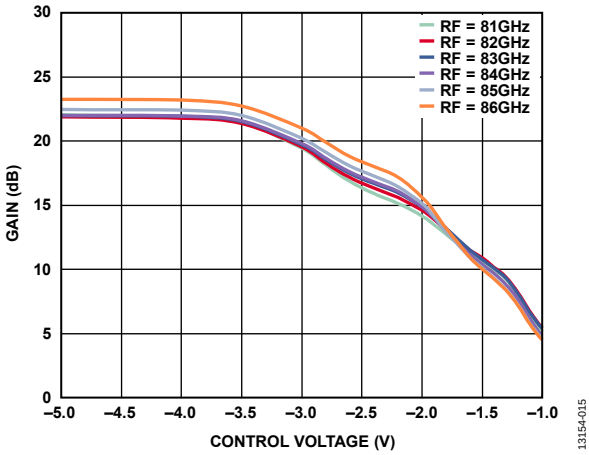

Figure 15. Gain vs. Control Voltage at Various RF Frequencies

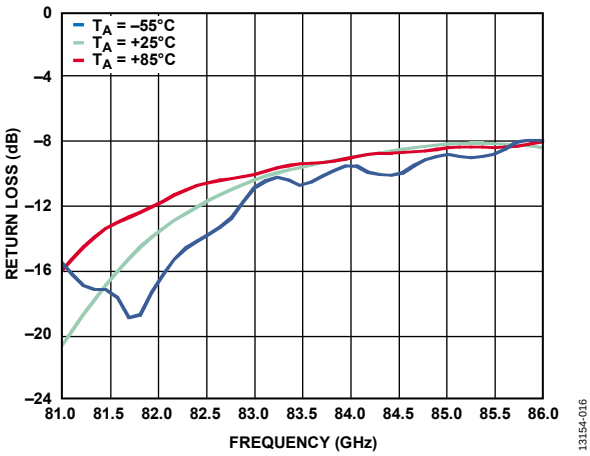

Figure 16. Output Return Loss vs. Frequency at Various Temperatures, $V_{CTL1}/V_{CTL2} = -5$ V

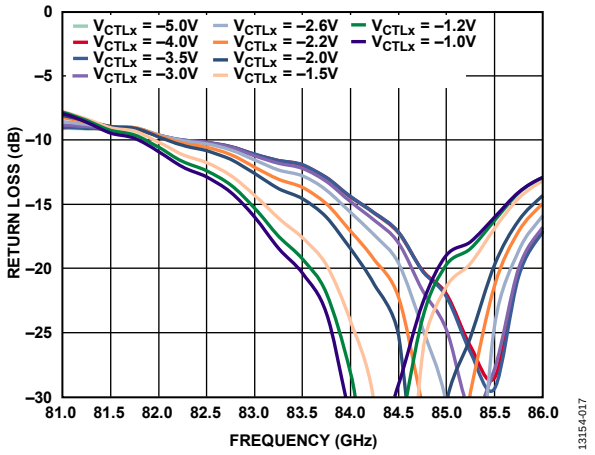

Figure 17. Input Return Loss vs. Frequency at Various Control Voltages

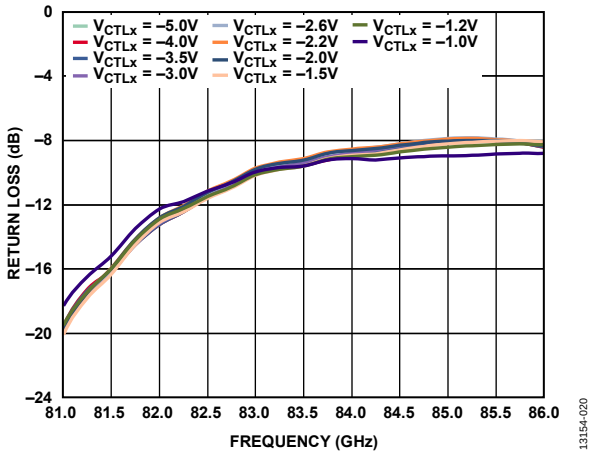

Figure 20. Output Return Loss vs. Frequency at Various Control Voltages

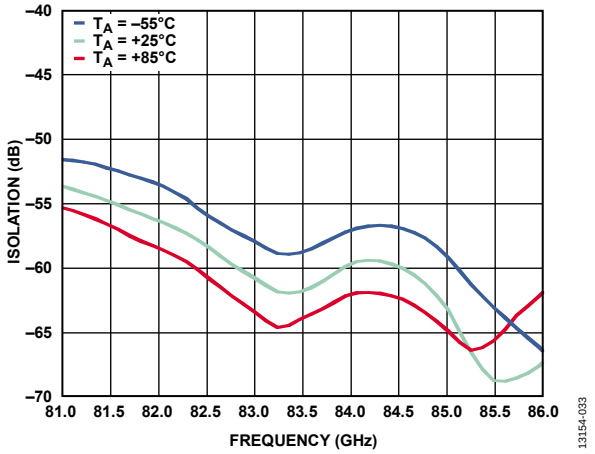

Figure 18. Reverse Isolation vs. Frequency at Various Temperatures, $V_{CTL1}/V_{CTL2} = -5$ V

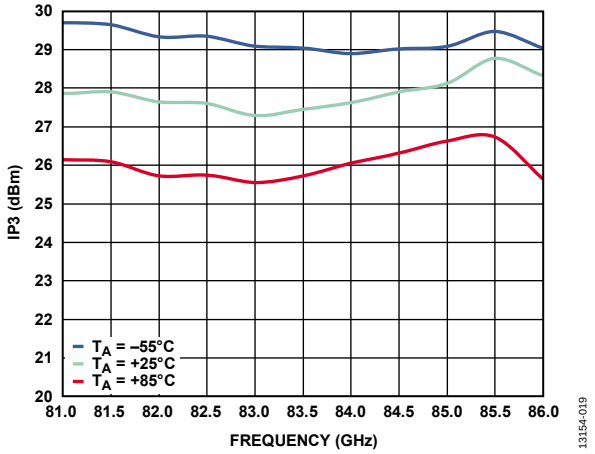

Figure 21. Output IP3 vs. Frequency at Various Temperatures, $P_{IN} = -10$ dBm/Tone, $V_{CTL1}/V_{CTL2} = -5$ V

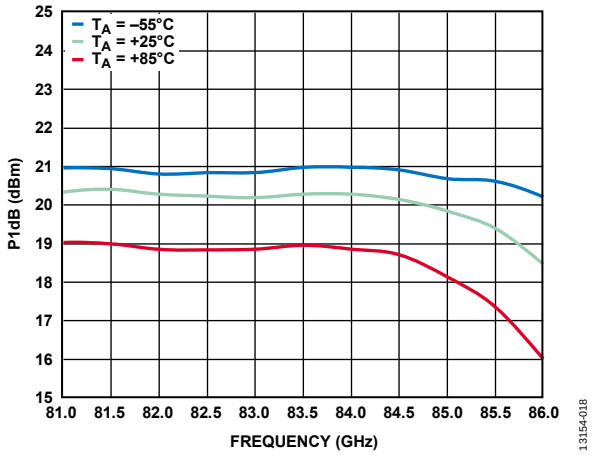

Figure 19. Output P1dB vs. Frequency at Various Temperatures, $V_{CTL1}/V_{CTL2} = -5$ V

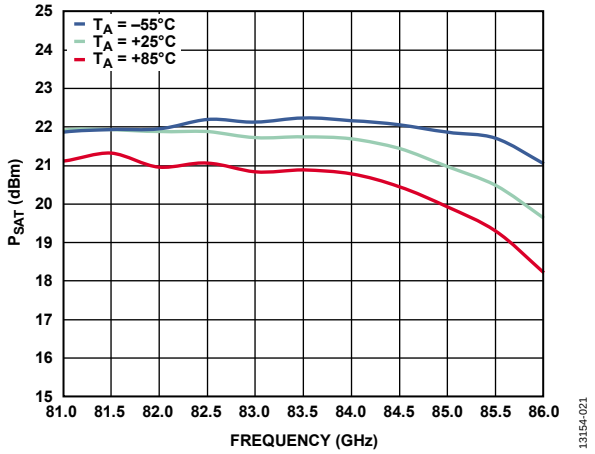

Figure 22. P_{SAT} vs. Frequency at Various Temperatures, $V_{CTL1}/V_{CTL2} = -5$ V

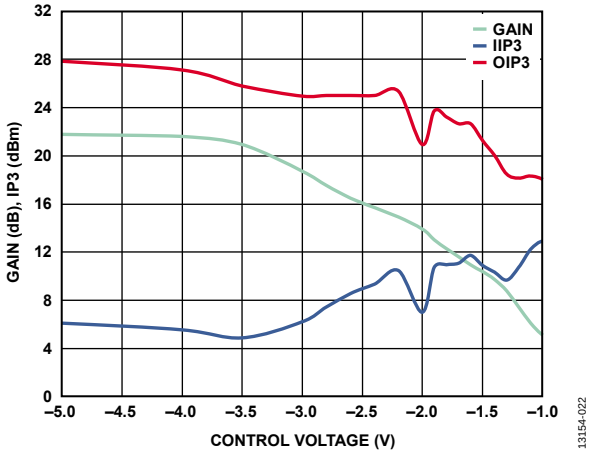

Figure 23. Gain and Input/Output IP3 vs. Control Voltage, P_{IN} = −10 dBm/Tone, RF = 81 GHz

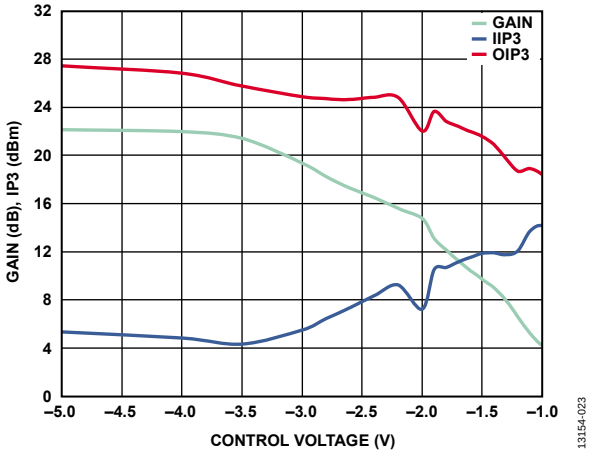

Figure 24. Gain and Input/Output IP3 vs. Control Voltage, P_{IN} = −10 dBm/Tone, RF = 83.5 GHz

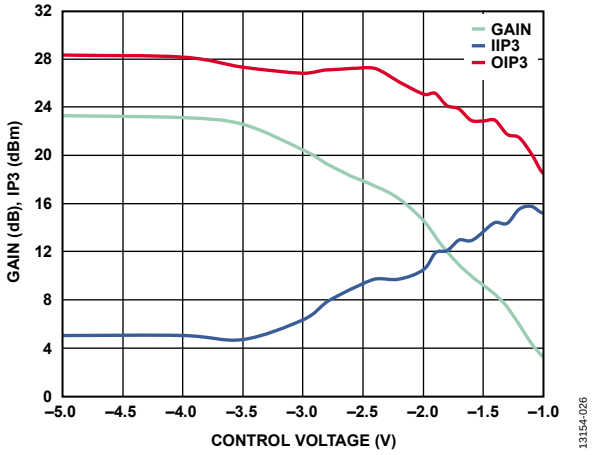

Figure 25. Gain and Input/Output IP3 vs. Control Voltage, P_{IN} = −10 dBm/Tone, RF = 86 GHz

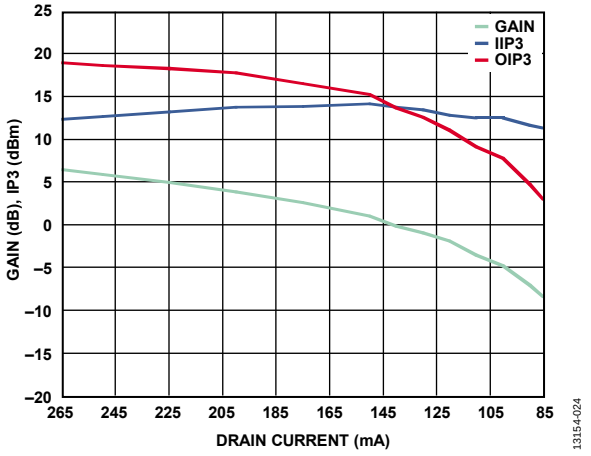

Figure 26. Gain and Input/Output IP3 vs. Drain Current, P_{IN} = −5 dBm/Tone, V_{CTL1}/V_{CTL2} = −1 V, RF = 81 GHz, Drain Current = (I_{DD1}/I_{DD2} Fixed at 50 mA) + (I_{DD3} to I_{DD6} Swept)

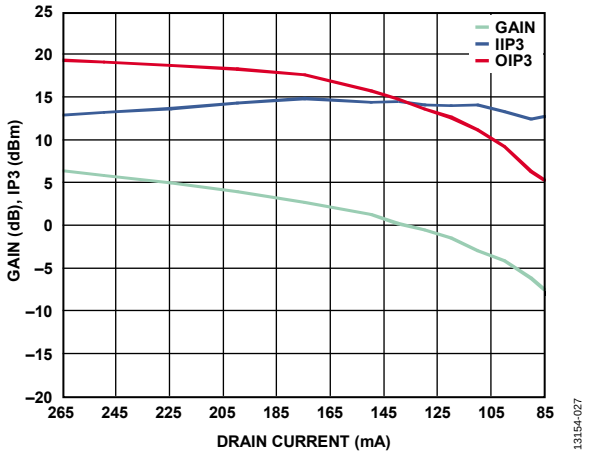

Figure 27. Gain and Input/Output IP3 vs. Drain Current, P_{IN} = −5 dBm/Tone, V_{CTL1}/V_{CTL2} = −1 V, RF = 83.5 GHz, Drain Current = (I_{DD1}/I_{DD2} Fixed at 50 mA) + (I_{DD3} to I_{DD6} Swept)

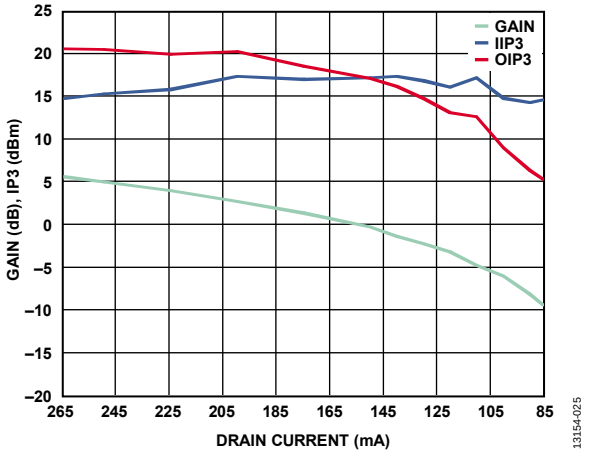

Figure 28. Gain and Input/Output IP3 vs. Drain Current, P_{IN} = −5 dBm/Tone, V_{CTL1}/V_{CTL2} = −1 V, RF = 86 GHz, Drain Current = (I_{DD1}/I_{DD2} Fixed at 50 mA) + (I_{DD3} to I_{DD6} Swept)

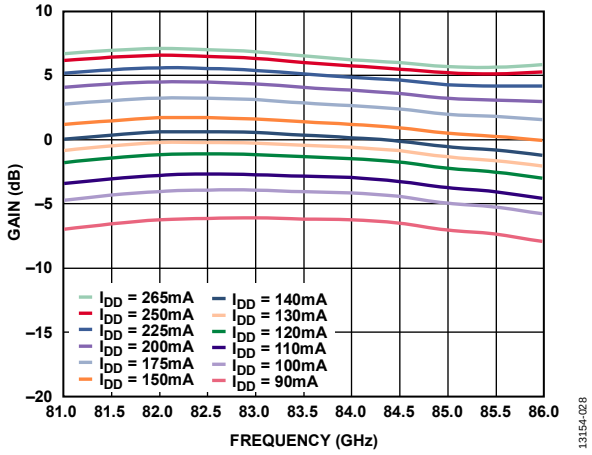

Figure 29. Gain vs. Frequency at Various Drain Currents, P_{IN} = −5 dBm/Tone, V_{CTL1}/V_{CTL2} = −1 V, Drain Current = (I_{DD1}/I_{DD2} fixed at 50 mA) + (I_{DD3} to I_{DD6} Swept)

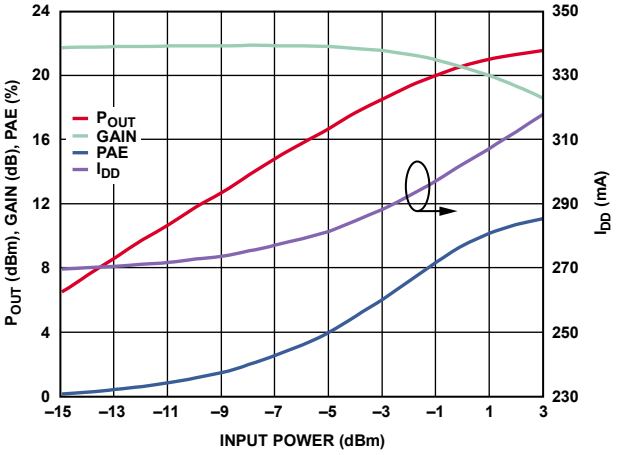

Figure 30. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, V_{CTL1}/V_{CTL2} = −5 V, RF = 83.5 GHz

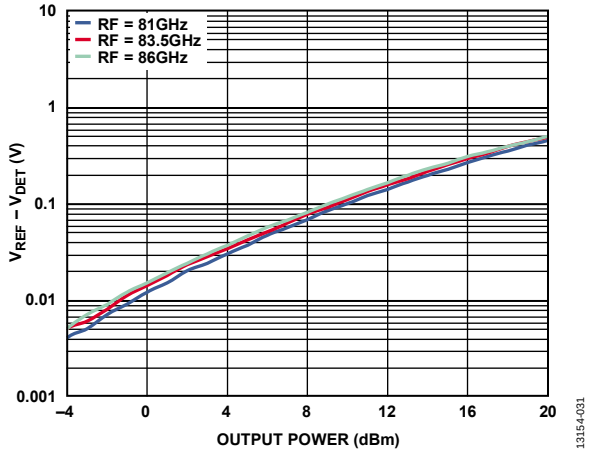

Figure 31. Detector Output Voltage ($V_{REF} - V_{DET}$) vs. Output Power at Various RF Frequencies, V_{CTL1}/V_{CTL2} = −5 V

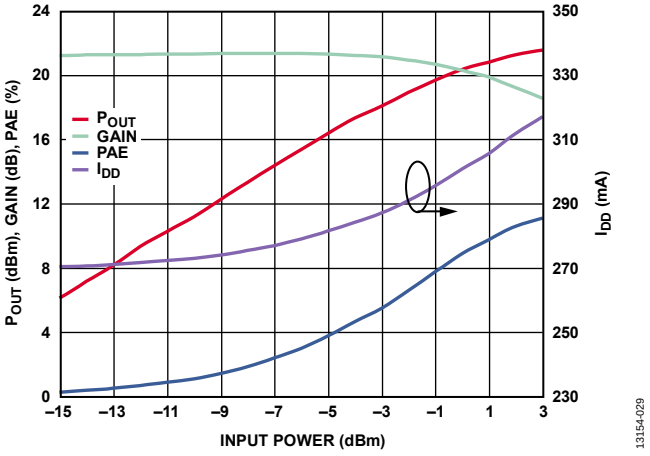

Figure 32. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, V_{CTL1}/V_{CTL2} = −5 V, RF = 81 GHz

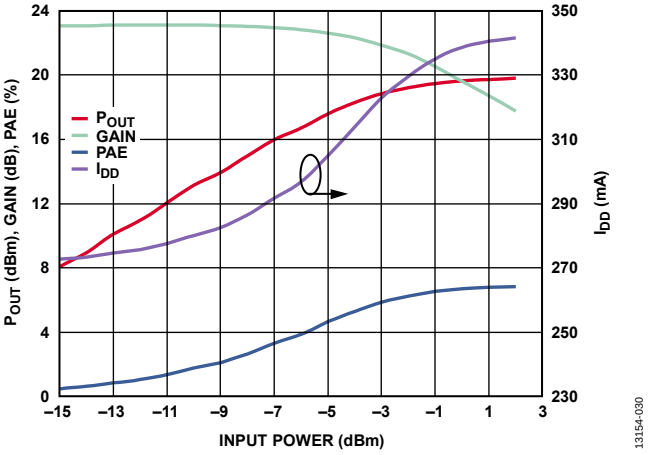

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power, V_{CTL1}/V_{CTL2} = −5 V, RF = 86 GHz

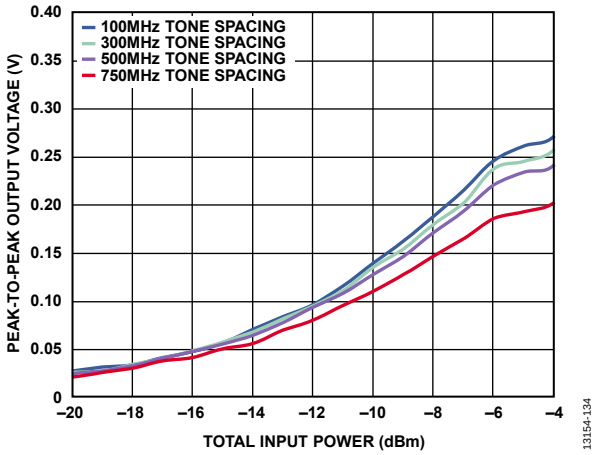

Figure 34. Envelope Detector Peak-to-Peak Output Voltage vs. Total Input Power at Various Tone Spacings, RF = 81 GHz, V_{CTL1}/V_{CTL2} = −5 V, V_{DET} = 4 V with 150 Ω Load Impedance at ENV_{DET}

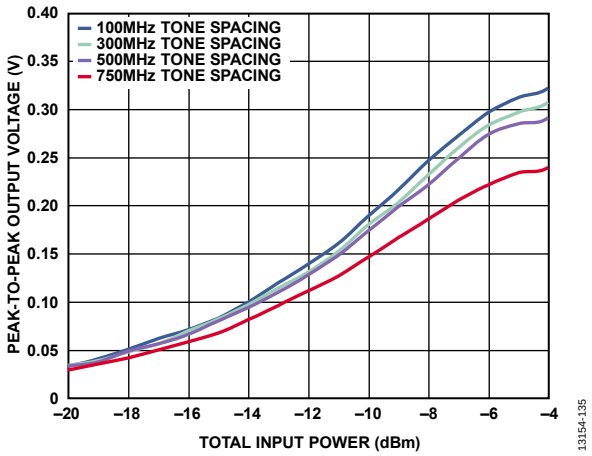

Figure 35. Envelope Detector Peak-to-Peak Output Voltage vs. Total Input Power at Various Tone Spacings, RF = 83.5 GHz, V_{CTL1}/V_{CTL2} = −5 V, V_{DET} = 4 V with 150 Ω Load Impedance at ENV_{DET}

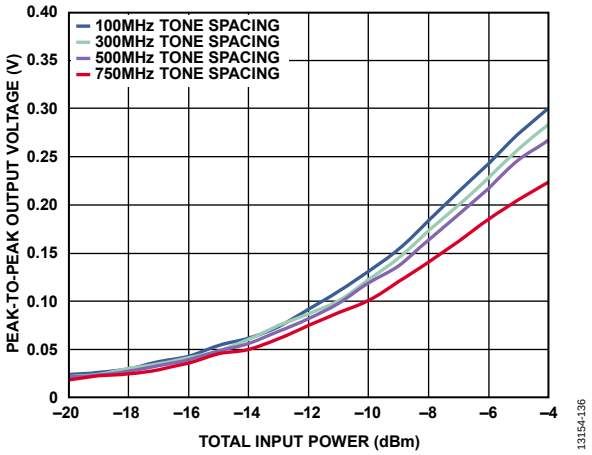

Figure 36. Envelope Detector Peak-to-Peak Output Voltage vs. Total Input Power at Various Tone Spacings, RF = 86 GHz, V_{CTL1}/V_{CTL2} = −5 V, V_{DET} = 4 V with 150 Ω Load Impedance at ENV_{DET}

THEORY OF OPERATION

The circuit architecture of the HMC8121 variable gain amplifier is shown in Figure 37. The HMC8121 uses multiple gain stages and staggered voltage variable attenuation stages to form a low noise, high linearity variable gain amplifier with a gain range of ~17 dB. The first stage is a low noise preamp, which is followed by the first voltage variable attenuator in the signal path. A portion of the signal is coupled away and further amplified before driving an on-chip envelope detector. The envelope detector provides an output that is proportional to the peak envelope power of the incoming signal. After the first attenuator, a second stage amplifier provides additional gain and isolation before driving the second variable attenuator block. Three cascaded gain stages follow the second variable attenuator. At the output of the last stage, another coupler taps off a small portion of the output signal. The coupled signal is presented to an on-chip diode detector for external monitoring of the output power. A matched reference diode is included to help correct for detector temperature dependencies. See the application circuit in Figure 38 for further details on biasing the different blocks and utilizing the detector features.

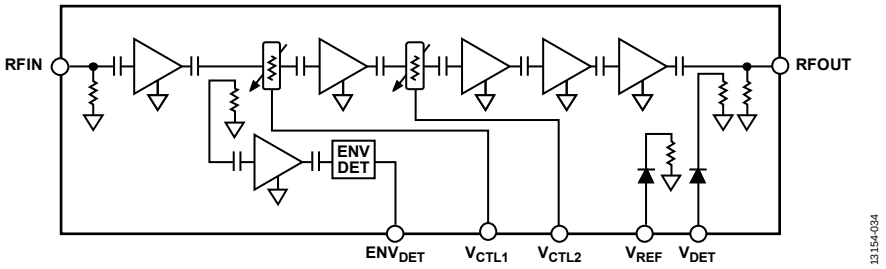

Figure 37. Variable Gain Amplifier Circuit Architecture

TYPICAL APPLICATION CIRCUIT

A typical application circuit for the HMC8121 is provided in Figure 38. For typical operation, drive the attenuator control pads from a single control voltage. It is important to bypass all the supply connections and attenuator control pads with adequate bypassing capacitors. Use single-layer chip capacitors with very high self-resonant frequency close to the HMC8121 die, bypassing each supply or control pad. Typically, 120 pF chip capacitors are used, followed by 0.01 µF and 4.7 µF surface-mount capacitors. Combine supply lines as shown in the application circuit schematic to minimize external component count and simplify power supply routing (see Figure 38). Pad 25 and Pad 26 are internally connected. Therefore, use either pad to connect the external bypass components of V_{DD1}/V_{DD2}.

The HMC8121 uses several amplifier, detector, and attenuator stages. All stages use depletion mode pHEMT transistors. It is important to follow the following power-up bias sequence to ensure transistor damage does not occur.

1. Apply a −5 V bias to the V_{CTL1} and V_{CTL2} pads.
2. Apply a −2 V bias to the V_{GG3} to V_{GG6} and V_{GG1}/V_{GG2} pads.
3. Apply 4 V to the V_{DD1} to V_{DD6} pads.
4. Adjust V_{GG1}/V_{GG2} and V_{GG3} to V_{GG6} between −2 V and 0 V to achieve a total amplifier drain current of 265 mA.

After bias is established, adjust the $V_{CTL1} = V_{CTL2}$ bias between −5 V and 0 V to achieve the desired gain.

To power down the HMC8121, follow the reverse procedure.

For additional guidance on general bias sequencing, see the *MMIC Amplifier Biasing Procedure* application note.

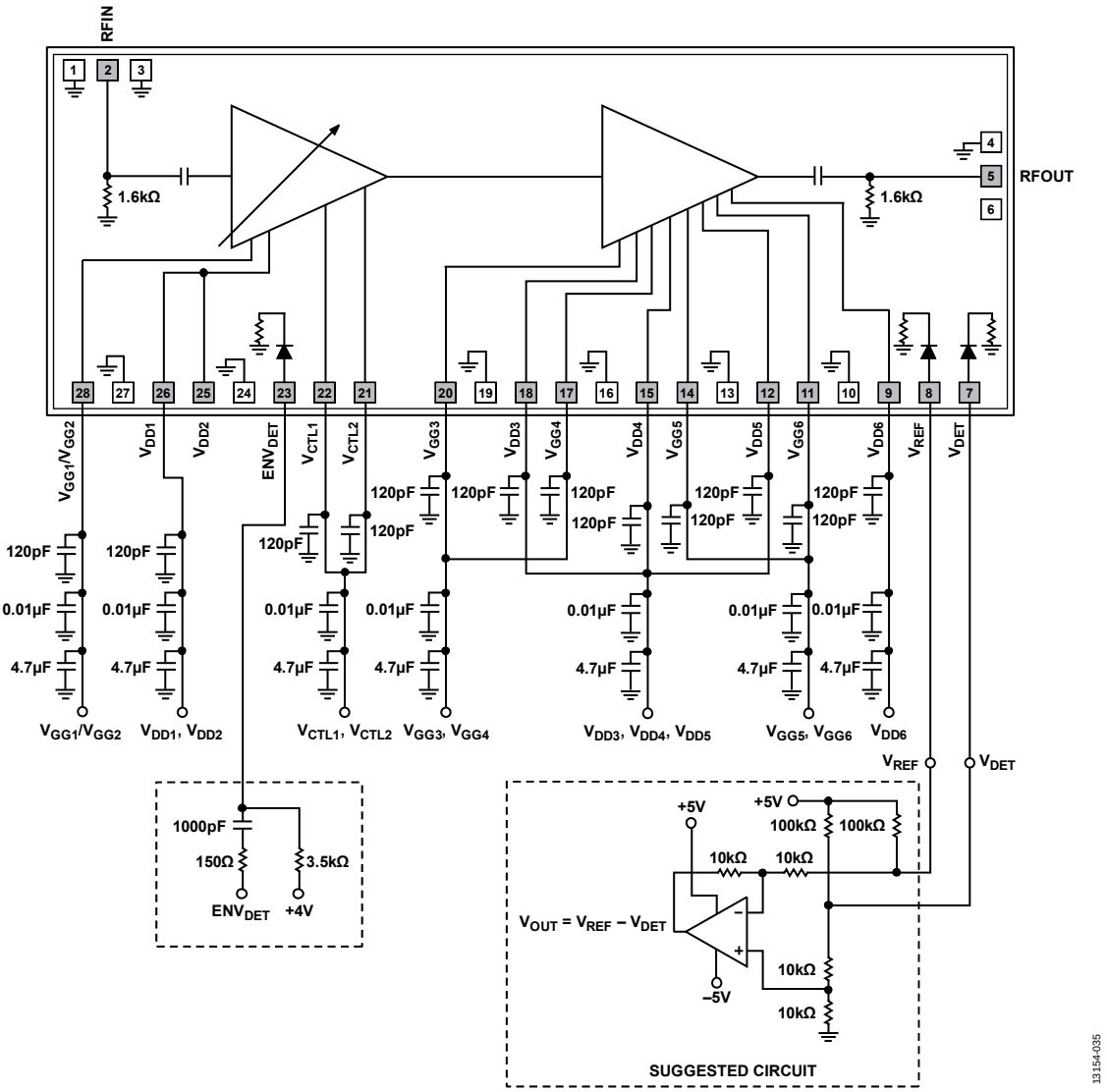

Figure 38. Typical Application Circuit

ASSEMBLY DIAGRAM

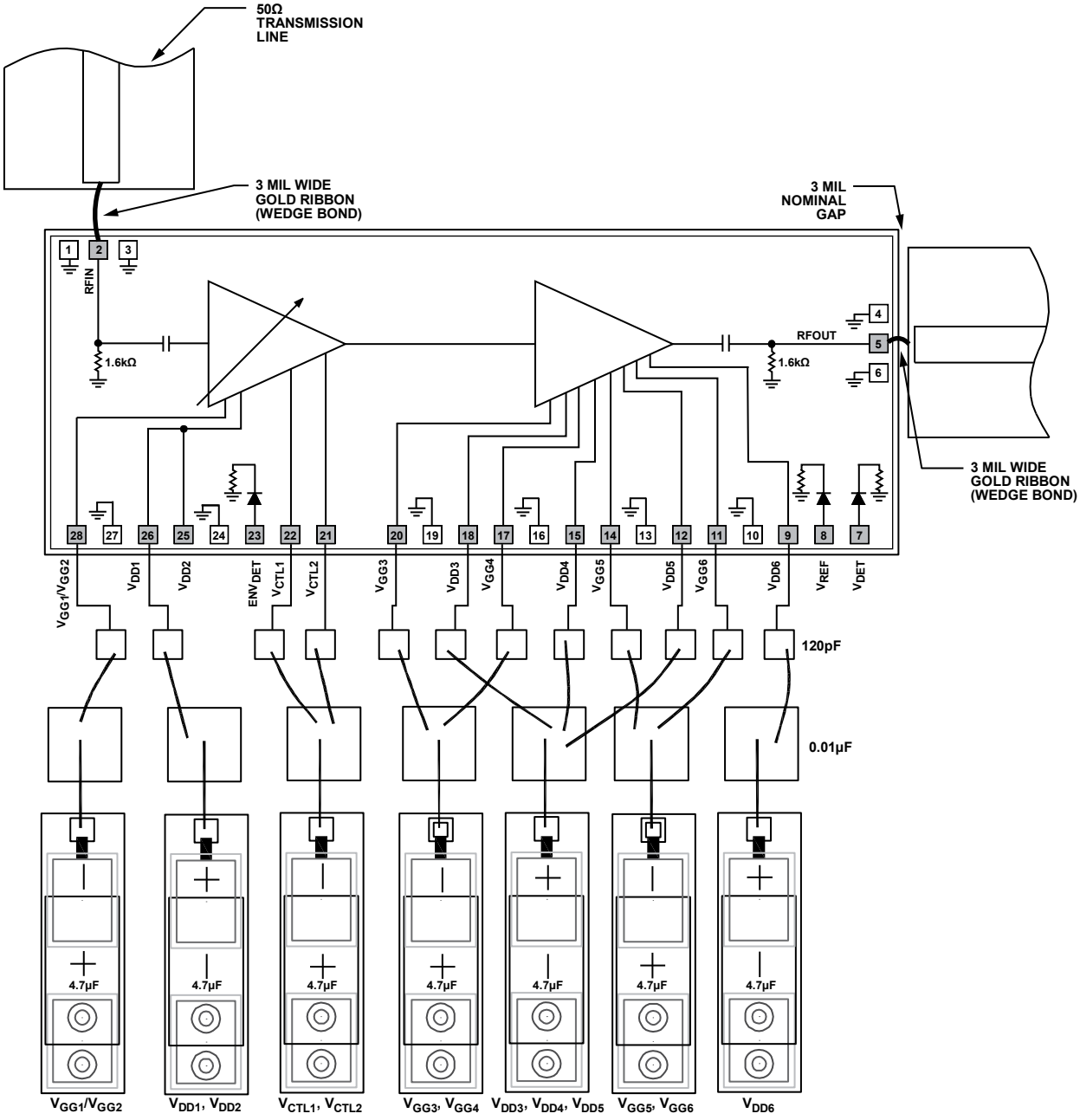

Figure 39. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 40).

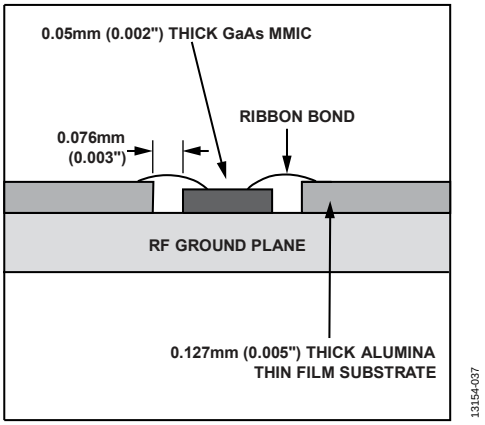

Figure 40. Routing RF Signals

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the following precautions.

Storage

All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% gold/20% tin preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

ABLEBOND 84-1LMIT is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with 0.003 in. × 0.0005 in. gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 0.001 in. (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

OUTLINE DIMENSIONS

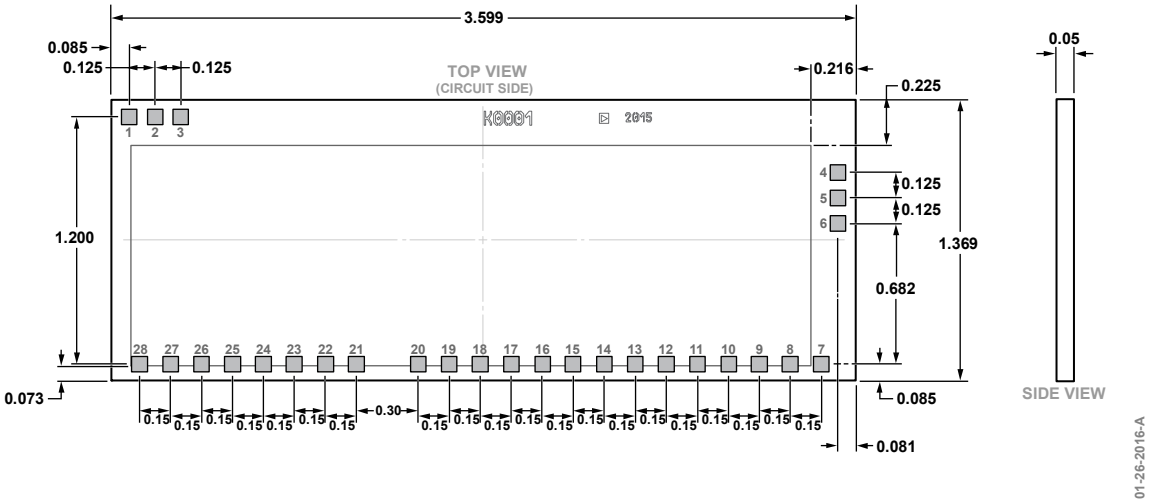

Figure 41. 28-Pad Bare Die [CHIP]
(C-28-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
HMC8121	−55°C to +85°C	28-Pad Bare Die [CHIP]	C-28-1
HMC8121-SX	−55°C to +85°C	28-Pad Bare Die [CHIP]	C-28-1

[1] The HMC8121-SX is two pairs of the die in a gel pack for the sample orders.
[2] This is a waffle pack option; contact Analog Devices, Inc., sales representatives for additional packaging options.

D13154-0-2/16(A)