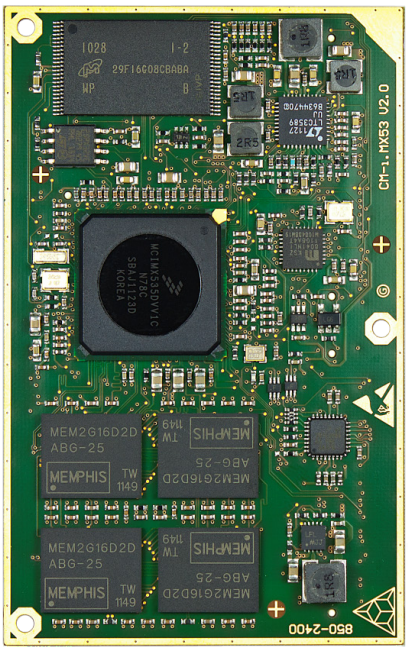
BLUETECHNIX
Embedding Ideas

CM-i.MX53



Hardware User Manual

Version 2.3

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Information

For further information on technology, delivery terms and conditions and prices please contact Bluetechnix (http://www.bluetechnix.com).

Warning

Due to technical requirements components may contain dangerous substances.

1 Introduction

The Core Module CM-i.MX53 is based on Freescale's next generation, high-performance, power-efficient, consumer multimedia applications processor i.MX53. This processor features OpenGL® ES 2.0 and OpenVG™ 1.1 hardware accelerators, a multi-format HD1080p video decoder and a HD720P video encoder hardware engine, dual display capability, a SATA controller, IEEE1588 time-stamping and numerous serial interfaces (SDIO, SPI, I2C, UART). Further features are integrated security solutions, USB 2.0 controllers, Ethernet controller and a camera input (CSI). The Core Module is available for both commercial and industrial temperature range. It addresses 1GByte DDR2-SDRAM, has an on-board NAND flash of 2GByte and an additional SPI-NOR flash of 4MByte.

The state of the art i.MX53 SoC in combination with the outstanding integration of several peripheral controllers, memory and voltage control, turn the CM-i.MX53 into a high-performance embedded platform for your future applications.

1.1 Overview

Figure 1-1 shows the main components of Core Module CM-i.MX53.

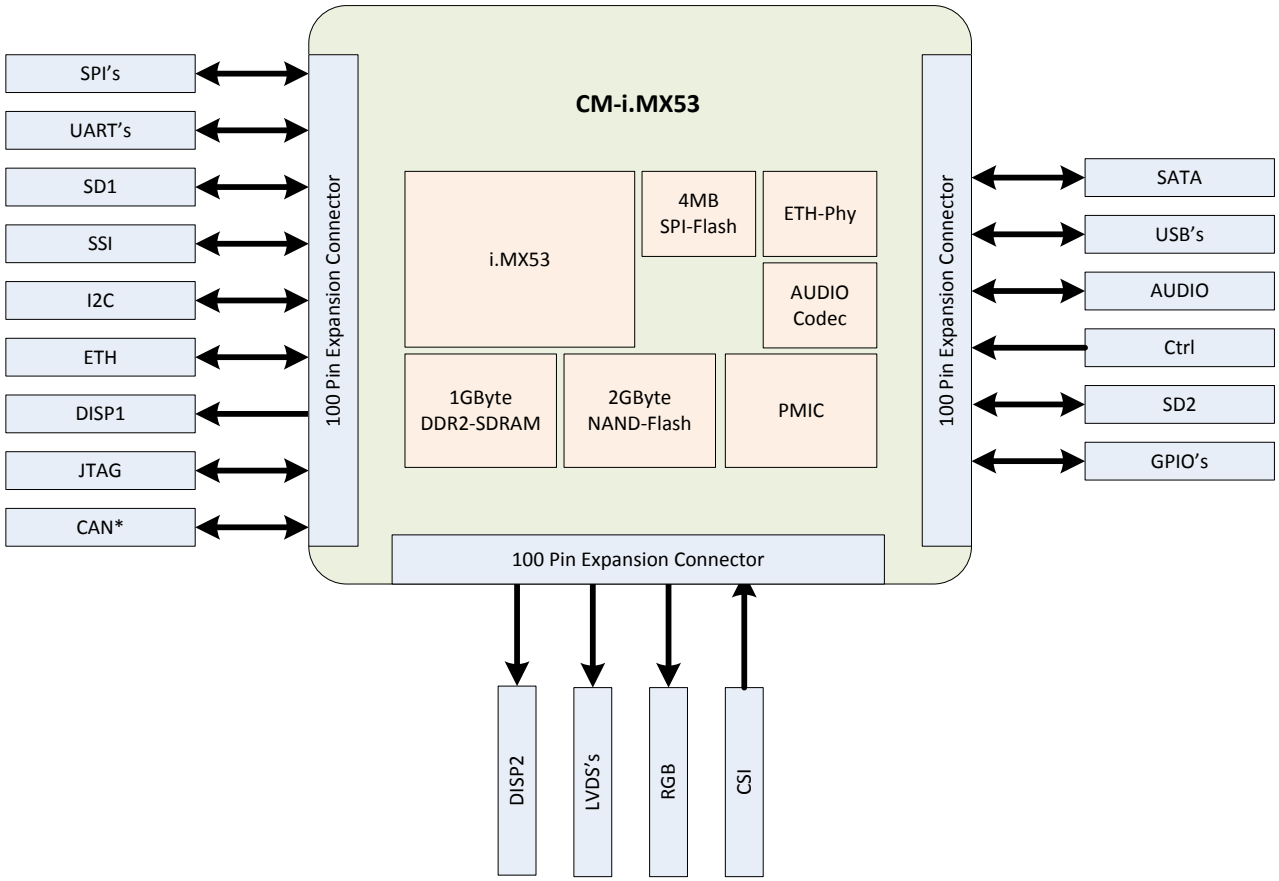

Figure 1-1: Main components of the CM-i.MX53 Core Module

* Depends on version – see chapter 8.1

1.2 Key Features

- **Freescale Application Processor i.MX53**
  - Industrial version (see chapter 8.1)
    MCIMX537CVV8C
  - Commercial version (see chapter 8.1)
    - MCIMX535DVV1C
- **1 GB DDR2-SDRAM**
  - Industrial version (see chapter 8.1)
    - MEM2G16D2DABG-25I
    - DDR2-SDRAM Clock up to 400MHz
    - 4x (128Mx16, 1Gbit at 1.8V)
  - Commercial version (see chapter 8.1)
    - MEM2G16D2DABG-25
    - DDR2-SDRAM Clock up to 400MHz
    - 4x (128Mx16, 1Gbit at 1.8V)
- **2 GB NAND-Flash**
  - Industrial version (see chapter 8.1)
    - MT29F16G08ABACAWP-IT:C
    - (16Gbit at 3.3V)
  - Commercial version (see chapter 8.1)
    - MT29F16G08CBABAWP:B
    - (16Gbit at 3.3V)
- **4 MB SPI-Flash**
  - M25PX32-VMW6E
  - (32Mbit at 3.3V)
- **PMIC**
  - LTC3589 & ADP2119
  - Energy Management
  - Power-up sequencer
- **Audio Codec**
  - SGTL5000XNAA3R2
- **Ethernet-Physical**
  - KSZ8041NLI
- **Connectors**
  - 3x UART
  - 2x SPI
  - 2x I^2C
  - CAN *
  - 2x SD
  - 2x DISP
  - 2x LVDS
  - CSI
  - ETH
  - USBOTG

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- USBH
- SATA
- Audio
- GPIO's
- CTRL
- JTAG
- Power Supply

* CAN is only available on the industrial version of the i.MX53! Depends on version – see chapter 8.1

1.3 Applications

- Tablets
- Smart Mobile Devices
- Human-Machine-Interface
- Medical Devices
- Video Conference Systems
- Imaging and Consumer Multimedia
- Set Top Boxes
- Video Conference Applications
- Portable Media Players
- Industrial Applications

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2 General Description

2.1 Functional Description

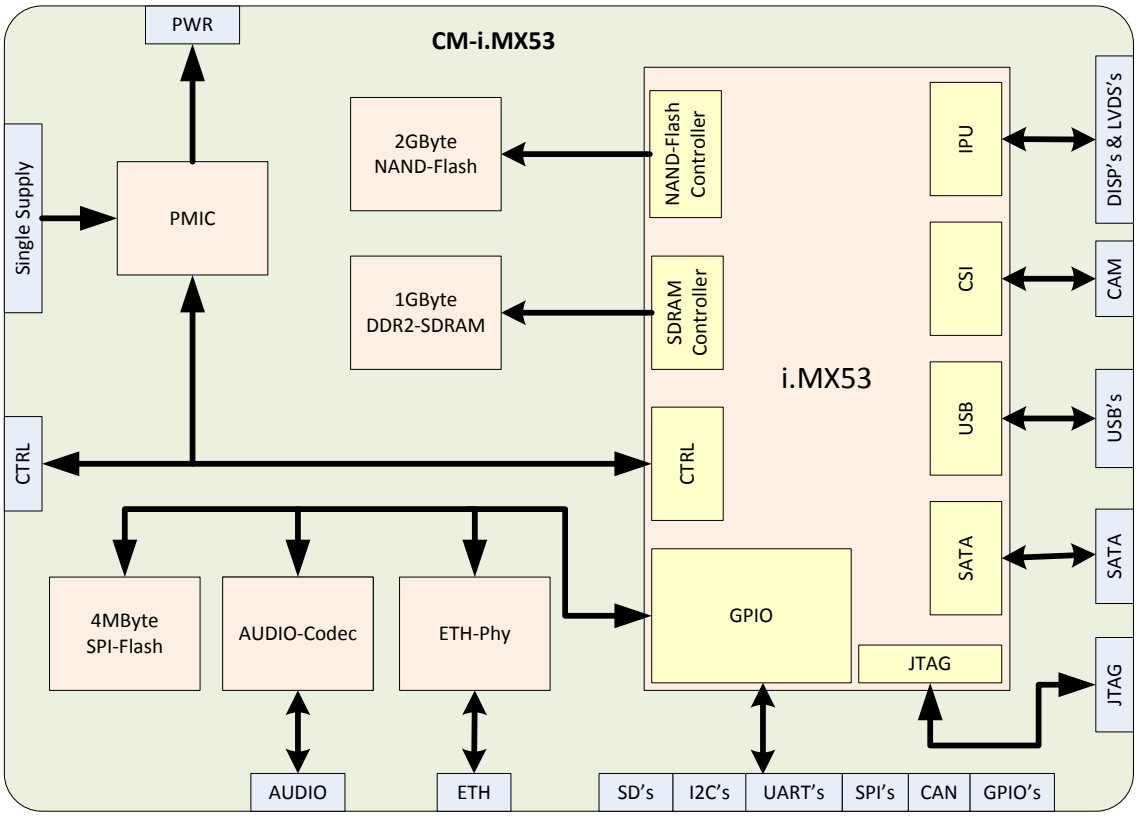

Figure 2-1: Functional overview

* CAN is only available at the industrial version of the i.MX53! Depends on version – see chapter 8.1

2.2 Boot Mode

The overall boot mode of the i.MX53 processor is determined by the BOOT_MODE[0..1] pins. For internal boot mode (BOOT_MODE[0..1] = 00), boot media is selected either by internal fuses, or by GPIOs which are sampled at power-up. For burning boot fuses, please consult the i.MX53 Reference Manual and the Software User Manual for the CM-i.MX53.

If boot media selection by GPIO sampling is desired, pull-down or pull-up resistors must be added to the specified pins. 4k7 Ohm resistors are recommended. See chapter 4 for the voltage level of these pins.

Table 1 contains permitted configuration options of BOOT_MODE pins, where “0” means a pull-down resistor is required, and “1” means a pull-up resistor is required.

Pin	Internal (see below)	USB/UART	Fuses
BOOT_MODE[1]	0	1	1
BOOT_MODE[0]	0	1	0

Table 1: Boot mode pins

Table 2 contains of the fuse/GPIO settings for the internal boot mode. *An empty cell means that this pin's value is not considered for a specific boot setting*.

Settings for SPI-NOR flash, NAND flash, and SATA disk are determined by the Core Module only. Settings for SD and MMC card are determined by the base board and may vary.

Settings that are open to the designer of a base board are marked with an asterisk (*). Please consult the i.MX53 Reference Manual for details.

eFuse Name	CM-i.MX53 Pin	SPI-NOR	NAND	SATA	SD (ESDHC3)	MMC (ESDHC3)
BOOT_CFG1[0]	ECSPI2.SS1	1	1	1	1	1
BOOT_CFG1[1]	DISP1.CLK	0*	0*	0*	0*	0*
BOOT_CFG1[2]	DISP1.D12		0			
BOOT_CFG1[3]	DISP1.D13	1	1	1	1*	1*
BOOT_CFG1[4]	DISP1.D14	1	0	0	1*	1*
BOOT_CFG1[5]	DISP1.D15	1	0	1	0	1
BOOT_CFG1[6]	DISP1.D16	0	0	0	1	1
BOOT_CFG1[7]	DISP1.D17	0	1	0	0	0
BOOT_CFG2[2]	DISP1.D6		0			
BOOT_CFG2[3]	DISP1.D7	1	1	1	1	1
BOOT_CFG2[4]	DISP1.D8	0*	0*	0*	0*	0*
BOOT_CFG2[5]	DISP1.D9	1	0		1	1
BOOT_CFG2[6]	DISP1.D10		1			0
BOOT_CFG2[7]	DISP1.D11		1			0*
BOOT_CFG3[1]	DISP1.DE		0 (Industrial) 1 (Commercial)			
BOOT_CFG3[2]	DISP1.D0	1	1	1	1	1
BOOT_CFG3[3]	DISP1.D1	0	0		0	0 (1)
BOOT_CFG3[4]	DISP1.D2	0	1		0	0
BOOT_CFG3[5]	DISP1.D3	1	1		1	1
BOOT_CFG3[6]	DISP1.D4		0			
BOOT_CFG3[7]	DISP1.D5		0			

Table 2: Boot configuration pins

The following additional boot sources are untested and not available on the DEV-i.MX53 evaluation board.

- SD or MMC on ESDHC2 interface (8-bit data width)
- SPI memory on ECSPI-1 or ECSPI-2 interfaces
- I2C memory on I2C-1 or I2C-3 interfaces

Please consult the i.MX53 Data Sheet and Reference Manual for IOMUX configuration and boot pins settings. Bluetechnix will support you finding a custom solution!

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2.3 Memory Map

Component	Memory area	Chip select
512 MB DDR2-800 SDRAM	0x7000_0000 – 0x8FFF_FFFF	CSD0
512 MB DDR2-800 SDRAM	0xB000_0000 – 0xCFFF_FFFF	CSD1

Table 3: Memory map

SPI-NOR and NAND flashes are not directly memory-mapped, but accessed via i.MX53 internal controllers. Please consult the i.MX53 Reference Manual for the i.MX53 memory map.

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3 Specifications

3.1 Electrical Specifications

3.1.1 Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit
V_{IN}	Input supply voltage	3.25	5.0	5.5	V
I_{IN}[1]	Input supply current @ V_{IN}=5.0V, T_{AMB}=25°C	TBD[1]	250[2]	2000[3]	mA
V_{OH}	High level output voltage	0.7*OVDD			V
V_{OL}	Low level output voltage			0.3*OVDD	V
I_{IH}[4]	IO input current	2		161	µA
I_{OZ}	Three state leakage current		TBD		µA
$I_{DEEPSLEEP}$	V_{IN} current in deep sleep mode		TBD		mA
I_{SLEEP}	V_{IN} current in sleep mode		TBD		mA
I_{IDLE}	V_{IN} current in deep sleep mode		TBD		mA
I_{400}	V_{IN} current in with core running at 400 MHz		TBD		mA
$I_{HIBERNATE}$	V_{IN} current in hibernate state		TBD		mA
I_{RTC}	V_{RTC} current			1	mA
f_{CCLKC}	Core clock frequency for industrial grade modules			800	MHz
f_{CCLKI}	Core clock frequency for commercial grade modules			1000	MHz

Table 4: Electrical characteristics

OVDD=Voltage Level look at section 4.

[1] Linux running in idle mode; TBD

[2] Linux writes file to SATA HDD; one USB devices plugged in; display output on HDMI interface; TBD

[3] Linux performing RAM Test; TBD

[4] Dependent on which internal Pull-up resistor is asserted

3.1.2 Maximum Ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only. Operation of the device at these or any other conditions greater than those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Min	Max	Unit
V_{IO}	Input or output voltage	-0.5	OVDD+0.3	V
V_{IN}	Input supply voltage	-0.3	6	V
I_{OH} /I_{OL}	Current per pin		10	mA
T_{AMBI}	Ambient temperature for industrial grade modules	-40	85[1]	°C
T_{AMBC}	Ambient temperature for commercial grade modules	0	70[1]	°C
T_{STO}	Storage temperature	-55	150	°C
φ_{AMB}	Relative ambient humidity		90	%

Table 5: Absolute maximum ratings

[1] If extreme high ambient temperatures are expected (75°C in industrial environments or 60°C for commercial products), the user has to apply a heat dissipator on CPU and DDR-RAM (avoid heat accumulation!). In

addition the die temperature should be monitored regularly, so that the CPU and RAM clock can be throttled if necessary.

3.1.3 Power Outputs

Symbol	Description	U [V]	I_{max}[1] [mA]
P_LDO1_1V3		1.3	10
P_LDO2_1V3		1.3	120
P_LDO3_1V8		1.8	200
P_LDO4_2V8		2.8	50
P_SW1_1V2		1.2	10
P_SW2_1V3		1.3	200
P_SW3_2V5		2.5	250
P_SW4_3V3		3.3	300
P_ANA_PLL_1V8		1.8	50
VA_ETH	Supply voltage for the Ethernet chokes	3.3	10

Table 6: Power Outputs

[1] I_{max}, an overstepping of this maximal current may cause permanent damage of the CM

The voltage levels and currents are only correct with the Bluetechnix default PMIC settings.

3.1.4 ESD Sensitivity

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

3.1.5 Cooling

If the core module is subject to high performance applications a passive or active cooling system should be planned to prevent damage to and guarantee the full functionality of the core module. The requirement of a cooling system depends also from the ambient temperature.

Following test was performed in a conditioning cabinet:

Firmware

- 1GHz Core clock
- 400MHz DDR2 clock
- Linux kernel running following tasks contemporaneously:
    - Audio test: record and play in a loop
    - GPU test: es11ex executed (high current consumption)
    - DDR2 memory test: linux memtest program, write/read 175MByte in a loop
    - NAND flash test: write/read with file system jffs2
    - SPI flash test: write/read with file system jffs2
    - USB test: write/read on USB stick with file system ext3

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Results

- Full functionality from 0°C to 50°C without heat sink on processor
- Full functionality from 0°C to 60°C with heat sink on processor

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4 Connector Description

For a detail signal description please consult the i.MX53 reference manual, available on the Freescale web site.

4.1 Connector X1

Pin No.	Signal Name	Type	Power Domain	Function	
1	ECSPI2.MISO	I	P_SW4_3V3	SPI MISO / GPIO2_25	
2	ECSPI2.MOSI	O	P_SW4_3V3	SPI MOSI / GPIO2_24	
3	ECSPI2.SCLK	O	P_SW4_3V3	SPI Clock / GPIO2_23	
4	ECSPI2.SS0	O	P_SW4_3V3	SPI Select 0 / GPIO2_26	
5	ECSPI2.SS1	O	P_SW4_3V3	SPI Select 1 / GPIO2_27	**BOOT_CFG1[0]**
6	P_SW4_3V3	PWR_O	3V3		
7	ECSPI1.MISO	I	P_SW4_3V3	SPI MISO / GPIO5_24	
8	ECSPI1.MOSI	O	P_SW4_3V3	SPI MOSI / GPIO5_23	
9	ECSPI1.SCLK	O	P_SW4_3V3	SPI CLK / GPIO5_22	
10	ECSPI1.SS0	O	P_SW4_3V3	SPI Select 0 / GPIO5_25	
11	ECSPI1.SS1	O	P_SW4_3V3	SPI Select 1 / GPIO3_19	
12	P_SW4_3V3	PWR_O	3V3		
13	SD.CMD	O	P_SW4_3V3	SD Command / GPIO7_4	
14	SD.CLK	O	P_SW4_3V3	SD Clock / GPIO7_5	
15	SD.D0	I/O	P_SW4_3V3	SD Data 0 / GPIO2_8	
16	SD.D1	I/O	P_SW4_3V3	SD Data 1 / GPIO2_9	
17	SD.D2	I/O	P_SW4_3V3	SD Data 2 / GPIO2_10	
18	SD.D3	I/O	P_SW4_3V3	SD Data 3 / GPIO2_11	
19	SD.CD	I	P_SW4_3V3	SD Card Detect / GPIO2_31	
20	SD.WP	I	P_SW4_3V3	SD Write Protect / GPIO3_15	
21	GND	PWR	GND		
22	UART3.RTS	O	P_SW4_3V3	UART Request To Send / GPIO7_8	
23	UART3.CTS	I	P_SW4_3V3	UART Clear To Send / GPIO7_7	
24	UART3.TXD	O	P_SW4_3V3	UART Transmit Data / GPIO7_9	
25	UART3.RXD	I	P_SW4_3V3	UART Receive Data / GPIO7_10	
26	P_SW4_3V3	PWR_O	3V3		
27	UART2.CTS	I	P_SW4_3V3	UART Clear To Send / GPIO7_2	
28	UART2.RTS	O	P_SW4_3V3	UART Request To Send / GPIO7_3	
29	UART2.TXD	O	P_SW4_3V3	UART Transmit Data / GPIO7_0	
30	UART2.RXD	I	P_SW4_3V3	UART Receive Data / GPIO7_1	
31	GND	PWR	GND		
32	OWIRE	I/O	P_SW4_3V3	One Wire Interface / GPIO7_6	
33	P_SW4_3V3	PWR_O	3V3		
34	AUD5.RSCK	I	P_SW4_3V3	AUD Receive Clock / GPIO3_25	
35	AUD5.RFS	I	P_SW4_3V3	AUD Receive Frame Sync / GPIO3_24	
36	AUD5.Rx	I	P_SW4_3V3	AUD Receive Data / GPIO4_9	
37	AUD5.TSCK	O	P_SW4_3V3	AUD Transmit Clock / GPIO4_6	
38	AUD5.Tx	O	P_SW4_3V3	AUD Transmit Data / GPIO4_7	
39	AUD5.TFS	O	P_SW3_2V5	AUD Transmit Frame Sync / GPIO5_12	
40	P_SW4_3V3	PWR_O	3V3		
41	I2C1.SCL	O	P_SW4_3V3	I2C Clock / GPIO5_27	

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Pin No.	Signal Name	Type	Power Domain	Function
42	I2C1.SDA	I/O	P_SW4_3V3	I2C Data / GPIO5_26
43	I2C3.SCL	O	P_SW4_3V3	I2C Clock / GPIO1_5
44	I2C3.SDA	I/O	P_SW4_3V3	I2C Data / GPIO1_6
45	P_LDO4_2V8	PWR_O	2V8	
46	JTAG.TCK	I	P_LDO4_2V8	JTAG Test Clock
47	JTAG.TMS	I	P_LDO4_2V8	JTAG Test Mode Select
48	JTAG.TDI	I	P_LDO4_2V8	JTAG Test Data Input
49	JTAG.TDO	O	P_LDO4_2V8	JTAG Test Data Output
50	JTAG.nTRST	I	P_LDO4_2V8	JTAG Test Reset
51	JTAG.nDE	I	P_LDO4_2V8	JTAG Debug / GPIO7_11
52	JTAG.MOD	I	P_LDO4_2V8	JTAG Mode Selection
53	ETH.LED_ACT	O	VA_ETH	ETH Activity LED Driver
54	ETH.LED_SPD	O	VA_ETH	ETH Speed LED Driver
55	VA_ETH	PWR_O	3V3	ETH Analog Voltage
56	ETH.Rx_N	I_DP	VA_ETH	ETH Receive Data-
57	ETH.Rx_P	I_DP	VA_ETH	ETH Receive Data+
58	GND	PWR	GND	
59	ETH.Tx_N	O_DP	VA_ETH	ETH Transmit Data-
60	ETH.Tx_P	O_DP	VA_ETH	ETH Transmit Data+
61	GND	PWR	GND	
62	CAN1.TX	O	P_SW4_3V3	CAN Transmit Data / GPIO4_10
63	CAN1.RX	I	P_SW4_3V3	CAN Receive Data / GPIO4_11
64	P_SW4_3V3	PWR_O	3V3	
65	UART1.RXD	I	P_SW4_3V3	UART Receive Data / GPIO6_18
66	UART1.TXD	O	P_SW4_3V3	UART Transmit Data / GPIO6_17
67	GND	PWR	GND	
68	P_VIN	PWR_I	VIN	
69	P_VIN	PWR_I	VIN	
70	P_VIN	PWR_I	VIN	
71	P_VIN	PWR_I	VIN	
72	P_VIN	PWR_I	VIN	
73	GND	PWR	GND	
74	RFU			
75	RFU			
76	DISP0.VSYNC	O	P_SW4_3V3	DISP Vertical Sync / GPIO3_18
77	DISP0.HSYNC	O	P_SW3_2V5	DISP Horizontal Sync / GPIO3_17
78	DISP0.CLK	O	P_SW3_2V5	DISP Clock / GPIO4_16
79	P_SW3_2V5	PWR_O	2V5	
80	DISP0.D17	O	P_SW3_2V5	DISP Data17 / GPIO5_11
81	DISP0.D16	O	P_SW3_2V5	DISP Data16 / GPIO5_10
82	DISP0.D15	O	P_SW3_2V5	DISP Data15 / GPIO5_9
83	DISP0.D14	O	P_SW3_2V5	DISP Data14 / GPIO5_8
84	DISP0.D13	O	P_SW3_2V5	DISP Data13 / GPIO5_7
85	DISP0.DE	O	P_SW3_2V5	DISP Data Enable / GPIO3_20
86	DISP0.D12	O	P_SW3_2V5	DISP Data12 / GPIO5_6
87	DISP0.D11	O	P_SW3_2V5	DISP Data11 / GPIO5_5
88	DISP0.D10	O	P_SW3_2V5	DISP Data10 / GPIO4_31
89	DISP0.D9	O	P_SW3_2V5	DISP Data9 / GPIO4_30
90	DISP0.D8	O	P_SW3_2V5	DISP Data8 / GPIO4_29
91	DISP0.D7	O	P_SW3_2V5	DISP Data7 / GPIO4_28

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Pin No.	Signal Name	Type	Power Domain	Function
92	GND	PWR	GND	
93	DISP0.D6	O	P_SW3_2V5	DISP Data6 / GPIO4_27
94	DISP0.D5	O	P_SW3_2V5	DISP Data5 / GPIO4_26
95	DISP0.D4	O	P_SW3_2V5	DISP Data4 / GPIO4_25
96	DISP0.D3	O	P_SW3_2V5	DISP Data3 / GPIO4_24
97	DISP0.D2	O	P_SW3_2V5	DISP Data2 / GPIO4_23
98	DISP0.D1	O	P_SW3_2V5	DISP Data1 / GPIO4_22
99	DISP0.D0	O	P_SW3_2V5	DISP Data0 / GPIO4_21
100	P_SW3_2V5	PWR_O	2V5	
301	GND	SHIELD		
302	GND	SHIELD		
303	GND	SHIELD		
304	GND	SHIELD		
305	GND	SHIELD		
306	GND	SHIELD		
307	GND	SHIELD		
308	GND	SHIELD		
309	GND	SHIELD		
310	GND	SHIELD		

Table 7: Connector description X1

4.2 Connector X2

Pin No.	Signal Name	Type	Power Domain	Function
101	SATA.TX_N	O_DP	P_SW3_2V5	SATA Transmit Data-
102	SATA.TX_P	O_DP	P_SW3_2V5	SATA Transmit Data+
103	SATA.TCK		P_SW3_2V5	SATA Test Clock / GPIO5_16
104	SATA.TDI		P_SW3_2V5	SATA Test Data Input / GPIO5_14
105	SATA.TDO		P_SW3_2V5	SATA Test Data Output / GPIO5_15
106	SATA.TMS		P_SW3_2V5	SATA Test Mode Section / GPIO5_17
107	P_SW3_2V5	PWR_O	2V5	
108	USBH1.VBUS	PWR	5V0	USB VBUS
109	USBH1.OC	I	P_SW4_3V3	USB Over Current / GPIO1_3
110	USBH1.PWR	O	P_SW4_3V3	USB Power Enable / GPIO1_0
111	USBOTG.OC	I	P_SW4_3V3	USB Over Current / GPIO4_14
112	USBOTG.PWR	O	P_SW4_3V3	USB Power Enable / GPIO4_15
113	USBOTG.ID	I	P_SW4_3V3	USB ID
114	GND	PWR	P_SW4_3V3	
115	AUD.MICBIAS	AO	3V3	AUDIO Microphone Bias
116	AUD.MIC	AI	3V3	AUDIO Microphone
117	GND	PWR	GND	
118	AUD.LIN.L	AI	3V3	AUDIO Line-In Left
119	AUD.LIN.R	AI	3V3	AUDIO Line-In Right
120	GND	PWR	GND	
121	AUD.LOUT.L	AO	3V3	AUDIO Line-Out Left
122	AUD.LOUT.R	AO	3V3	AUDIO Line-Out Right
123	AUD.HP.L	AO	3V3	AUDIO Headphone Left
124	HP_GND	PWR	GND	AUDIO Headphone GND
125	AUD.HP.R	AO	3V3	AUDIO Headphone Right

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Pin No.	Signal Name	Type	Power Domain	Function
126	CTRL.PWM1	O	P_SW4_3V3	Pulse Width Modulation Output / GPIO1_9
127	CTRL.PWM2	O	P_SW3_2V5	Pulse Width Modulation Output / GPIO1_19
128	VDD_FUSE	PWR	3V3	Fuse Programming Voltage (leave unconnected if unused)
129	CTRL.PWR_ON	I	P_ANA_PLL_1V8	
130	P_ANA_PLL_1V8	PWR_O	1V8	
131	CTRL.nRESET_IN	I	P_ANA_PLL_1V8	Soft Reset
132	CTRL.nPOR	I 10k Pull-Up	P_ANA_PLL_1V8	Hard Reset
133	CTRL.ON	I/O	P_LDO1_1V3	Start-Up PMIC if PIN is low for 400ms
134	CTRL.nVSTY	O	P_LDO1_1V3	
135	CTRL.nWDI	O	P_SW4_3V3	
136	P_LDO1_1V3	PWR_O	1V3	
137	GND	PWR	GND	
138	RFU			
139	RFU			
140	RFU			
141	RFU			
142	P_SW4_3V3	PWR_O	3V3	
143	GPIO.(3V3)_0	I/O	P_SW4_3V3	GPIO3_23
144	GPIO.(3V3)_1	I/O	P_SW4_3V3	GPIO3_14
145	GPIO.(3V3)_2	I/O	P_SW4_3V3	GPIO3_13
146	GPIO.(3V3)_3	I/O	P_SW4_3V3	GPIO4_5 / CLKO
147	RFU			
148	RFU			
149	RFU			
150	GND	PWR	GND	
151	GND	PWR	GND	
152	GPIO.(2V8)_4	I/O	P_LDO4_2V8	GPIO4_4
153	GPIO.(2V8)_3	I/O	P_LDO4_2V8	GPIO4_3
154	GPIO.(2V8)_2	I/O	P_LDO4_2V8	GPIO4_2
155	GPIO.(2V8)_1	I/O	P_LDO4_2V8	GPIO4_1
156	GPIO.(2V8)_0	I/O	P_LDO4_2V8	GPIO4_0
157	P_LDO4_2V8	PWR_O	2V8	
158	GND	PWR	GND	
159	GPIO.(2V5)_3	I/O	P_SW3_2V5	GPIO5_13
160	GPIO.(2V5)_2	I/O	P_SW3_2V5	GPIO1_18
161	GPIO.(2V5)_1	I/O	P_SW3_2V5	GPIO1_17
162	GPIO.(2V5)_0	I/O	P_SW3_2V5	GPIO1_16
163	P_SW3_2V5	PWR_O	2V5	
164	CTRL.BM1	I	P_ANA_PLL_1V8	Boot Mode1
165	CTRL.BM0	I	P_ANA_PLL_1V8	Boot Mode0
166	VIN	PWR_I	VIN	
167	VIN	PWR_I	VIN	
168	VIN	PWR_I	VIN	
169	VIN	PWR_I	VIN	
170	GND	PWR	GND	
171	GND	PWR	GND	
172	GND	PWR	GND	
173	GND	PWR	GND	
174	SD2.WP	I	P_SW4_3V3	SD Write Protect / GPIO1_2
175	SD2.CD	I	P_SW4_3V3	SD Card Detect / GPIO2_31

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Pin No.	Signal Name	Type	Power Domain	Function
176	SD2.D7	I/O	P_SW4_3V3	SD Data7 / GPIO2_15
177	SD2.D6	I/O	P_SW4_3V3	SD Data6 / GPIO2_14
178	SD2.D5	I/O	P_SW4_3V3	SD Data5 / GPIO2_13
179	SD2.D4	I/O	P_SW4_3V3	SD Data4 / GPIO2_12
180	P_SW4_3V3	PWR_O	3V3	
181	SD2.D3	I/O	P_SW4_3V3	SD Data3 / GPIO1_12
182	SD2.D2	I/O	P_SW4_3V3	SD Data2 / GPIO1_13
183	SD2.D1	I/O	P_SW4_3V3	SD Data1 / GPIO1_14
184	SD2.D0	I/O	P_SW4_3V3	SD Data0 / GPIO1_15
185	SD2.CLK	O	P_SW4_3V3	SD CLK / GPIO1_10
186	SD2.CMD	O	P_SW4_3V3	SD Command / GPIO1_11
187	GND	PWR	GND	
188	USBOTG.VBUS	PWR	5V0	USB VBUS
189	USBOTG.D_P	I/O_DP	5V0	USB Data+
190	USBOTG.D_N	I/O_DP	5V0	USB Data-
191	GND	PWR	GND	
192	USBH1.D_P	I/O_DP	5V0	USB Data+
193	USBH1.D_N	I/O_DP	5V0	USB Data-
194	SATA.DTB1		P_SW3_2V5	SATA xx / GPIO1_21
195	SATA.DTB0		P_SW3_2V5	SATA xx / GPIO1_20
196	SATA.REFCLK_P	I_DP	P_SW3_2V5	SATA Reference Clock+
197	SATA.REFCLK_N	I_DP	P_SW3_2V5	SATA Reference Clock-
198	GND	PWR	GND	
199	SATA.RX_P	I_DP	P_SW3_2V5	SATA Receive Data+
200	SATA.RX_N	I_DP	P_SW3_2V5	SATA Receive Data-
311	GND	SHIELD		
312	GND	SHIELD		
313	GND	SHIELD		
314	GND	SHIELD		
315	GND	SHIELD		
316	GND	SHIELD		
317	GND	SHIELD		
318	GND	SHIELD		
319	GND	SHIELD		
320	GND	SHIELD		

Table 8: Connector description X2

4.3 Connector X3

Pin No.	Signal Name	Type	Voltage Level	Function	
201	P_SW3_2V5	PWR_O	2V5		
202	DISP1.D14	O	P_SW4_3V3	DISP Data14 / GPIO2_19	**BOOT_CFG1[4]**
203	DISP1.D15	O	P_SW4_3V3	DISP Data15 / GPIO2_18	**BOOT_CFG1[5]**
204	DISP1.D16	O	P_SW4_3V3	DISP Data16 / GPIO2_17	**BOOT_CFG1[6]**
205	DISP1.D17	O	P_SW4_3V3	DISP Data17 / GPIO2_16	**BOOT_CFG1[7]**
206	DISP1.D18	O	P_SW4_3V3	DISP Data18 / GPIO6_6	
207	DISP1.D19	O	P_SW4_3V3	DISP Data19 / GPIO5_4	
208	DISP1.D20	O	P_SW4_3V3	DISP Data20 / GPIO3_31	
209	DISP1.D21	O	P_SW4_3V3	DISP Data21 / GPIO3_30	
210	DISP1.D22	O	P_SW4_3V3	DISP Data22 / GPIO3_26	

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Pin No.	Signal Name	Type	Voltage Level	Function	
211	DISP1.D23	O	P_SW4_3V3	DISP Data23 / GPIO3_27	
212	DISP1.CLK	O	P_SW4_3V3	DISP Clock / GPIO2_22	**BOOT_CFG1[1]**
213	DISP1.HSYNC	O	P_SW4_3V3	DISP Horizontal Sync / GPIO3_11	
214	DISP1.VSYNC	O	P_SW4_3V3	DISP Vertical Sync / GPIO3_12	
215	DISP1.DE	O	P_SW4_3V3	DISP Data Enable / GPIO3_10	**BOOT_CFG3[1]**
216	LVDS0.TX3_P	O_DP	P_SW3_2V5	LVDS Transmit Data3+ / GPIO7_22	
217	LVDS0.TX3_N	O_DP	P_SW3_2V5	LVDS Transmit Data3- / GPIO7_23	
218	LVDS0.TX2_P	O_DP	P_SW3_2V5	LVDS Transmit Data2+ / GPIO7_26	
219	LVDS0.TX2_N	O_DP	P_SW3_2V5	LVDS Transmit Data2- / GPIO7_27	
220	LVDS0.TX1_P	O_DP	P_SW3_2V5	LVDS Transmit Data1+ / GPIO7_28	
221	LVDS0.TX1_N	O_DP	P_SW3_2V5	LVDS Transmit Data1- / GPIO7_29	
222	LVDS0.TX0_P	O_DP	P_SW3_2V5	LVDS Transmit Data0+ / GPIO7_30	
223	LVDS0.TX0_N	O_DP	P_SW3_2V5	LVDS Transmit Data0- / GPIO7_31	
224	LVDS0.CLK_P	O_DP	P_SW3_2V5	LVDS Clock+ / GPIO7_24	
225	LVDS0.CLK_N	O_DP	P_SW3_2V5	LVDS Clock- / GPIO7_25	
226	GND	PWR	GND		
227	FIRI.RXD	I	P_SW4_3V3	FIRI Receive Data / GPIO1_7	
228	FIRI.TXD	O	P_SW4_3V3	FIRI Transmit Data / GPIO1_8	
229	GND	PWR	GND		
230	RGB.R	O	P_LDO4_2V8	AV Out Red	
231	RGB.R_B	I	P_LDO4_2V8	AV Out Red_Back	
232	RGB.G	O	P_LDO4_2V8	AV Out Green	
233	RGB.G_B	I	P_LDO4_2V8	AV Out Green_Back	
234	RGB.B	O	P_LDO4_2V8	AV Out Blue	
235	RGB.B_B	I	P_LDO4_2V8	AV Out Blue_Back	
236	RFU				
237	RFU				
238	RFU				
239	RFU				
240	RFU				
241	GND	PWR	GND		
242	RFU				
243	RFU				
244	RFU				
245	RFU				
246	RFU				
247	RFU				
248	RFU				
249	RFU				
250	RFU				
251	RFU				
252	RFU				
253	RFU				
254	RFU				
255	EN_PERI	O	P_SW4_3V3	Enable Signal for Peripheral Supply	
256	EIM_WAIT	O	P_SW4_3V3	EIM WAIT / GPIO5_0	
257	EIM_BLCK	O	P_SW4_3V3	EIM Burst Clock	
258	P_SW4_3V3	PWR_O	3V3		
259	CSI0.DE	I	P_SW4_3V3	CSI Data Enable / GPIO5_20	
260	CSI0.PCLK	I	P_SW4_3V3	CSI Pixel Clock / GPIO5_18	
261	CSI0.HSYNC	I	P_SW4_3V3	CSI Data Enable / GPIO5_19	

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Pin No.	Signal Name	Type	Voltage Level	Function	
262	CSI0.VSYNC	I	P_SW4_3V3	CSI Vertical Sync / GPIO5_21	
263	GND	PWR	GND		
264	CSI0.D9	I	P_SW4_3V3	CSI Data9 / GPIO6_5	
265	CSI0.D8	I	P_SW4_3V3	CSI Data8 / GPIO6_4	
266	CSI0.D7	I	P_SW4_3V3	CSI Data7 / GPIO6_3	
267	CSI0.D6	I	P_SW4_3V3	CSI Data6 / GPIO6_2	
268	CSI0.D5	I	P_SW4_3V3	CSI Data5 / GPIO6_1	
269	P_SW4_3V3	PWR_O	P_SW4_3V3		
270	CSI0.D4	I	P_SW4_3V3	CSI Data4 / GPIO6_0	
271	CSI0.D3	I	P_SW4_3V3	CSI Data3 / GPIO5_31	
272	CSI0.D2	I	P_SW4_3V3	CSI Data2 / GPIO5_30	
273	CSI0.D1	I	P_SW4_3V3	CSI Data1 / GPIO5_29	
274	CSI0.D0	I	P_SW4_3V3	CSI Data0 / GPIO5_28	
275	P_SW3_2V5	PWR_O	2V5		
276	LVDS1.CLK_N	O_DP	P_SW3_2V5	LVDS CLK- / GPIO6_27	
277	LVDS1.CLK_P	O_DP	P_SW3_2V5	LVDS CLK+ / GPIO6_26	
278	LVDS1.TX0_N	O_DP	P_SW3_2V5	LVDS Transmit Data 0- / GPIO6_31	
279	LVDS1.TX0_P	O_DP	P_SW3_2V5	LVDS Transmit Data 0+ / GPIO6_30	
280	LVDS1.TX1_N	O_DP	P_SW3_2V5	LVDS Transmit Data 1- / GPIO6_29	
281	LVDS1.TX1_P	O_DP	P_SW3_2V5	LVDS Transmit Data 1+ / GPIO6_28	
282	LVDS1.TX2_N	O_DP	P_SW3_2V5	LVDS Transmit Data 2- / GPIO6_25	
283	LVDS1.TX2_P	O_DP	P_SW3_2V5	LVDS Transmit Data 2+ / GPIO6_24	
284	LVDS1.TX3_N	O_DP	P_SW3_2V5	LVDS Transmit Data 3- / GPIO6_23	
285	LVDS1.TX3_P	O_DP	P_SW3_2V5	LVDS Transmit Data 3+ / GPIO6_22	
286	DISP1.D13	O	P_SW4_3V3	DISP Data13 / GPIO2_20	**BOOT_CFG1[3]**
287	DISP1.D12	O	P_SW4_3V3	DISP Data12 / GPIO2_21	**BOOT_CFG1[2]**
288	DISP1.D11	O	P_SW4_3V3	DISP Data11 / GPIO2_28	**BOOT_CFG2[7]**
289	DISP1.D10	O	P_SW4_3V3	DISP Data10 / GPIO2_29	**BOOT_CFG2[6]**
290	DISP1.D9	O	P_SW4_3V3	DISP Data9 / GPIO3_0	**BOOT_CFG2[5]**
291	DISP1.D8	O	P_SW4_3V3	DISP Data8 / GPIO3_1	**BOOT_CFG2[4]**
292	DISP1.D7	O	P_SW4_3V3	DISP Data7 / GPIO3_2	**BOOT_CFG2[3]**
293	GND	PWR	GND		
294	DISP1.D6	O	P_SW4_3V3	DISP Data6 / GPIO3_3	**BOOT_CFG2[2]**
295	DISP1.D5	O	P_SW4_3V3	DISP Data5 / GPIO3_4	**BOOT_CFG3[7]**
296	DISP1.D4	O	P_SW4_3V3	DISP Data4 / GPIO3_5	**BOOT_CFG3[6]**
297	DISP1.D3	O	P_SW4_3V3	DISP Data3 / GPIO3_6	**BOOT_CFG3[5]**
298	DISP1.D2	O	P_SW4_3V3	DISP Data2 / GPIO3_7	**BOOT_CFG3[4]**
299	DISP1.D1	O	P_SW4_3V3	DISP Data1 / GPIO3_8	**BOOT_CFG3[3]**
300	DISP1.D0	O	P_SW4_3V3	DISP Data0 / GPIO3_9	**BOOT_CFG3[2]**
321	GND	SHIELD			
322	GND	SHIELD			
323	GND	SHIELD			
324	GND	SHIELD			
325	GND	SHIELD			
326	GND	SHIELD			
327	GND	SHIELD			
328	GND	SHIELD			
329	GND	SHIELD			
330	GND	SHIELD			

Table 9: Connector description X3

5 Application Information/Guidelines

5.1 Supply Voltage Decoupling

For better stability we recommend to add a 100nF capacitor to each power supply pin and an additional 47µF tantalum capacitor to the V_{IN} voltage rail next to the module.

5.2 Power Outputs

For better stability we recommend to add a 100nF capacitor to each used power output pin and an additional 2.2µF tantalum capacitor to each voltage rail next to the module.

5.3 Peripheral Supply

NOTE: **EN_PERI** (Pin 255) indicates when the base board is permitted to power its peripherals. Do not power your peripherals until this signal line is high, otherwise the Core Module can be seriously damaged! When EN_PERI is active high the Core Module has powered up properly and all of the required power lines are available.

5.4 Reset circuit

There are two Reset Inputs for the CM-i.MX53, which have different reset strength. The first one is CTRL.nPOR which will reset the entire i.MX53 as during a power up. Only this Reset mode lets the i.MX53 detect a changed boot mode. The second one, CTRL.nRESET_IN, is a soft reset which only resets the i.MX53 CPU (ARM core).

5.5 Differential pairs

All signals/pins named *_N/*_P (for example: LVDS1.CLK_N and LVDS1.CLK_P) are differential pairs which should be routed with a differential impedance of 100Ω for LVDS and SATA or 90Ω for USB for a good signal integrity and to prevent EMI problems.

5.6 Signals

All signals which are not differential pairs should be routed with a single ended impedance of 50Ohm to minimize EMI.

5.7 Application Example Schematics

Have a look at our DEV-i.MX5x schematics, which can be found at http://www.bluetechnix.com/goto/dev-i.mx53kit to get application examples.

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6 Mechanical Outline

6.1 Top View

Figure 6-1 shows the top view of the mechanical outline of the CM-i.MX53 Core Module. All dimensions are given in millimeters! Outline dimensions +/- 0,5mm.

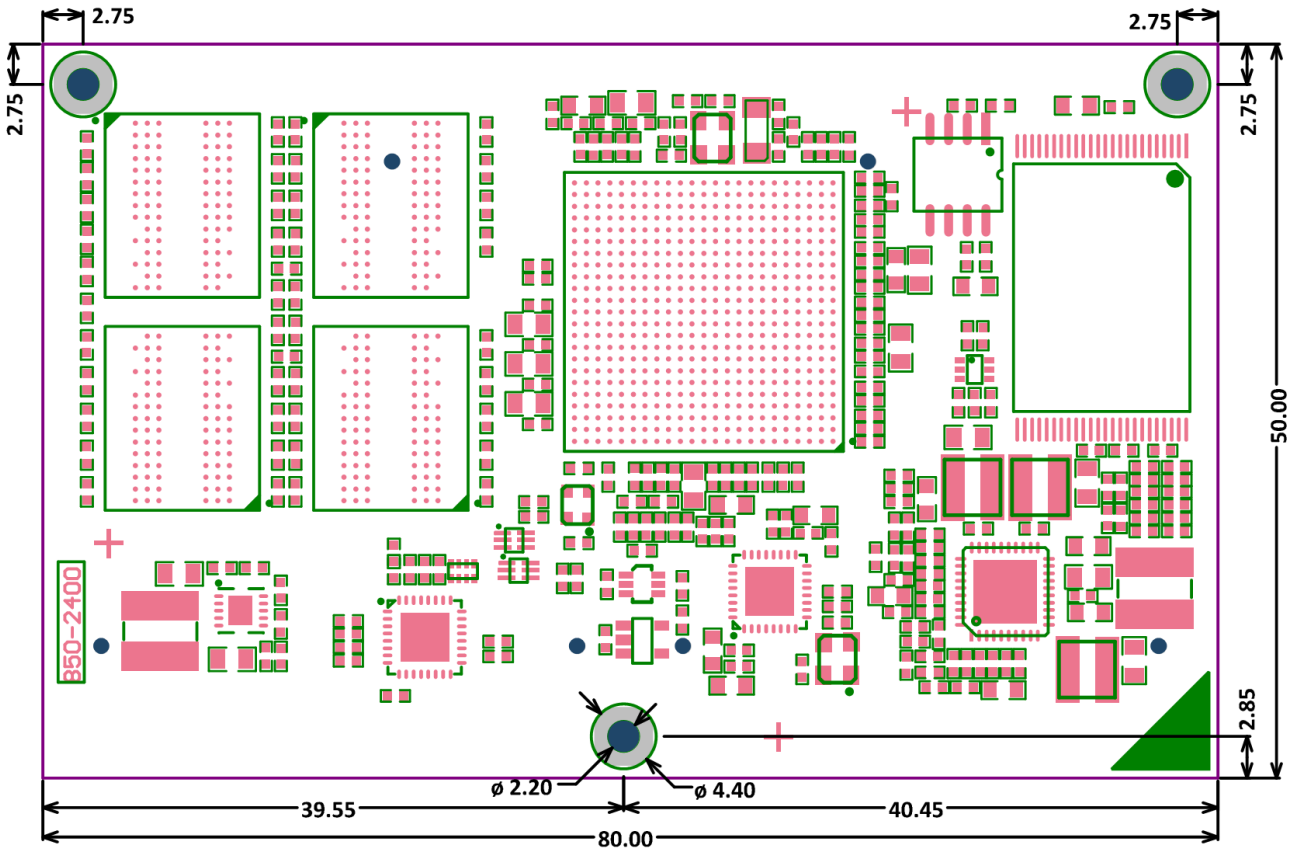

Figure 6-1: Mechanical outline (top view)

6.2 Bottom View

Figure 6-2 shows the bottom of the mechanical outline of the CM-i.MX53 Core Module. All dimensions are given in millimeters!

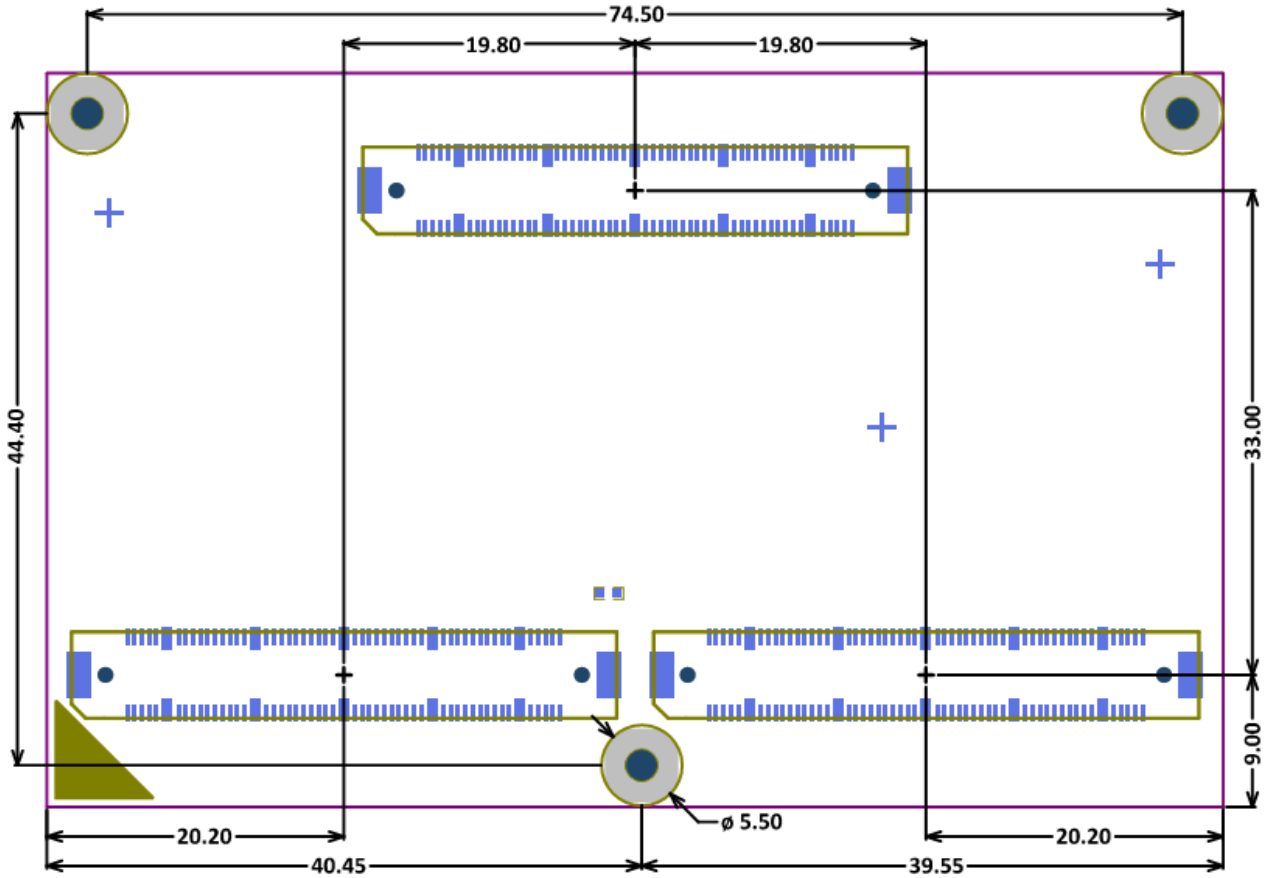

Figure 6-2: Mechanical outline and Bottom Connectors (bottom view)

6.3 Side View

Figure 6-3 shows the mechanical outline of the side of the CM-i.MX53 Core Module. All dimensions are given in millimeters!

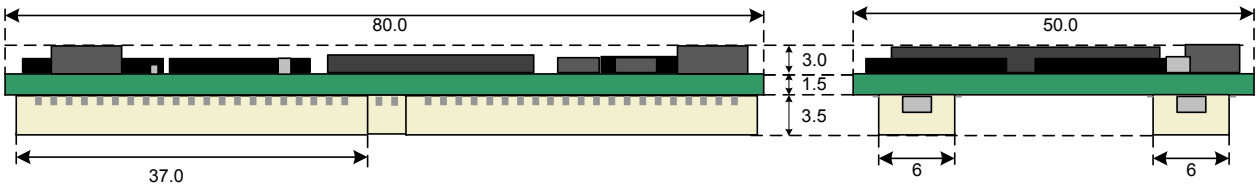

Figure 6-3: Mechanical outline (side view)

6.4 Footprint

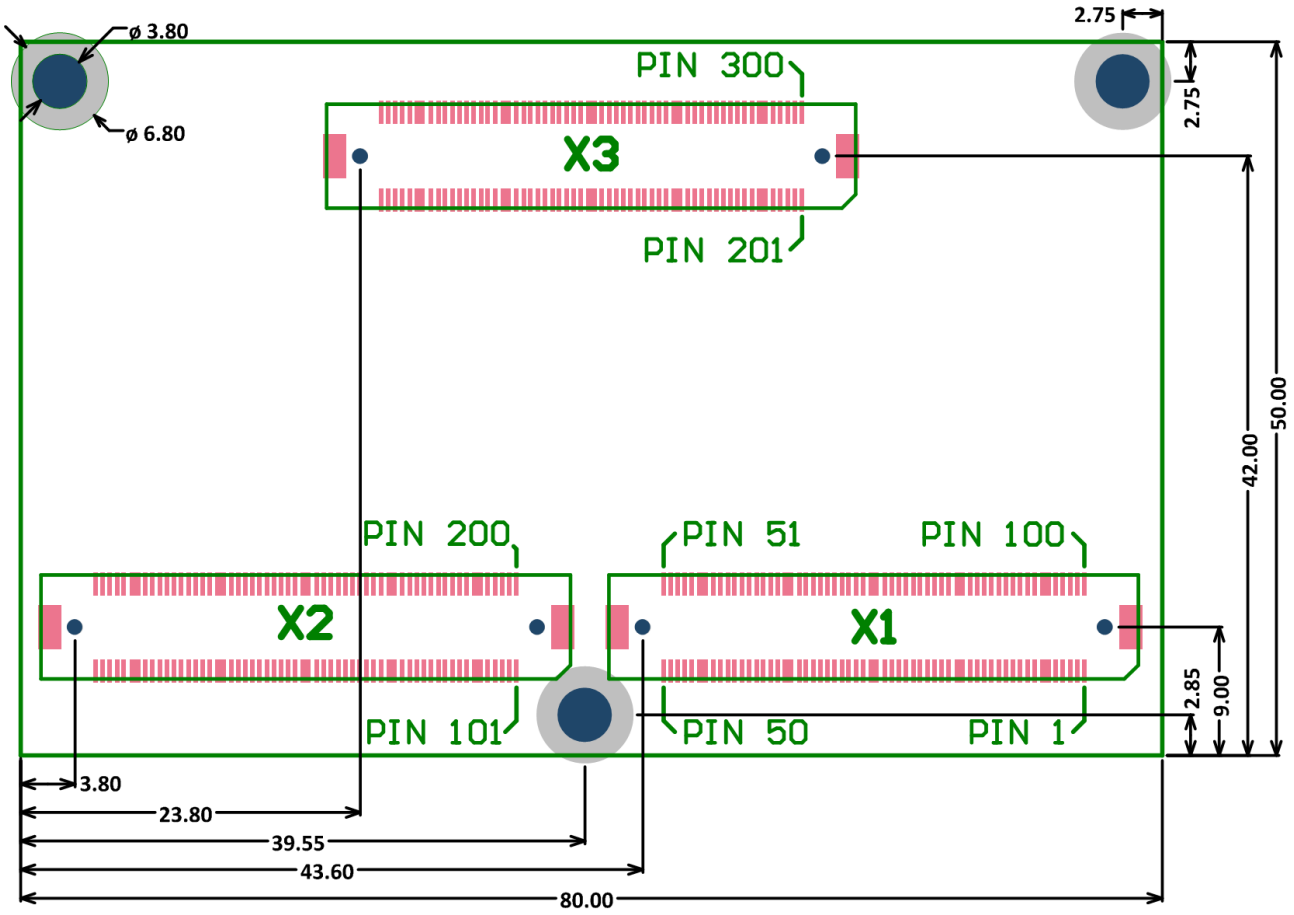

Figure 6-4: Footprint (top view)

The footprint for Altium Designer is available on request. The used connector is FX-10A-100S/10SV from Hirose. For detailed dimensions of the connectors please see the datasheet from the manufacturer's web site.

The mounting holes are designed for reflow solderable spacers SMTSO-M2-4 from PEM. For further details regarding dimensions and paste expansion please refer the manufacturer's website. If simple holes are desired on the base board, identical ones as on the Core Module are recommended.

6.5 Connectors

Connector Core Module	Manufacturer	Manufacturer Part No.
X1, X2, X3	Hirose	FX-10A-100P/10SV

Table 10: Core Module connector types

The Core Module features 3 connectors. The base board has to use the opposite connectors (FX-10A-100S/10SV).

7 Support

7.1 General Support

General support for products can be found at Bluetechnix' support site https://support.bluetechnix.at/wiki

7.2 Board Support Packages

Board support packages, boot loaders and further software downloads can be downloaded at the Products wiki page at https://support.bluetechnix.at/wiki

7.3 i.MX Software Support

7.3.1 Linux

Linux BSP and images of derivates can be found at Bluetechnix' support site https://support.bluetechnix.at/wiki at the software section of the related product.

7.3.2 Win CE

WinCE is only supported on ARM platforms. Please contact Bluetechnix for support information.

7.4 i.MX® Design Services

Based on more than seven years of experience with Blackfin and i.MX, Bluetechnix offers development assistance as well as custom design services and software development.

7.4.1 Upcoming Products and Software Releases

Keep up to date with all product changes, releases and software updates of Bluetechnix at http://www.bluetechnix.com.

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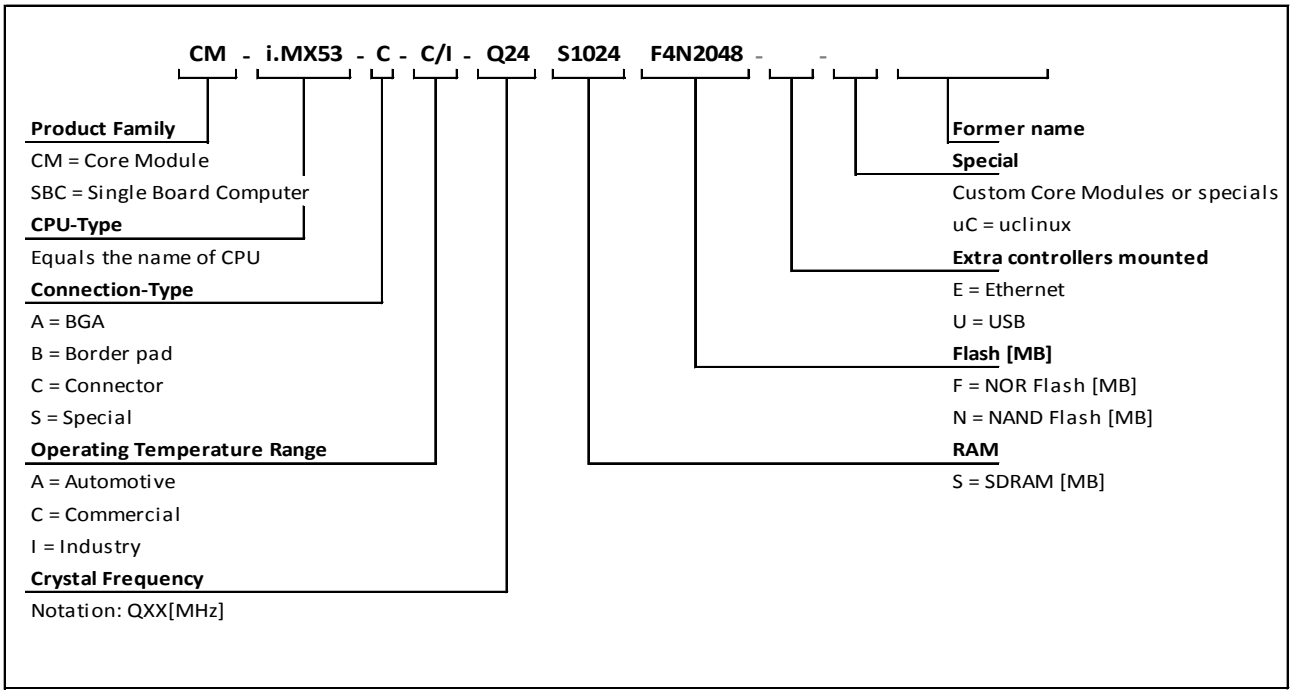
8 Ordering Information



8.1 Predefined mounting options for CM-i.MX53

Article Number	Name	Temperature Range
100-1470-2	CM-i.MX53-C-I-Q24S1024F4N2048	Industrial
100-1470-2-TR	CM-i.MX53-C-I-Q24S1024F4N2048	Industrial Tape reel 50 pcs. per reel
100-1471-2	CM-i.MX53-C-C-Q24S1024F4N2048	Commercial
100-1471-2-TR	CM-i.MX53-C-C-Q24S1024F4N2048	Commercial Tape reel 50 pcs. per reel

Table 11: Ordering information

8.2 Development equipment

Article Number	Name	Description
100-4120	DEV-i.MX53 Development KIT	Consists of DEV-i.Mx5x and one CM-i.MX53-C-C-Q24S1024F4N2048

Table 12: CM-i.MX53 development equipment

NOTE: Custom Core Modules are available on request! Please contact Bluetechnix (office@bluetechnix.com) if you are interested in custom Core Modules.

9 Dependability

9.1 MTBF

Please keep in mind that a part stress analysis would be the only way to obtain significant failure rate results, because MTBF numbers just represent a statistical approximation of how long a set of devices should last before failure. Nevertheless, we can calculate an MTBF of the Core Module using the bill of material. We take all the components into account. The PCB and solder connections are excluded from this estimation. For test conditions we assume an ambient temperature of 30°C of all Core Module components except the i.MX processor (80°C) and the memories (70°C). We use the MTBF Calculator from ALD (http://www.aldservice.com/) and use the reliability prediction MIL-217F2 Part Stress standard. Please get in touch with Bluetechnix (office@bluetechnix.com) if you are interested in the MTBF result.

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10 Product History

10.1 Version Information

10.1.1 CM-i.MX53-C-I-Q24S1024F4N2048

Version	Component	Type
2.0.1	Processor	MCIMX537CVV8C
	RAM	MEM2G16D2DABG-25I
	SPI-Flash	M25PX32-VMW6E
	NAND-Flash	MT29F16G08ABACAWP-IT:C
	ETH PHY	KSZ8041NLI
	Audio	SGTL5000XNAA3R2 (only from -20°C to 70°C)
1.1.0	Processor	MCIMX536AVV8C
	RAM	MEM2G16D2DABG-25I
	SPI-Flash	M25PX32-VMW6E
	NAND-Flash	MT29F16G08ABACAWP-IT:C
	ETH PHY	KSZ8041NLI
	Audio	SGTL5000XNAA3R2

Table 10-1: Overview CM-i.MX53-C-I-Q24S1024F4N2048 product changes

10.1.2 CM-i.MX53-C-C-Q24S1024F4N2048

Version	Component	Type
2.0.1	Processor	MCIMX535DVV1C
	RAM	MEM2G16D2DABG-25
	SPI-Flash	M25PX32-VMW6E
	NAND-Flash	MT29F16G08CBABAWP:B
	ETH PHY	KSZ8041NLI
	Audio	SGTL5000XNAA3R2
1.1.0	Processor	MCIMX535DVV1C
	RAM	MEM2G16D2DABG-25
	SPI-Flash	M25PX32-VMW6E
	NAND-Flash	MT29F16G08CBABAWP:B
	ETH PHY	KSZ8041NLI
	Audio	SGTL5000XNAA3R2

Table 10-2: Overview CM-i.MX53-C-C-Q24S1024F4N2048 product changes

10.2 Anomalies

Version	Date	Description
2.0.1	2012-11-27	If an external supplied USB-Device is connected the PMIC may not start up.
1.1.0	2011-07-24	No anomalies reported yet.

Table 10-3: Overview product anomalies

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11 Document Revision History

11.1 Document Revision History

Version	Date	Document Revision
3	2013 04 10	Updated Table7
2	2013 01 23	Release of V2.0 of the Document
1	2009 12 03	First release V1.0 of the Document

Table 11.1: Revision history