IDTF0480NBGI
Datasheet

Matched Broadband RF VGA **400MHz to 2700MHz**

General Description

This document describes the specifications for the IDTF0480 400 MHz to 2700 MHz RF Digital Variable Gain Amplifier used in receiver, transmitter and other applications.

IDTF0480 RF DVGA provides 13 dB typical maximum gain (no attenuation) with 4 dB noise figure and 23 dB gain adjustment in 1 dB steps designed to operate with a single 5 V supply. Nominally, the device offers +41 dBm output IP3 using 100 mA of I_{CC}.

This device is packaged in a 5x5 32-pin thin QFN with 50 ohm single-ended RF input and RF output impedances for ease of integration into the signal-path lineup.

Competitive Advantage

In many applications, digital step attenuators followed by RF amplifiers are used in the Receive path. The IDTF0480 RF DVGA provides very high reliability by combining a silicon Glitch-Free™ DSA & a Zero-Distortion™ RF amplifier in a single, compact QFN package. Utilizing IDT's technology, the resultant RF VGA provides +41 dBm OIP3 performance across a very wide bandwidth of 400 MHz to 2700 MHz at approximately 100 mA of current. Furthermore the device is internally matched so there is no need to optimize external matching elements.

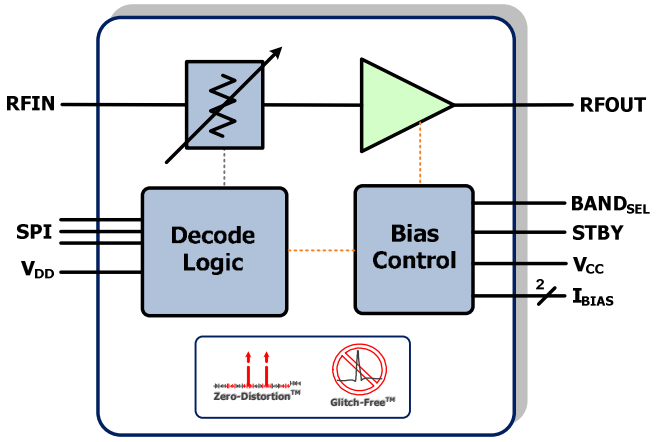
Applications

- Multi-mode, Multi-carrier Receivers
- PCS1900 Base Stations
- DCS1800 Base Stations
- WiMAX and LTE Base Stations
- UMTS/WCDMA 3G Base Stations
- PHS/PAS Base Stations
- Point to Point Infrastructure
- Public Safety Infrastructure
- Broadband Repeaters
- GPS Receivers
- Distributed Antenna Systems
- Cable Infrastructure
- Digital Radio

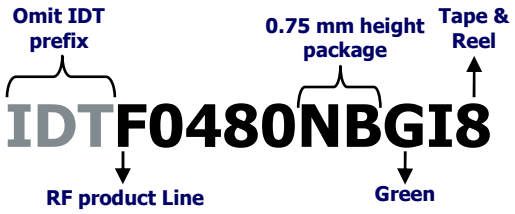
Features

- 400 MHz – 2700 MHz
- < 1 dB overshoot between gain transitions
- 13 dB typical max gain
- 23 dB gain range, 1 dB gain step resolution
- Excellent linearity +41 dBm OIP3
- Noise Figure 4 dB
- I_{CC} = 100 mA
- 1.3 mA standby current
- SPI interface
- 50 Ω input and output impedance
- Broadband, Internally Matched
- Gain increases vs. frequency to counteract system board losses
- 5x5 32-pin TQFN package

Device Block Diagram



Ordering Information



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
VCC to GND	V_{CC}	-0.3	+5.5	V
SPI DATA, SPI CSb, SPI CLK, LogicCTL	V_{diD}	-0.3	+3.6	V
STBY, Band_Select	V_{Cntl}	-0.3	V_{cc} + 0.25	V
R_Bias1	I_{R1}		+1.5	mA
R_Bias2	I_{R1}		+0.8	mA
RFIN externally applied DC voltage	V_{RFin}	+1.4	+3.6	V
RFOUT externally applied DC voltage	V_{RFout}	V_{cc} - 0.15	V_{cc} + 0.15	V
RF Input Power (RFIN) applied for 24 hours maximum	P_{in}		+22	dBm
Continuous Power Dissipation	P_{diss}		1.5	W
Junction Temperature	T_j		150	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)			Class 2 (2000 V)	
ElectroStatic Discharge – CDM (JEDEC 22-C101F)			Class C2 (500 V)	

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

θ_{JA} (Junction – Ambient)	40 °C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	4 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

IDTF0480 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage(s)	V_{CC}	All VCC pins	4.75		5.25	V
Operating Temperature Range	T_{CASE}	Case Temperature	-40		+105	°C
RF Freq Range	F_{RF}	Operating Range	400		2700	MHz
RF Source Impedance	Z_{RFI}	Single Ended		50		Ω
RF Load Impedance	Z_{RFO}	Single Ended		50		Ω

IDTF0480 SPECIFICATION

See F0480 Typical Application Circuit. Specifications apply when operated as an RF DVGA, V_{CC} = +5.00 V, T_C = +25 °C, Max gain setting, output power = 0 dBm, Z_{RFI} = Z_{RFO} = 50 Ω, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Logic Input High	V_{IH}	JEDEC 3.3V logic	***2.0***[1]			V
Logic Input Low	V_{IL}	JEDEC 3.3V logic			***0.8***	V
Logic Input High	V_{IH}	JEDEC 1.8V logic	***1.1***			V
Logic Input Low	V_{IL}	JEDEC 1.8V logic			***0.63***	V
Logic Current	I_{IH}, I_{IL}	STBY, Band_Select	***-10***		***+10***	µA
		SPI_	***-4***		***+4***	
		Logic CTL	***-35***		***+35***	
Supply Current[3]	I_{CC_LB}	Low Band Configuration		100		mA
	I_{CC_MB}	Mid Band Configuration		117	***128***	
	I_{CC_HB}	High Band Configuration		109		
	I_{CC_STBY}	Standby Mode		1.3	***1.7***	
Startup time		50% of STBY going low to Gain within ± 1 dB with no attenuation.		250		ns
Gain adjustment range	G_{ADJ}			23		dB
Gain step	G_{STEP}			1		dB
Max Attenuator Glitch	$ATTN_G$	Step from 15 to 16 dB or 16 to 15 dB		0.5		dB
Gain Settling Time	G_{ST}	50% of CSb to ± 0.1 dB of settled gain		500		ns
Serial Clock Speed					***10***	MHz
CSb to first serial clock rising edge	A	SPI 3 wire Bus. 50% of CSb falling edge to 50% of CLK rising edge.	***10***			ns
Serial Data Hold Time	B	SPI 3 wire Bus. 50% of CLK rising edge to 50% of Data falling edge.	***10***			ns
Final serial clock rising edge to CSb	C	SPI 3 wire Bus. 50% of CLK rising edge to 50% of CSB rising edge.	***10***			ns

Note 1: Items in min/max columns in ***bold italics*** are Guaranteed by Test.
Note 2: Items in min/max columns that are not bold/italics are Guaranteed by Design Characterization.
Note 3: During standby mode, SPI is to be left ON and previous state shall be maintained when device is powered up.

IDTF0480 Specification - Lowband Performance

See F0480 Typical Application Circuit. Specifications apply when operated as an RF DVGA, V_{CC} = +5.00 V, T_C = +25 °C, F_{RF} = 900 MHz, Band_Select = LB setting, Max gain setting, output power = 0 dBm, Z_{RFI} = Z_{RFO} = 50 Ω, the evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RF input return loss	RL_{IN_LB}			15		dB
RF output return loss	RL_{Out_LB}			20		dB
Gain	G_{MAX_LB}		***11.5***	12.6	***13.4***	dB
	G_{MIN_LB}	Maximum attenuation	***-11.2***	-10.2	***-9.4***	
	G_{TEMP_LB}	Variation over Temperature		± 0.3		
	G_{VAR_LB}	Max gain variation over frequency[5]		0.1		
Step Error	$G_{ACC\ LB}$	Between adjacent states		± 0.1		dB
Absolute Error	G_{ABSACC_LB}	Relative to maximum gain		± 0.2		dB
Phase deviation	$G_{PH\_ADJ\_LB}$	Between adjacent states at maximum gain		1		Deg
Noise Figure	NF_{LB}			3.9		dB
	NF_{LB_MG}	T_{case} = +105 °C		4.8		
	NF_{LB_RG}	22 dB attenuation		25.9		
Output Third Order Intercept Point	$OIP3_{\_LB\text{-}1}$	Pout = 0 dBm/Tone, 1 MHz tone separation		41.5		dBm
	$OIP3_{\_LB\text{-}2}$	Pout = -10 dBm/Tone, 1 MHz tone separation		40.5		
	$OIP3_{\_LB\text{-}3}$	Pout = 0 dBm/Tone, 1 MHz tone separation, Worst case in the operating temperature range	39	41		
	$OIP3_{\_LB\text{-}6dB}$	Pout = 0 dBm/Tone, 1 MHz tone separation with 6 dB attenuation		41		
Output 1 dB Power Compression	$OP1dB_{\_LB}$		***20.6***	22.2		dBm
Output 0.2 dB Power Compression	$OP0.2dB_{\_LB}$			20		dBm
Output Saturated Power	$PSAT_{\ LB}$	3 dB compression		22.3		dBm
Reverse Isolation	REV_{ISO_LB}			18		dB

Note 5: Including frequency and ripple variations valid within each individual 3GPP band.

IDTF0480 Specification - Midband Performance

See F0480 Typical Application Circuit. Specifications apply when operated as an RF DVGA, V_{CC} = +5.00 V, T_C = +25 °C, F_{RF} = 2000 MHz, Band_Select = HB setting, Max gain setting, output power = 0 dBm, Z_{RFI} = Z_{RFO} = 50 Ω, the evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
RF input return loss	RL_{IN_MB}			13		dB
RF output return loss	RL_{Out_MB}			17		dB
Gain	G_{MAX_MB}		***11.9***	13.1	***14.2***	dB
	G_{MIN_MB}	Maximum attenuation	***-11***	-9.9	***-8.7***	
	G_{TEMP_MB}	Variation over Temperature		± 0.3		
	G_{VAR_MB}	Max gain variation over frequency[5]		0.1		
Step Error	G_{ACC_MB}	Between adjacent states		± 0.1		dB
Absolute Error	G_{ABSACC_MB}	Relative to maximum gain	***- 0.6***	± 0.2	***+ 0.6***	dB
Phase deviation	$G_{PH\_ADJ\_MB}$	Between adjacent states at maximum gain		2		Deg
Noise Figure	NF_{MB}			4.5		dB
	NF_{MB_MG}	T_{case} = +105 °C		5.5	5.9	
	NF_{MB_RG}	22 dB attenuation		26.7	28.2	
Output Third Order Intercept Point	$OIP3_{\_MB-1}$	Pout = 0 dBm/Tone, 1 MHz tone separation	***38***	41.5		dBm
	$OIP3_{\_MB-2}$	Pout = -10 dBm/Tone, 1 MHz tone separation		42.5		
	$OIP3_{\_MB-3}$	Pout = 0 dBm/Tone, 1 MHz tone separation, Worst case in the operating temperature range	39	41.1		
	$OIP3_{\_MB-6dB}$	Pout = 0 dBm/Tone, 1 MHz tone separation with 6 dB attenuation		41.5		
Output 1 dB Power Compression	$OP1dB_{\_MB}$			22.2		dBm
Output 0.2 dB Power Compression	$OP0.2dB_{\_MB}$			18.5		dBm
Output Saturated Power	$PSAT_{\_MB}$	3 dB compression		22.7		dBm
Reverse Isolation	REV_{ISO_MB}			18		dB

IDTF0480 Specification - Highband Performance

See F0480 Typical Application Circuit. Specifications apply when operated as an RF DVGA, V_{CC} = +5.00 V, T_C = +25 °C, F_{RF} = 2700 MHz, Band_Select = HB setting, Max gain setting, output power = 0 dBm, Z_{RFI} = Z_{RFO} = 50 Ω, the evaluation board and connector losses are de-embedded, unless otherwise noted.

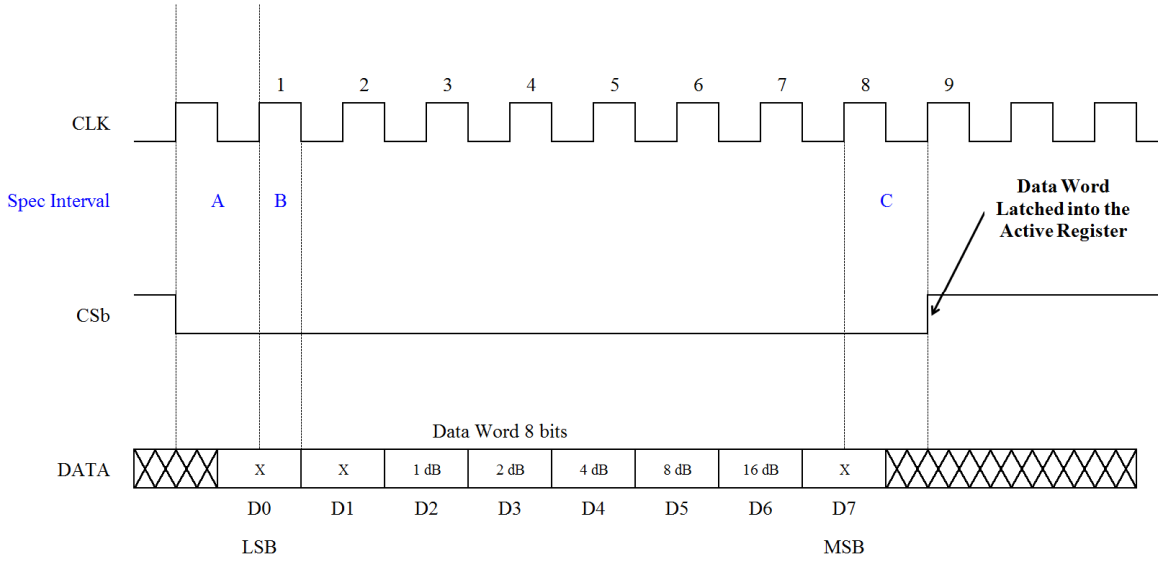
Parameter	Symbol	Conditions	Min	Typ	Max	Units
RF input return loss	RL_{IN_HB}			12		dB
RF output return loss	RL_{Out_HB}			15		dB
Gain	G_{MAX_HB}		***12.2***	13.5	***14.4***	dB
	G_{MIN_HB}	Maximum attenuation	***-10.7***	-9.5	***-8.4***	
	G_{TEMP_HB}	Variation over Temperature		± 0.3		
	G_{VAR_HB}	Max gain variation over frequency[5]		0.1		
Step Error	G_{ACC_HB}	Between adjacent states		± 0.1		dB
Absolute Error	G_{ABSACC_HB}	Relative to maximum gain		± 0.2		dB
Phase deviation	$G_{PH\_ADJ\_HB}$	Between adjacent states at maximum gain		3		Deg
Noise Figure	NF_{HB}			5		dB
	NF_{HB_MG}	T_{case} = +105 °C		5.8		
	NF_{HB_RG}	22 dB attenuation		26.8		
Output Third Order Intercept Point	$OIP3_{\_HB-1}$	Pout = 0 dBm/Tone, 1 MHz tone separation		39.2		dBm
	$OIP3_{\_HB-2}$	Pout = -10 dBm/Tone, 1 MHz tone separation		38.5		
	$OIP3_{\_HB-3}$	Pout = 0 dBm/Tone, 1 MHz tone separation, Worst case in the operating temperature range	35.5	36.7		
	$OIP3_{\_HB-6dB}$	Pout = 0 dBm/Tone, 1 MHz tone separation with 6 dB attenuation		39		
Output 1 dB Power Compression	$OP1dB_{\_HB}$			21.8		dBm
Output 0.2 dB Power Compression	$OP0.2dB_{\_HB}$			21.6		dBm
Output Saturated Power	$PSAT_{\_HB}$	3 dB compression		22.2		dBm
Reverse Isolation	REV_{ISO_HB}			18		dB

SERIAL CONTROL MODE

Data is clocked in LSB first via serial mode. Note the timing diagram below.

Note – *The IDTF0480 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When CSb is high (> V_{IH}), the CLK input is disabled and serial data (DATA) is not clocked into the shift register. It is recommended that CSb be pulled high (>V_{IH}) when the device is not being programmed.*

SERIAL REGISTER TIMING DIAGRAM: (Note the Timing Spec Intervals in **Blue**)



SERIAL MODE DEFAULT CONDITION:

When the device is first powered up it will default to the **Maximum Attenuation** setting as described below:

Default Register Settings

x	x	1	1	1	1	1	x
D0	D1	D2	D3	D4	D5	D6	D7
LSB							MSB

Figure 1 - SPI timing diagram & default register settings

F0480 DVGA ATTENUATION WORD TRUTH TABLE (LSB = first in)

The SPI interface should be built up by an 8-bit word (defined as MOSI) where 5 bits are used for attenuation setting per the example shown below. **BOLD** indicates bits used for programming the attenuator; data bits 2 through 6.

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	ATTENUATION SETTING
x	Low	Low	Low	Low	Low	x	x	insertion loss
x	Low	Low	Low	Low	High	x	x	1 dB
x	Low	Low	Low	High	Low	x	x	2 dB
x	Low	Low	High	Low	Low	x	x	4 dB
x	Low	High	Low	Low	Low	x	x	8 dB
x	High	Low	Low	Low	Low	x	x	16 dB
x	High	Low	High	High	Low	x	x	22 dB
x	High	Low	High	High	High	x	x	23 dB (max)
x	High	High	Low	Low	Low	x	x	23 dB (max)
x	High	High	Low	Low	High	x	x	23 dB (max)
x	High	High	Low	High	Low	x	x	23 dB (max)
x	High	High	Low	High	High	x	x	23 dB (max)
x	High	High	High	Low	Low	x	x	23 dB (max)
x	High	High	High	Low	High	x	x	23 dB (max)
x	High	High	High	High	Low	x	x	23 dB (max)
x	High	High	High	High	High	x	x	23 dB (max)

STANDBY TRUTH TABLE*

PARAMETER	LEVEL	FUNCTION
STBY	0 Volts or Open Circuit	Power On
	+5 Volts	Power Off

*** Startup/Power on requirements:**

SPI shall be left on during Standby mode. When the circuit is initially powered up (+5V applied on pin 12/13), the default VGA setting should be minimum gain (max attenuation setting). If the attenuator is programmed in Standby mode, the programmed setting will be active when the device is taken out of Standby mode.

SPI LOGIC LEVEL CONTROL - PIN 11

PARAMETER	LEVEL	FUNCTION
LogicCTL	3.3 Volts or open Circuit	3.3V logic
	0 Volts	1.8V logic

SUGGESTED C5, R7, AND R8 VALUES FOR OPTIMUM PERFORMANCE (UNLESS OTHERWISE NOTED IN TOCS)

Band	Freq Range (MHz)	Band Select Pin 15	R7 (kΩ)	R8 (kΩ)	C5 (pF)	I_{CC} (mA)
Low-Band	700 - 1100	LB (Open)	2.2	9.1	9	100
Mid-Band	1100 - 2200	HB (GND)	2.4	27	9	117
High-Band	2200 - 2700	HB (GND)	2.67	75	6	109
Broad-Band (p. 16 TOCs)	400 - 2700	HB (GND)	2.2	20	9	124

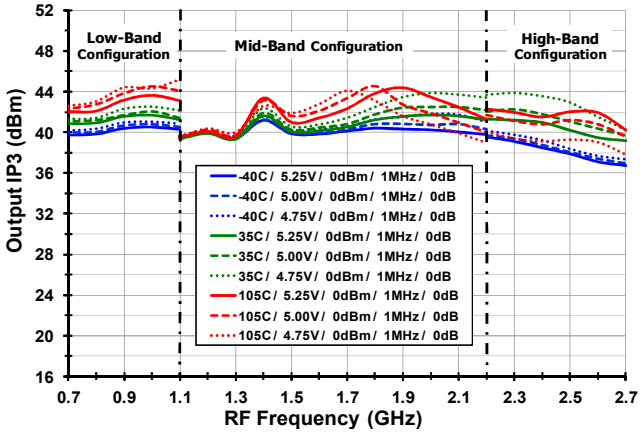
TYPICAL OPERATING CONDITIONS

Unless otherwise noted for the TOC graphs, the following conditions apply

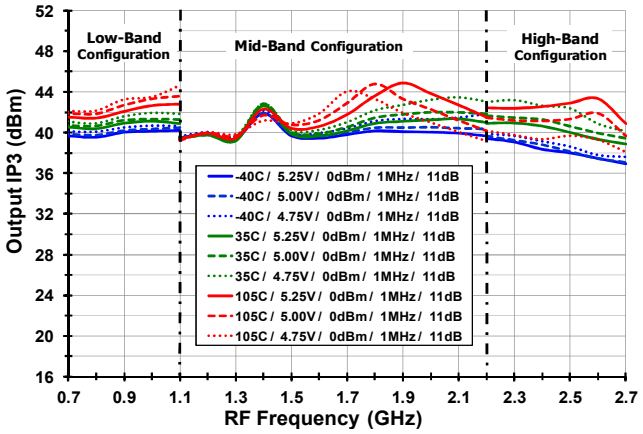
- **Vcc = 5.0 V**
- **Pout = 0 dBm / Tone**
- **1 MHz Tone Spacing**
- **T_{CASE} = 35 °C, T_{AMB} = 25 °C**
- **ATTN setting = 0 dB (Max Gain)**
- **EVkit losses (traces and connectors) fully de-embedded**

TYPICAL OPERATING CONDITIONS [IP3, COMPRESSION] (-1-)

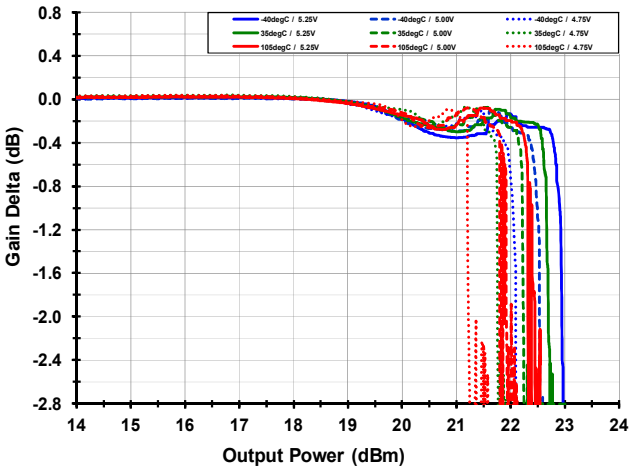
Output IP3 [0 dBm/Tone, 1M Tone Spacing, 0dB ATTN]



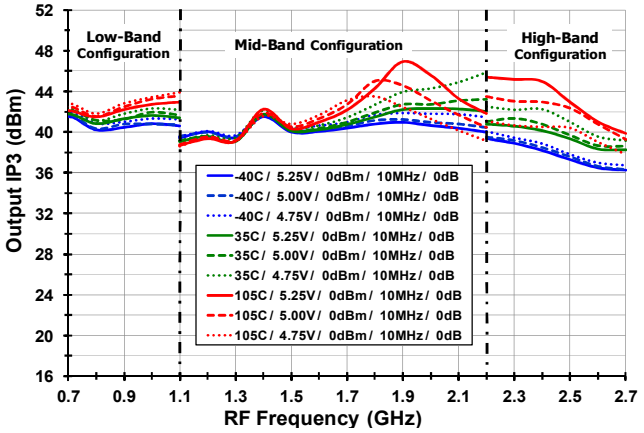
Output IP3 [0 dBm/Tone, 1M Tone Spacing, 11dB ATTN]



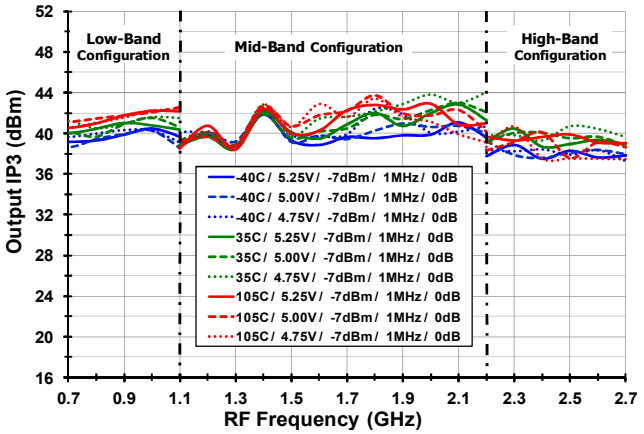
Gain Compression [900 MHz]



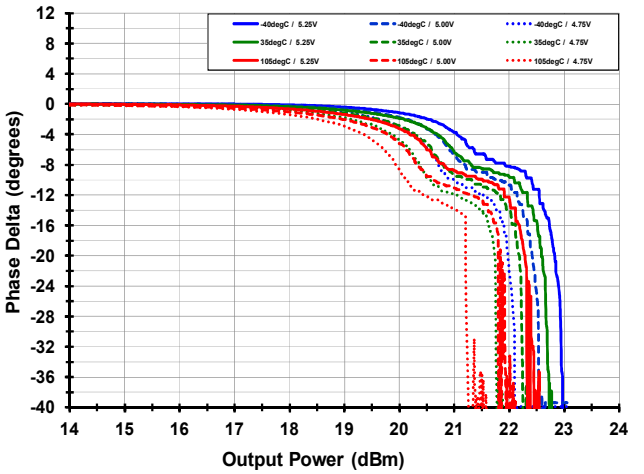
Output IP3 [0 dBm/Tone, 10M Tone Spacing, 0 dB ATTN]



Output IP3 [-7 dBm/Tone, 1M Tone Spacing, 0dB ATTN]

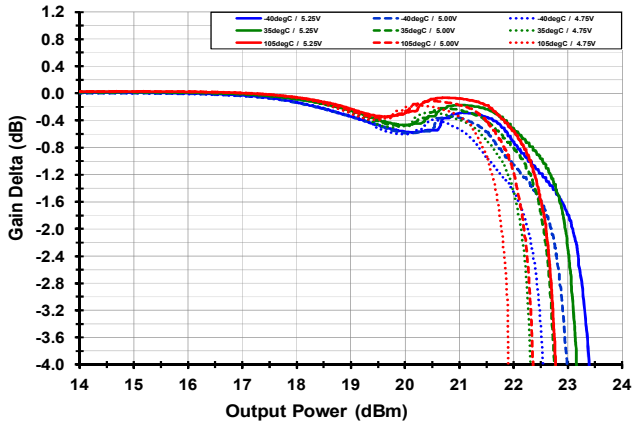


Phase Compression [900 MHz]

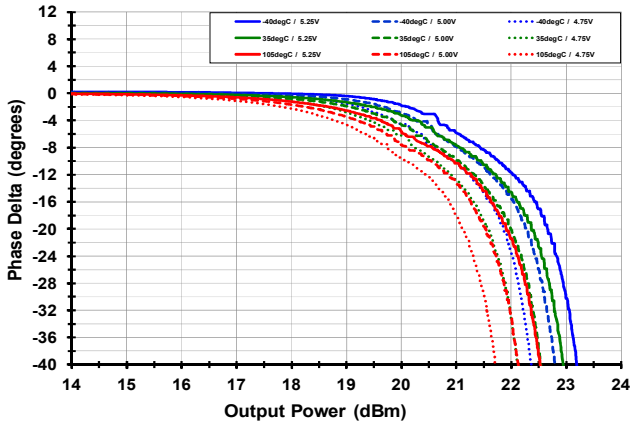


TOCs [Compression, NF] (-2-)

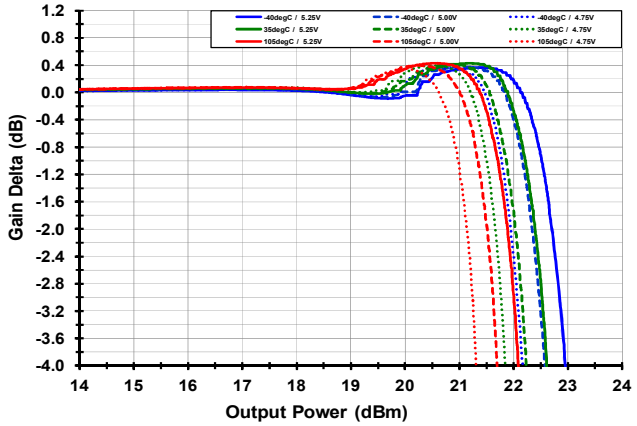
Gain Compression [2000 MHz]



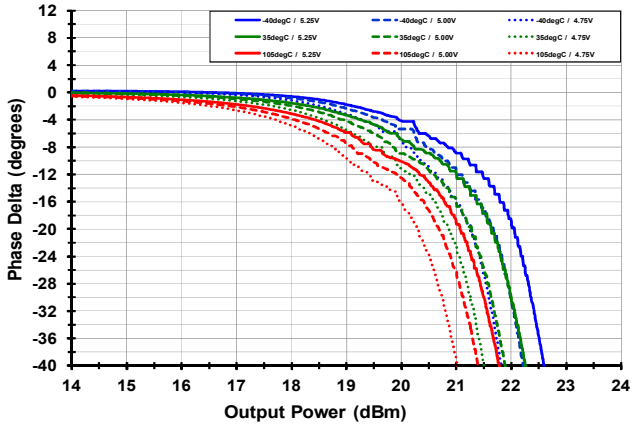
Phase Compression [2000 MHz]



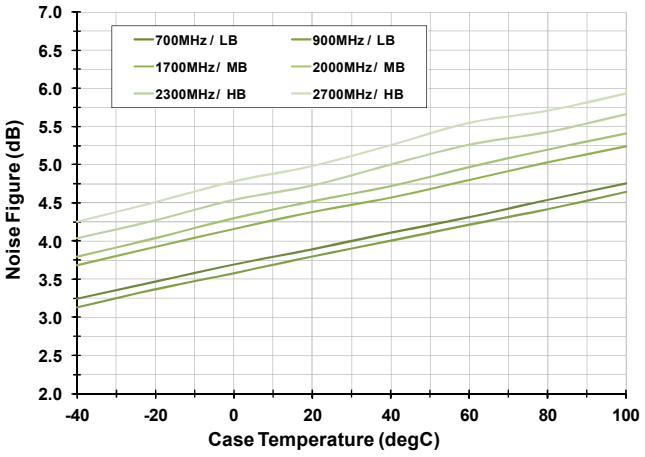
Gain Compression [2700 MHz]



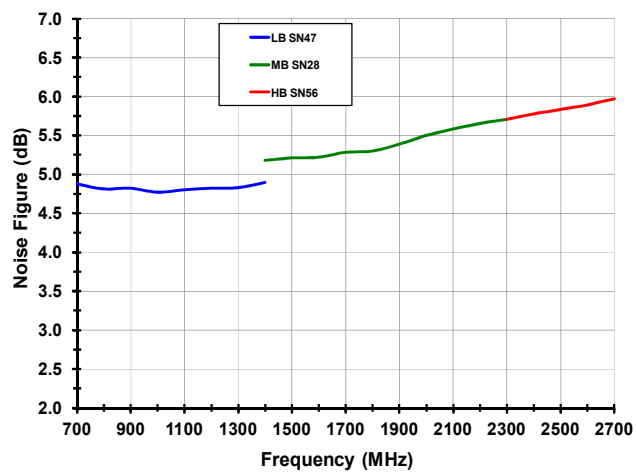
Phase Compression [2700 MHz]



Noise Figure vs. Temperature

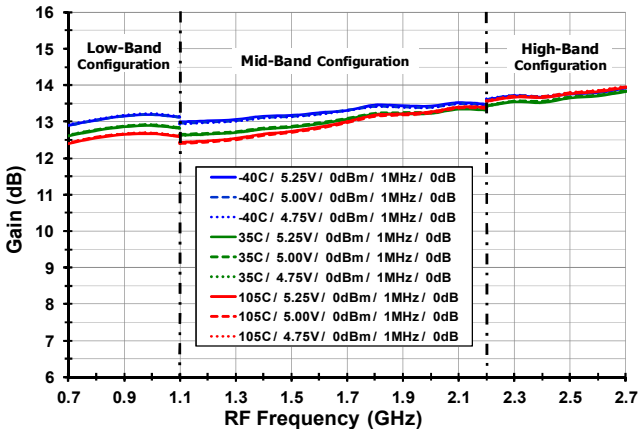


Worst Case NF vs. Frequency [105C, 5.25V]

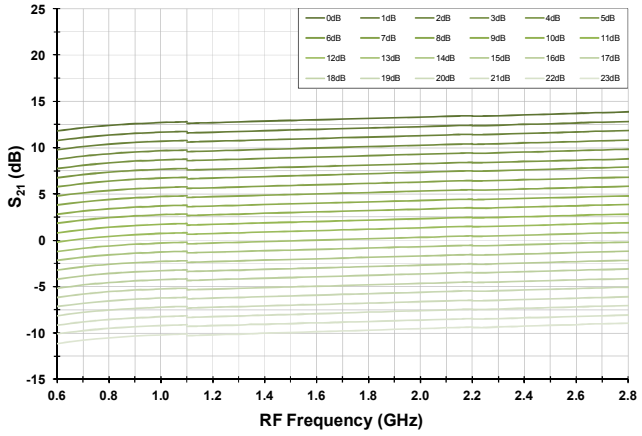


TOCs [GAIN, S-PARAMS WITHOUT C5, ATTN ERROR] (-3-)

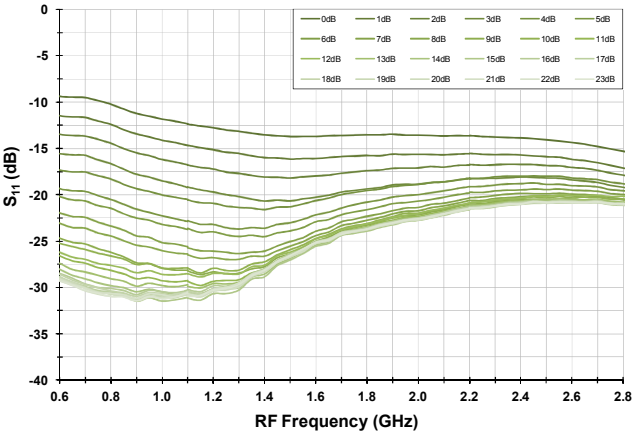
Gain vs. Temperature and Voltage



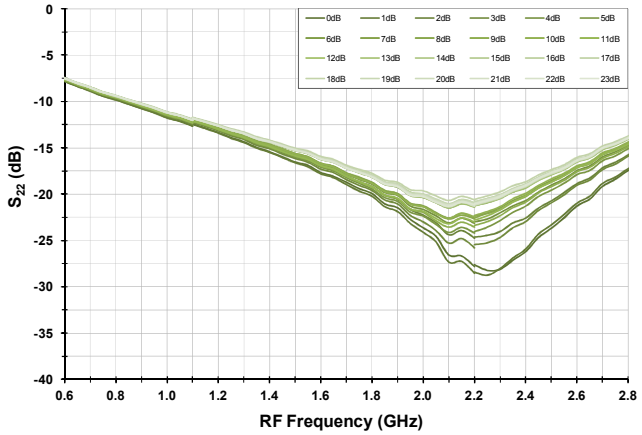
S21 (device only) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]



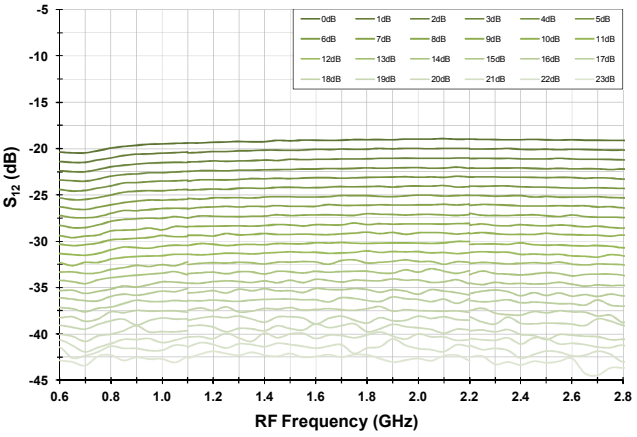
S11 (device only) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]



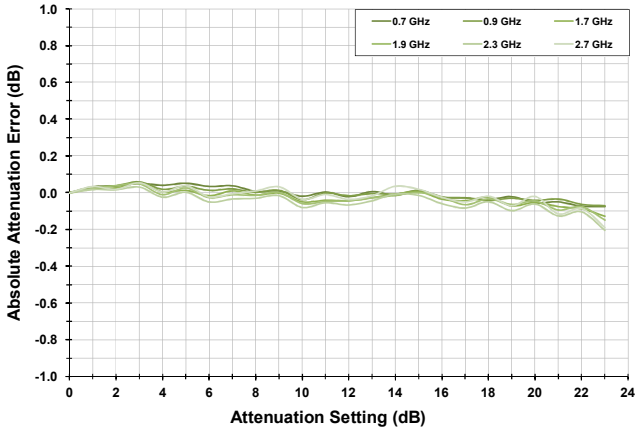
S22 (device only) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]



S12 (device only) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]

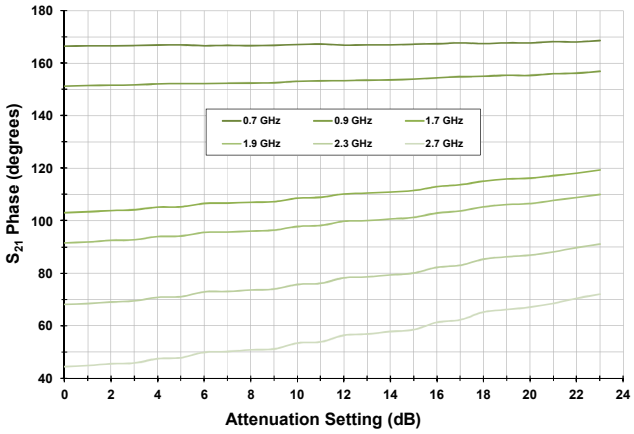


INL (device only) [T_{AMB} = 25C, V_{CC} = 5.00V]

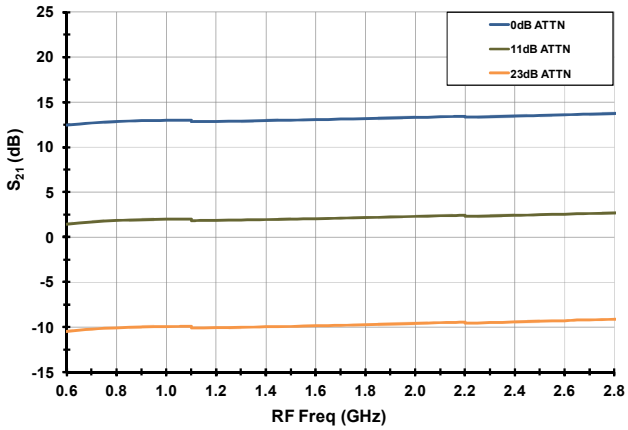


TOCs [Phase Error, S-params with C5, Stability] (-4-)

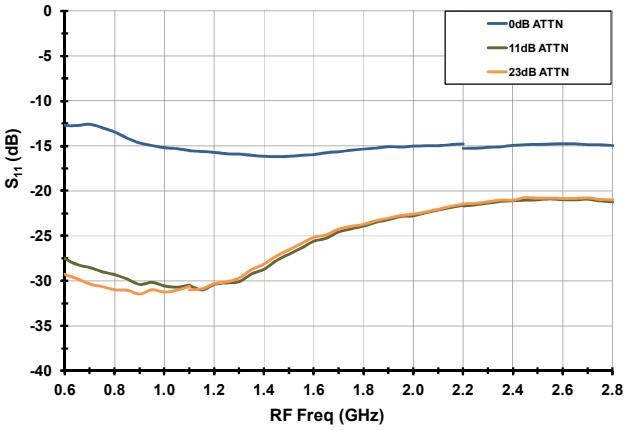
Phase Delta (device only) [T_{AMB} = 25C, V_{CC} = 5.00V]



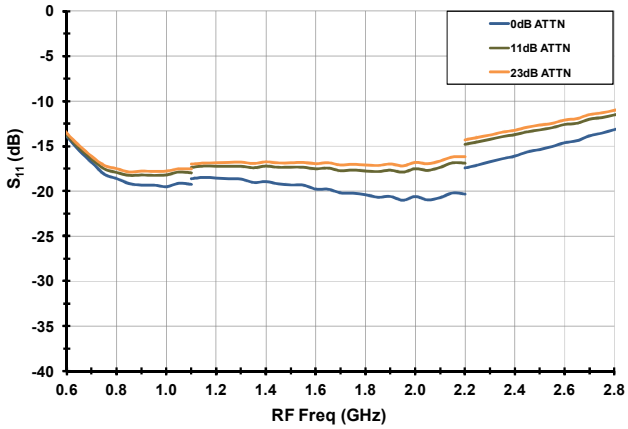
S21 (device+C5 cap) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]



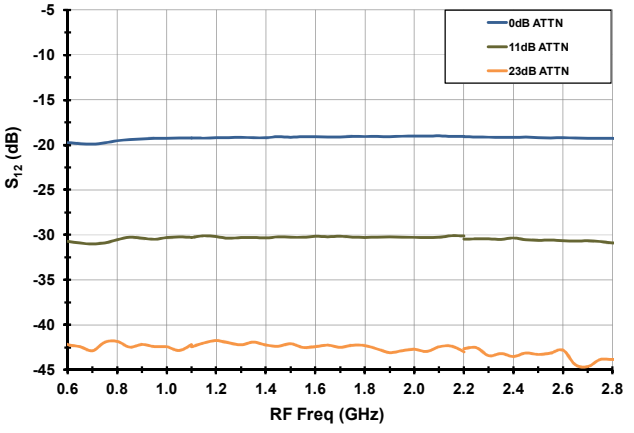
S11 (device+C5 cap) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]



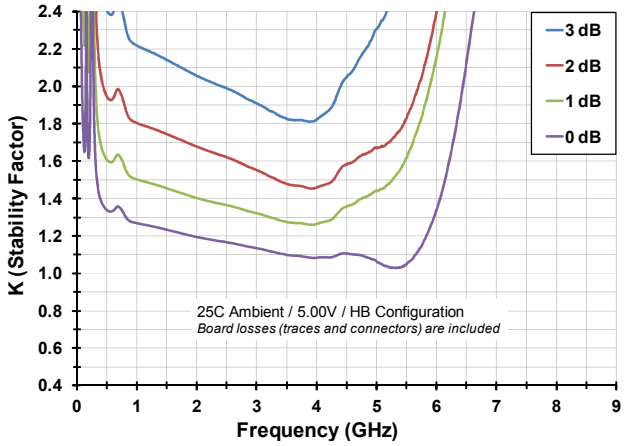
S22 (device+C5 cap) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]



S12 (device+C5 cap) [T_{AMB} = 25C, V_{CC} = 5.00 Volts]

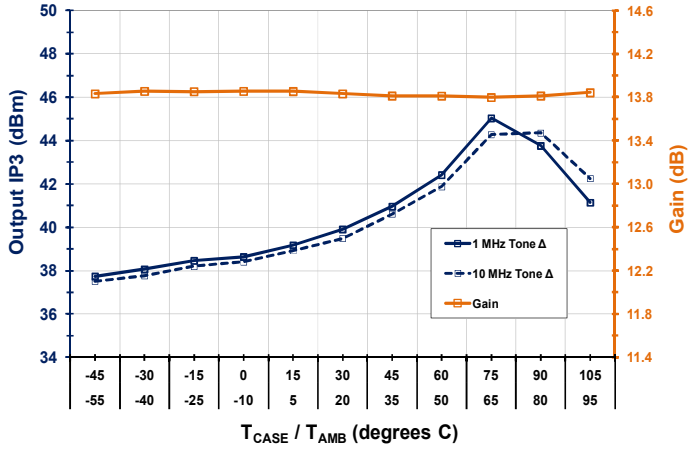


Stability v. ATTN [see discusson on p.18]

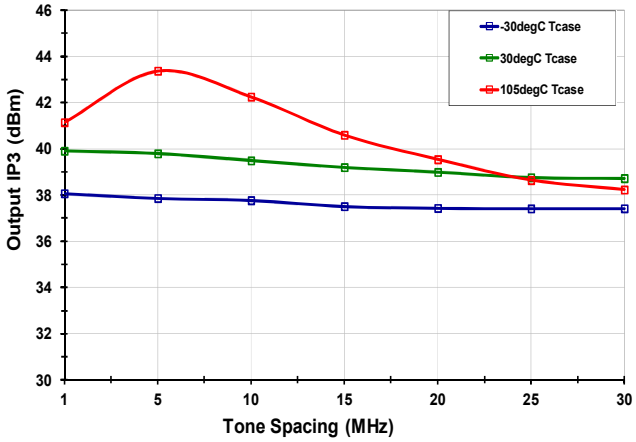


TOCs [MORE IP3, EVKIT LOSSES] (-5-)

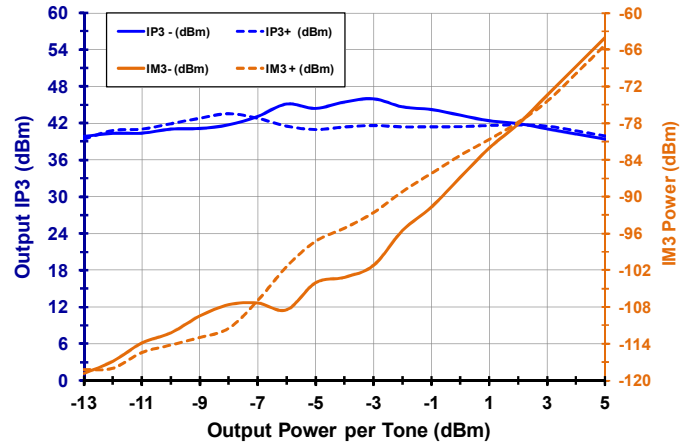
OIP3 vs. Temperature [2.5 GHz, 5.00V]



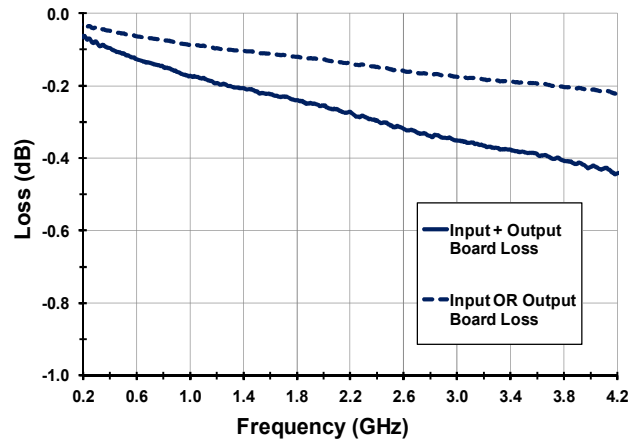
OIP3 vs. Tone Spacing [2.5 GHz, 5.00V]



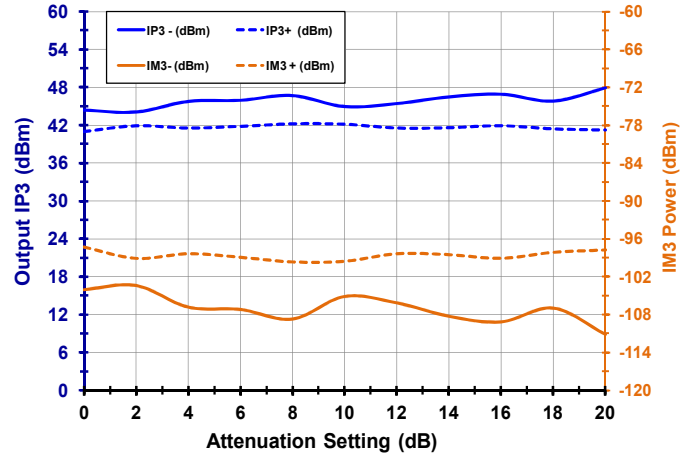
OIP3 vs. Output Power [2.5 GHz, T_{AMB} = 85C]



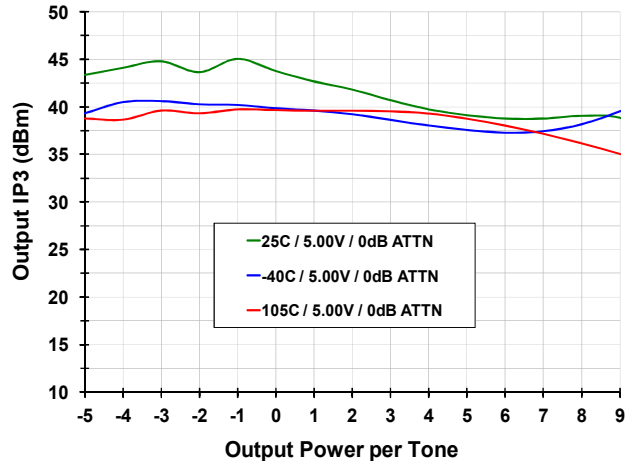
EVKit losses [connector and traces] (Rev 02 RO)



OIP3 v. ATTN [2.5 GHz, T_{AMB} = 85C, Pout = -5 dBm]

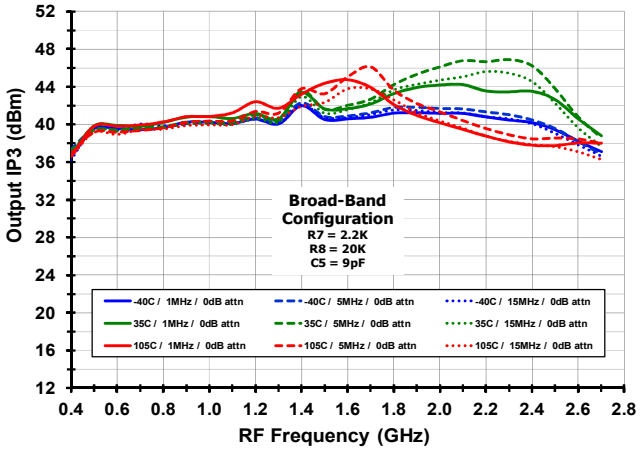


OIP3 vs. Output Power [2.7 GHz, Δf = 1 MHz]

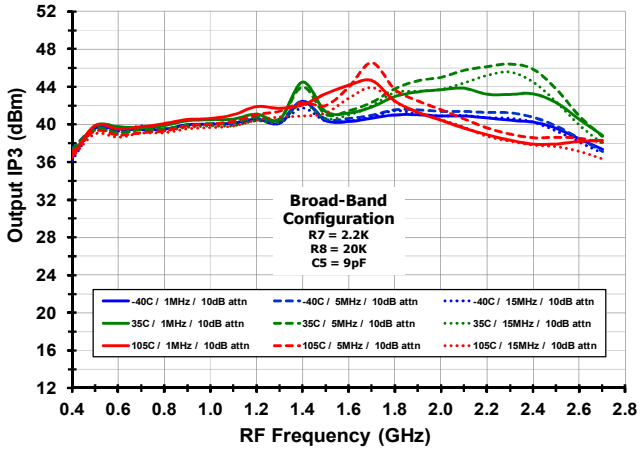


TOCs [BROADBAND CONFIG] (-6-)

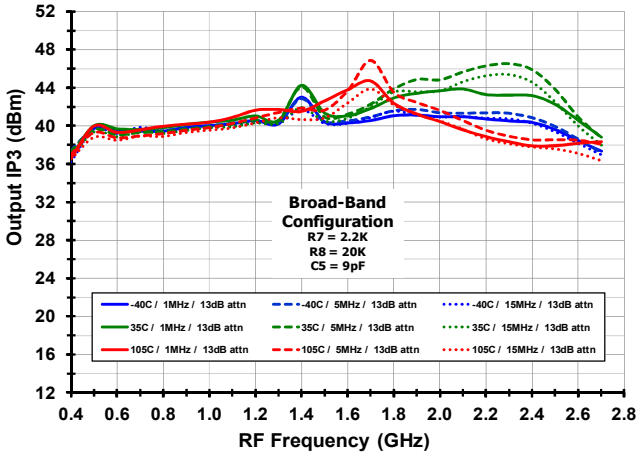
OIP3 vs. T_{CASE} & Tone Offset [0 dB ATTN]



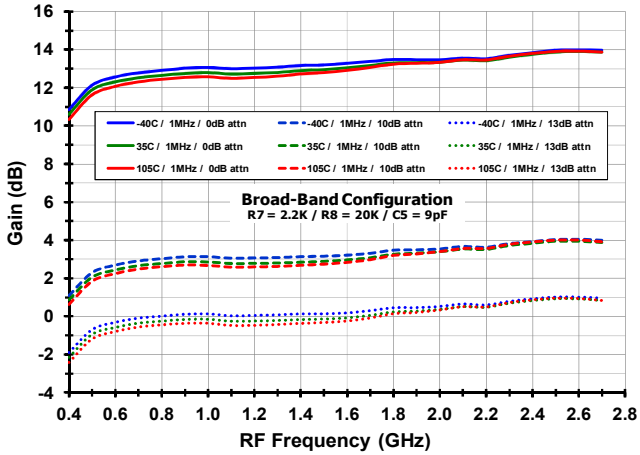
OIP3 vs. T_{CASE} & Tone Offset [10 dB ATTN]



OIP3 vs. T_{CASE} & Tone Offset [13 dB ATTN]



Gain vs. T_{CASE} & ATTN setting



Wideband OIP2 [T_{AMB} = 25C, Pout = -10 dBm/Tone]

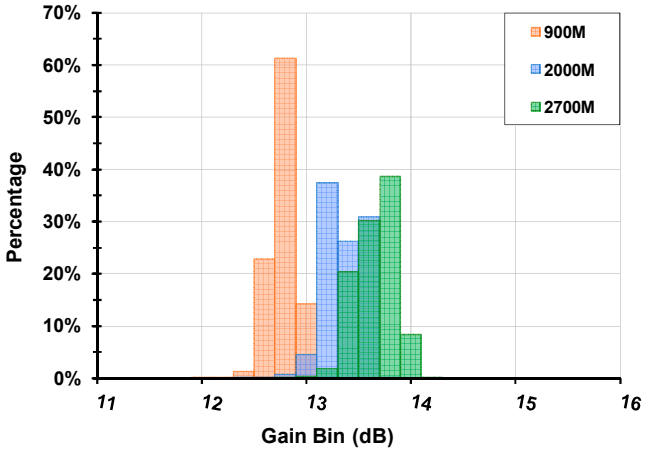
MHz F_1	MHz F_2	MHz IMD_2-	MHz IMD_2+	dBm IMD_2-	dBm OIP_2-	dBm IMD_2+	dBm OIP_2+
700	1950	1250	2650	-71.1	**51.1**	-69.3	**49.3**
700	1720	1020	2420	-70.4	**50.4**	-69.6	**49.6**
700	2650	1950		-71.8	**51.8**		
824	900		1724			-71.5	**51.5**
900	1720	820	2620	-70.4	**50.4**	-70.3	**50.3**
1755	2600	845		-69.4	**49.4**		
1900	2600	700		-69.3	**49.3**		

Wideband OIP2 [T_{AMB} = 25C, Pout = 0 dBm/Tone]

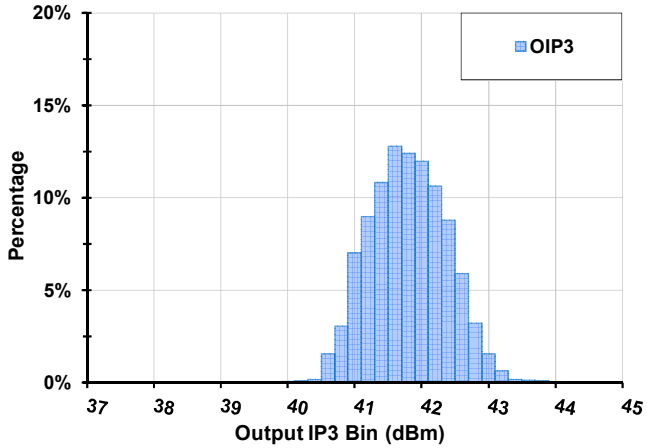
MHz F_1	MHz F_2	MHz IMD_2-	MHz IMD_2+	dBm IMD_2-	dBm OIP_2-	dBm IMD_2+	dBm OIP_2+
700	1950	1250	2650	-50.9	**50.9**	-49.2	**49.2**
700	1720	1020	2420	-50.2	**50.2**	-49.5	**49.5**
700	2650	1950		-51.4	**51.4**		
824	900		1724			-51.2	**51.2**
900	1720	820	2620	-50.0	**50.0**	-50.2	**50.2**
1755	2600	845		-49.0	**49.0**		
1900	2600	700		-48.9	**48.9**		

TOCs [HISTOGRAMS] (-7-)

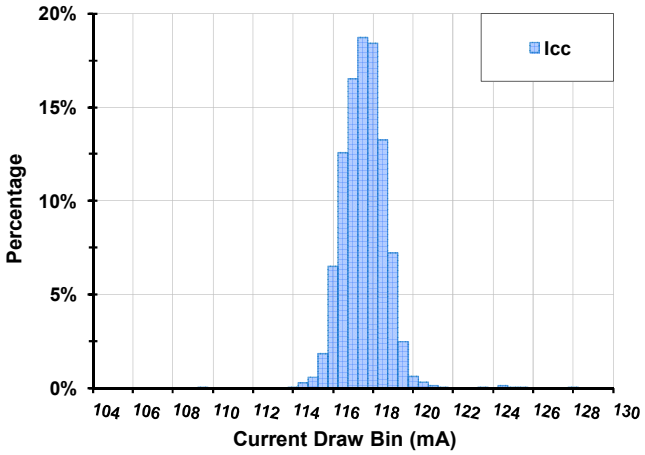
Gain [N = 2107]



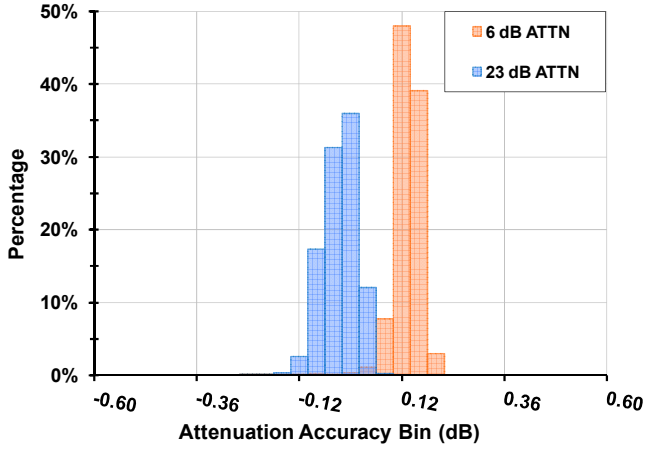
OIP3 [Freq = 2.0 GHz, N = 2107]



Total Current [MidBand Config, N = 2107]



ATTN Accuracy [Freq = 2.0 GHz, N = 2107]



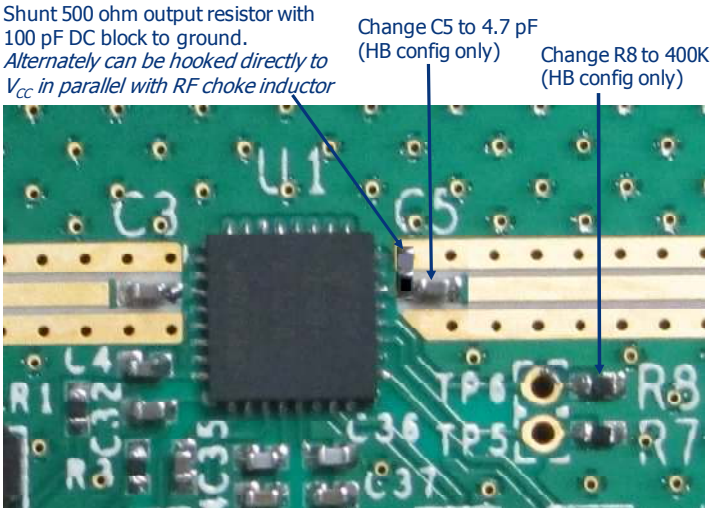
STABILITY CONSIDERATIONS

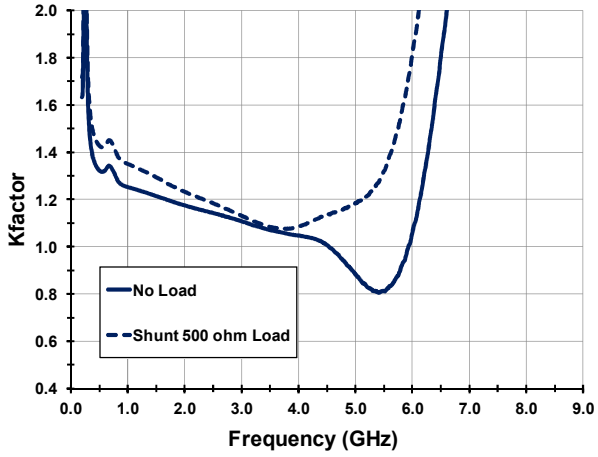
The IDTF0480 EVkit is unconditionally stable as shown on page 14, bottom right graph.

One can ensure that the device itself is unconditionally stable (Rollett Stability factor [K] > 1) regardless of trace and connector losses present in the actual application by adding a shunt 500 ohm resistor at the output. For the HB configuration , it is also advised to change R8 to 400K and C5 to 4.7 pF.

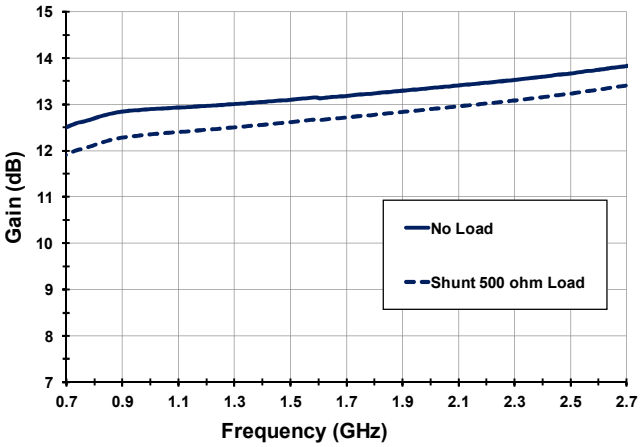
This 500 ohm shunt load will reduce the gain by about 0.4 dB but leave the rest of the performance parameters such as IP3, S22, etc. virtually unchanged.

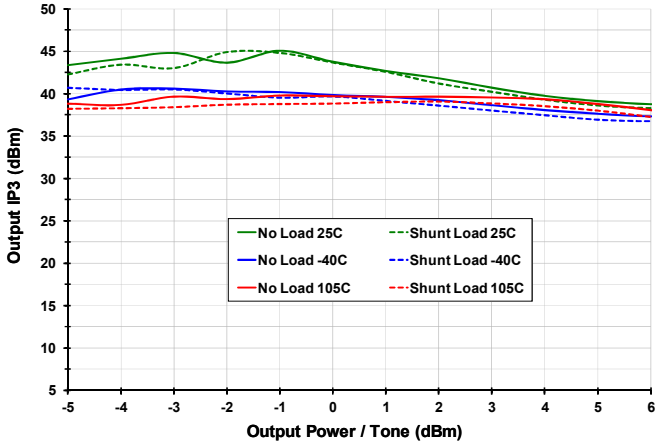
The 500 ohm shunt load will ensure that the device is unconditionally stable WITHOUT the presence of the input and output traces and connectors associated with the EVkit. In all cases we do recommend that the output capacitor, C5, be placed as close to the output of the package as possible.





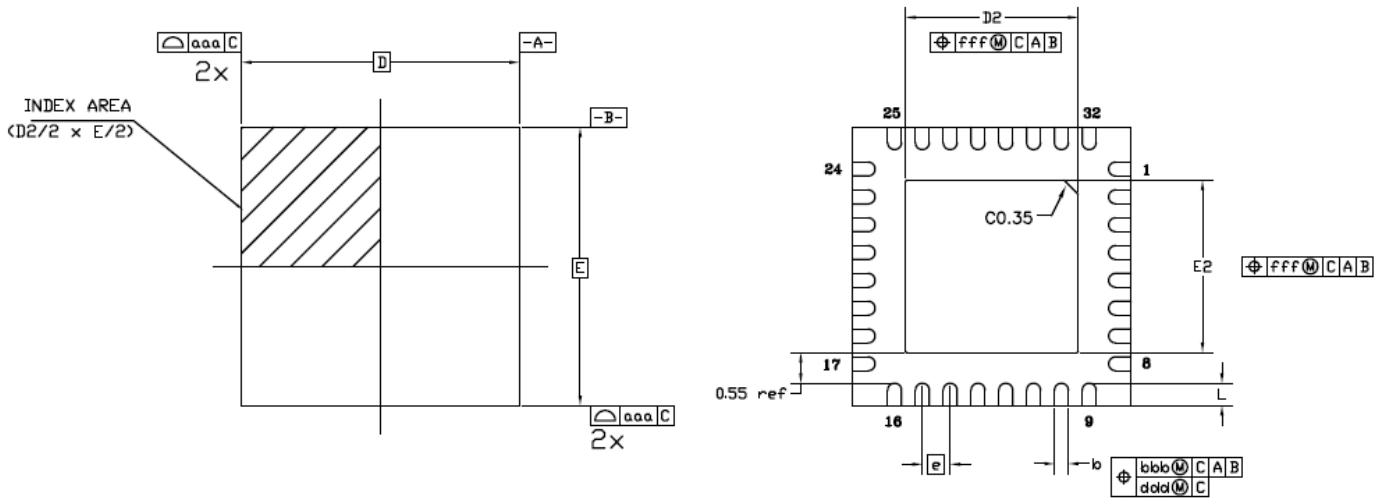
Gain Comparison (25C Ambient) and Output IP3 Comparison (2.7 GHz Frequency)

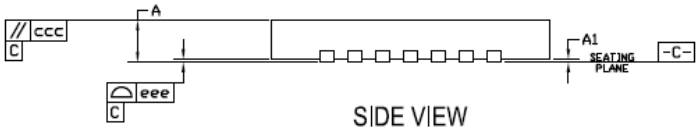




PACKAGE DRAWING

(5MM X 5MM 32-PIN TQFN), USE EXPOSED PAD (EPAD) OPTION P1





SYMBOL	DIMENSION		
	MIN	NOM	MAX
L	0.30	0.40	0.50
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	.20	.25	.30
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

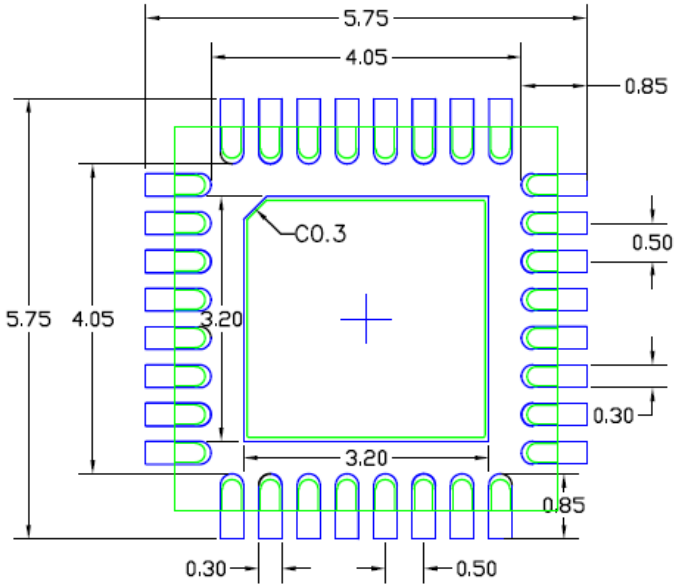
EPAD OPTION

SYMBOL	P1			P2		
	MIN	NOM	MAX	MIN	NOM	MAX
E2	3.00	3.10	3.20	3.10	3.30	3.40
D2	3.00	3.10	3.20	3.10	3.30	3.40

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.

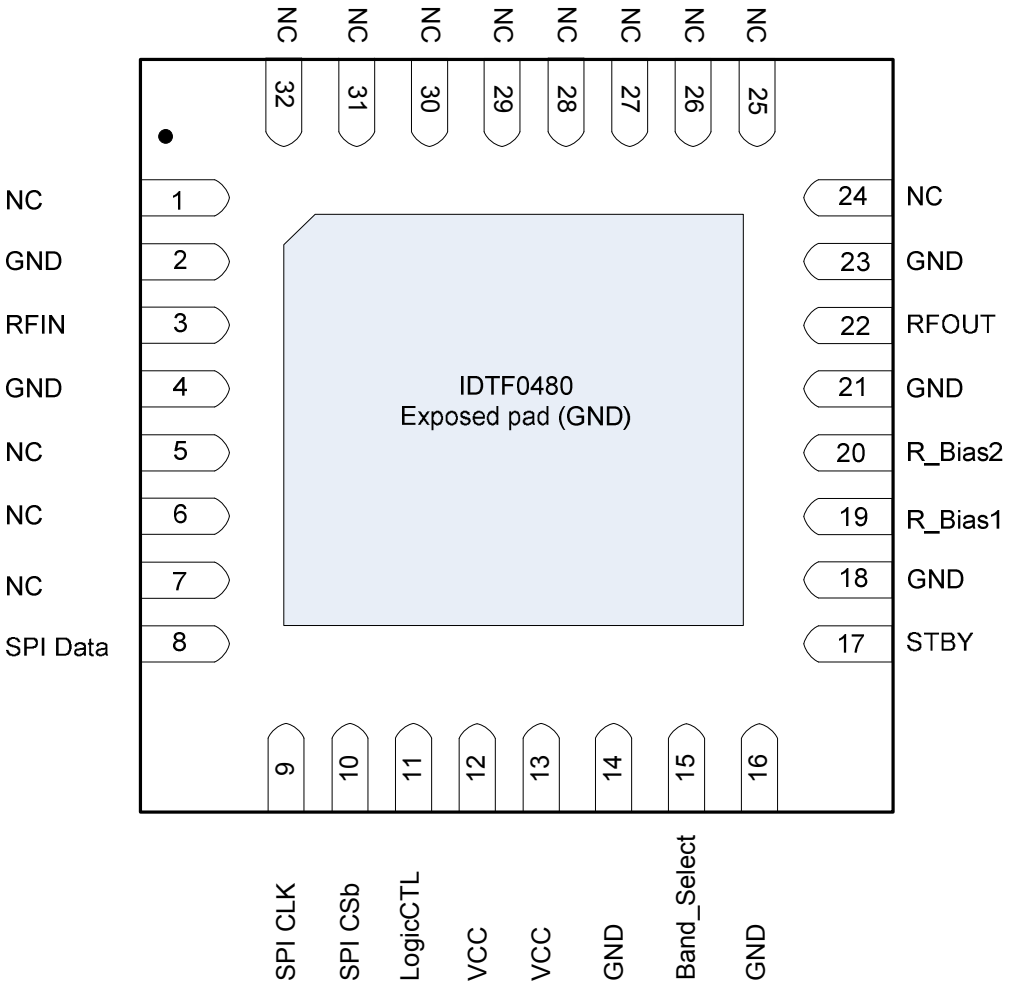
LAND PATTERN DIMENSION



EPAD 3.1 mm SQ

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

PIN DIAGRAM

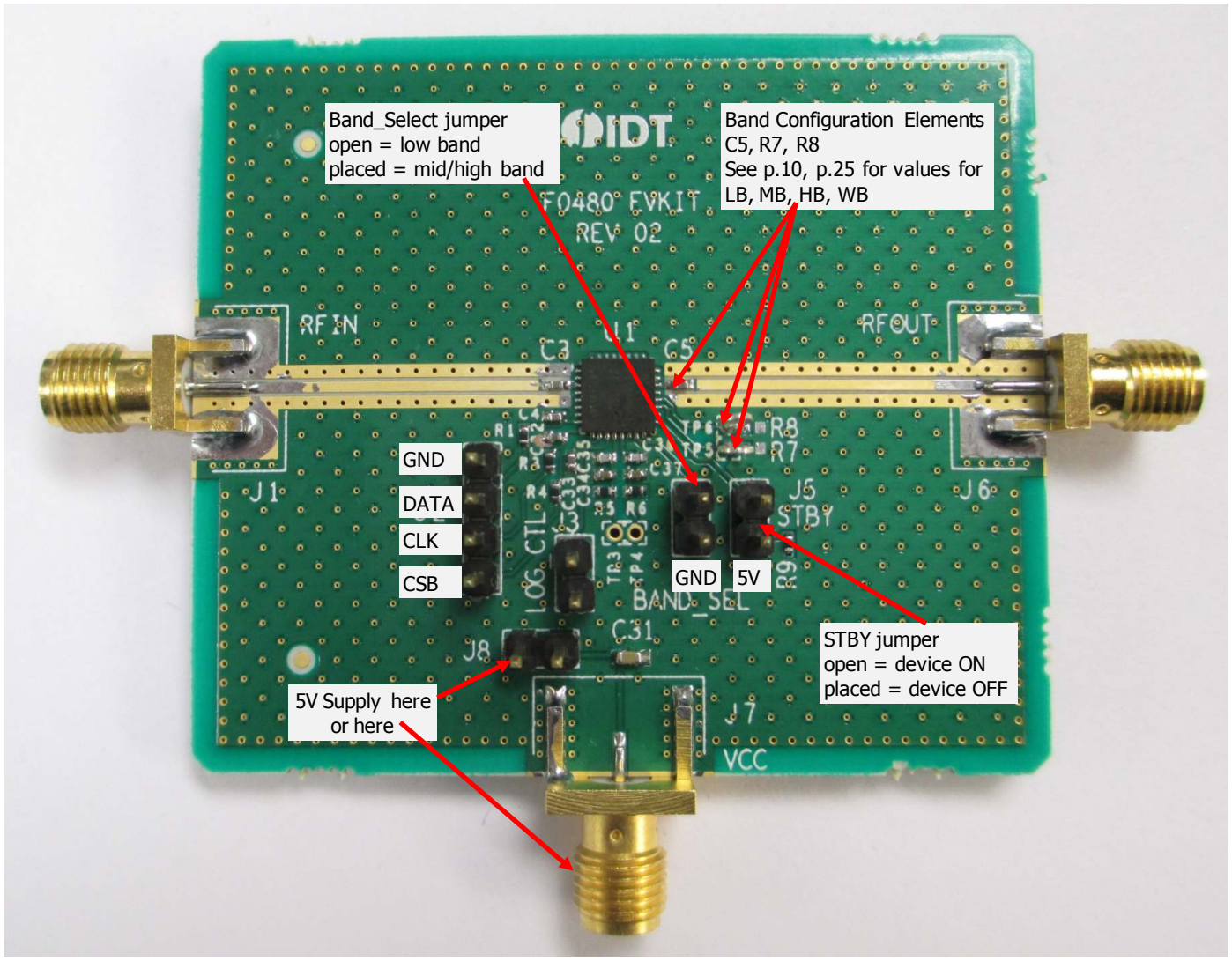

NC 32
NC 31
NC 30
NC 29
NC 28
NC 27
NC 26
NC 25
NC 1
GND 2
RFIN 3
GND 4
NC 5
NC 6
NC 7
SPI Data 8
24 NC
23 GND
22 RFOUT
21 GND
20 R_Bias2
19 R_Bias1
18 GND
17 STBY
IDTF0480
Exposed pad (GND)
9 SPI CLK
10 SPI CSb
11 LogicCTL
12 VCC
13 VCC
14 GND
15 Band_Select
16 GND

PIN DESCRIPTION

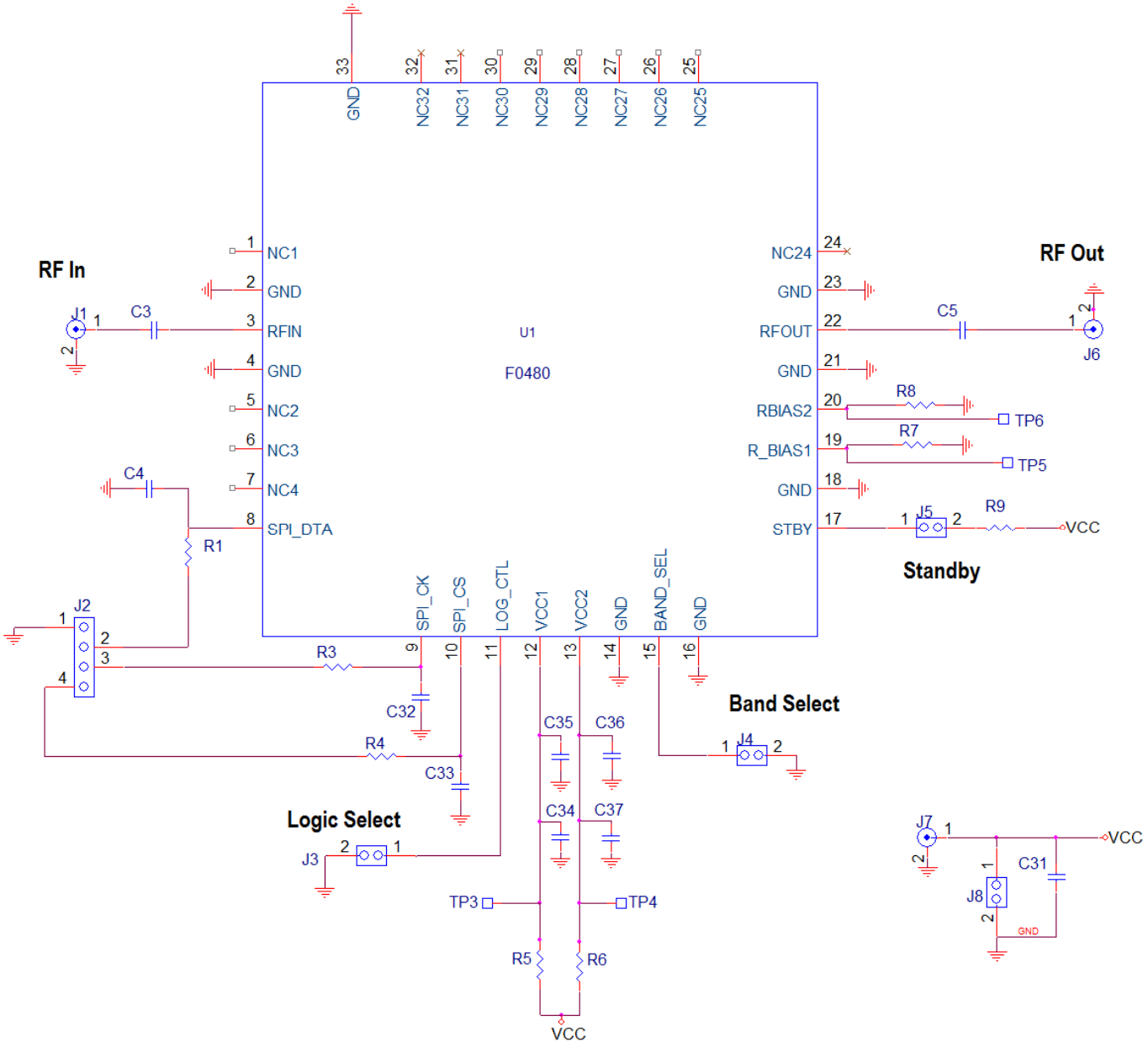
Pin	Name	Function
1, 5, 6, 7, 24, 25, 26, 27, 28, 29, 30, 31, 32	N.C.	No Connection. Not internally connected. OK to connect to VCC. OK to connect to GND.
2, 4, 14, 16, 18, 21, 23	GND	Ground these pins.
3	RFIN	RF input internally matched to 50 Ω. Must use external DC block as close to the pin as possible.
8	SPI Data[1]	Data input: 3.3V or 1.8V CMOS compatible. Set LogicCTL pin 11 for desired logic voltage.
9	SPI CLK[1]	Clock input: 3.3V or 1.8V CMOS compatible. Set LogicCTL pin 11 for desired logic voltage.
10	SPI CSb[1]	Chip Select input: 3.3V or 1.8V CMOS compatible. Set LogicCTL pin 11 for desired logic voltage. Active LOW shifts data.
11	LogicCTL	LogicCTL ≥ V_{IH} or Open Circuit sets 3.3V logic for SPI pins 8, 9, and 10. LogicCTL ≤ V_{IL} sets 1.8V logic for SPI pins 8, 9, and 10. A ~100Kohm pull-up resistor connects between the input and Vcc/2. For 1.8V logic, connect 0 Ω resistor to GND.
12	VCC	5 V Power Supply. Tie to VCC and connect 2 bypass capacitors with values 1000 pf (closest to pin) and 0.1 µF. See Typical Application Circuit for details.
13	VCC	5 V Power Supply. Tie to VCC and connect 2 bypass capacitors with values 1000 pf (closest to pin) and 0.1 µF. See Typical Application Circuit for details.
15	Band_Select	Leave pin open circuited for lowband select and connect 0 Ω resistor to GND for highband select. A ~1.5Mohm pull-up resistor connects between the input and VCC. 3.3V and 1.8V CMOS logic compatible.
17	STBY	Standby (Low/Open = device power ON, High = device power OFF with SPI still powered ON). A ~1Mohm pull-down resistor connects between the input and GND. 3.3V and 1.8V CMOS logic compatible
19	R_Bias1	Connect external resistor to GND to optimize amplifier bias. Used in conjunction with pin 20.
20	R_Bias2	Connect external resistor to GND to optimize amplifier bias. Used in conjunction with pin 19.
22	RFOUT	RF output. Must use external DC block as close to the pin as possible.
33	— EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the noted RF performance.

1. The SPI interface should be built up by an 8-bit word where 5 bits are used for attenuation setting (see F0480 DVGA Attenuation word truth table above).

EvKit Picture



EVKIT / APPLICATIONS CIRCUIT



EVKIT / APPLICATIONS CIRCUIT (CONT)

EVKIT BOM

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C5	1	**LB Mode -** CAP CER 9PF 50V C0G (0402)	GRM1555C1H9R0DZ01D	Murata
		1	**MB Mode -** CAP CER 9PF 50V C0G (0402)	GRM1555C1H9R0DZ01D	
		1	**HB Mode -** CAP CER 6PF 50V C0G (0402)	GRM1555C1H6R0DZ01D	
		1	**BB Mode -** CAP CER 9PF 50V C0G (0402)	GRM1555C1H9R0DZ01D	
2	C4, C32, C33	3	CAP CER 2PF 50V C0G (0402)	GRM1555C1H2R0BA01D	Murata
3	C3	1	CAP CER 47PF 50V C0G (0402)	GRM1555C1H470JZ01D	Murata
4	C35, C36	2	CAP CER 1000PF 50V C0G (0402)	GRM1555C1H102JA01D	Murata
5	C34, C37	2	CAP CER 0.1UF 16V 10% X7R (0402)	GRM155R71C104KA88D	Murata
6	C31	1	CAP CER 10UF 6.3V X5R 0603	GRM188R60J106ME47D	Murata
7	R6, R9	2	RES 0.0 OHM 1/10W (0402) SMD	ERJ-2GE0R00X	Panasonic
8	R5	1	RES 20 OHM 1/10W 1% (0402) SMD	ERJ-2RKF20R0X	Panasonic
9	R1, R3, R4	3	RES 4700 OHM 1/10W 5% (0402) SMD	ERJ-2GEJ472X	Panasonic
10	R7	1	**LB Mode -** RES 2.2 KOHM 1/10W (0402) SMD	ERJ-2RKF2201X	Panasonic
		1	**MB Mode -** RES 2.4 KOHM 1/10W (0402) SMD	ERJ-2RKF2401X	
		1	**HB Mode -** RES 2.67 KOHM 1/10W (0402) SMD	ERJ-2RKF2671X	
		1	**BB Mode -** RES 2.2 KOHM 1/10W (0402) SMD	ERJ-2RKF2201X	
11	R8	1	**LB Mode -** RES 9.1 KOHM 1/10W (0402) SMD	ERJ-2RKF9101X	Panasonic
		1	**MB Mode -** RES 27 KOHM 1/10W (0402) SMD	ERJ-2RKF2702X	
		1	**HB Mode -** RES 75 KOHM 1/10W (0402) SMD	ERJ-2RKF7502X	
		1	**BB Mode -** RES 20 KOHM 1/10W (0402) SMD	ERJ-2RKF2002X	
12	J1, J6, J7	3	SMA_END_LAUNCH (small)	142-0711-821	Emerson Johnson
13	J3, J4, J5, J8	4	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M
14	J2	1	CONN HEADER VERT SGL 4POS GOLD	961104-6404-AR	3M
15	U1	1	RF Amp	F0480	IDT
16		1	Printed Circuit Board	F0480 EVKIT	SBC

APPLICATIONS INFORMATION

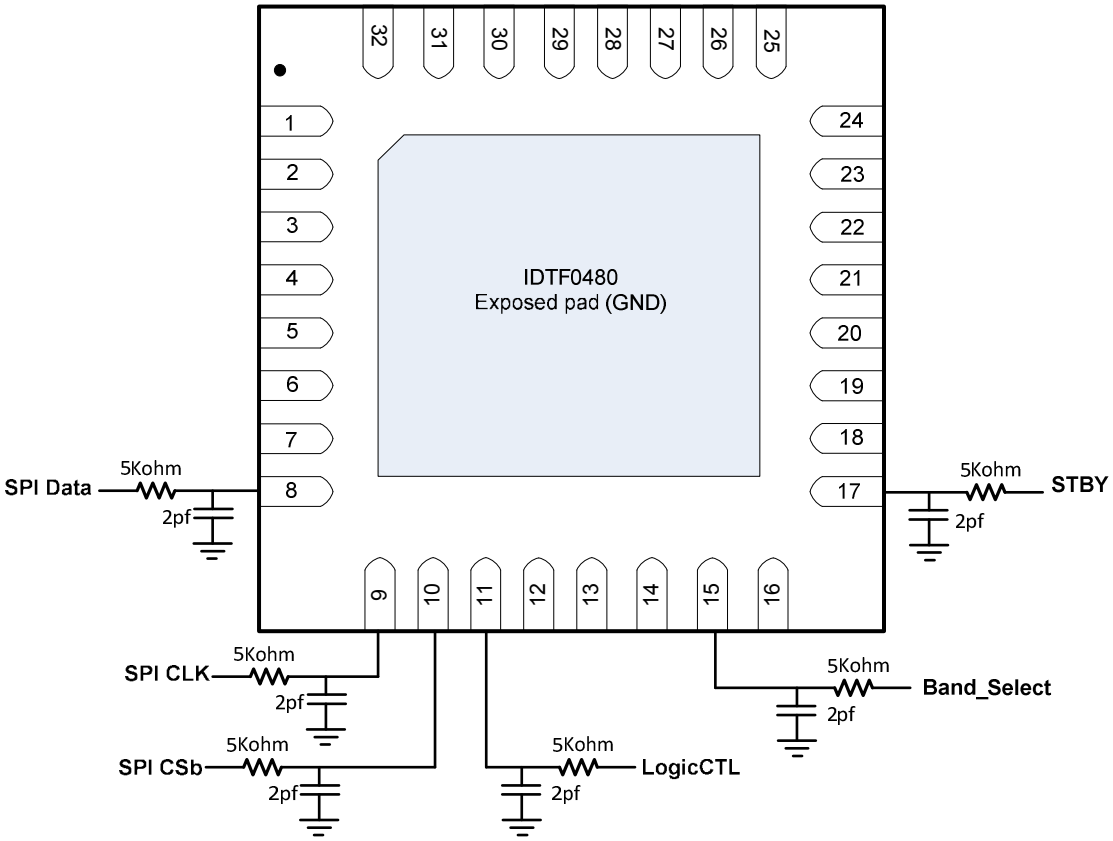
IDTF0480 has been optimized for use in high performance RF applications from 700 MHz to 2700 MHz.

Power Supplies

A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to SPI and control pins 8, 9, 10, 11, 15, and 17 as shown below. Note the recommended resistor and capacitor values do not necessarily match the EV kit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to overload the control line



TOP MARKINGS