TDA7266P

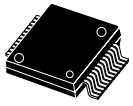
3+3W DUAL BRIDGE AMPLIFIER

PRODUCT PREVIEW

1 FEATURES

- TECHNOLOGY BI20II
- WIDE SUPPLY VOLTAGE RANGE (3.5 - 12V)
- OUTPUT POWER:
  - 3+3W @THD = 10%, R_L = 8Ω, V_{CC} = 7.5V
  - 4+4W Music Power @THD = 10%, R_L = 8Ω, V_{CC} = 8.5V
- SINGLE SUPPLY
- MINIMUM EXTERNAL COMPONENTS:
  - NO SVR CAPACITOR
  - NO BOOTSTRAP
  - NO BOUCHEROT CELLS
  - INTERNALLY FIXED GAIN
- STAND-BY & MUTE FUNCTIONS
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

Figure 1. Package



PowerSSO24 (Slug Down)

Table 1. Order Codes

Part Number	Package
TDA7266P	PowerSSO24 (Slug Down)

2 DESCRIPTION

The TDA7266P is a dual bridge amplifier specially designed for LCD TV/Monitor, PC Motherboard, TV and Portable Audio applications.

Figure 2. Test and Application Diagram

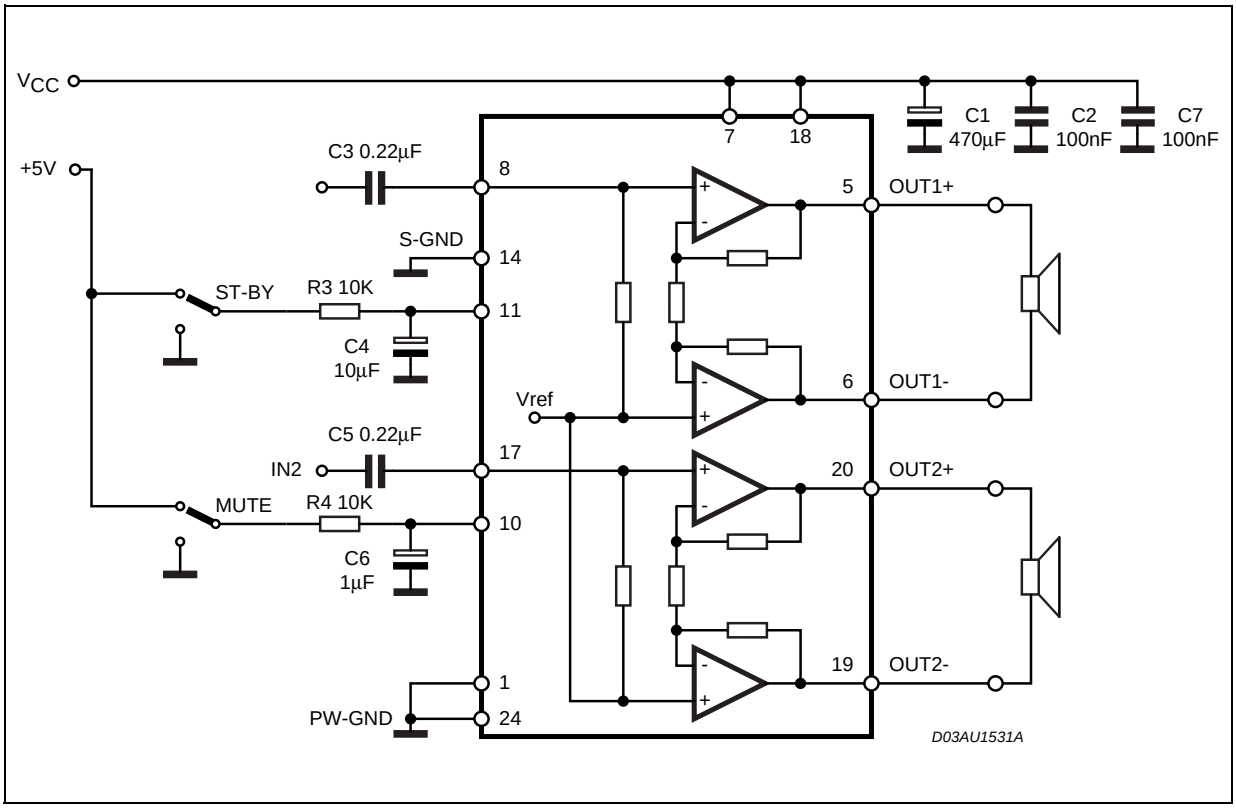
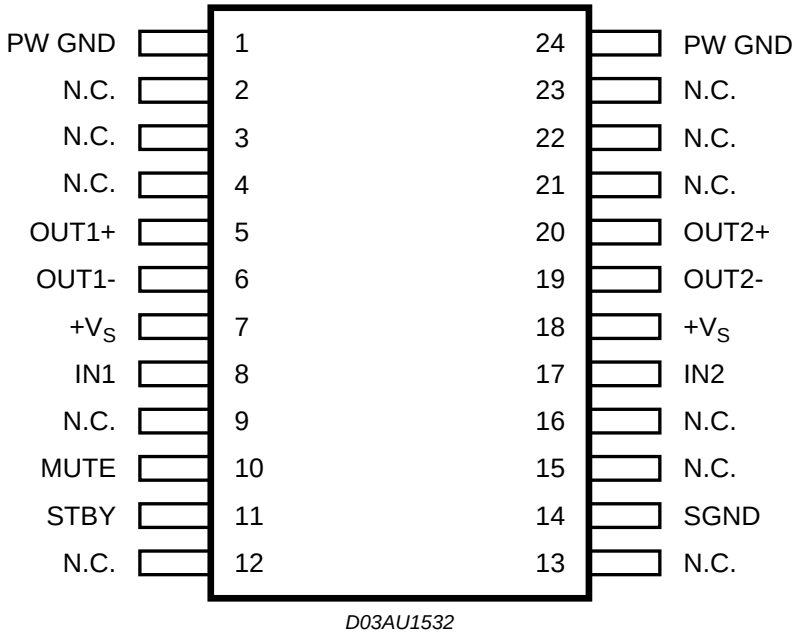


Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	20	V
I_O	Output Peak Current (internally limited)	1.5	A
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

Figure 3. Pin Connection (Top view)



D03AU1532

Table 3. Themal Data

Symbol	Parameters		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to Case	Typ.	1.5	°C/W

Table 4. Electrical Characteristcs

(Refer to test circuit; V_{CC} = 7.5V, R_L = 8Ω, f = 1KHz, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Range		3.5		12	V
I_q	Total Quiescent Current			40		mA
V_{OS}	Output Offset Voltage				120	mV
P_O	Output Power	THD 10%		3		W
P_O	Output Music Power (*)			4		W
THD	Total Harmonic Distortion	P_O = 1W		0.03	0.2	%
		P_O = 0.1W to 2W f = 100Hz to 15KHz			1	%
SVR	Supply Voltage Rejection	f = 100Hz, VR =0.5V	40	56		dB
CT	Crosstalk		46	60		dB
A_{MUTE}	Mute Attenuation		60	80		dB
T_w	Thermal Threshold			150		°C
G_V	Closed Loop Voltage Gain		25	26	27	dB
ΔG_V	Voltage Gain Matching				0.5	dB
R_i	Input Resistance		25	30		KΩ
VT_{MUTE}	Mute Threshold	for V_{CC} > 6.4V; Vo = -30dB	2.3	2.9	4.1	V
		for V_{CC} < 6.4V; Vo = -30dB	$V_{CC}/2$ -1	$V_{CC}/2$ -0.75	$V_{CC}/2$ -0.5	V
VT_{ST-BY}	St-by Threshold		0.8	1.3	1.8	V
I_{ST-BY}	St-by Current V6 = GND				100	µA
e_N	Total Output Voltage	A Curve		150		µV

(*) Measured on demoboard of figure 8 with gaussian noise signal which simulates Music/Speech programmes.

3 APPLICATIVE SUGGESTIONS

3.1 STAND-BY AND MUTE FUNCTIONS

3.1.1 (A) Microprocessor Application

In order to avoid annoying "Pop-Noise" during Turn-On/Off transients, it is necessary to guarantee the right St-by and mute signals sequence.It is quite simple to obtain this function using a microprocessor (Fig. 4 and 5).

At first St-by signal (from µP) goes high and the voltage across the St-by terminal (Pin 11) starts to increase exponentially. The external RC network is intended to turn-on slowly the biasing circuits of the amplifier, this to avoid "POP" and "CLICK" on the outputs.

When this voltage reaches the St-by threshold level, the amplifier is switched-on and the external capacitors in series to the input terminals (C1, C3) start to charge.

It's necessary to mantain the mute signal low until the capacitors are fully charged, this to avoid that the device goes in play mode causing a loud "Pop Noise" on the speakers.

A delay of 100-200ms between St-by and mute signals is suitable for a proper operation.

Figure 4. Microprocessor Application

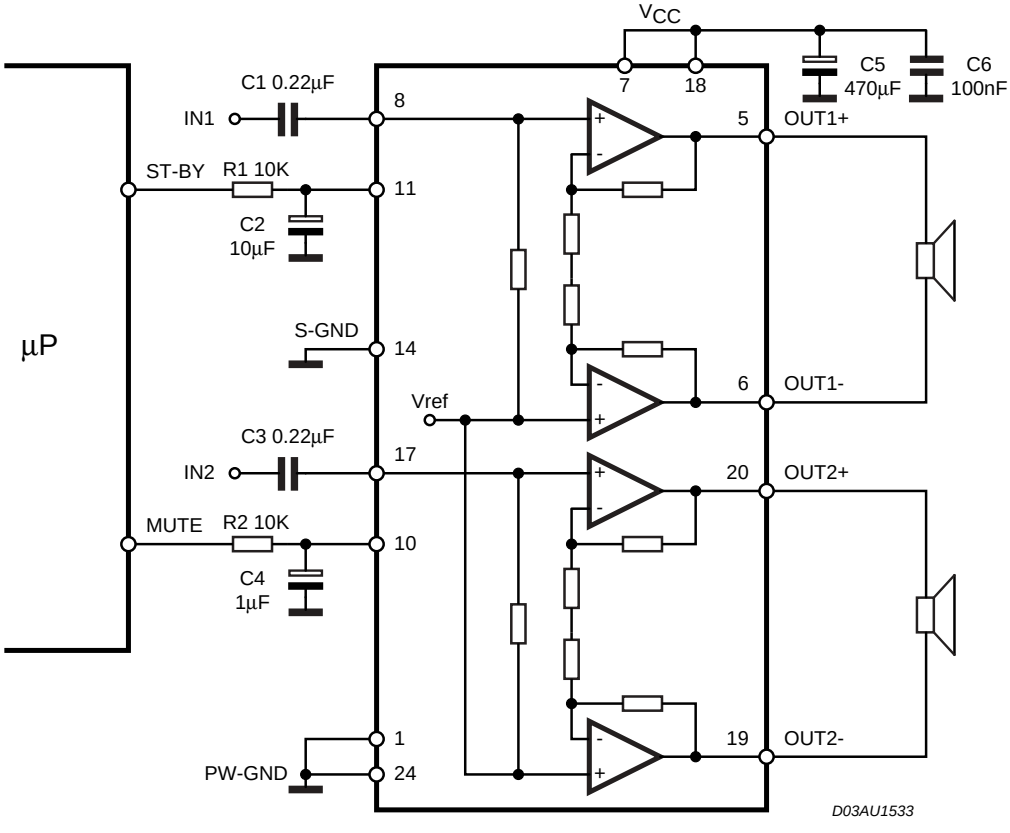
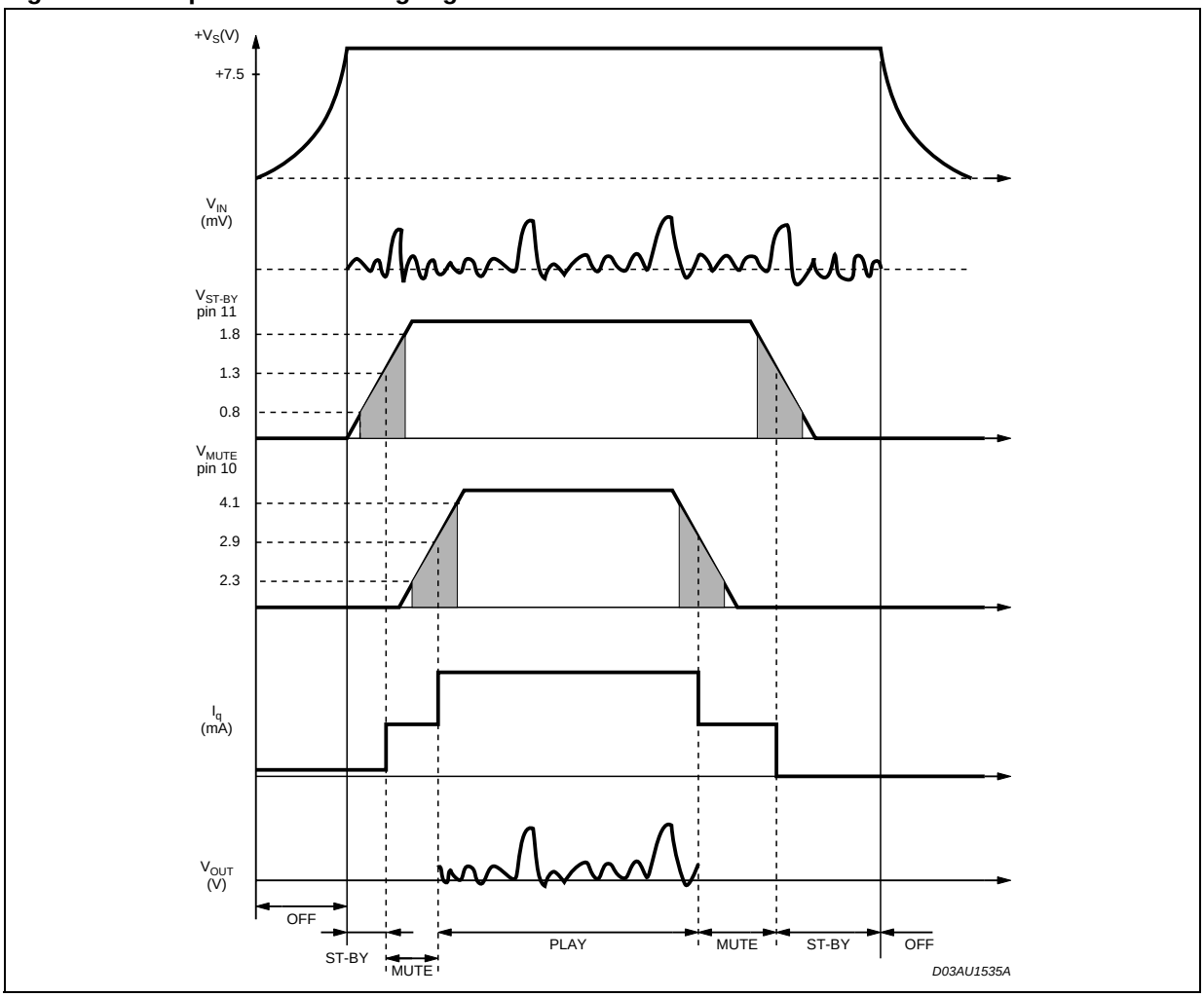


Figure 5. Microprocessor Driving Signals



3.1.2 B) Low Cost Application

In low cost applications where the µP is not present, the suggested circuit is shown in fig.6.

The St-by and mute terminals are tied together and they are connected to the supply line via an external voltage divider.

The device is switched-on/off from the supply line and the external capacitor C4 is intended to delay the St-by and mute threshold exceeding, avoiding "Popping" problems.
So to avoid any popping or clicking sond, it is important to clock:

a **Correct Sequence:** At turn-ON, the Stand-by must be removed at first, then the Mute must be released after a delay of about 100-200ms. On the contrary at turn-OFF the Mute must be activated as first and then the Stand-by.
With the values suggested in the Application circuit the right operation is guaranteed.

b **Correct Threshold Voltages:** In order to avoid that due to the spread in the internal thresholds (see the above limits) a wrong external voltage causes uncertain commutations for the two functions we suggest to use the following values:

Mute for Vcc>6.4V	:	VT = 2.3V
Mute for Vcc<6.4V	:	VT = Vcc/2 - 1
Stand-by	:	VT = 0.8V

Figure 6. Stand-alone low-cost Application

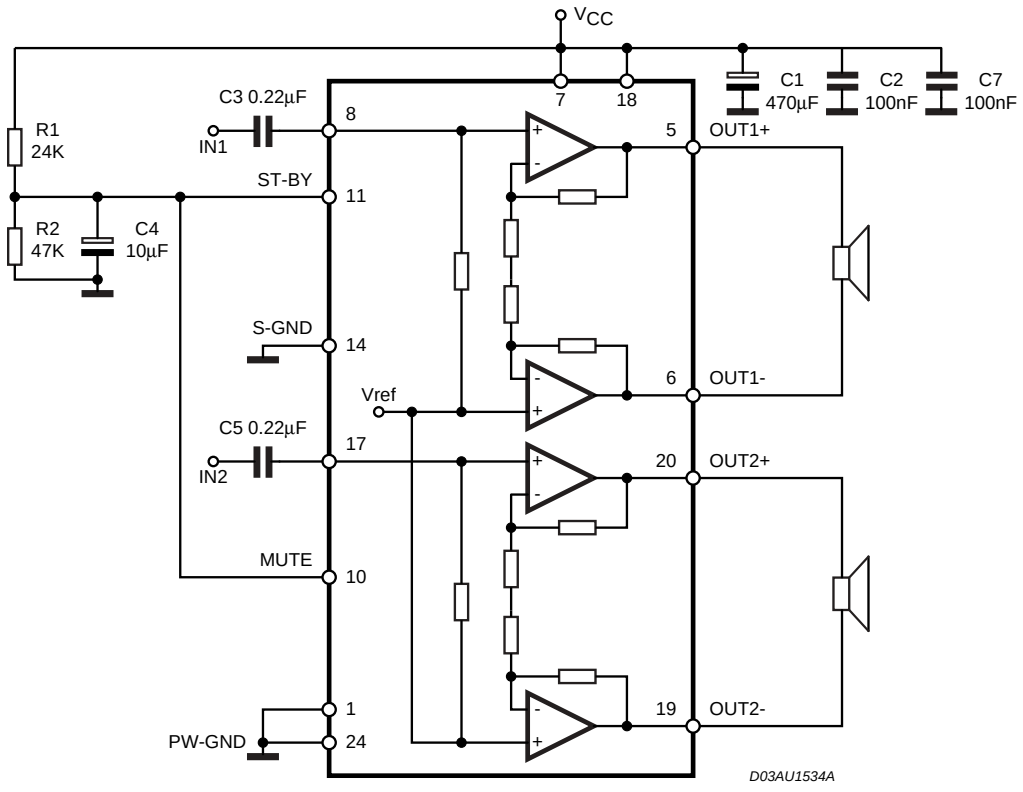


Figure 7. Application Circuit

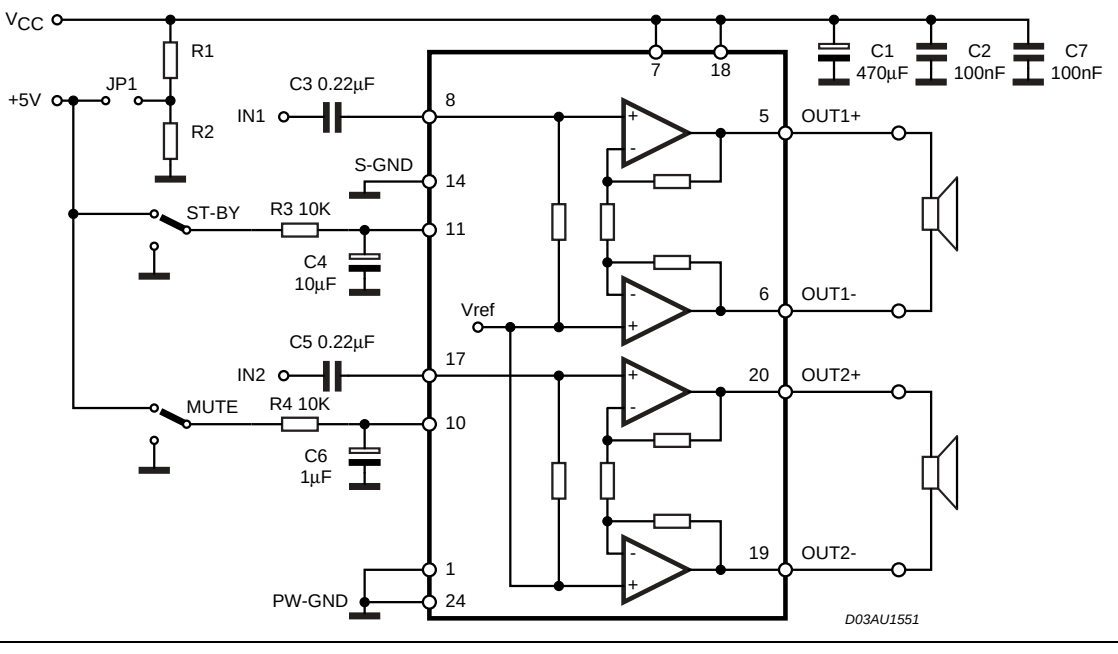


Figure 8. PCB Component Layout

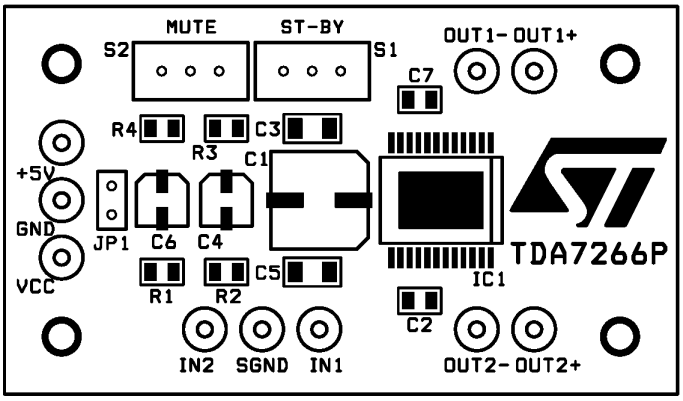


Figure 9. PCB Copper Top (Top view)

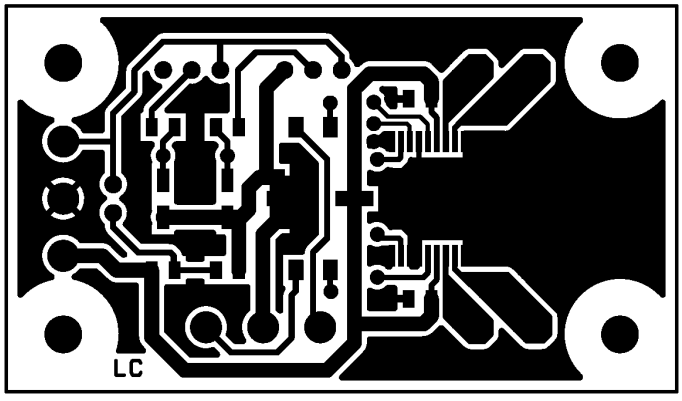
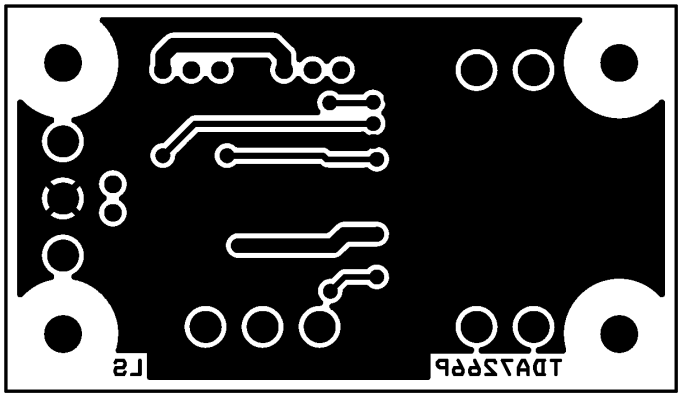


Figure 10. PCB Copper Bottom (Top view)



4 PCB LAYOUT AND EXTERNAL COMPONENTS

Regarding the PCB layout care must be taken for three main subjects:

1) Signal and Power Gnd separation

2) Dissipating Copper Area

3) Filter Capacitors positioning

1) Signal and Power Gnd separation:

To the Signal GND must be referred the Audio Input Signals, the Mute and Stand-by Voltages and the device PIN.14. This Gnd path must be as clean as possible in order to improve the device THD+Noise and to avoid spurious oscillations across the speakers.
The Power GND is directly connected to the Output power Stage transistors (Emitters) and is crossed by large amount of current, this path is also used in this device to dissipate the heating generated (no needs of external heatsinker).
Referring to the typical application circuit, the separation between the two GND paths must be obtained connecting them separately (star routing) to the bulk
Electrolithic capacitor C1 (470µF).
Regarding the Power Gnd dimensioning we have to consider the Dissipated Power the Thermal Protection Threshold and the Package thermal Characteristics.

2) Dissipating Copper Area:

Dissipated Power:
The max dissipated power happens for a THD near 1% and is given by the formula:

$$P_{dmax(W)} = 2 \cdot \frac{V_{CC}^2}{\pi^2 \frac{Rl}{2}} + I_q V_{CC}$$

This gives for: Vcc = 7.5V, Rl = 8Ω ,Iq = 40mA a dissipated power of Pd = 3W.

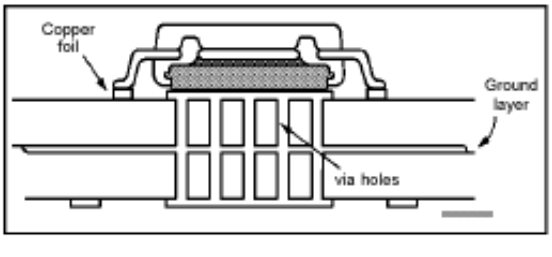
Thermal Protection:

The thermal protection threshold is placed at a junction temperature of 150°C.

Package Thermal Characteristics:

The thermal resistance Junction to Ambient obtainable with a GND copper Area of 3x3 cm and with 16 via holes (see picture) is about 25°C/W. This means that with the above mentioned max dissipated Power (Pd=3W) we can expect a 75°C, this gives a safety margin before the thermal protection intervention in the consumer environments where a 50°C ambient is specified as maximum

Figure 11.



3)Filter Capacitors Positioning:
The two Ceramic capacitors C2/C7 (100nF) must be placed as close as possible
respectively to the two Vcc pins (7 - 18) in order to avoid the possibiltiy of oscillations arising on the output Audio signals.

5 TYPICAL CHARACTERISTICS (Referred to application circuit of figure 8 unless otherwise specified)

Figure 12. Distortion vs Frequency

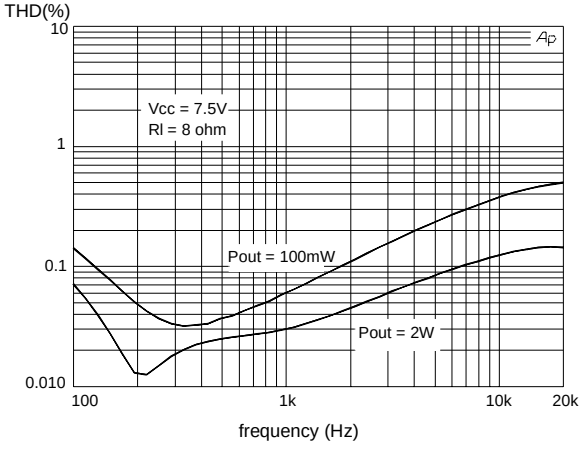


Figure 13. Distortion vs Output Power

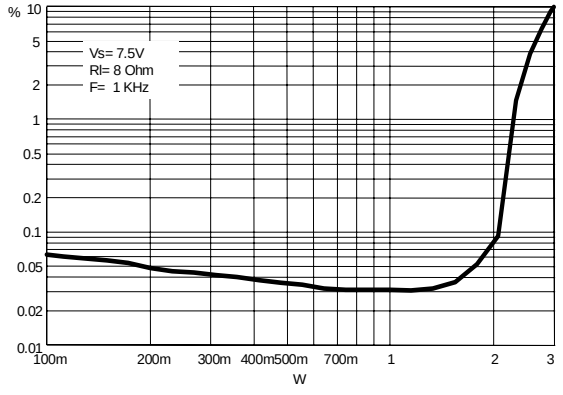


Figure 14. Distortion vs Output Power

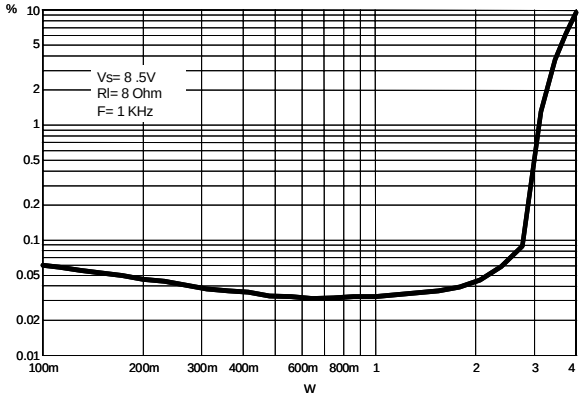


Figure 15. Gain vs Frequency

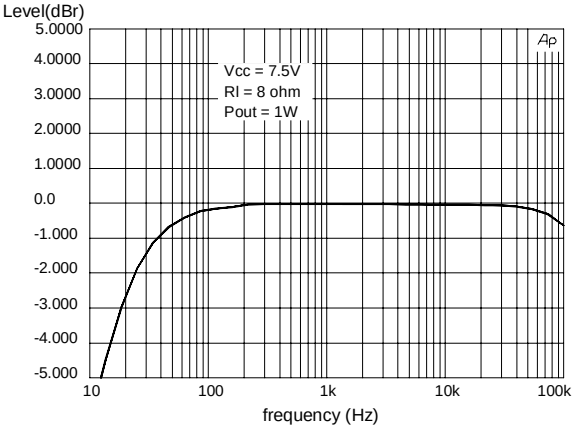


Figure 16. Mute Attenuation vs Vpin.10

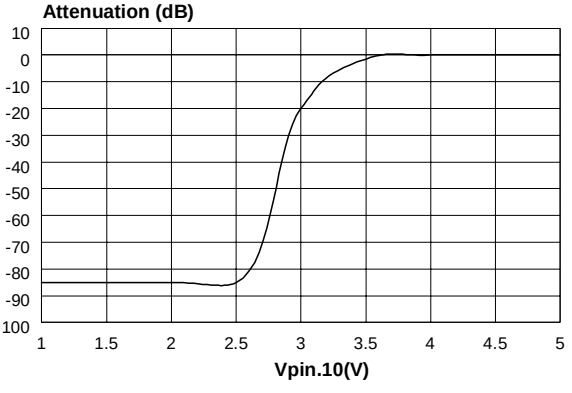


Figure 17. Stand-By attenuation vs Vpin 11

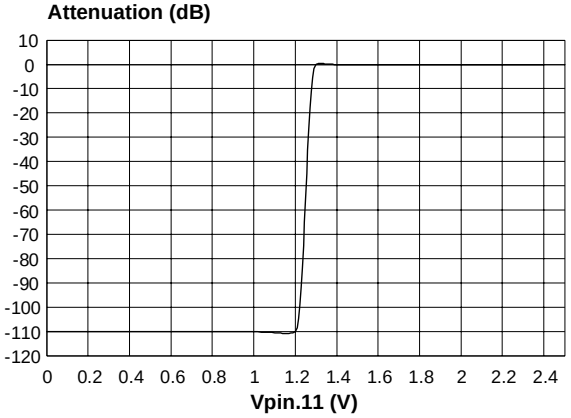
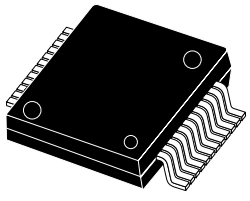


Figure 18. PowerSSO24 Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.15		2.47	0.084		0.097
A2	2.15		2.40	0.084		0.094
a1	0		0.075	0		0.003
b	0.33		0.51	0.013		0.020
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.4		7.6	0.291		0.299
e		0.8			0.031	
e3		8.8			0.346	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
L	0.55		0.85	0.022		0.033
N	10° (max)					
X	4.10		4.70	0.161		0.185
Y	6.50		7.10	0.256		0.279

(1) “D and E1” do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006”)
(2) No intrusion allowed inwards the leads.
(3) Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side

OUTLINE AND MECHANICAL DATA



PowerSSO24

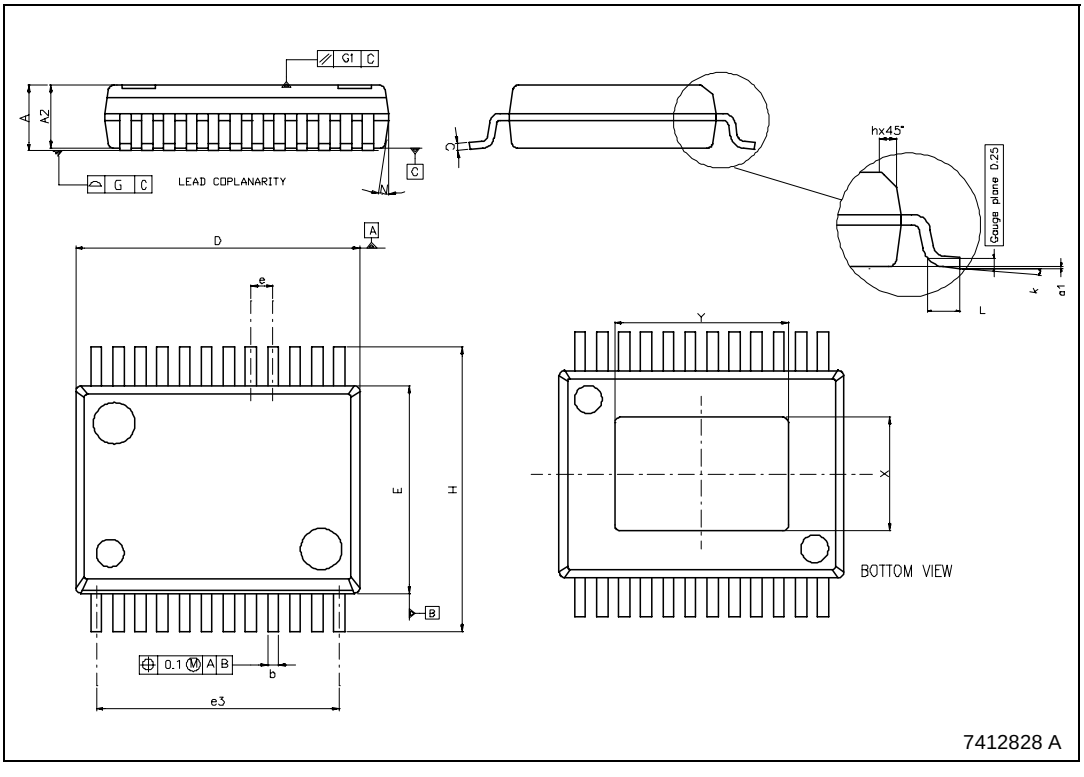


Table 5. Revision History

Date	Revision	Description of Changes
May 2004	1	First Issue
July 2004	2	Electrical Characteristics: Deleted TYP. Value VCC