



# NX1029X

60 / 50 V, 330 / 170 mA N/P-channel Trench MOSFET

Rev. 1 — 12 August 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV (N-channel) and 1 kV (P-channel)
- AEC-Q101 qualified

### 1.3 Applications

- Level shifter
- Power supply converter
- Load switch
- Switching circuits

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR2 (P-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$	-	-	-50	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-	-170	mA
<b>TR1 (N-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$	-	-	60	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-	-	330 mA
<b>TR1 (N-channel), Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 500\text{ mA};$ pulsed; $t_p \leq 300\text{ }\mu\text{s};$ $\delta \leq 0.01$ ; $T_j = 25^\circ\text{C}$	-	1	1.6	$\Omega$
<b>TR2 (P-channel), Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -100\text{ mA};$ $T_j = 25^\circ\text{C}$	-	4.5	7.5	$\Omega$

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

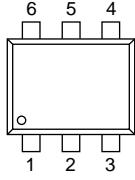
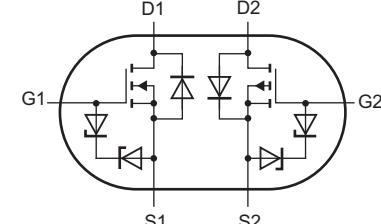
**nexperia**

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1		
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

SOT666 (SOT666)

017aaa262

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX1029X	SOT666	plastic surface-mounted package; 6 leads	SOT666

## 4. Marking

Table 4. Marking codes

Type number	Marking code <sup>[1]</sup>
NX1029X	AD

[1] % = placeholder for manufacturing site code.

## 5. Limiting values

**Table 5. Limiting values**

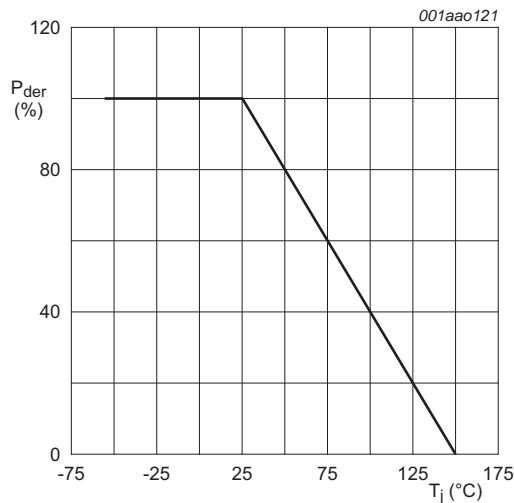
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>TR2 (P-channel)</b>					
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$	-	-50	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-170	mA
		$V_{GS} = -10\text{ V}; T_{amb} = 100^\circ\text{C}$	[1]	-110	mA
$I_{DM}$	peak drain current	$T_{amb} = 25^\circ\text{C}$ ; single pulse; $t_p \leq 10\ \mu\text{s}$	-	-0.7	A
$P_{tot}$	total power dissipation	$T_{amb} = 25^\circ\text{C}$	[2]	330	mW
		$T_{sp} = 25^\circ\text{C}$	[1]	390	mW
			-	1090	mW
<b>TR1 (N-channel)</b>					
$V_{DS}$	drain-source voltage	$T_j = 25^\circ\text{C}$	-	60	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25^\circ\text{C}$	[1]	-330	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 100^\circ\text{C}$	[1]	-210	mA
$I_{DM}$	peak drain current	$T_{amb} = 25^\circ\text{C}$ ; single pulse; $t_p \leq 10\ \mu\text{s}$	-	1.2	A
$P_{tot}$	total power dissipation	$T_{amb} = 25^\circ\text{C}$	[2]	330	mW
		$T_{sp} = 25^\circ\text{C}$	[1]	390	mW
			-	1090	mW
<b>Per device</b>					
$P_{tot}$	total power dissipation	$T_{amb} = 25^\circ\text{C}$	[2]	-	500 mW
$T_j$	junction temperature		-55	150	°C
$T_{amb}$	ambient temperature		-55	150	°C
$T_{stg}$	storage temperature		-65	150	°C
<b>TR1 (N-channel), Source-drain diode</b>					
$I_S$	source current	$T_{amb} = 25^\circ\text{C}$	[2][1]	-	330 mA
<b>TR2 (P-channel), Source-drain diode</b>					
$I_S$	source current	$T_{amb} = 25^\circ\text{C}$	[1]	-	-170 mA
<b>TR1 N-channel), ESD maximum rating</b>					
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	2000 V
<b>TR2 (P-channel), ESD maximum rating</b>					
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	1000 V

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

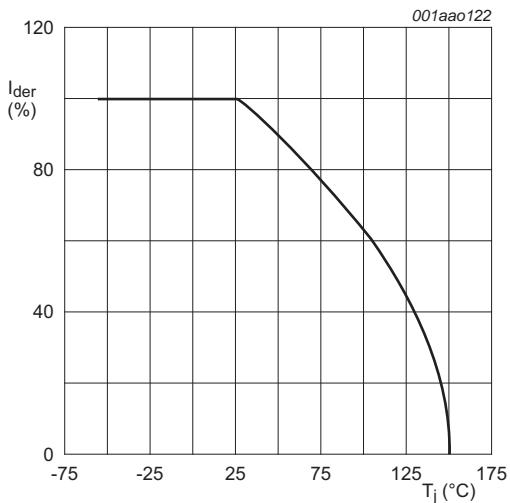
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[3] Measured between all pins.



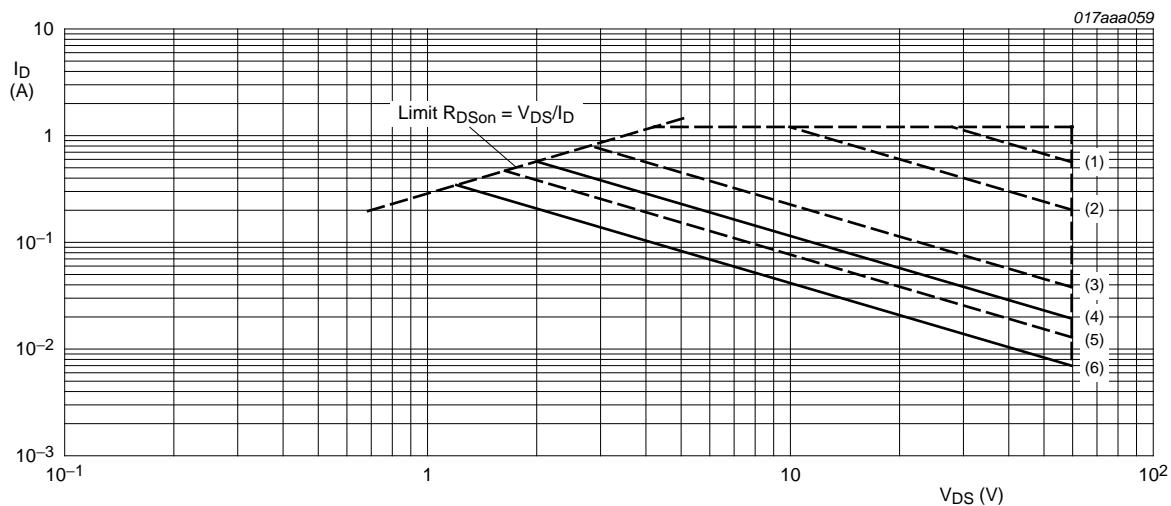
$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$

**Fig 1.** Normalized total power dissipation as a function of junction temperature



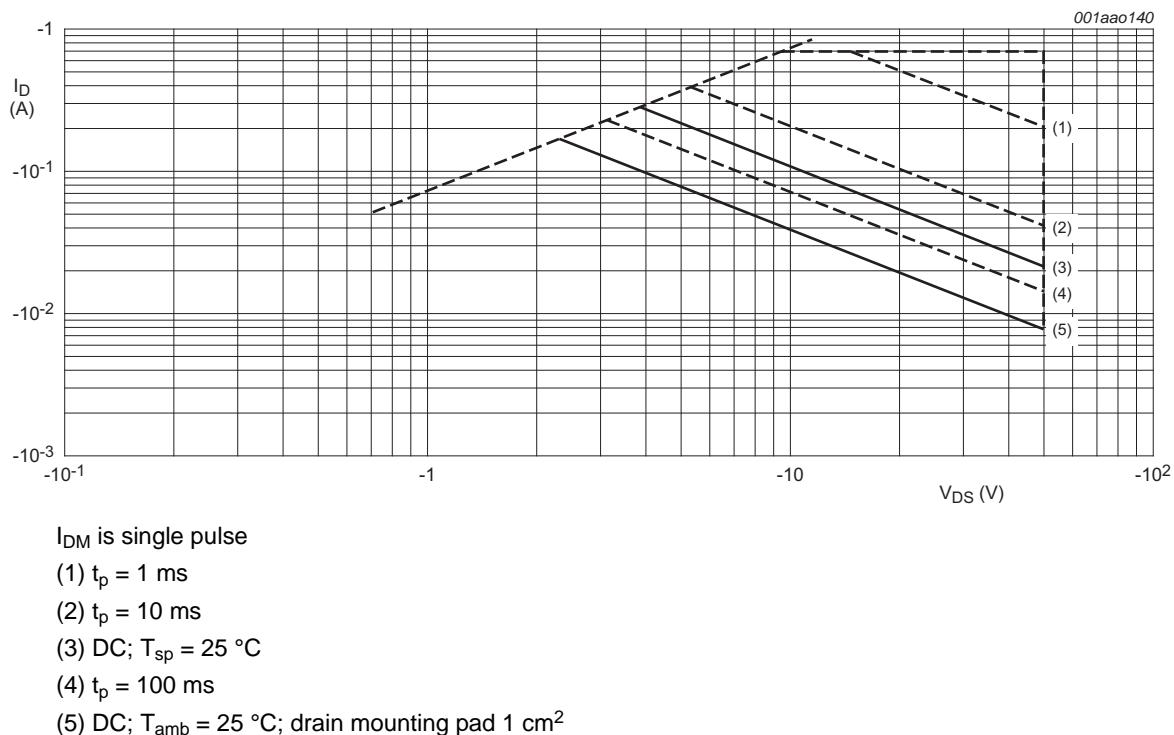
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

**Fig 2.** Normalized continuous drain current as a function of junction temperature



$I_{DM}$  = single pulse  
 (1)  $t_p = 100 \mu\text{s}$   
 (2)  $t_p = 1 \text{ ms}$   
 (3)  $t_p = 10 \text{ ms}$   
 (4) DC;  $T_{sp} = 25^\circ\text{C}$   
 (5)  $t_p = 100 \text{ ms}$   
 (6) DC;  $T_{amb} = 25^\circ\text{C}$ ; drain mounting pad  $1 \text{ cm}^2$

**Fig 3.** Safe operating area TR1 (N-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage



**Fig 4. Safe operating area TR2 (P-channel); junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

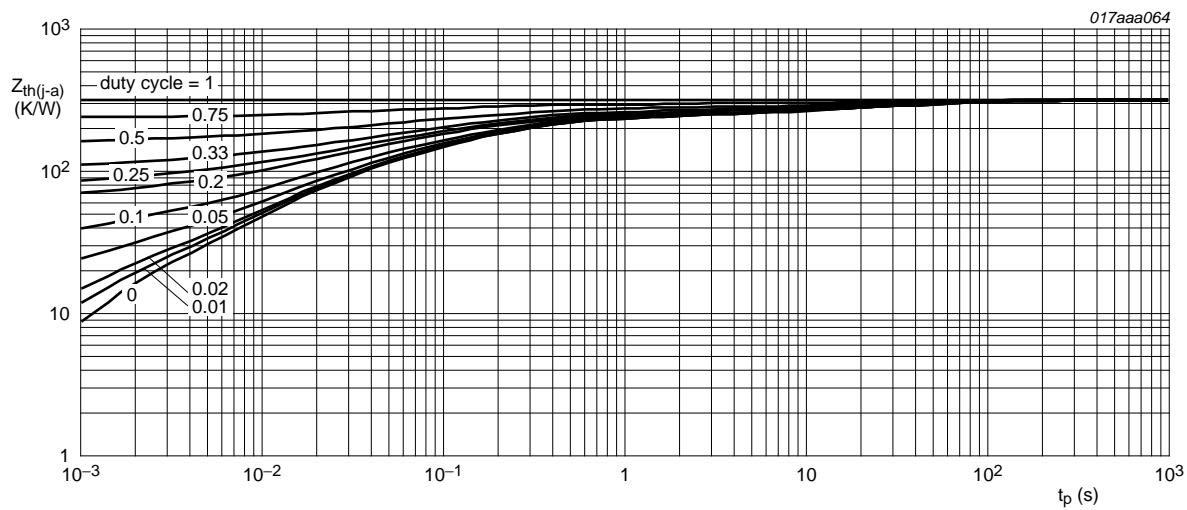
## 6. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per device</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250 K/W
<b>TR1 (N-channel)</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	330	380	K/W
			[2]	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	115	K/W
<b>TR2 (P-channel)</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	330	380	K/W
			[2]	280	320	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	115	K/W

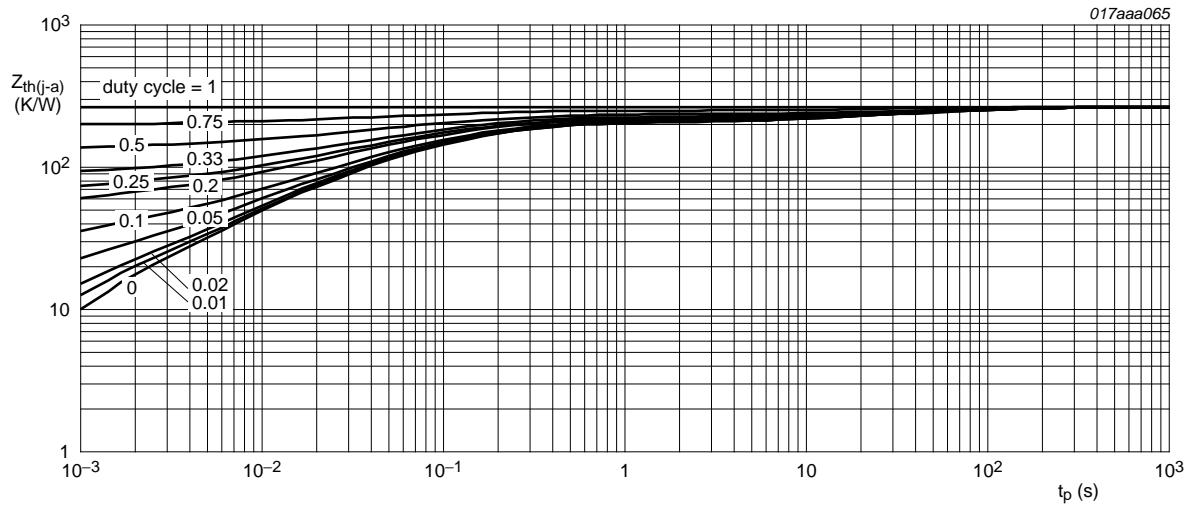
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.



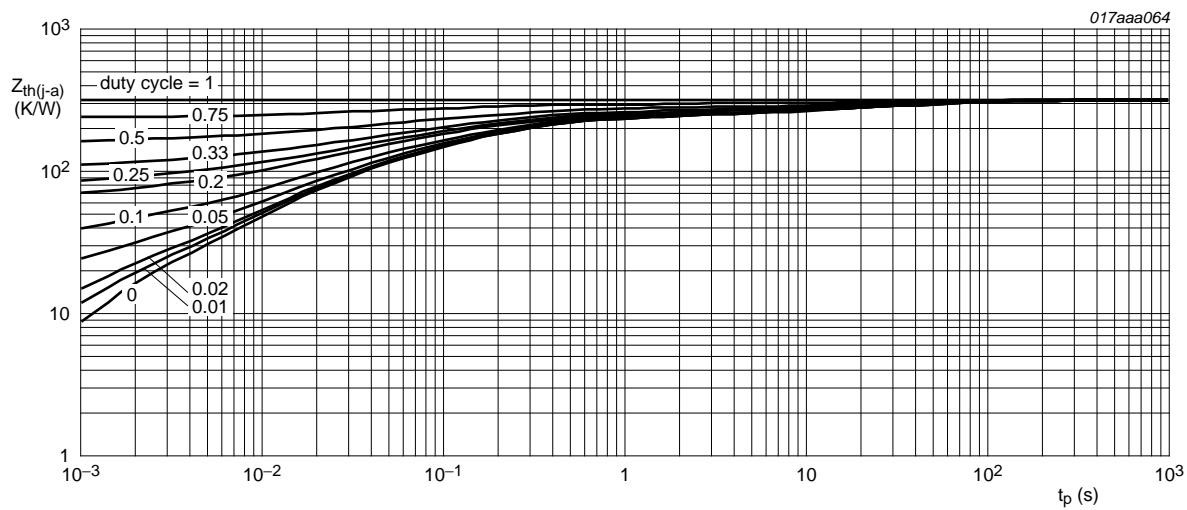
FR4 PCB, standard footprint

**Fig 5. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



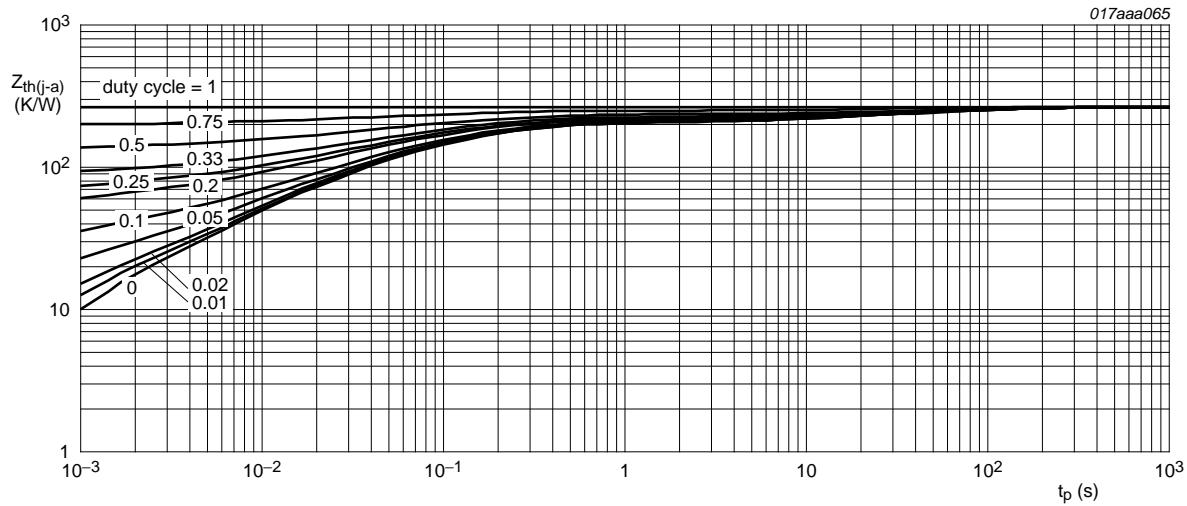
FR4 PCB, mounting pad for drain 1 cm<sup>2</sup>

**Fig 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB, standard footprint

**Fig 7. TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**



FR4 PCB, mounting pad for drain 1 cm<sup>2</sup>

**Fig 8. TR2: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR2 (P-channel), Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -10 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	-50	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$	-1.1	-1.6	-2.1	V
$I_{DSS}$	drain leakage current	$V_{DS} = -50 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -50 V; V_{GS} = 0 V; T_j = 150^\circ C$	-	-	-2	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	-10	$\mu A$
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	-10	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 V; I_D = -100 mA; T_j = 25^\circ C$	-	4.5	7.5	$\Omega$
		$V_{GS} = -10 V; I_D = -100 mA; T_j = 150^\circ C$	-	8	13.5	$\Omega$
		$V_{GS} = -5 V; I_D = -100 mA; T_j = 25^\circ C$	-	5.1	8.5	$\Omega$
$g_{fs}$	transfer conductance	$V_{DS} = -10 V; I_D = -100 mA; T_j = 25^\circ C$	-	150	-	$mS$
<b>TR1 (N-channel), Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	60	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25^\circ C$	1.1	1.6	2.1	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 150^\circ C$	-	-	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	10	$\mu A$
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	10	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 500 mA; pulsed; t_p \leq 300 \mu s; \delta \leq 0.01; T_j = 25^\circ C$	-	1	1.6	$\Omega$
		$V_{GS} = 10 V; I_D = 500 mA; pulsed; t_p \leq 300 \mu s; \delta \leq 0.01; T_j = 150^\circ C$	-	2.25	3.6	$\Omega$
		$V_{GS} = 5 V; I_D = 50 mA; pulsed; t_p \leq 300 \mu s; \delta \leq 0.01; T_j = 25^\circ C$	-	1.3	2	$\Omega$
$g_{fs}$	transfer conductance	$V_{DS} = 10 V; I_D = 100 mA; T_j = 25^\circ C$	-	550	-	$mS$
<b>TR2 (P-channel), Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -25 V; I_D = -180 mA; V_{GS} = -5 V; T_j = 25^\circ C$	-	0.26	0.35	$nC$
$Q_{GS}$	gate-source charge		-	0.12	-	$nC$
$Q_{GD}$	gate-drain charge		-	0.09	-	$nC$
$C_{iss}$	input capacitance	$V_{DS} = -25 V; f = 1 MHz; V_{GS} = 0 V; T_j = 25^\circ C$	-	24	36	$pF$
$C_{oss}$	output capacitance		-	4.5	-	$pF$
$C_{rss}$	reverse transfer capacitance		-	1.3	-	$pF$
$t_{d(on)}$	turn-on delay time	$V_{DS} = -30 V; R_L = 250 \Omega; V_{GS} = -10 V; R_{G(ext)} = 6 \Omega; T_j = 25^\circ C$	-	13	26	ns
$t_r$	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	48	96	ns
$t_f$	fall time		-	25	-	ns

Table 7. Characteristics ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR1 (N-channel), Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$V_{DS} = 30 \text{ V}$ ; $I_D = 300 \text{ mA}$ ; $V_{GS} = 4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.5	0.6	nC
$Q_{GS}$	gate-source charge		-	0.2	-	nC
$Q_{GD}$	gate-drain charge		-	0.1	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ;	-	33	50	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$	-	7	-	pF
$C_{rss}$	reverse transfer capacitance		-	4	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 50 \text{ V}$ ; $R_L = 250 \Omega$ ; $V_{GS} = 10 \text{ V}$ ;	-	5	10	ns
$t_r$	rise time	$R_{G(\text{ext})} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	6	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	12	24	ns
$t_f$	fall time		-	7	-	ns
<b>TR2 (P-channel), Source-drain diode characteristics</b>						
$V_{SD}$	source-drain voltage	$I_S = -115 \text{ mA}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.48	-0.85	-1.2	V
<b>TR1 (N-channel), Source-drain diode characteristics</b>						
$V_{SD}$	source-drain voltage	$I_S = 115 \text{ mA}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	0.47	0.75	1.1	V

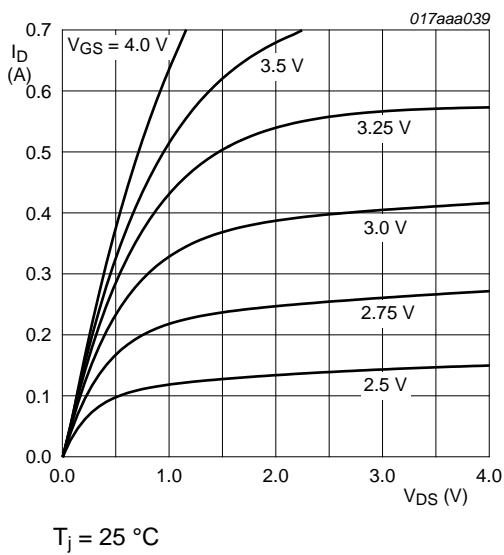


Fig 9. TR1: Output characteristics: drain current as a function of drain-source voltage; typical values

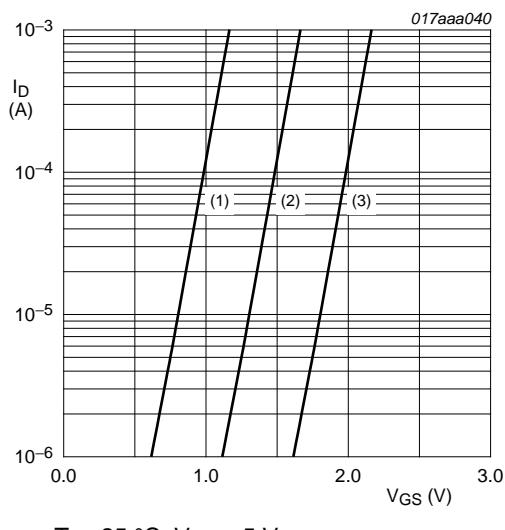
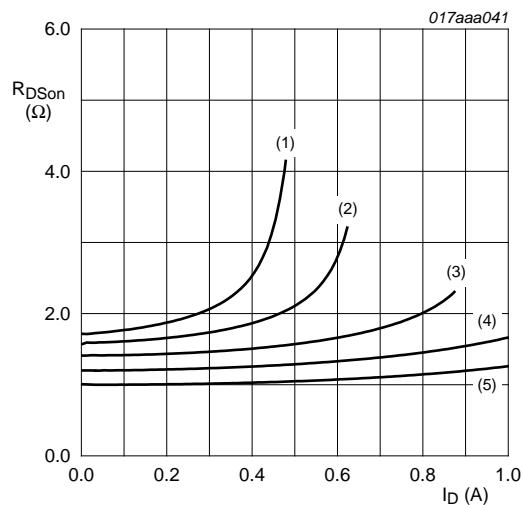


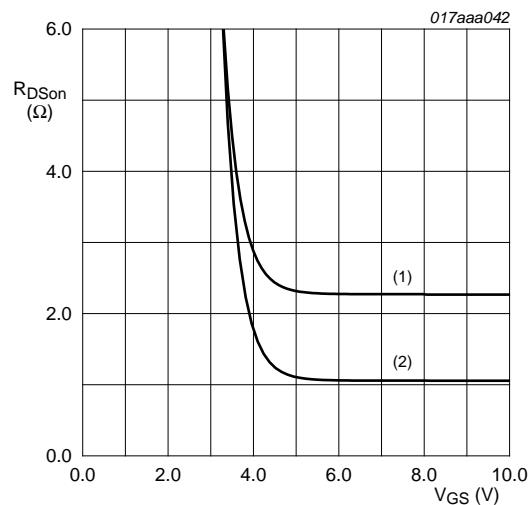
Fig 10. TR1: Sub-threshold drain current as a function of gate-source voltage



$T_j = 25^\circ\text{C}$

- (1)  $V_{GS} = 3.25\text{ V}$
- (2)  $V_{GS} = 3.5\text{ V}$
- (3)  $V_{GS} = 4\text{ V}$
- (4)  $V_{GS} = 5\text{ V}$
- (5)  $V_{GS} = 10\text{ V}$

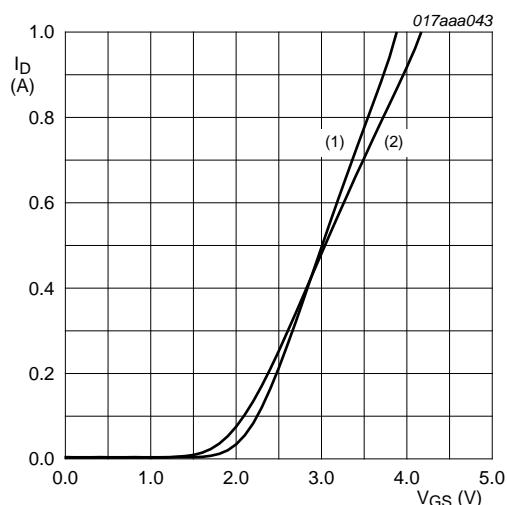
**Fig 11. TR1: Drain-source on-state resistance as a function of drain current; typical values**



$I_D = 500\text{ mA}; \text{ pulsed}; t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01$

- (1)  $T_j = 150^\circ\text{C}$
- (2)  $T_j = 25^\circ\text{C}$

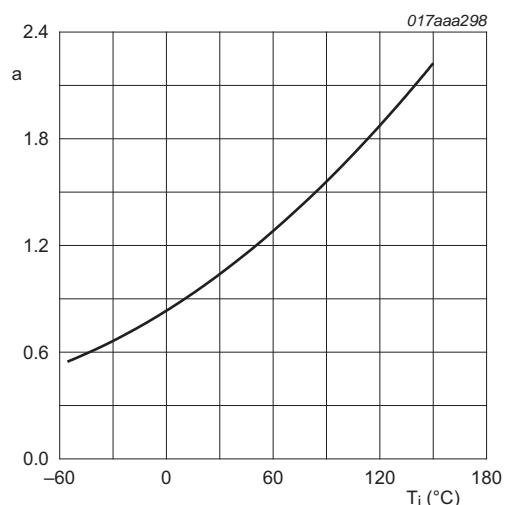
**Fig 12. TR1: Drain-source on-state resistance as a function of gate-source voltage; typical values**



$V_{DS} > I_D \times R_{DSon}$

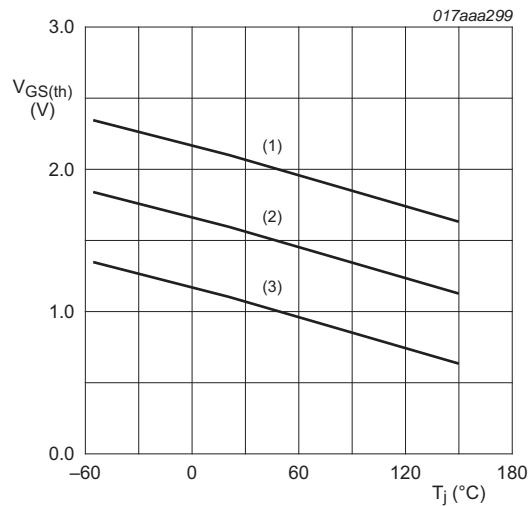
- (1)  $T_j = 25^\circ\text{C}$
- (2)  $T_j = 150^\circ\text{C}$

**Fig 13. TR1: Transfer characteristics: drain current as a function of gate-source voltage; typical values**



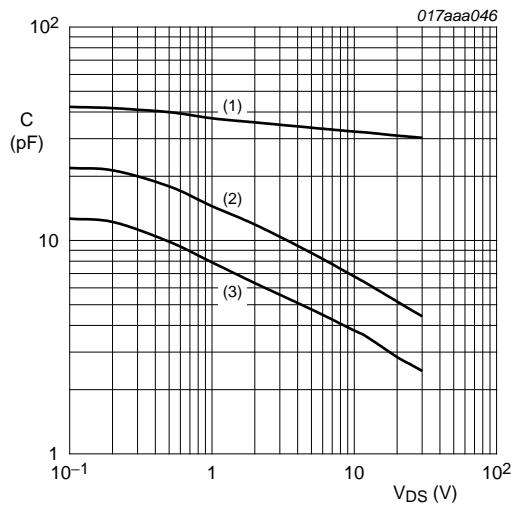
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

**Fig 14. TR1: Normalized drain-source on-state resistance as a function of junction temperature; typical values**



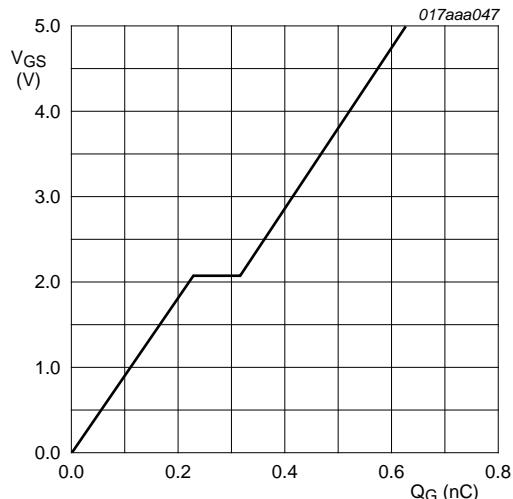
$I_D = 0.25$  mA;  $V_{DS} = V_{GS}$   
(1) maximum values  
(2) typical values  
(3) minimum values

**Fig 15. TR1: Gate-source threshold voltage as a function of junction temperature**



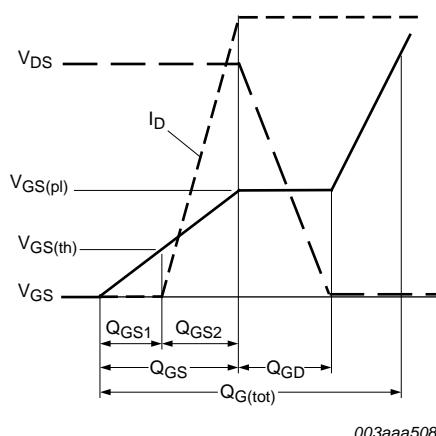
$f = 1$  MHz;  $V_{GS} = 0$  V  
(1)  $C_{iss}$   
(2)  $C_{oss}$   
(3)  $C_{rss}$

**Fig 16. TR1: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

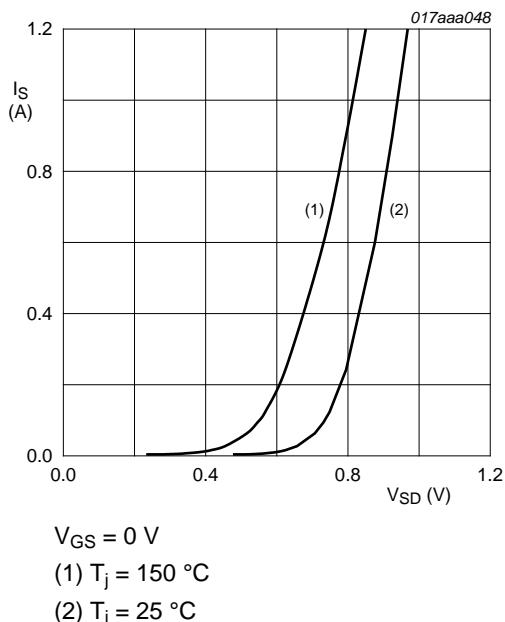


$I_D = 300$  mA;  $V_{DS} = 30$  V;  $T_{amb} = 25$  °C

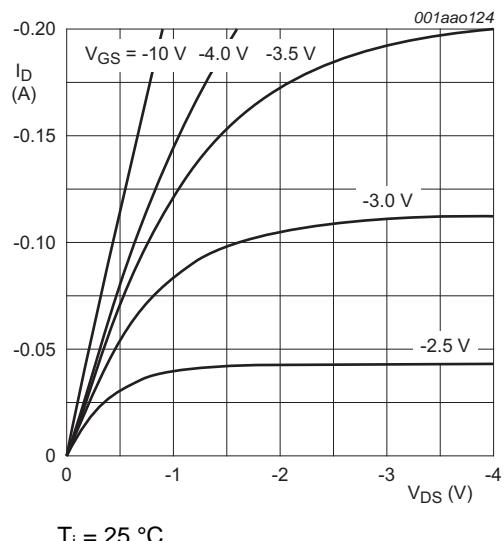
**Fig 17. TR1: Gate-source voltage as a function of gate charge; typical values**



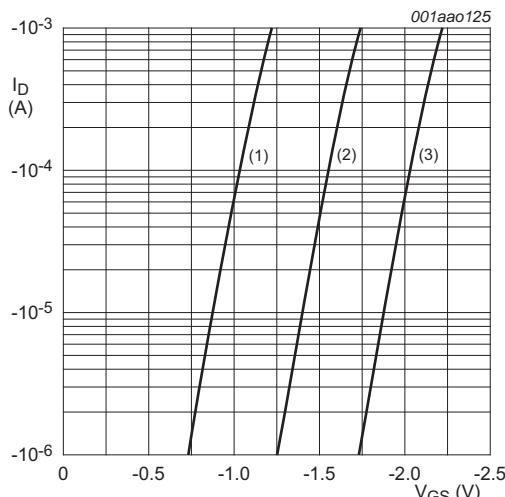
**Fig 18. Gate charge waveform definitions**



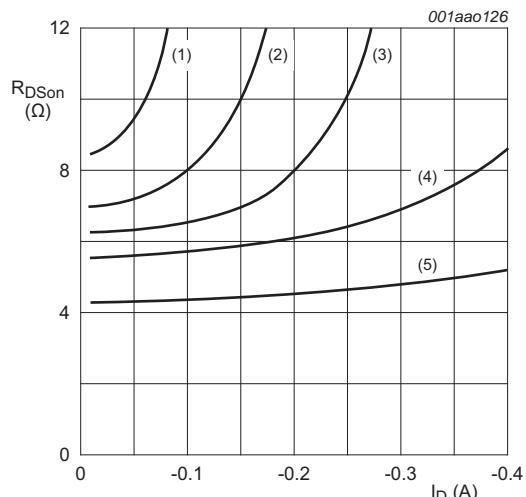
**Fig 19. TR1: Source current as a function of source-drain voltage; typical values**



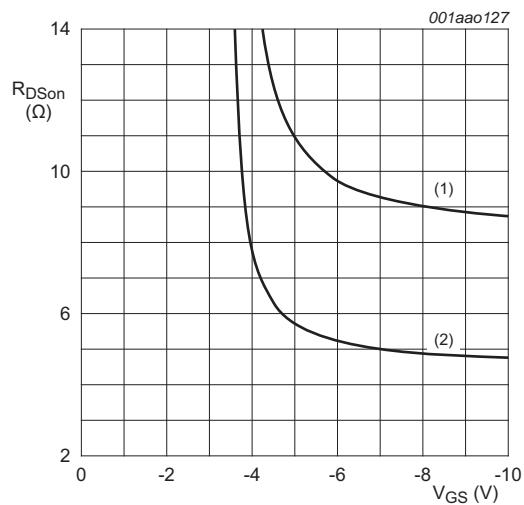
**Fig 20. TR2: Output characteristics: drain current as a function of drain-source voltage; typical values**



**Fig 21. TR2: Sub-threshold drain current as a function of gate-source voltage**

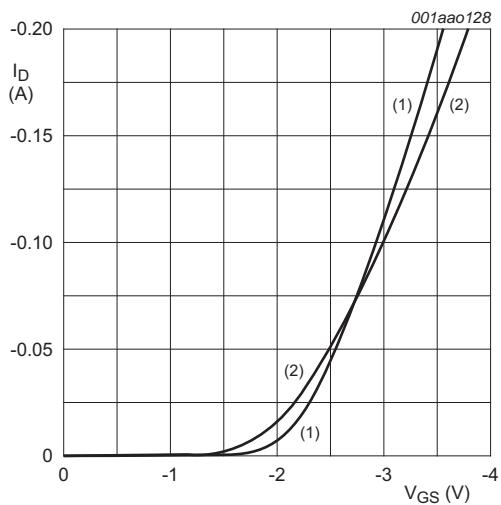


**Fig 22. TR2: Drain-source on-state resistance as a function of drain current; typical values**



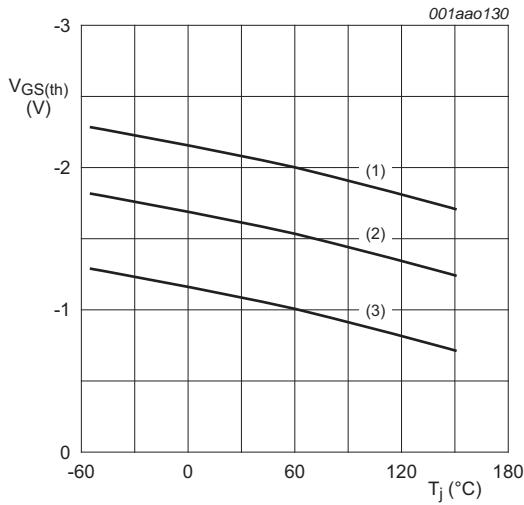
$I_D = -200 \text{ mA}$   
 (1)  $T_j = 150 \text{ }^\circ\text{C}$   
 (2)  $T_j = 25 \text{ }^\circ\text{C}$

**Fig 23. TR2: Drain-source on-state resistance as a function of gate-source voltage; typical values**



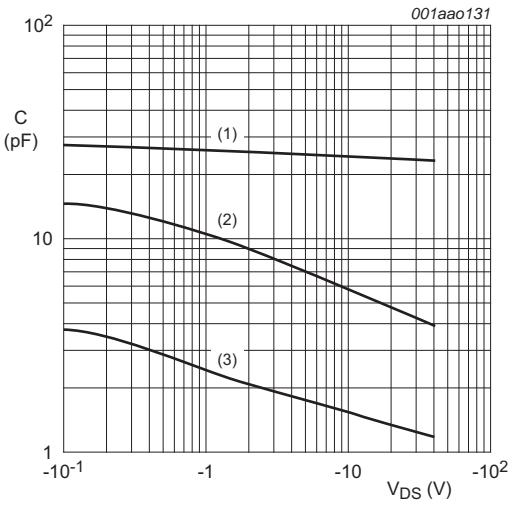
$V_{DS} > I_D \times R_{DS(on)}$   
 (1)  $T_j = 25 \text{ }^\circ\text{C}$   
 (2)  $T_j = 150 \text{ }^\circ\text{C}$

**Fig 24. TR2: Transfer characteristics: drain current as a function of gate-source voltage; typical values**



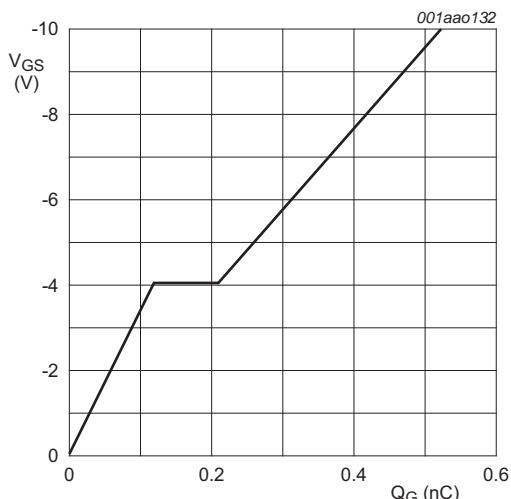
$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

**Fig 25. TR2: Gate-source threshold voltage as a function of junction temperature**



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

**Fig 26. TR2: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$I_D = -180$  mA;  $V_{DS} = -25$  V;  $T_{amb} = 25$  °C

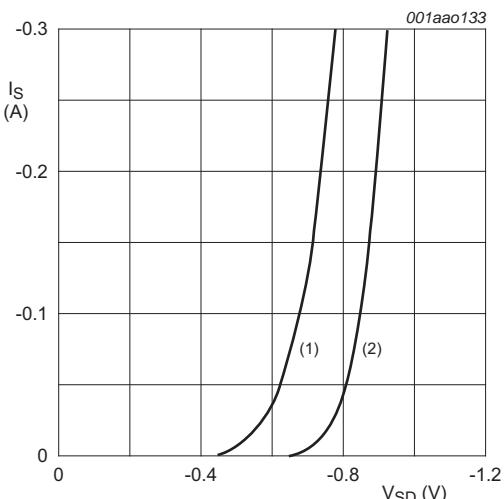


Fig 28. TR2: Source current as a function of source-drain voltage; typical values

## 8. Test information

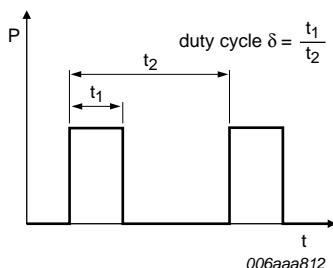


Fig 29. Duty cycle definition

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 9. Package outline

Plastic surface-mounted package; 6 leads

SOT666

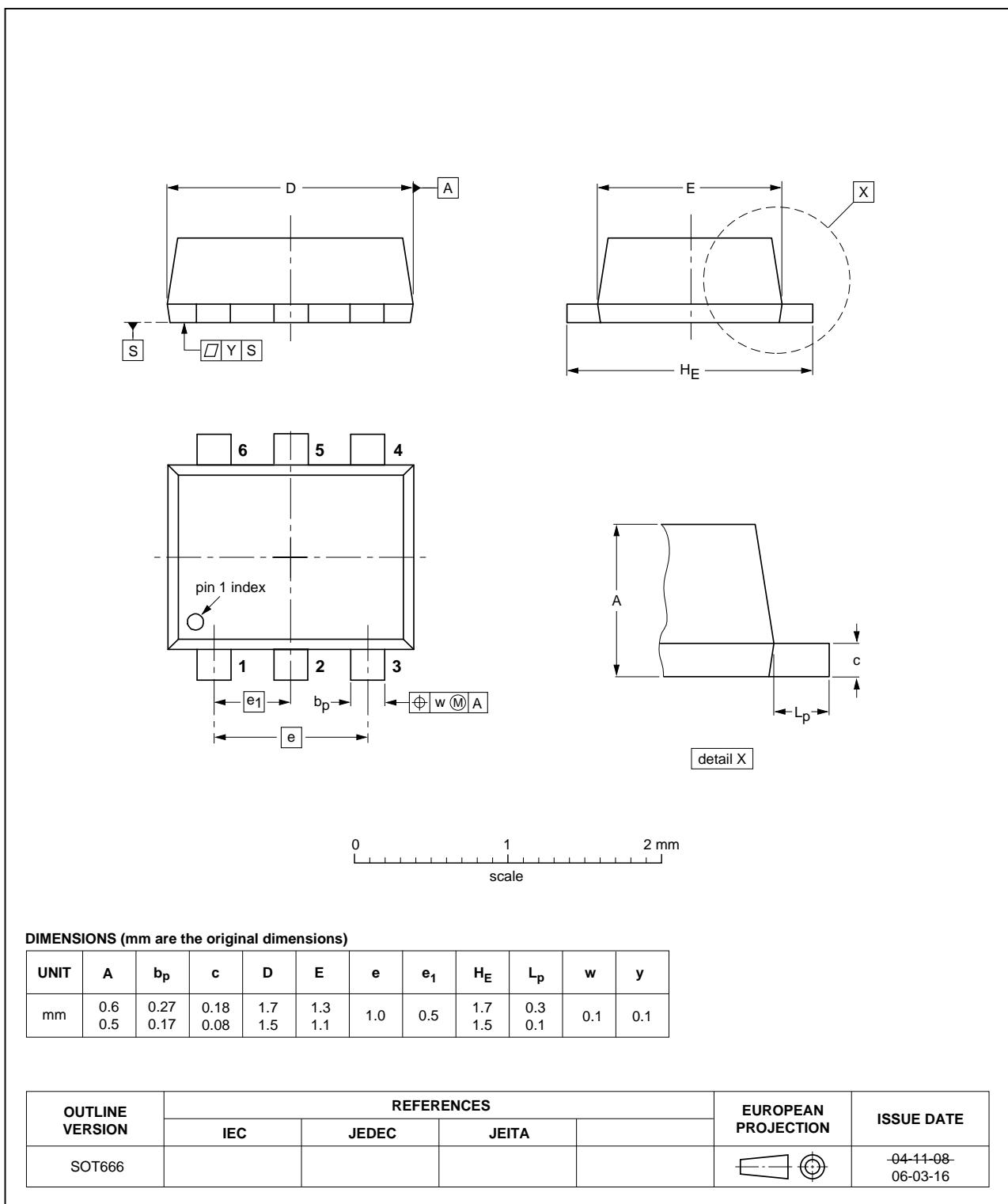


Fig 30. Package outline SOT666 (SOT666)

## 10. Soldering

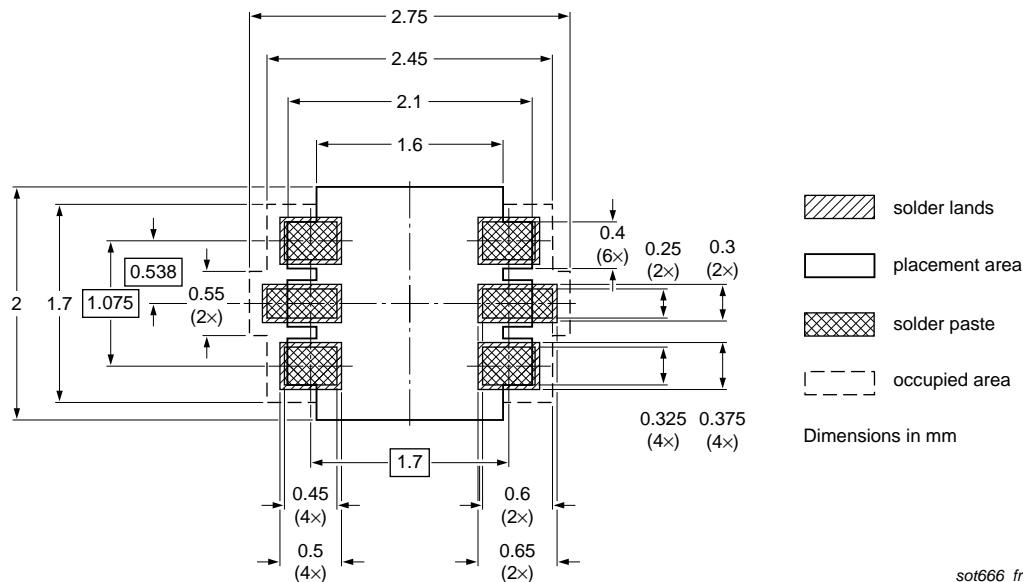


Fig 31. Reflow soldering footprint for SOT666 (SOT666)

## 11. Revision history

**Table 8. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX1029X v.1	20110812	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status [1] [2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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