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**I<sup>2</sup>C-Compatible (2-Wire) Serial EEPROM**  
**64-Kbit (8,192 x 8)**

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**DATASHEET**

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**Features**

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- Low-voltage and Standard-voltage Operation
  - $V_{CC} = 1.7V$  to  $5.5V$
- Internally Organized as 8,192 x 8 (64K)
- I<sup>2</sup>C-compatible (2-Wire) Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 400kHz (1.7V) and 1MHz (2.5V, 2.7V, 5.0V) Compatibility
- Write Protect Pin for Hardware Protection
- 32-byte Page Write Mode
  - Partial Page Writes Allowed
- Self-timed Write Cycle (5ms Max)
- High Reliability
  - Endurance: 1,000,000 Write Cycles
  - Data Retention: 100 Years
- Lead-free/Halogen-free Devices Available
- Green Package Options (Pb/Halide-free/RoHS Compliant)
  - 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, 8-pad XDFN, 8-ball VFBGA, and 4-ball/5-ball/6-ball WLCSP Packages
- Die Sale Options: Wafer Form, Waffle Pack, and Bumped Wafers

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**Description**

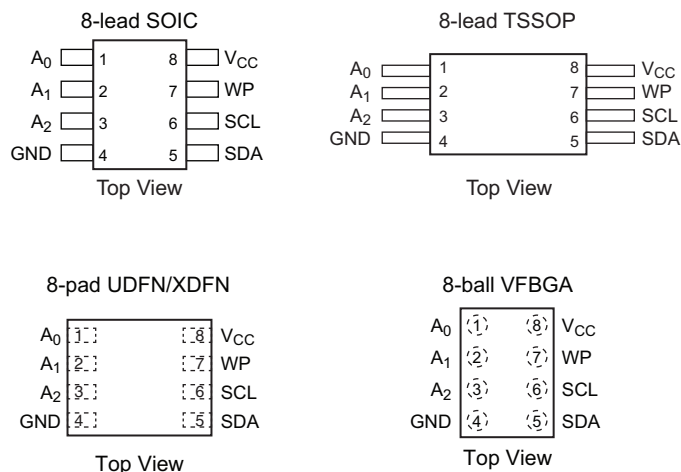
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The Atmel® AT24C64D provides 65,536-bits of Serial Electrically Erasable and Programmable Read-Only Memory (EEPROM) organized as 8,192 words of 8 bits each. The device's cascading feature allows up to eight devices to share a common 2-wire bus. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space-saving 8-lead JEDEC SOIC, 8-lead TSSOP, 8-pad UDFN, 8-pad XDFN, 8-ball VFBGA, and 4-ball/5-ball/6-ball WLCSP packages. In addition, this device operates from 1.7V to 5.5V.

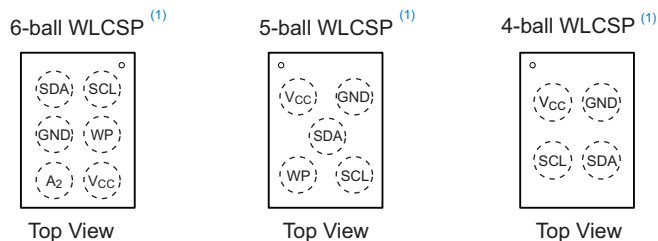
# 1. Pin Configurations and Pinouts

**Table 1-1. Pin Configuration**

Pin	Function
A <sub>0</sub>	Address Input
A <sub>1</sub>	Address Input
A <sub>2</sub>	Address Input
GND	Ground
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
V <sub>CC</sub>	Device Power Supply



Note: 1. For use of the 4-ball, 5-ball, and 6-ball WLCSP packages, please refer to [Section 7. Device Addressing on page 9](#) for details about setting the A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub> hardware address bits.



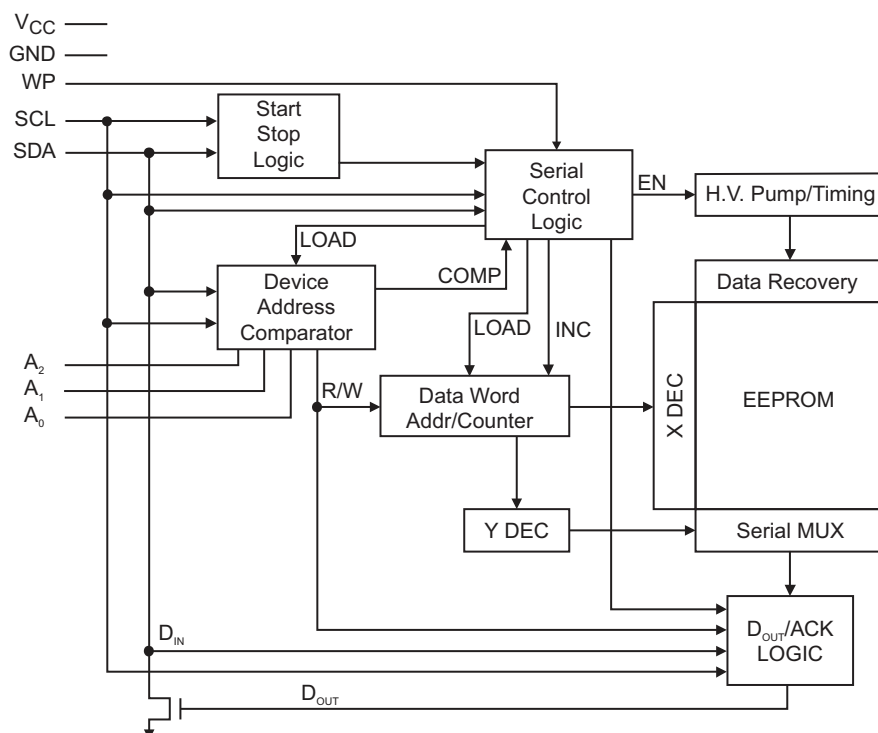
Note: Drawings are not to scale

# 2. Absolute Maximum Ratings\*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any pin with respect to ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

\*Notice: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 3. Block Diagram



### 4. Pin Descriptions

**Serial Clock (SCL):** The SCL input is used to positive-edge clock data into each EEPROM device and negative-edge clock data out of each device.

**Serial Data (SDA):** The SDA pin is bidirectional for serial data transfer. This pin is open drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

**Device Addresses ( $A_2$ ,  $A_1$ ,  $A_0$ ):** The  $A_2$ ,  $A_1$ , and  $A_0$  pins are device address inputs that are hard wired (directly to GND or to  $V_{CC}$ ) for compatibility with other Atmel AT24C devices. When the pins are hard wired, as many as eight 64K devices may be addressed on a single bus system. (Device addressing is discussed in detail in [Section 7.](#), “Device Addressing” on page 9). A device is selected when a corresponding hardware and software match is true. If these pins are left floating, the  $A_2$ ,  $A_1$ , and  $A_0$  pins will be internally pulled down to GND. However, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the address pins to a known state. When using a pull-up resistor, Atmel recommends using 10k $\Omega$  or less.

**Write Protect (WP):** The Write Protect input, when connected to GND, allows normal Write operations. When WP is connected directly to  $V_{CC}$ , all Write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND; however, due to capacitive coupling that may appear during customer applications, Atmel recommends always connecting the WP pins to a known state. When using a pull-up resistor, Atmel recommends using 10k $\Omega$  or less.

**Table 4-1. Write Protect**

WP Pin Status	Part of the Array Protected
At $V_{CC}$	Full Array
At GND	Normal Read/Write Operations

## 5. Memory Organization

**AT24C64D, 64K Serial EEPROM:** The 64K is internally organized as 256 pages of 32-bytes each. Random word addressing requires a 13-bit data word address.

### 5.1 Pin Capacitance

**Table 5-1. Pin Capacitance<sup>(1)</sup>**

Applicable over recommended operating range from:  $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ ,  $V_{CC} = 5.5\text{V}$ .

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance (SDA)	8	pF	$V_{I/O} = 0\text{V}$
$C_{IN}$	Input Capacitance ( $A_0$ , $A_1$ , $A_2$ , and SCL)	6	pF	$V_{IN} = 0\text{V}$

Note: 1. This parameter is characterized and is not 100% tested.

### 5.2 DC Characteristics

**Table 5-2. DC Characteristics**

Applicable over recommended operating range from:  $T_{AI} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 1.7\text{V}$  to  $5.5\text{V}$  (unless otherwise noted).

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V <sub>CC1</sub>	Supply Voltage			1.7		5.5	V
I <sub>CC1</sub>	Supply Current	V <sub>CC</sub> = 5.0V	Read at 400kHz		0.4	1.0	mA
I <sub>CC2</sub>	Supply Current	V <sub>CC</sub> = 5.0V	Write at 400kHz		2.0	3.0	mA
I <sub>SB1</sub>	Standby Current	V <sub>CC</sub> = 1.7V	V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub>			1.0	μA
		V <sub>CC</sub> = 5.0V				6.0	μA
I <sub>LI</sub>	Input Leakage Current V <sub>CC</sub> = 5.0V	V <sub>IN</sub> = V <sub>CC</sub> or V <sub>SS</sub>			0.10	3.0	μA
I <sub>LO</sub>	Output Leakage Current V <sub>CC</sub> = 5.0V	V <sub>OUT</sub> = V <sub>CC</sub> or V <sub>SS</sub>			0.05	3.0	μA
V <sub>IL</sub>	Input Low Level <sup>(1)</sup>			-0.6		V <sub>CC</sub> x 0.3	V
V <sub>IH</sub>	Input High Level <sup>(1)</sup>			V <sub>CC</sub> x 0.7		V <sub>CC</sub> + 0.5	V
V <sub>OL1</sub>	Output Low Level	V <sub>CC</sub> = 1.7V	I <sub>OL</sub> = 0.15mA			0.2	V
V <sub>OL2</sub>	Output Low Level	V <sub>CC</sub> = 3.0V	I <sub>OL</sub> = 2.1mA			0.4	V

Note: 1.  $V_{IL}$  min and  $V_{IH}$  max are reference only and are not tested.

## 5.3 AC Characteristics

**Table 5-3. AC Characteristics (Industrial Temperature)**

Applicable over recommended operating range from:  $T_{AI} = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 1.7\text{V}$  to  $5.5\text{V}$ ,  $CL = 100\text{pF}$  (unless otherwise noted). Test conditions are listed in [Note 2](#).

Symbol	Parameter	1.7V		2.5V, 5.0V		Units
		Min	Max	Min	Max	
$f_{SCL}$	Clock Frequency, SCL		400		1000	kHz
$t_{LOW}$	Clock Pulse Width Low	1300		400		ns
$t_{HIGH}$	Clock Pulse Width High	600		400		ns
$t_I$	Noise Suppression Time <sup>(1)</sup>		100		50	ns
$t_{AA}$	Clock Low to Data Out Valid	50	900	50	550	ns
$t_{BUF}$	Time the bus must be free before a new transmission can start <sup>(1)</sup>	1300		500		ns
$t_{HD.STA}$	Start Hold Time	600		250		ns
$t_{SU.STA}$	Start Set-up Time	600		250		ns
$t_{HD.DAT}$	Data In Hold Time	0		0		ns
$t_{SU.DAT}$	Data In Set-up Time	100		100		ns
$t_R$	Inputs Rise Time <sup>(1)</sup>		300		300	ns
$t_F$	Inputs Fall Time <sup>(1)</sup>		300		100	ns
$t_{SU.STO}$	Stop Set-up Time	600		250		ns
$t_{DH}$	Data Out Hold Time	50		50		ns
$t_{WR}$	Write Cycle Time		5		5	ms
Endurance <sup>(1)</sup>	25°C, Page Mode, 3.3V	1,000,000				Write Cycles

Notes: 1. This parameter is ensured by characterization and is not 100% tested.

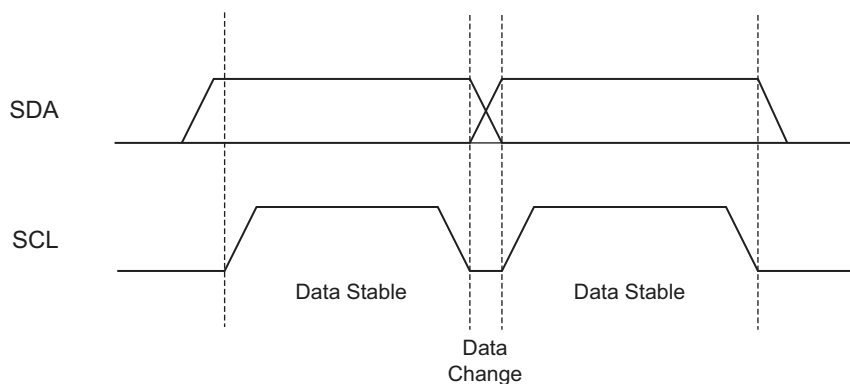
2. AC measurement conditions:

- $R_L$  (connects to  $V_{CC}$ ): 1.3k $\Omega$  (2.5V, 5.5V), 10k $\Omega$  (1.7V)
- Input pulse voltages: 0.3 $V_{CC}$  to 0.7 $V_{CC}$
- Input rise and fall times:  $\leq 50\text{ns}$
- Input and output timing reference voltages: 0.5 x  $V_{CC}$

## 6. Device Operation

**Clock and Data Transitions:** The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

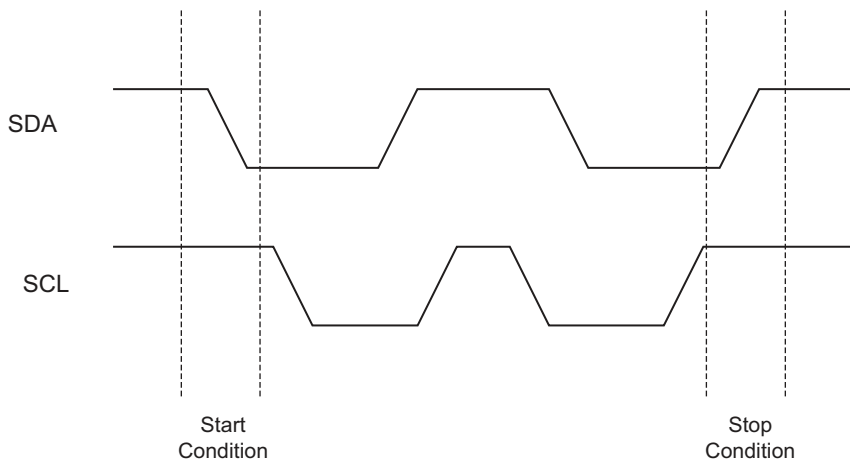
**Figure 6-1. Data Validity**



**Start Condition:** A high-to-low transition of SDA with SCL high is a Start condition that must precede every command.

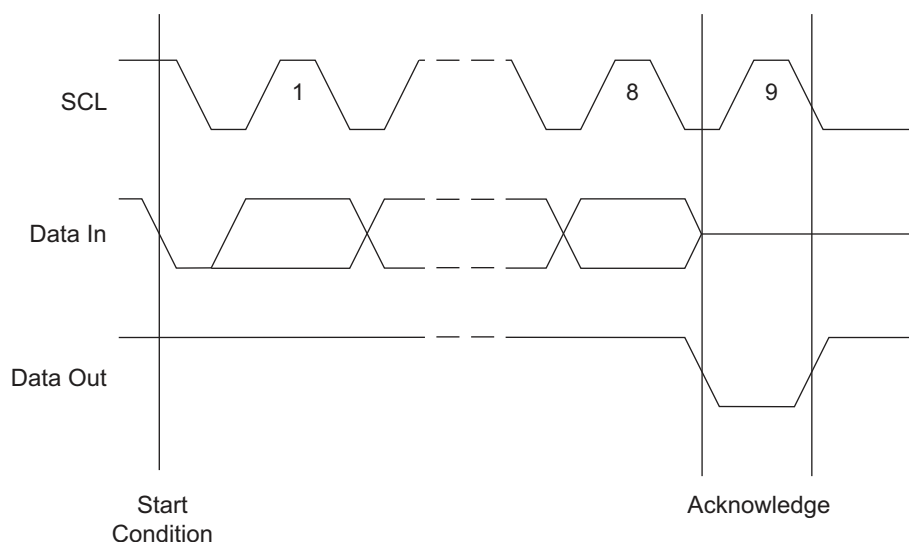
**Stop Condition:** A low-to-high transition of SDA with SCL high is a Stop condition. After a Read sequence, the Stop Condition will place the EEPROM in a standby power mode.

**Figure 6-2. Start and Stop Definition**



**Acknowledge:** All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The receiving device sends a zero during the ninth clock cycle to acknowledge that it has received each word. This zero response is referred to as an Acknowledge.

**Figure 6-3. Output Acknowledge**



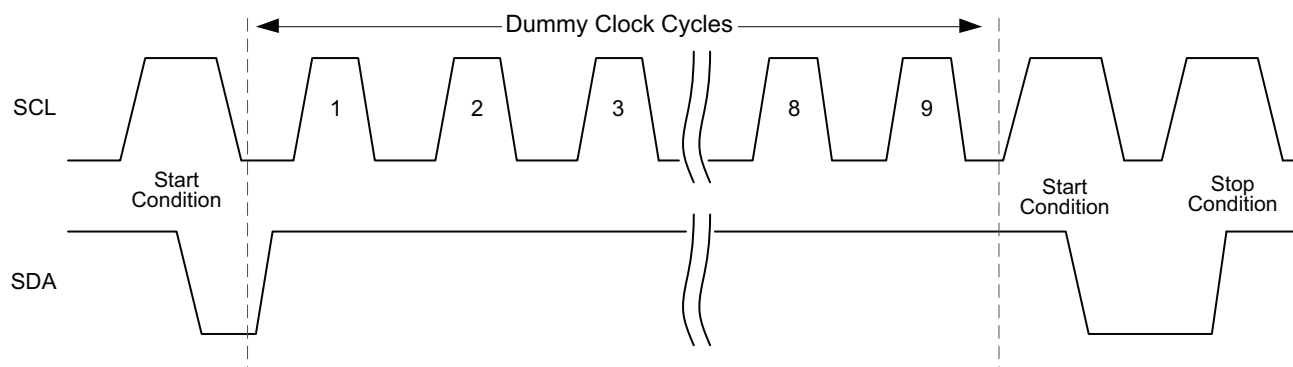
**Standby Mode:** The AT24C64D features a low-power standby mode that is enabled upon power-up and after the receipt of the Stop condition and the completion of any internal operations.

**Software Reset:** After an interruption in protocol, power loss or system reset, any 2-wire part can be protocol reset by following these steps:

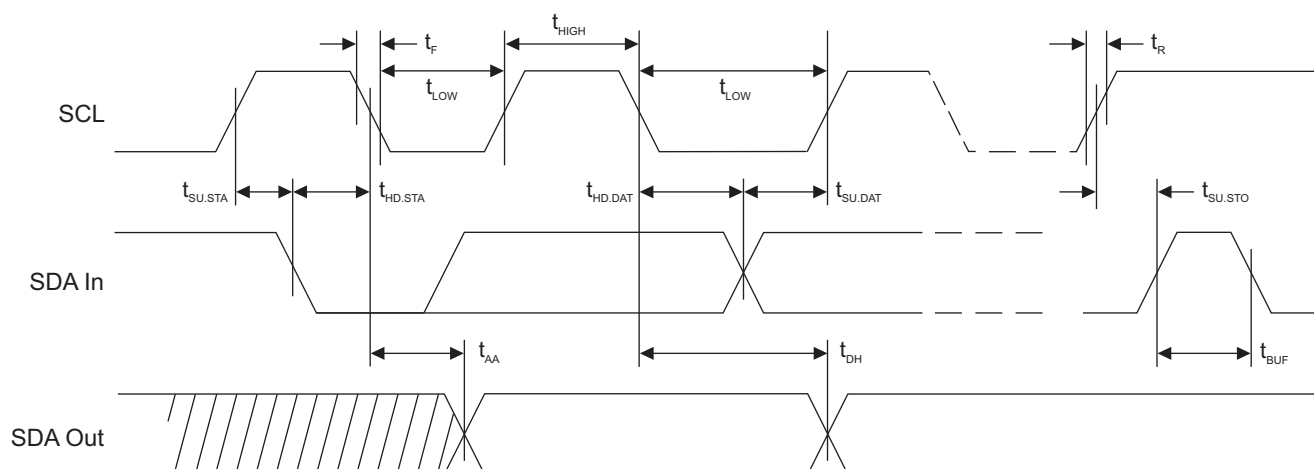
1. Create a Start condition (if possible).
2. Clock nine cycles.
3. Create another Start followed by Stop condition as shown below.

The device should be ready for the next communication after the above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

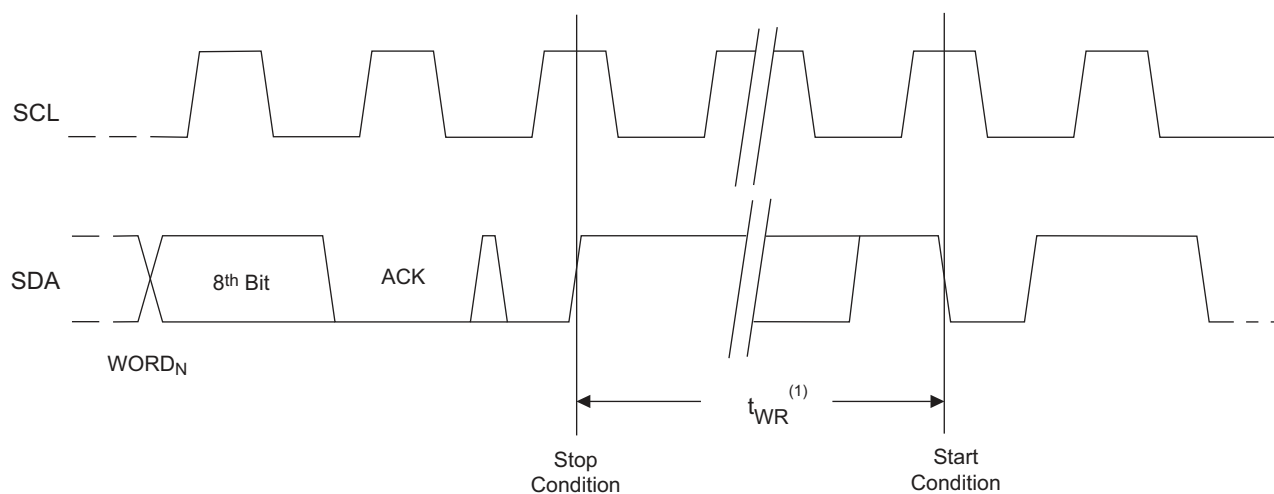
**Figure 6-4. Software Reset**



**Figure 6-5. Bus Timing**



**Figure 6-6. Write Cycle Timing**



Note: 1. The write cycle time  $t_{WR}$  is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.



## 7. Device Addressing

The 64K EEPROM requires an 8-bit device address word following a start condition to enable the chip for a read or write operation. The device address word consists of a mandatory '1010' sequence for the first four most significant bits (bit 7, bit 6, bit 5, and bit 4 as seen in Figure 7-1). This is common to all 2-wire Serial EEPROM devices.

The next three bits are the A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub> device address bits to allow as many as eight devices on the same bus. These bits must compare to their corresponding hard wired input pins, where applicable. The A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub> pins use an internal proprietary circuit that pulls them to GND if the pins are allowed to float.

When utilizing the 6-ball WLCSP package, the A<sub>1</sub> and A<sub>0</sub> pins are not available and are internally pulled to ground; therefore, the A<sub>1</sub> and A<sub>0</sub> device address bits must always be set to a Logic 0 condition to communicate with the device. This condition is depicted in Figure 7-1 below.

When utilizing the 5-ball WLCSP package, the A<sub>2</sub>, A<sub>1</sub> and A<sub>0</sub> pins are not available. The A<sub>2</sub> and A<sub>1</sub> pins are internally pulled to ground and thus the A<sub>2</sub> and A<sub>1</sub> device address bits must always be set to a Logic 0 condition to communicate with the device. The A<sub>0</sub> pin is internally connected to V<sub>CC</sub> in this specific package only; therefore, the A<sub>0</sub> software bit must be set to Logic 1 to communicate to the device. This condition is depicted in Figure 7-1 below.

When utilizing the 4-ball WLCSP package, the A<sub>2</sub>, A<sub>1</sub>, and A<sub>0</sub> pins are not available and are internally pulled to ground; therefore, the A<sub>2</sub>, A<sub>1</sub> and A<sub>0</sub> device address bits must always be set to a Logic 0 condition to communicate with the device. This condition is depicted in Figure 7-1 below.

The eighth bit of the device address is the Read/Write operation select bit. A read operation is initiated if this bit is high, and a Write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a compare is not made, the device will return to a standby state.

**Figure 7-1. Device Addressing**

Package	Device Type Identifier				Hardware Address Bits			R/W Select
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SOIC, TSSOP, UDFN, XDFN, and VFBGA	1	0	1	0	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	R/ $\overline{W}$
6-ball WLCSP	1	0	1	0	A <sub>2</sub>	0	0	R/ $\overline{W}$
5-ball WLCSP	1	0	1	0	0	0	1	R/ $\overline{W}$
4-ball WLCSP	1	0	1	0	0	0	0	R/ $\overline{W}$

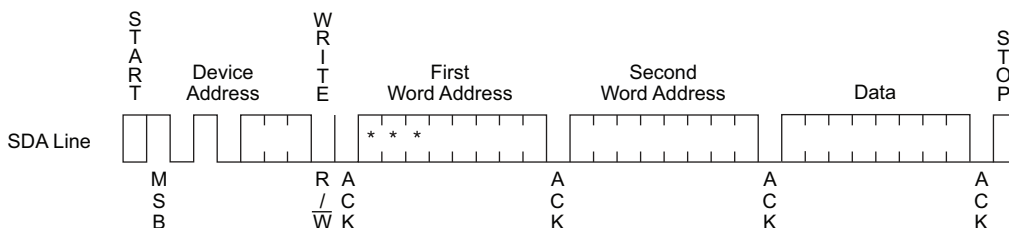
MSBLSB

**Data Security:** AT24C64D has a hardware data protection scheme that allows the user to write protect the whole memory when the WP pin is at V<sub>CC</sub>. The 4-ball WLCSP does not include a WP pin, and therefore no write protection is possible in this package only.

## 8. Write Operations

**Byte Write:** A Write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero, and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, must then terminate the Write sequence with a Stop condition. At this time, the EEPROM enters an internally-timed Write cycle,  $t_{WR}$ , to the nonvolatile memory (See Figure 6-6). All inputs are disabled during this Write cycle and the EEPROM will not respond until the Write is complete.

**Figure 8-1. Byte Write**

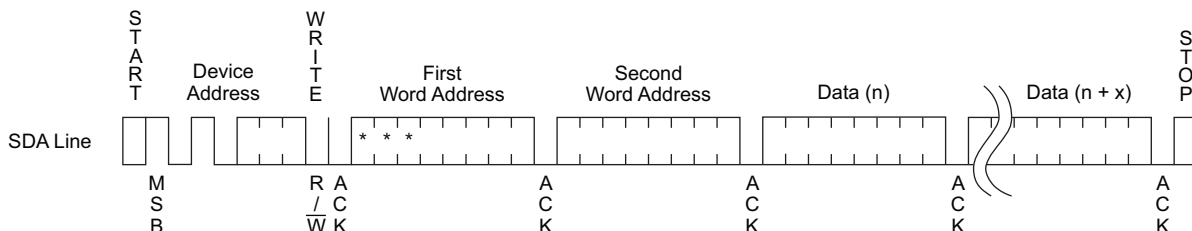


Note: \* = Don't care bit.

**Page Write:** The 64K EEPROM is capable of 32-byte Page Writes.

A Page Write is initiated the same way as a Byte Write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the Page Write sequence with a Stop condition.

**Figure 8-2. Page Write**



Note: \* = Don't care bit.

The data word address lower five bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 32 data words are transmitted to the EEPROM, the data word address will roll-over and the previously loaded data will be altered. The address roll-over during Write is from the last byte of the current page to the first byte of the same page.

**Acknowledge Polling:** Once the internally-timed Write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a Start condition followed by the device address word. The Read/Write bit is representative of the operation desired. Only if the internal Write cycle has completed will the EEPROM respond with a zero, allowing the Read or Write sequence to continue.

## 9. Read Operations

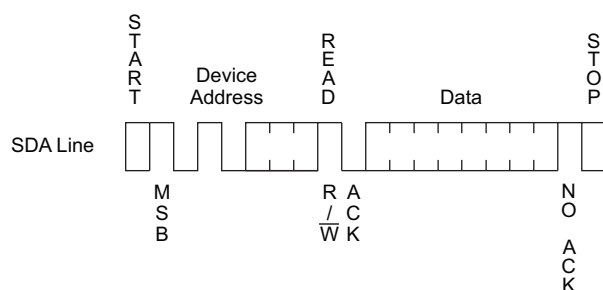
Read operations are initiated the same way as Write operations with the exception that the Read/Write select bit in the device address word is set to one. There are three Read operations:

- Current Address Read
- Random Address Read
- Sequential Read

**Current Address Read:** The internal data word address counter maintains the last address accessed during the last Read or Write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page, to the first byte of the first page.

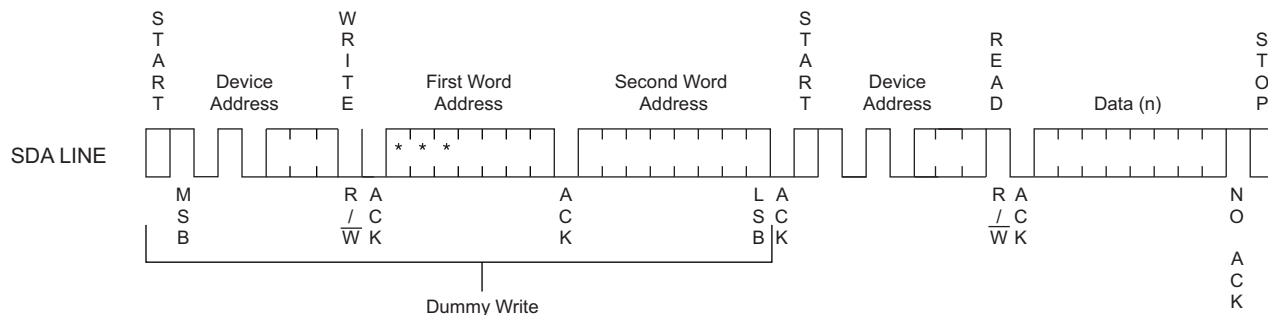
Once the device address with the Read/Write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input zero but does generate a Stop condition.

**Figure 9-1. Current Address Read**



**Random Read:** A Random Read requires a dummy Byte Write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a Current Address Read by sending a device address with the Read/Write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero but does generate a Stop condition.

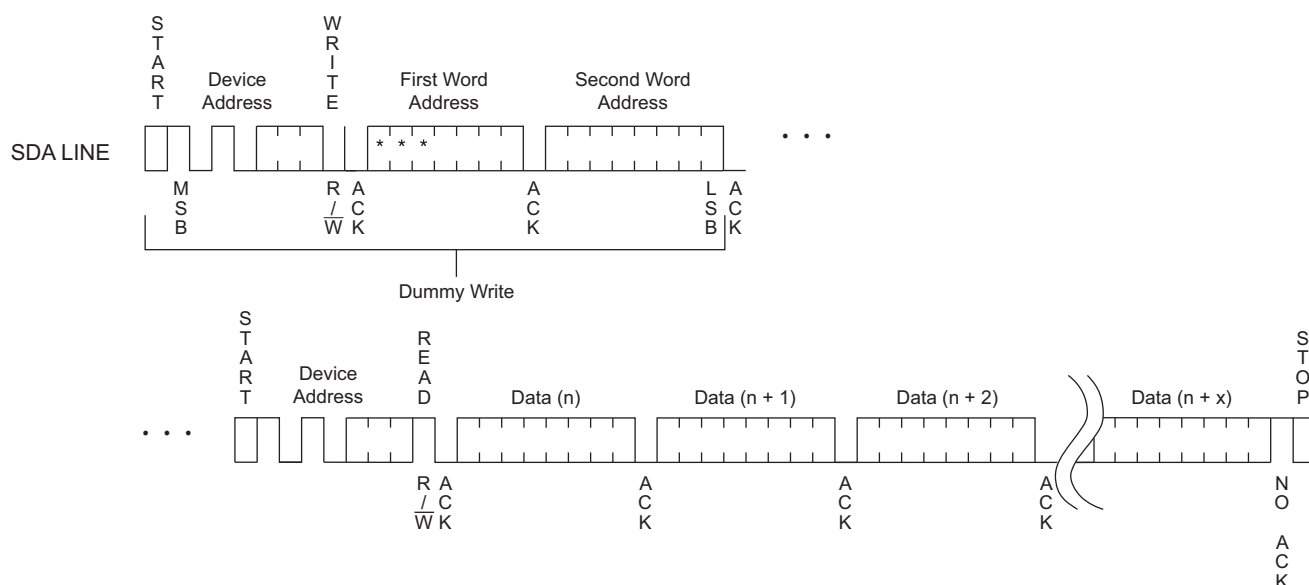
**Figure 9-2. Random Read**



Note: \* = Don't care bit.

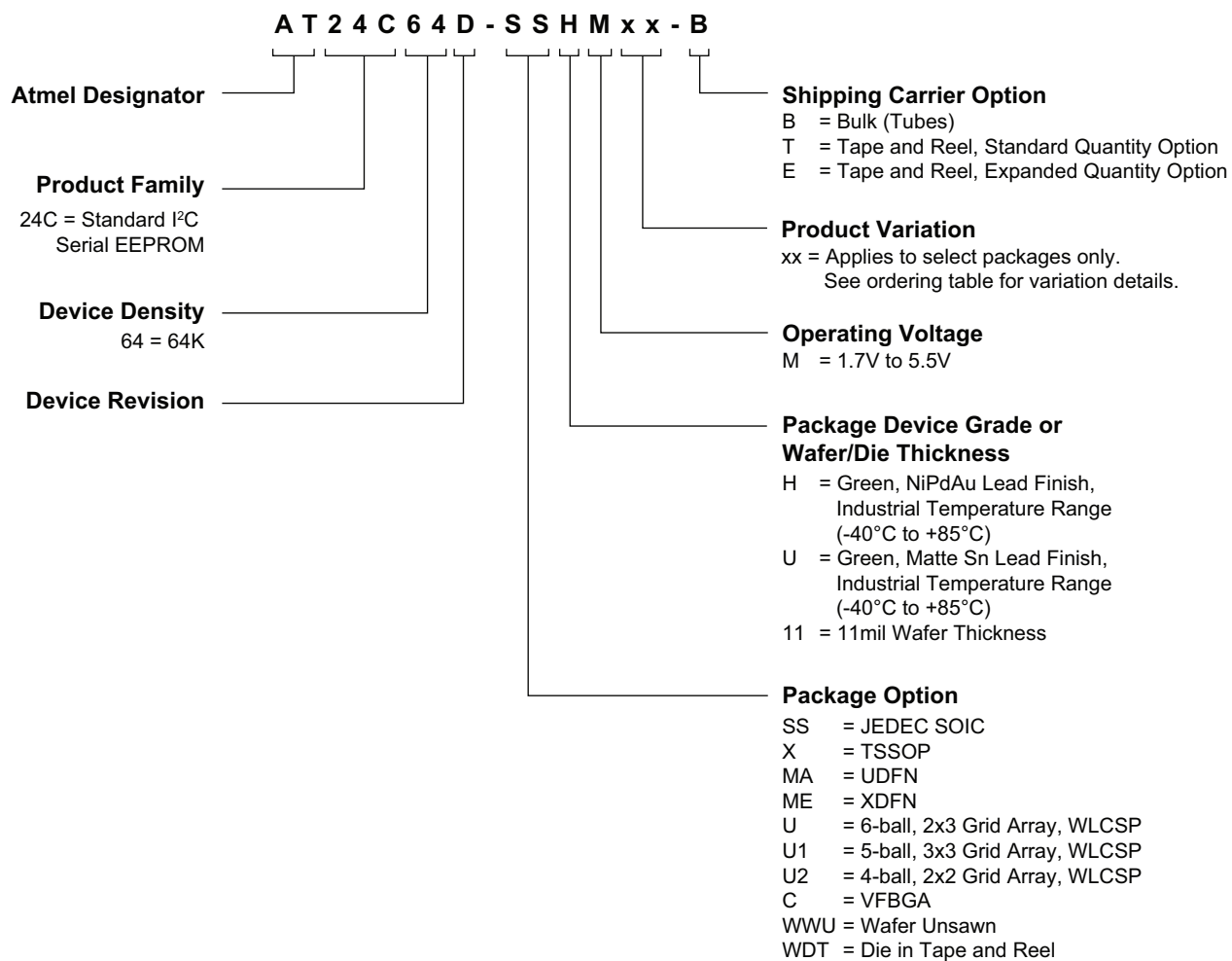
**Sequential Read:** Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address maximum address is reached, the data word address will roll-over and the Sequential Read will continue from the beginning of the array. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a Stop condition.

**Figure 9-3. Sequential Read**



Note: \* = Don't care bit.

## 10. Ordering Code Detail



## 11. Part Markings

### AT24C64D: Package Marking Information

8-lead SOIC	8-lead TSSOP	8-pad XDFN
8-pad UDFN	4, 5, and 6-ball WLCSP	8-ball VFBGA

Note 1: ● designates pin 1

Note 2: Package drawings are not to scale

Catalog Number Truncation				
AT24C64D		Truncation Code ###: 64D		
Date Codes				Voltages
Y = Year		M = Month	WW = Work Week of Assembly	% = Minimum Voltage
5: 2015	9: 2019	A: January	02: Week 2	M: 1.7V min
6: 2016	0: 2020	B: February	04: Week 4	
7: 2017	1: 2021	...	...	
8: 2018	2: 2022	L: December	52: Week 52	
Country of Assembly		Lot Number		Grade/Lead Finish Material
@ = Country of Assembly		AAA...A = Atmel Wafer Lot Number		U: Industrial/Matte Tin/SnAguCu H: Industrial/NiPdAu
Trace Code				Atmel Truncation
XX = Trace Code (Atmel Lot Numbers Correspond to Code) Example: AA, AB.... YZ, ZZ				AT: Atmel ATM: Atmel ATML: Atmel

4/27/2015

Atmel		TITLE	DRAWING NO.	REV.
Package Mark Contact: DL-CSO-Assy_eng@atmel.com		24C64DSM, AT24C64D Package Marking Information	24C64DSM	E

## 12. Ordering Information

Atmel Ordering Code	Lead Finish	Package	Delivery Information		Operating Range
			Form	Quantity	
AT24C64D-SSHM-B	NiPdAu (Lead-free/Halogen-free)	8S1	Bulk (Tubes)	100 per Tube	Industrial Temperature (-40°C to 85°C)
AT24C64D-SSHM-T			Tape and Reel	4,000 per Reel	
AT24C64D-XHM-B		8X	Bulk (Tubes)	100 per Tube	
AT24C64D-XHM-T			Tape and Reel	4,000 per Reel	
AT24C64D-MAHM-T		8MA2	Tape and Reel	5,000 per Reel	
AT24C64D-MAHM-E			Tape and Reel	15,000 per Reel	
AT24C64D-MEHM-T		8ME1	Tape and Reel	5,000 per Reel	
AT24C64D-UUM0B-T <sup>(1)</sup>	SnAgCu (Lead-free/Halogen-free)	6U-2	Tape and Reel	5,000 per Reel	
AT24C64D-U1UM0B-T <sup>(1)</sup>		5U-4	Tape and Reel	5,000 per Reel	
AT24C64D-U2UM0B-T <sup>(1)</sup>		4U-12	Tape and Reel	5,000 per Reel	
AT24C64D-CUM-T		8U2-1	Tape and Reel	5,000 per Reel	
AT24C64D-WWU11M <sup>(2)</sup>	N/A	Wafer Sale	Note 2		

Notes: 1. WLCSP Package:

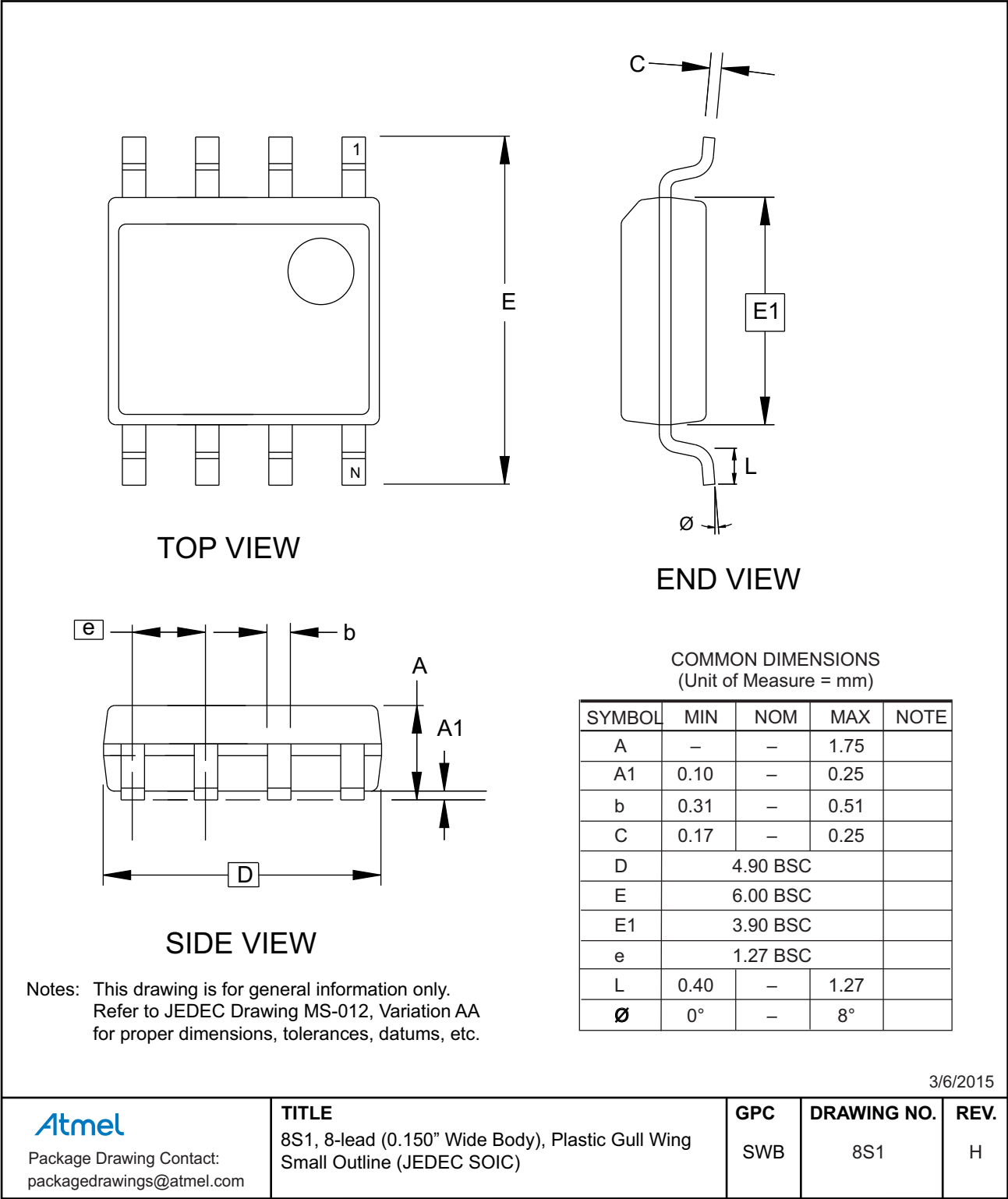
- This device includes a backside coating to increase product robustness.
- **CAUTION:** Exposure to ultraviolet (UV) light can degrade the data stored in the EEPROM cells. Therefore, customers who use a WLCSP product must ensure that exposure to ultraviolet light does **not** occur.

2. Contact Atmel Sales for Wafer sales.

Package Type	
8S1	8-lead, 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
8X	8-lead, 4.40mm body, Plastic Thin Shrink Small Outline Package (TSSOP)
8MA2	8-pad, 2.00mm x 3.00mm body, 0.50mm pitch, Dual No Lead (UDFN)
8ME1	8-pad, 1.80mm x 2.20mm body, Extra Thin DFN (XDFN)
6U-2	6-ball, 2x3 Grid Array, Wafer Level Chip Scale Package (WLCSP)
5U-4	5-ball, 3x3 Grid Array, Wafer Level Chip Scale Package (WLCSP)
4U-12	4-ball, 2x2 Grid Array, Wafer Level Chip Scale Package (WLCSP)
8U2-1	8-ball, Die Ball Grid Array (VFBGA)

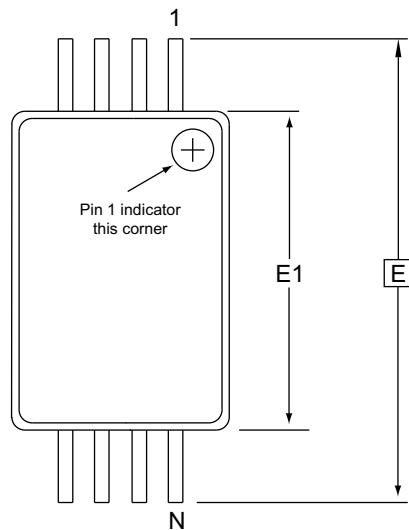
13. Packaging Information

13.1 8S1 — 8-lead JEDEC SOIC

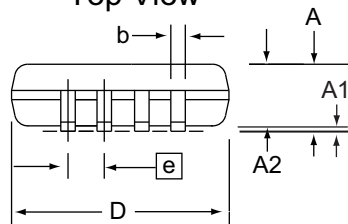




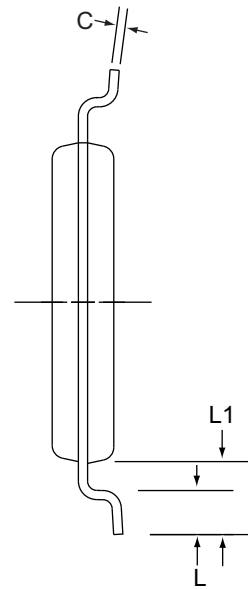
## 13.2 8X — 8-lead TSSOP



Top View



Side View



End View

COMMON DIMENSIONS  
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E	6.40 BSC			
E1	4.30	4.40	4.50	3, 5
b	0.19	0.25	0.30	4
e	0.65 BSC			
L	0.45	0.60	0.75	
L1	1.00 REF			
C	0.09	-	0.20	

- Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
  2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
  3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
  4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
  5. Dimension D and E1 to be determined at Datum Plane H.

2/27/14

**Atmel**

Package Drawing Contact:  
packagedrawings@atmel.com

### TITLE

8X, 8-lead 4.4mm Body, Plastic Thin  
Shrink Small Outline Package (TSSOP)

### GPC

TNR

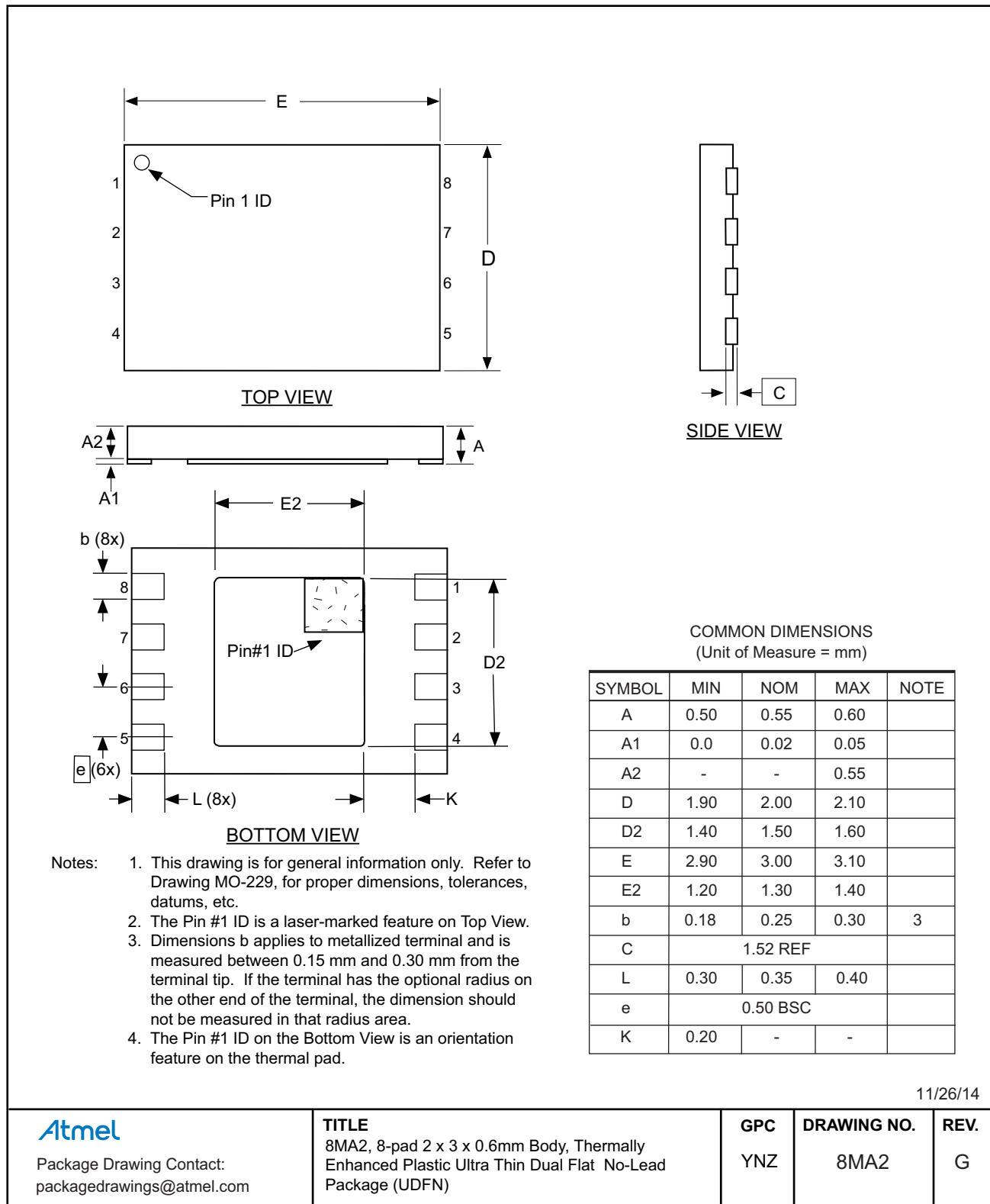
### DRAWING NO.

8X

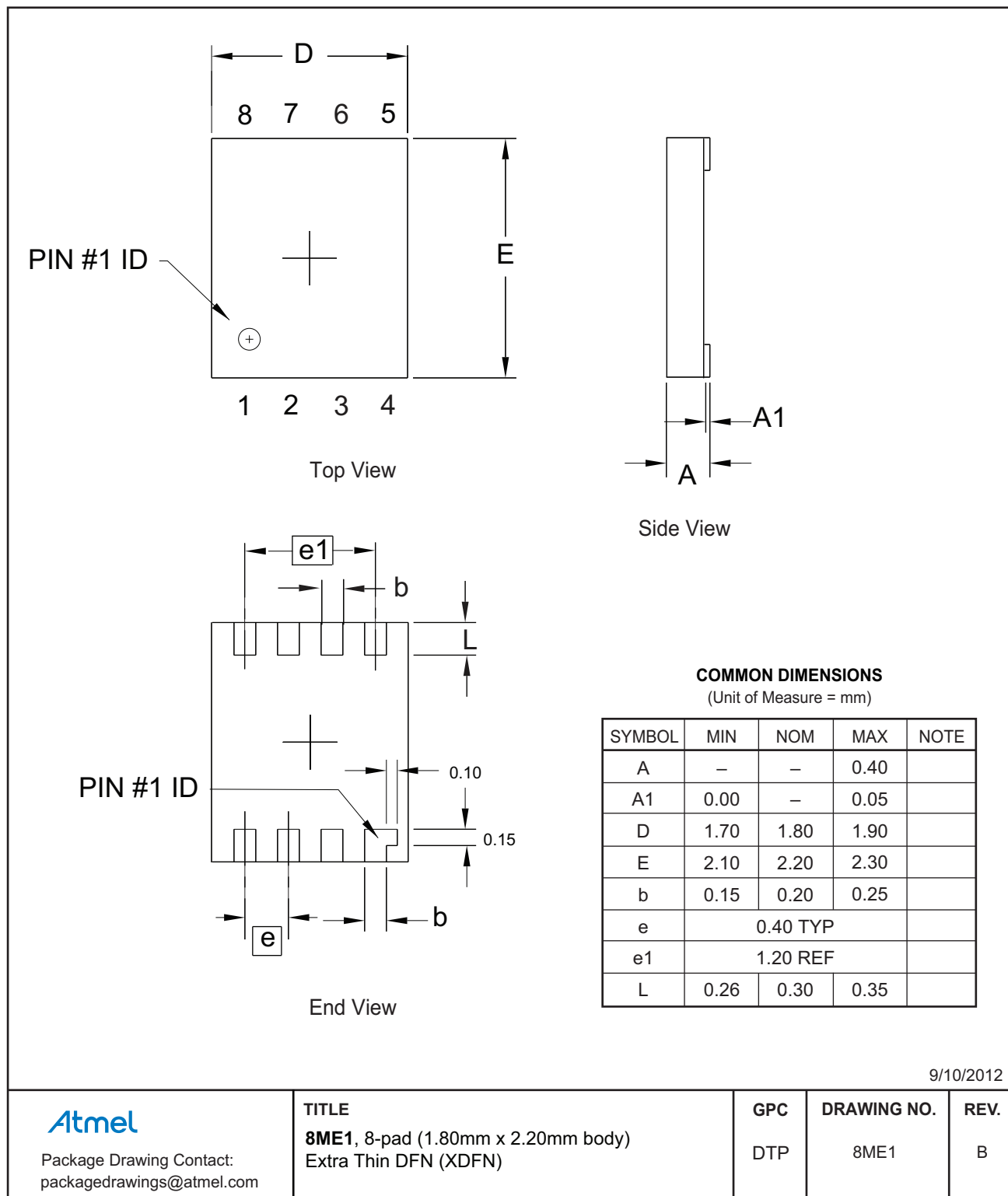
### REV.

E

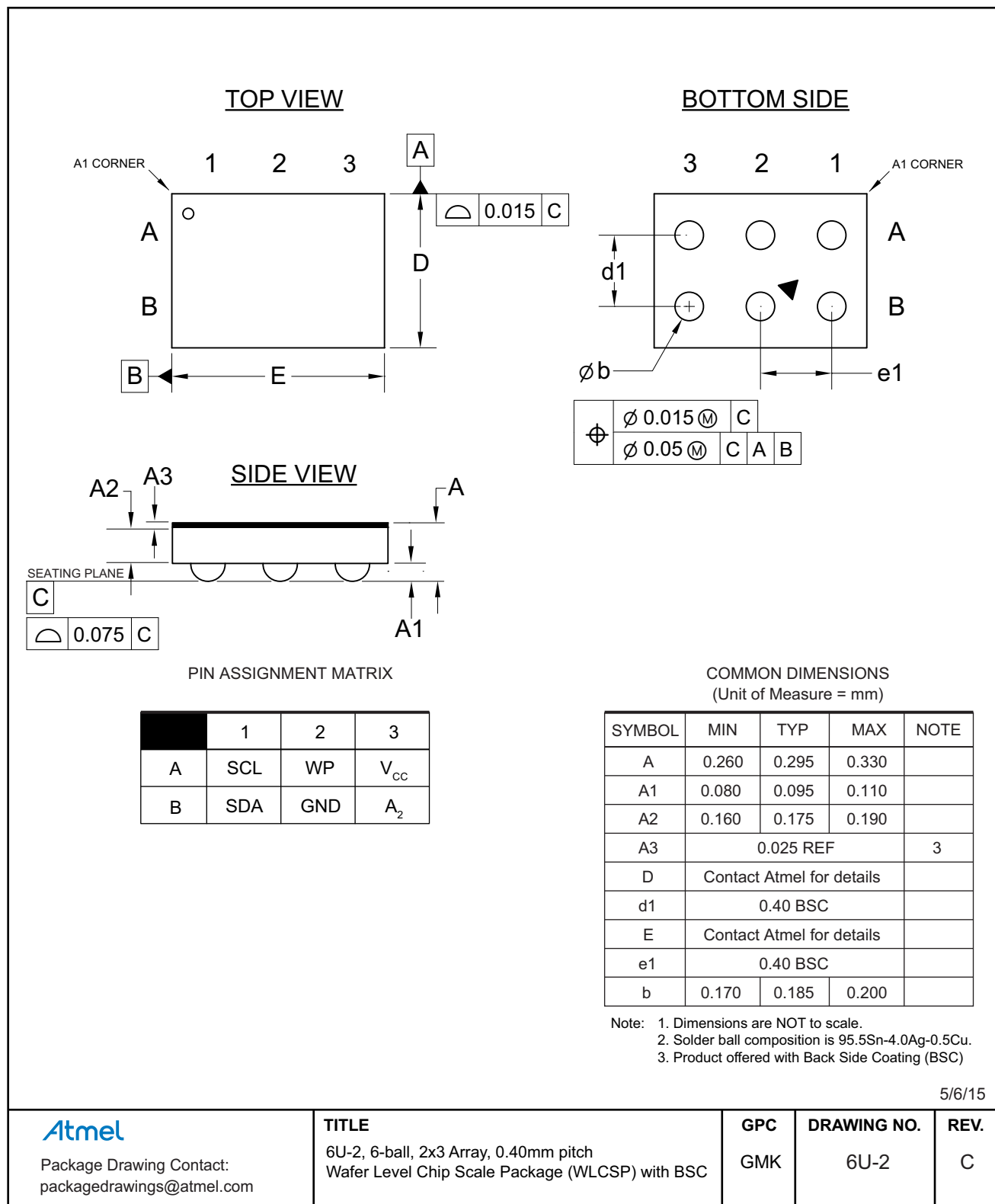
### 13.3 8MA2 — 8-pad UDFN



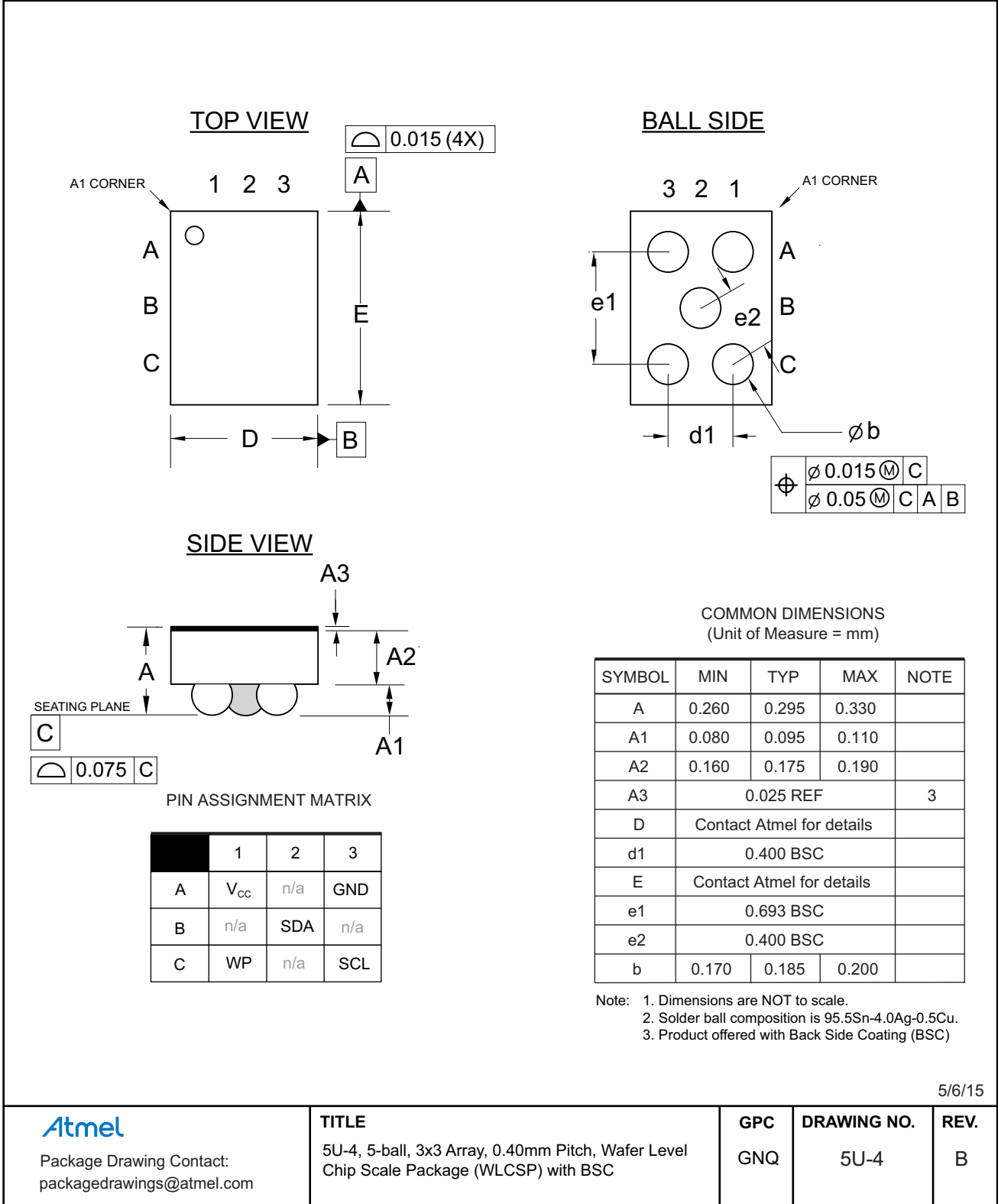
### 13.4 8ME1 — 8-pad XDFN



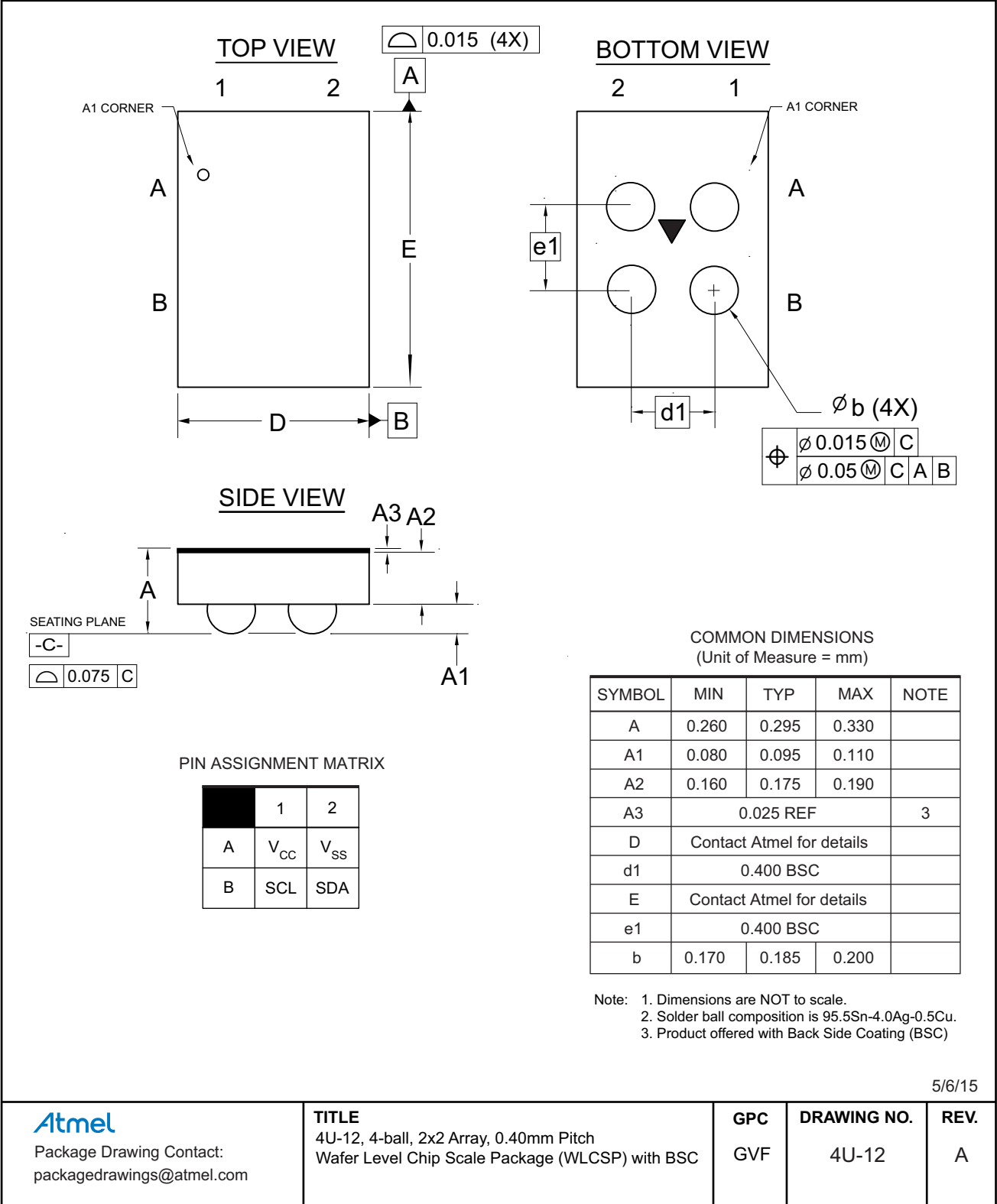
## 13.5 6U-2 — 6-ball WLCSP



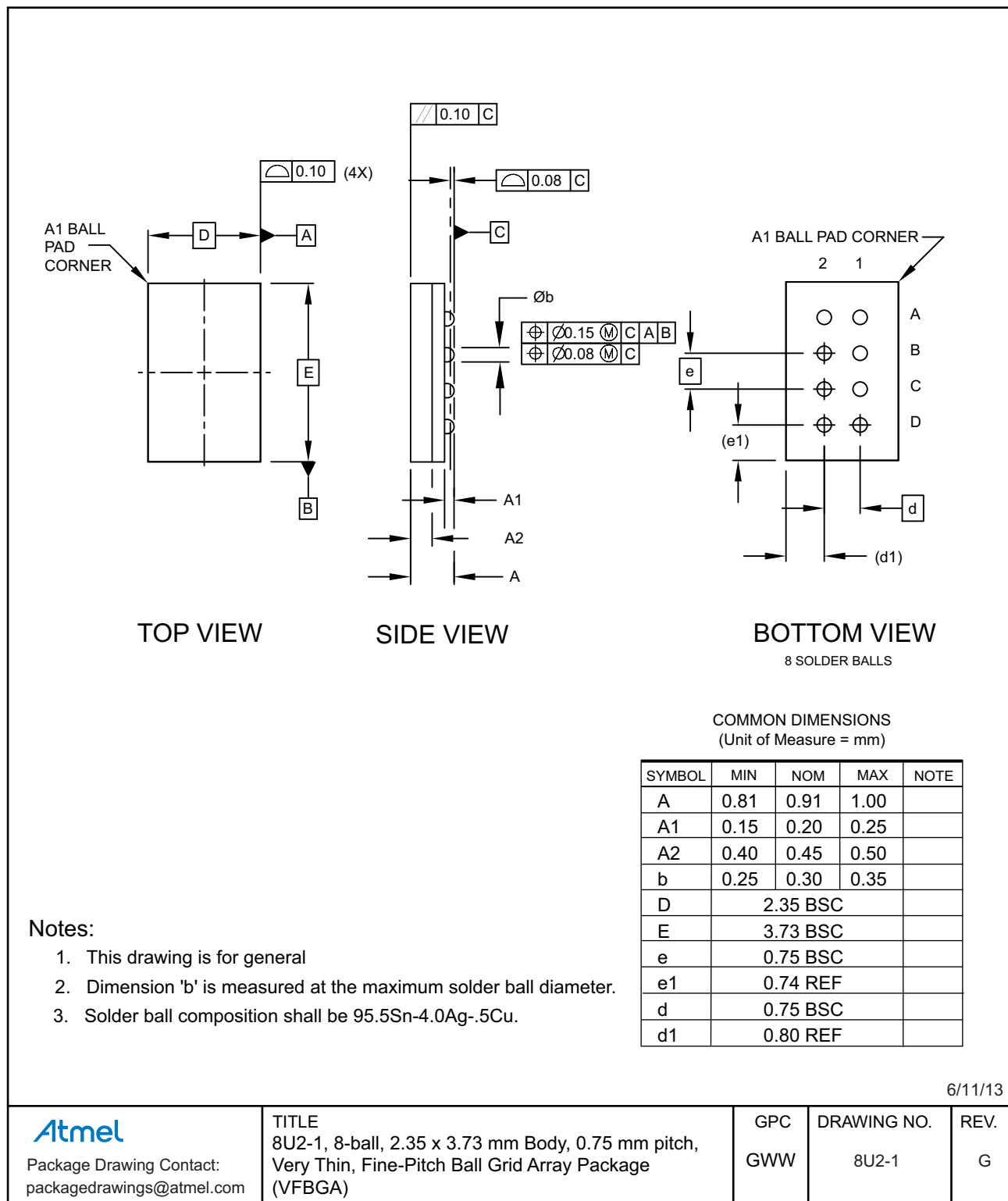
13.6 5U-4 — 5-ball WLCSP



13.7 4U-12 — 4-ball WLCSP



## 13.8 8U2-1 — 8-ball VFBGA



## 14. Revision History

Doc. Rev.	Date	Comments
8850D	05/2015	Added the 4-ball WLCSP, AT24C64D-U2UM0B-T option. Updated the 8S1 package drawing.
8850C	02/2015	Updated the 6-ball and 5-ball WLCSP package outline drawings to reflect offering of product with backside coating.
8850B	12/2014	Added the AT24C64D-MAHM-E product offering. Updated the 8X, 8MA2, 5U-2, and 8U2-1 package outline drawings and the ordering information.
8850A	08/2013	Initial document release.



