

# LCD Segment Driver series

## 80-segment Drivers

### (20SEG×4COM)


**BU9796FS**

No.09044EAT02

#### ●Description

This is LCD segment driver for 80 segment type display. There is a lineup which is suitable for multi function display and is integrated display RAM and power supply circuit for LCD driving with 4 common output type: BU9796FS.

#### ●Features

- 1) 2wire serial interface
- 2) Integrated RAM for display data (DDRAM) : 20 × 4bit (Max 80 Segment)
- 3) LCD driving port: 4 Common output, 20 Segment output
- 4) Display Duty: 1/4 duty
- 5) Integrated Oscillation circuit
- 6) Integrated Buffer AMP for LCD driving power supply circuit
- 7) Support 1/2bias, 1/3bias select
- 8) No external components
- 9) Low voltage / low power consumption design: 2.5~5.5V

#### ●Applications

Telephone, FAX, Portable equipments (POS, ECR, PDA etc.),  
DSC, DVC, Car audio, Home electrical appliance, Meter equipment etc.

#### ● Absolute Maximum Ratings (Ta=25degree, VSS=0V)

Parameter	Symbol	Limits	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 ~ +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 ~ +7.0	V	LCD drive voltage
Allowable loss	Pd	0.64	W	When use more than Ta=25°C, subtract 6.4mW per degree.
Input voltage range	VIN	-0.5 ~ VDD+0.5	V	
Operational temperature range	Topr	-40 ~ +85	degree	
Storage temperature range	Tstg	-55 ~ +125	degree	

\*This product is not designed against radioactive ray.

#### ● Recommend operating conditions (Ta=25degree, VSS=0V)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	0	-	VDD-2.4	V	LCD drive voltage

\* Please use in the range of  $VDD - VLCD \geq 2.4V$

●Electrical Characteristics

DC Characteristics (VDD=2.5~5.5V, VLCD=0V, VSS=0V, Ta=-40~85degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN	TYP	MAX		
"H" level input voltage	VIH	0.7VDD	-	VDD	V	
"L" level input voltage	VIL	VSS	-	0.3VDD	V	
"H" level input current	IIH	-	-	1	uA	
"L" level input current	IIL	-1	-	-	uA	
LCD Driver on resistance	SEG	RON	-	3	-	Iload=±10uA
	COM	RON	-	3	-	
VLCD supply voltage	VLCD	0	-	VDD-2.4	V	VDD-VLCD≥2.4V
Standby current	IDD1	-	-	5	uA	Display off, Oscillation off
Power consumption	IDD2	-	12.5	30	uA	VDD=3.3V, VLCD=0V, Ta=25degree Power save mode SR = Power save mode1, Power save mode FR = Power save mode1 1/3 bias, Frame inverse
Frame frequency	fCLK	56	80	104	Hz	Power save mode FR = Normal mode

MPU interface Characteristics (VDD=2.5~5.5V, VLCD=0V, VSS=0V, Ta=-40~85degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN.	TYP.	MAX.		
Input rise time	tr	-	-	0.3	us	
Input fall time	tf	-	-	0.3	us	
SCL cycle time	tSCYC	2.5	-	-	us	
"H" SCL pulse width	tSHW	0.6	-	-	us	
"L" SCL pulse width	tSLW	1.3	-	-	us	
SDA setup time	tSDS	100	-	-	ns	
SDA hold time	tSDH	100	-	-	ns	
Buss free time	tBUF	1.3	-	-	us	
START condition hold time	tHD;STA	0.6	-	-	us	
START condition setup time	tSU;STA	0.6	-	-	us	
STOP condition setup time	tSU;STO	0.6	-	-	us	

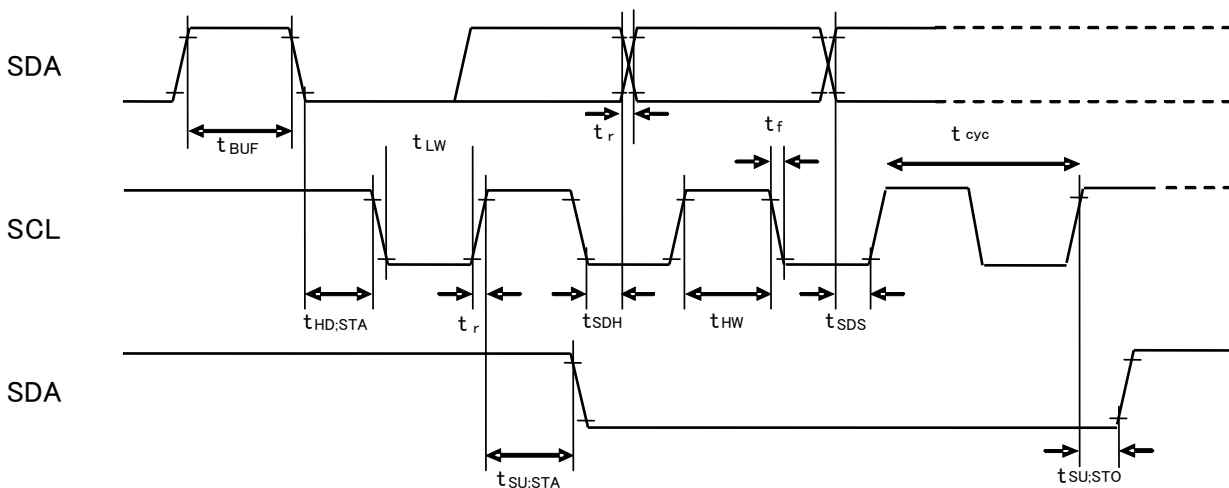


Fig. 1 interface timing

● Block Diagram

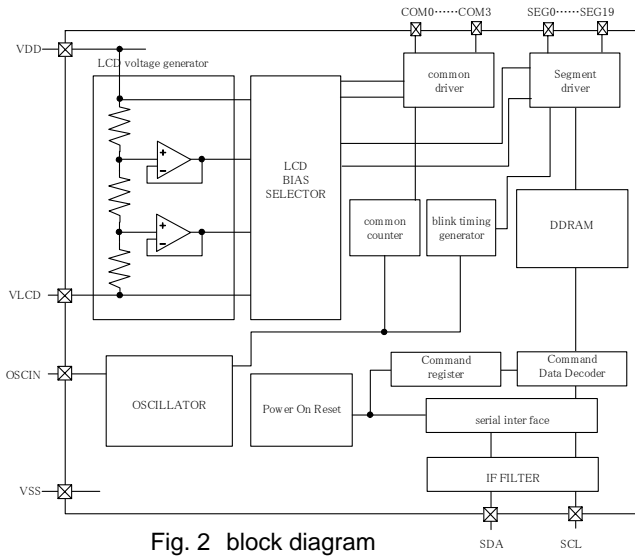


Fig. 2 block diagram

● Pin Arrangement

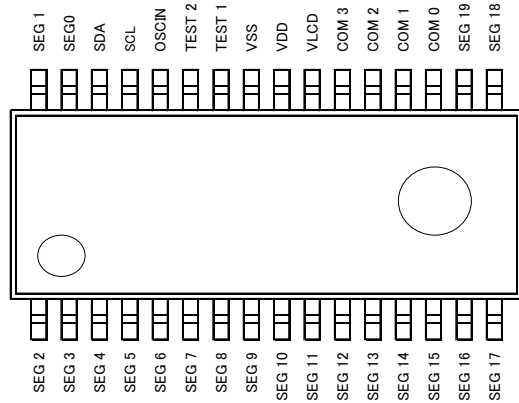


Fig. 3 Pin arrangement

● Terminal description

Terminal	Terminal No.	I/O	Function
TEST1	26	I	Test input (ROHM use only) Must be connect to VSS
TEST2	27	I	Test input (ROHM use only) TEST2="L": POR circuit enable TEST2="H": POR circuit disenable, refer to "Cautions in Power ON/OFF"
OSCIN	28	I	External clock input Ext clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SDA	30	I/O	serial data in-out terminal
SCL	29	I	serial data transfer clock
VSS	25		GND
VDD	24		Power supply
VLCD	23		Power supply for LCD driving
SEG0-19	31,32 1-18	O	SEGMENT output for LCD driving
COM0-3	19-22	O	COMMON output for LCD driving

● Command Description

D7 (MSB) is bit for command or data judgment.  
Refer to Command and data transfer method.

C: 0: Next byte is RAM write data.  
1: Next byte is command.

○ Display control (DISCTL)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Power save mode FR

Setup	P4	P3	Reset initialize condition
Normal mode	0	0	○
Power save mode1	0	1	
Power save mode2	1	0	
Power save mode3	1	1	

Set LCD drive waveform

Setup	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

Set Power save mode SR

Setup	P1	P0	Reset initialize condition
Power save mode1	0	0	
Power save mode2	0	1	
Normal mode	1	0	○
High power mode	1	1	

\* Please keep condition  $VDD-VLCD \geq 3.0V$  in High power mode.

○ Mode Set (MODE SET)

MSB				LSB			
D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

(\*: Don't Care)

Set display ON and OFF

Setup	P3	Reset initialize condition
Display OFF	0	○
Display ON	1	

Set bias level

Setup	P3	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

○ Address set (ADSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

The range of address can be set as 00000 to 10011(2).

○ Set IC Operation (ICSET)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	*	P1	P0

(\*: Don't Care)

Set software reset execution

Setup	P1
No operation	0
Software Reset execute	1

Set oscillator mode

setup	P0	Reset initialize condition
Internal oscillation	0	○
External clock input	1	

○ Blink control (BLKCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

(\*: Don't Care)

Set blink mode

Blink mode (Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

○ All Pixel control (APCTL)

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON, OFF

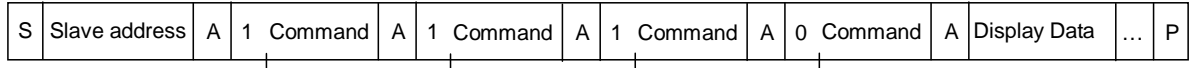
APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

APOFF	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

●Function description

○ Command transfer method

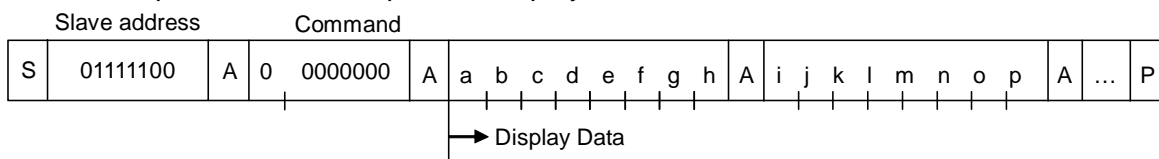
1byte after Slave Address always becomes command input.  
 MSB (“command or data judge bit”) of command decide to next data is command or display data.  
 When set “command or data judge bit”=‘1’, next byte will be command.  
 When set “command or data judge bit”=‘0’, next byte data is display data.



Once it becomes display data transfer condition, it cannot input command.  
 When want to input command again, please generate “START condition” once.

○ Write display and transfer method

This device has Display Data RAM (DDRAM) of 50×4=200bit.  
 The relationship between data input and display data, DDRAM data and address are as follows;



DDRAM address

		00	01	02	03	04	05	06	07	...	2Fh	30h	31h		
BIT	0	a	e	i	m										COM0
	1	b	f	j	n										COM1
	2	c	g	k	o										COM2
	3	d	h	l	p										COM3
		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7			SEG47	SEG48	SEG49	

Data transfer to DDRAM happens every 4bit data. So It will be finished to transfer with no need to wait ACK.

○ Reset initialize condition

Initial condition after execute Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Refer to Command Description about initialize value of register.

●Cautions in Power ON/OFF

This device has “P.O.R” (Power-On Reset) circuit and Software Reset function.  
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended  $t_R$ ,  $t_F$ ,  $t_{OFF}$ , and  $V_{bot}$  spec below in order to ensure P.O.R operation

\* It has to set TEST2="L" to be valid in POR circuit.

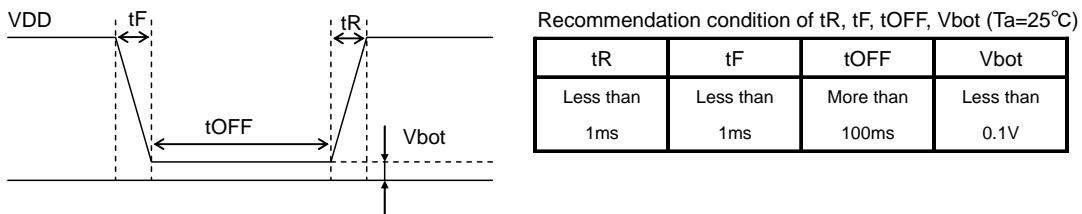


Fig. 4 Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.

\* It has to keep the following sequence in the case of TEST2="H". As POR circuit is invalid status.  
But it is not able to accept Command input in Power off status, it has to take care that software reset is not perfectly alternative method of POR function.

- (1) Generate STOP condition

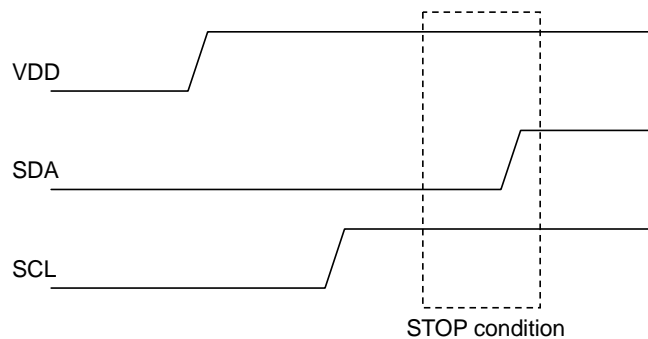


Fig. 5 Stop condition

- (2) Generate START condition.
- (3) Issue slave address
- (4) Execute Software Reset (ICSET) command

●IO Equivalent Circuit

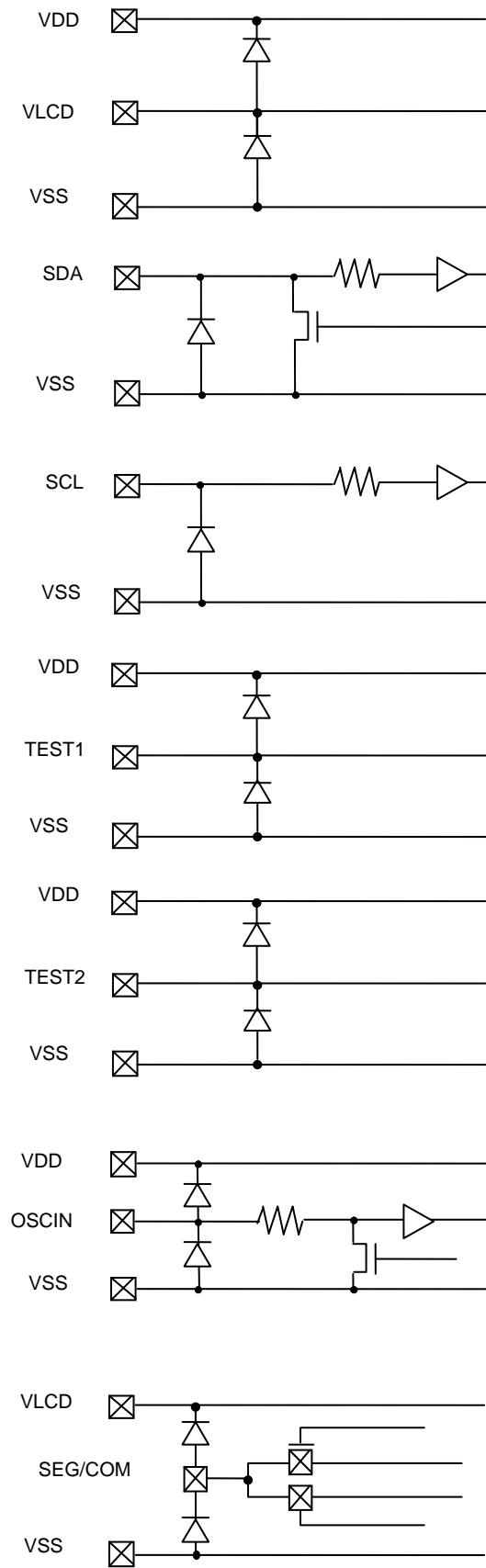


Fig. 6 I/O equivalent circuit



**●Notes for use****(1) Absolute Maximum Ratings**

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

**(2) Operating conditions**

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

**(3) Reverse connection of power supply connector**

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

**(4) Power supply line**

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner. Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

**(5) GND voltage**

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

**(6) Short circuit between terminals and erroneous mounting**

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

**(7) Operation in strong electromagnetic field**

Be noted that using ICs in the strong electromagnetic field can malfunction them.

**(8) Inspection with set PCB**

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

**(9) Input terminals**

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

**(10) Ground wiring pattern**

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

**(11) External capacitor**

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals

In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current

When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

●Ordering part number

B	D
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Part No.

9	7	9	6
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Part No.

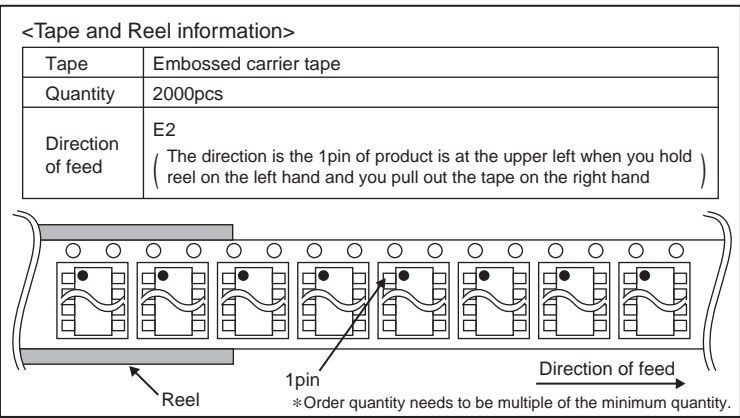
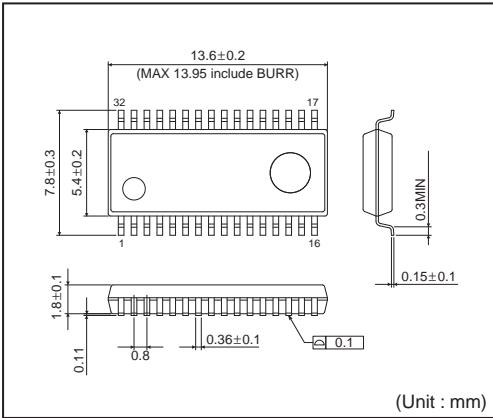
F	S
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Package  
FS: SSOP-A32

E	2
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Packaging and forming specification  
E2: Embossed tape and reel

SSOP-A32



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