Document Number S32R372
Rev. 4, 08/2018

# S32R372

# S32R372 Data Sheet

## Features

- Dual issue computation cores: Power Architecture® e200z7 32-bit CPU
- 1.3 MB on-chip code flash memory (FMC flash memory) with ECC
- 1 MB on-chip SRAM with ECC
- RADAR processing
  - Signal Processing Toolbox (SPT) for RADAR signal processing acceleration
  - Cross Triggering Engine (CTE) for precise timing generation and triggering
  - MIPICSI2 interface to connect external RADAR RX ADCs
- Memory protection
  - Each core memory protection unit provides 24 entries
  - Data and instruction bus system memory protection unit (SMPU) with 16 region descriptors each
  - Register protection
- Clock generation
  - 40 MHz external crystal (XOSC)
  - 16 MHz Internal oscillator (IRCOSC)
  - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
  - Low-jitter PLL
- Functional safety
  - Enables ASIL-B applications
  - Fault Collection and Control Unit (FCCU) for fault collection and fault handling
  - Memory Error Management Unit (MEMU) for memory error management
  - Safe eDMA controller
  - Self-Test Control Unit (STCU2)
  - Error Injection Module (EIM)
  - On-chip voltage monitoring
  - Clock Monitor Unit (CMU)
- Security
  - Cryptographic Security Engine (CSE2)
  - Supports censorship and life-cycle management
- Timers
  - Two Periodic Interval Timers (PIT) with 32-bit counter resolution
  - Two System Timer Module (STM)
  - Two Software Watchdog Timers (SWT)
  - One eTimer module with 6 channels each
  - One FlexPWM module for 12 PWM signals
- Communication interfaces
  - Two Serial Peripheral interface (SPI) modules
  - One LINFlexD module
  - Two inter-IC communication interface (I2C) modules
  - Two FlexCAN modules supporting CAN FD with configurable buffers
- Debug functionality
  - 4-pin JTAG interface and Nexus/Aurora interface for serial high-speed tracing
  - e200z7 core: Nexus development interface (NDI) per IEEE-ISTO 5001-2012 Class 3+
- Two analog-to-digital converters (SAR ADC)
  - Each ADC supports up to 16 input channels
  - Cross Trigger Unit (CTU)
- On-chip voltage DC/DC regulator for core supply generation (VREG)
- Two Temperature Sensors (TSENS)

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

# Table of Contents


1 Introduction....3
1.1 Chip comparison....3
1.2 Feature list....4
1.3 Block diagram....8
2 Ordering parts....9
2.1 Determining valid orderable parts....9
3 Part identification....9
3.1 Description....9
3.2 Format....9
3.3 Fields....9
4 General....11
4.1 Introduction....11
4.2 Absolute maximum ratings....11
4.3 Operating conditions....13
4.4 Supply current characteristics....14
4.5 Voltage regulator electrical characteristics....15
4.6 Electromagnetic Compatibility (EMC) specifications....19
4.7 Electrostatic discharge (ESD) characteristics....19
5 I/O Parameters....20
5.1 I/O pad DC electrical characteristics....20
5.2 I/O pad AC specifications....21
5.3 Aurora LVDS driver electrical characteristics....22
5.4 Reset pad electrical characteristics....22
6 Peripheral operating requirements and behaviors....24
6.1 Clocks and PLL Specifications....24
7 Analog....27
7.1 ADC electrical characteristics....27
8 Memory modules....29
8.1 Flash memory program and erase specifications....29
8.2 Flash memory Array Integrity and Margin Read specifications....30
8.3 Flash memory module life specifications....31
8.4 Data retention vs program/erase cycles....32
8.5 Flash memory AC timing specifications....32
8.6 Flash memory read wait-state and address-pipeline control settings....33
9 Communication modules....34
9.1 SPI timing specifications....34
9.2 LINFlexD timing specifications....39
9.3 I2C timing....39
10 Debug modules....40
10.1 JTAG/CJTAG interface timing....40
10.2 Nexus Aurora debug port timing....43
11 WKPU/NMI timing specifications....44
12 External interrupt timing (IRQ pin)....45
13 Temperature sensor electrical characteristics....45
14 Radar module....46
14.1 MIPICSI2 D-PHY electrical and timing specifications....46
14.2 MIPICSI2 disclaimer....49
15 Thermal characteristics....50
15.1 General notes for specifications at maximum junction temperature....51
15.2 References....53
16 Packaging....53
17 Reset sequence....54
17.1 Reset sequence duration....54
17.2 Reset sequence description....54
18 Power sequencing requirements....57
19 Package pinouts and signal descriptions....58
20 Release Notes....59

# 1 Introduction

## 1.1 Chip comparison

The following table provides a comparison and their proposed features of three devices S32R372, S32R274 and MPC5775K . For full details of all of the family derivatives please contact your marketing representative.

**Table 1. S32R372 Chip comparison table**

| Feature | S32R372 | S32R274 | MPC5775K |
|---|---|---|---|
| CPUs | 2x e200z7260 | 2x e200z7260<br>e200z420 lock-step | |
| SIMD | SPE2 + EFP2 (both z7) | SPE2 + EFP2 (both z7) | SPE2 + EFP2 (both z7) |
| Maximum Operating Frequency | 240 MHz | 240 MHz (z7) 180 MHz (z4) | 266 MHz (z7) 133 MHz (z4) |
| Flash | 1.3 MB with ECC | 2 MB with ECC | 4 MB with ECC |
| EEPROM support | 32K (emulation) | 64K (emulation) | 96K (emulation) |
| RAM | 1 MB with ECC | 1.5 MB with ECC | 1.5 MB with ECC |
| ECC | end-to-end | | |
| MPU | CoreMPU: 24 entries per core<br>SystemMPU: 2x16 entries | | |
| eDMA | safe eDMA with 32 channels, 64 triggers | | |
| Control ADC[1] | 2x 12-bit SAR ADC, 1 MSps input mux for 16 external channels | 2x 12-bit SAR ADC, 1 MSps input mux for 16 external channels | 4x 12bit SAR ADC, 1 MSps, input mux for 37 external channels |
| RADAR ADC | - | 4x 12-bit ΣΔ ADC, 10 MSps | 8x 12-bit ΣΔ ADC, 10 MSps |
| SPT | 1x v2.5 | 1x v2 | 1x v1 |
| CTE[1] | 1x | | |
| WGM | - | 1x | 1x |
| CTU | 1x | 1x | 2x |
| SWT | 2x | 3x | 3x |
| STM | 2x | 3x | 3x |
| PIT | 2x | | |
| CRC | 2x | | |
| SEMA42 | 1x | | |
| LINFlexD[2] | 1x | 1x | 4x |
| FlexCAN | 2x FlexCAN-FD | 3x FlexCAN including 2x FlexCAN-FD | 4x FlexCAN + 1x MCAN-FD |
| SPI[1] | 2x | 2x | 4x |

*Table continues on the next page...*

**Table 1. S32R372 Chip comparison table (continued)**

| Feature | S32R372 | S32R274 | MPC5775K |
|---|---|---|---|
| I²C[3] | 2x | 2x | 3x |
| Zipwire | - | 1x LFAST+SIPI, 320MHz | |
| FlexRay | - | 1x dual channel | |
| Ethernet | - | 10/100 and >100 Mbps, RMII/MII/ RGMII I/F, AVB support | 10/100Mbps, RMII/MII I/F, AVB support |
| FlexPWM[1] | 1x, 12 PWM channels | 1x, 12 PWM channels | 2x, 12 PWM channels each |
| eTimer[1] | 1x, 6 channels | 2x, 6 channels each | 3x, 6channels each |
| External ADC interface | 1x 2 lanes MIPICSI2 Rx, 1Gbps/lane | 1x 4 lanes MIPICSI2 Rx, 1Gbps/lane | 1x PDI (16-bit data, clock, sync) |
| IRCOSC | 16 MHz | | |
| XOSC | 40 MHz | | |
| FMPLL | dual system PLL, 1x FM modulated | | |
| DAC | - | 1x 12-bit 10MSps | 1x 12-bit 2MSps |
| SIUL2[1] | 1x | | |
| BAM | 1x | | |
| INTC | 1x | | |
| SSCM | 1x | | |
| FCCU/FOSU | 1x | | |
| MEMU | 1x | | |
| STCU2 | 1x | | |
| CSE | 1x | 1x | - |
| PASS | 1x | 1x | - |
| TDM | 1x | 1x | - |
| MC_ME | 1x | | |
| MC_CGM | 1x | | |
| MC_RGM | 1x | | |
| TSENS | 2x | | |
| Debug | JTAGC, JTAGM, CJTAG, with class3+Nexus, Aurora only | | |
| Safety Level | ISO26262 SEooC ASIL-B | ISO26262 SEooC ASIL-B to ASIL-D | |
| Temp. Range (Tj) | -40 to +150˚C | | |

1. This chip offers limited functionality with 10 mm x 10 mm outline. For details see Feature list
2. Available only with 14 mm x 14 mm outline for this chip.
3. Single I²C available with 10 mm x 10 mm outline for this chip.

## 1.2 Feature list

On-chip modules available within the device include the following features:

- Two computation cores: Power Architecture e200z7 32-bit CPU

    - Dual issue: up to two instructions per clock cycle
    - Harvard architecture with 64-bit bus for data instructions
    - 16 KB instruction cache and 16 KB data cache
    - 64 KB data local memory
        - with background load/store: backdoor access
        - 0-wait state for all read and 32/64-bit write accesses
        - Low number of wait states for backdoor accesses
    - Support for decorated storage
    - Using variable length encoding (VLE) for higher code density
    - 4-way integer processing unit (SPE2)
    - 2-way single-precision Floating Point Unit (EFP2)
- 1.3 MB on-chip code flash (FMC flash) with ECC
    - Three ports (one per CPU, one for RADAR processing) shared between code and data flash with 4 × 256 bit buffer for code and data flash including prefetch functions
    - Data flash is part of the code flash module
    - Including 32 KB EEPROM emulation
- 1 MB on-chip SRAM with ECC
    - Decorated memory controller to support atomic read-modify-write operations
    - Single- and double-bit error visibility is supported
    - Four ports (one per CPU, one for RADAR processing, one for all other) and up to 6 banks allow simultaneous accesses from different masters to different banks
- RADAR processing
    - Signal Processing Toolbox (SPT) for RADAR signal processing acceleration
    - Cross Triggering Engine (CTE) for precise timing generation and triggering[1]
    - MIPICSI2 interface to connect external ADCs
        - Two data lanes, with up to 1 GB/s per lane and in total
        - One clock lane
- Memory protection
    - Each core memory protection unit provides 24 entries
    - Data and instruction bus system memory protection Unit (SMPU) with 16 region descriptors each
    - Register protection
- Clock generation
    - 40 MHz external crystal (XOSC)
    - 16 MHz Internal oscillator (IRCOSC)
    - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
    - Low-jitter SDPLL
- Functional safety

1. This chip offers limited functionality with 10 mm x 10 mm outline.

- Typical use: ASIL B applications
- End-to-end ECC ensuring full protection of all data access throughout the system, from each system masters through the crossbar and to the memories and peripherals
- FCCU for fault collection and fault handling
- MEMU for memory error management
- safe eDMA controller
- User selectable Memory BIST (MBIST) can be enabled to run out of various reset conditions or during runtime
- Self-Test Control Unit (STCU2)
- Error Injection Module (EIM)
- On-chip voltage monitoring
- Clock Monitor Unit (CMU) to support monitoring of critical clocks

- Security
  - Hardware Security Module (CSE2) enabling advanced security management
  - Supports censorship and life-cycle management via Password and Device Security (PASS) module
  - Diary control for tamper detection (TDM)
- Support Modules
  - Global Interrupt controller (INTC) capable of routing interrupts to any CPU
  - Semaphore unit to manage access to shared resources
  - Two CRC computation units with four polynomials
  - 32-channels eDMA controller with multiple transfer request sources using DMAMUX
  - Boot Assist Module (BAM) supports internal flash programming via a serial link (LIN / CAN)
- Timers
  - Two Periodic Interval Timers (PIT) with 32-bit counter resolution
  - Two System Timer Module (STM)
  - Two Software Watchdog Timers (SWT)
  - One eTimer modules with 6 channels[2]
  - One FlexPWM module for 12 PWM signals[1]
- Communication interfaces
  - Two Serial Peripheral interface (SPI) module[3]
  - Two inter-IC communication interface (I2C) modules[4]
  - One LINFlexD module[5]
  - Two FlexCAN modules supporting CAN FD with configurable buffers
- Debug functionality

2. Less channel in 10 mm x 10 mm outline.
3. One SPI offers less number of chip-selects in 10 mm x 10 mm outline.
4. Single $I^2C$ in 10 mm x 10 mm outline.
5. Available only with 14 mm x 14 mm outline for this chip.

    - 4-pin JTAG interface and Nexus/Aurora interface for serial high-speed tracing
    - e200Z7 cores: Nexus development interface (NDI) per IEEE-ISTO 5001-2012 Class 3+
    - All platform bus masters can be monitored via Nexus/Aurora
    - Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) (IEEE 1149.1) and 1149.7 (cJTAG)
    - On-chip control for Nexus development interface by JTAGM module
- Two analog-to-digital converters (SAR ADC)
    - Each ADC supports up to 16 input channels[2]
    - Cross Trigger Unit to enable synchronization of ADC conversions with eTimer
- On-chip voltage DC/DC regulator for core supply generation (VREG)[5]
- Two Temperature Sensors (TSENS)

# 1.3 Block diagram

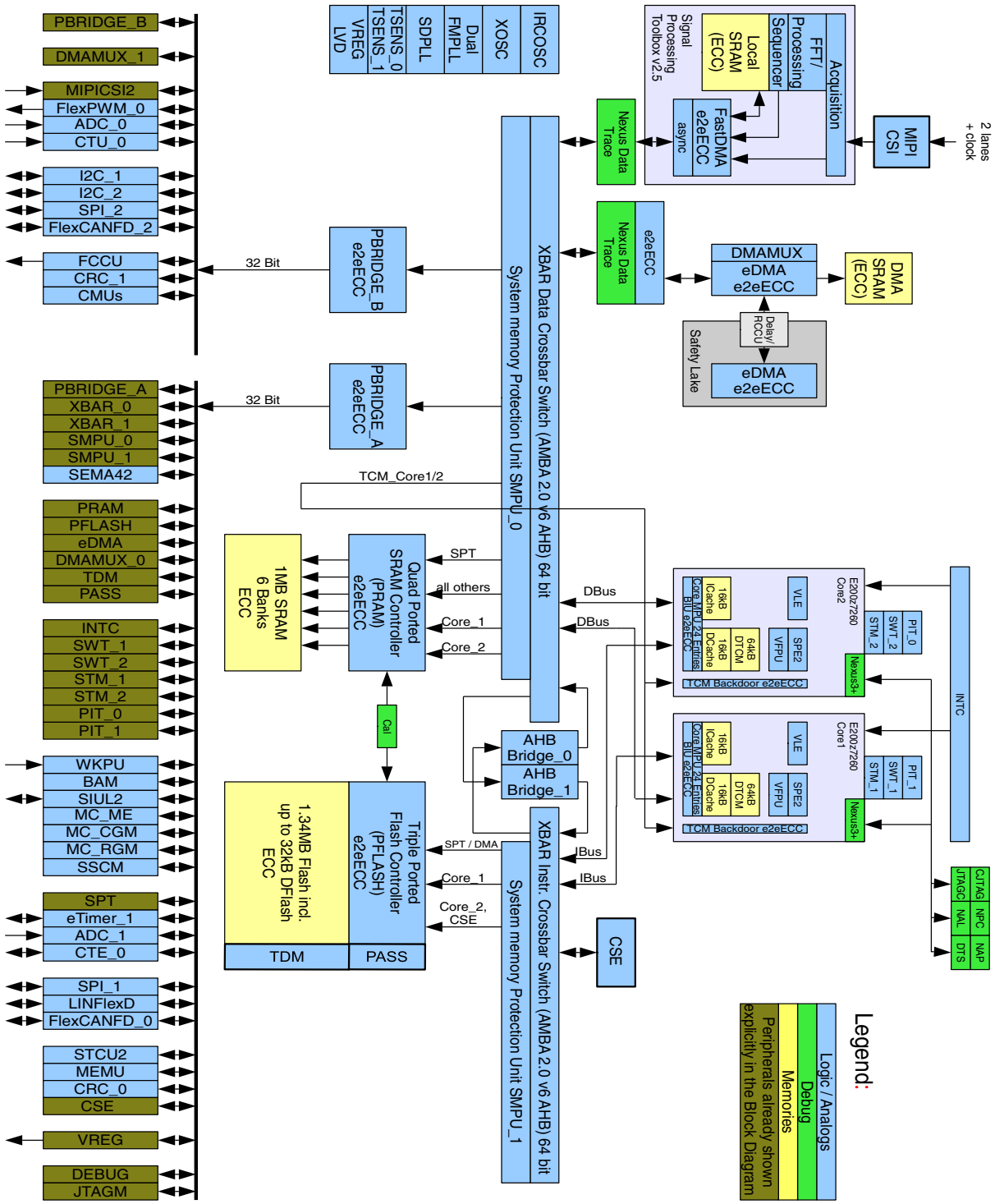



**Figure 1. Architecture Block Diagram**

# 2 Ordering parts

## 2.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the device number.

# 3 Part identification

## 3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 3.2 Format

Part numbers for this device have the following format: S32R372.

## 3.3 Fields

This section lists the possible values for each field in the part number (not all combinations are valid):

**Part identification**

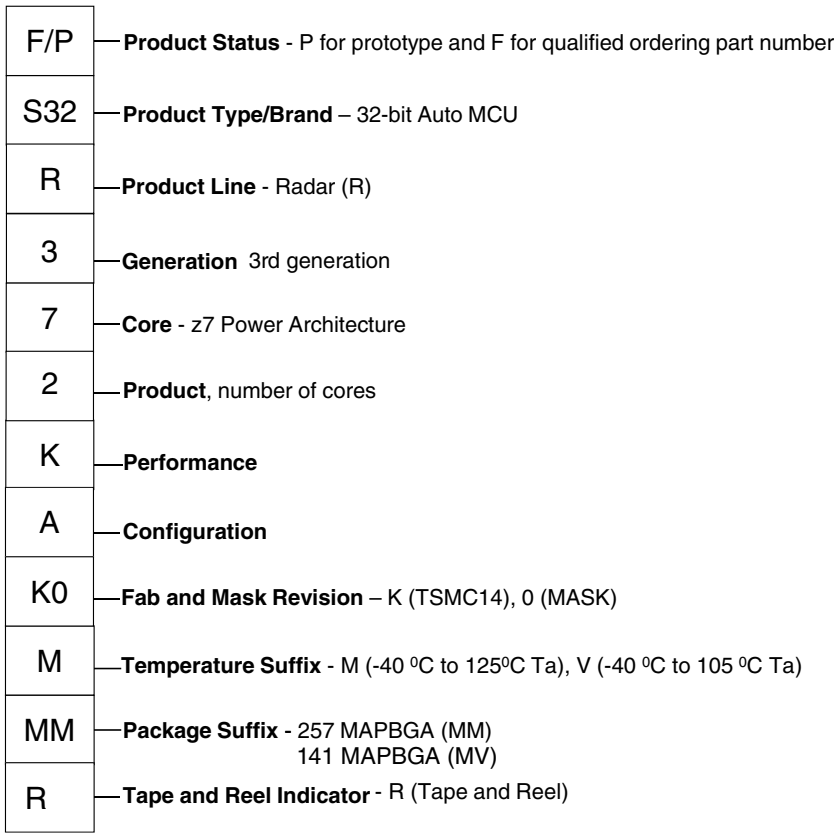



**Figure 2. Commercial product code structure**

**Table 2. ASCII code for performance**

| Perf (MHz) | Z7 | Z7 |
|---|---|---|
| S | 240 | 240 |

**Table 3. ASCII code for 257 MAPBGA configuration**

| 257MAPBGA | Configuration | 1.3 MB Flash | 768 KB RAM | 1 MB RAM | CSE |
|---|---|---|---|---|---|
| PS32R372SAK0MMM | A | Yes | No | Yes | Yes |
| FS32R372SBK0MMM | B | Yes | Yes | No | Yes |
| FS32R372SCK0MMM | C | Yes | Yes | No | No |
| FS32R372SDK0MMM | D | Yes | No | Yes | Yes |
| FS32R372SEK0MMM | E | Yes | No | Yes | No |

**Table 4. ASCII code for 141MAPBGA configuration**

| 141MAPBGA | Configuration | 1.3 MB Flash | 768 KB RAM | 1 MB RAM | CSE |
|---|---|---|---|---|---|
| PS32R372SAK0MMV | A | Yes | No | Yes | Yes |
| FS32R372SBK0MMV | B | Yes | Yes | No | Yes |
| FS32R372SCK0MMV | C | Yes | Yes | No | No |
| FS32R372SDK0MMV | D | Yes | No | Yes | Yes |
| FS32R372SEK0MMV | E | Yes | No | Yes | No |

# 4 General

## 4.1 Introduction

The electrical specifications are preliminary and are undergoing initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

## 4.2 Absolute maximum ratings

**NOTE**

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

**Table 5. Absolute maximum ratings**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD_HV_PMU}$ | 3.3 V PMU supply voltage | — | –0.3 | 3.63[1, 2] | V |
| $V_{DD_HV_REG3V8}$ | SMPS driver input Supply Voltage | — | –0.3 | 5.5 | V |

*Table continues on the next page...*

## Table 5. Absolute maximum ratings (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD_HV_IO*}$ | 3.3 V Input/Output Supply Voltage, and PWM IO Supply | — | –0.3 | 3.63[1, 2] | V |
| $V_{SS_HV_IOx}$ | Input/output ground voltage | — | –0.1 | 0.1 | V |
| $V_{DD_HV_FLA}$ | 3.3 V flash supply voltage | — | –0.3 | 3.63[1, 2] | V |
| $V_{DD_HV_RAW}$ | AFE RAW supply voltage | — | –0.1 | 4 | V |
| $V_{DD_HV_DAC}$ | AFE DAC supply voltage | — | –0.1 | 4 | V |
| $V_{DD_LV_IO*}$ | Aurora supply voltage[3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{DD}$ | 1.25 V core supply voltage[3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{SS}$ | 1.25 V core supply ground | — | –0.3 | 0.3 | V |
| $V_{SS_LV_OSC}$ | Oscillator amplifier ground | — | –0.1 | 0.1 | V |
| $V_{DD_LV_PLL0}$ | System PLL supply voltage [3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{DD_HV_ADCREF0/1}$ | ADC_0 and ADC_1 high reference voltage | — | –0.3 | 5.5 | V |
| $V_{SS_HV_ADCREF0/1}$ | ADC_0 and ADC_1 ground and low reference voltage | — | –0.1 | 0.1 | V |
| $V_{DD_HV_ADC}$ | 3.3 V ADC supply voltage | — | –0.3 | 4.0 [1, 2] | V |
| $V_{SS_HV_ADC}$ | 3.3 V ADC supply ground | — | –0.1 | 0.1 | V |
| $TV_{DD}$ | Supply ramp rate[6] | — | 0.00005 | 0.1 | V/µs |
| $V_{IN_XOSC}$ | Voltage on XOSC pins with respect to ground | — | -0.3 | 1.47 | V |
| $V_{INA}$ | Voltage on SAR ADC analog pin with respect to ground ($V_{SS_HV_ADCREFx}$) | — | –0.3 | 6.0 | V |
| $V_{IN}$ | Voltage on any digital pin with respect to ground ($V_{SS_HV_IOx}$) | Relative to $V_{DD_HV_IOx}$ | –0.3 | $V_{DD_HV_IOx}$ + 0.3[7] | V |
| $V_{DD_LV_DPHY}$ | MIPICSI2 DPHY voltage supply[3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{SS_LV_DPHY}$ | MIPICSI2 DPHY supply ground | — | –0.3 | 0.3 | V |
| $I_{INJPAD}$ | Injected input current on any pin during overload condition[8] | — | –5 | +5 | mA |
| $I_{INJSUM}$ | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | mA |
| $T_{STG}$ | Storage temperature | — | –55 | 150 | °C |

1. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
2. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
3. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum $T_J$ = 150°C; remaining time as defined in note 5 and note 6.
4. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum $T_J$ = 150°C; remaining time as defined in note 6.
5. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum $T_J$=150°C.
6. $TV_{DD}$ is relevant for all external supplies.
7. Only when $V_{DD_HV_IOx}$ < 3.63 V.
8. No input current injection circuitry on AFE pins.

## 4.3 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the datasheet are valid, except where explicitly noted. The device operating conditions must not be exceeded, or the functionality of the device is not guaranteed.

**Table 6. Device operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{DD_HV_PMU}$ | 3.3V PMU Supply Voltage | — | 3.13[2] | 3.3 | 3.6 | V |
| $V_{DD_HV_REG3V8}$ | SMPS driver input Supply Voltage | — | 3.13 | 3.8 | 5.5 | V |
| $V_{DD}$ | Core Supply Voltage | — | 1.19[2] | 1.25 | 1.31[3] | V |
| $V_{DD_HV_IO*}$ | Main GPIO 3V Supply Voltage, and PWM IO Supply Voltage | — | 3.13[2] | 3.3 | 3.6 | V |
| $V_{DD_LV_IO_*}$ | Aurora Supply Voltage | — | 1.19 | 1.25 | 1.31 | V |
| $V_{DD_LV_PLL0}$ | System PLL Supply Voltage | — | 1.19[2] | — | 1.31 | V |
| $V_{DD_HV_FLA}$[4] | Flash Supply Voltage | — | 3.13[2] | 3.3 | 3.6 | V |
| $V_{DD_HV_ADC}$ | SAR ADC Supply Voltage (HVD supervised) | — | 3.13[2] | 3.3 | 3.6[5] | V |
| $V_{DD_HV_RAW}$[6] | 3.3V AFE RAW Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD_HV_DAC}$ | 3.3V AFE DAC Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD_HV_ADCREF0/1}$ | ADC_0 and ADC_1 high reference voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{IN}$ | Voltage on digital pin with respect to ground ($V_{SS_HV_IOx}$) | — | — | — | $V_{DD_HV_IOx}$ + 0.3 | V |
| $V_{INA}$[7] | Voltage on SAR ADC analog pin with respect to ground ($V_{SS_HV_ADCREFx}$) | — | — | — | $V_{DD_HV_ADCREFx}$ | V |
| $V_{DD_LV_DPHY}$ | MIPICSI2 DPHY voltage supply | | 1.19 | 1.25 | 1.31 | V |
| $T_A$,[8] | Ambient temperature at full performance[9] | — | –40 | — | 125 | °C |
| $T_J$[8] | Junction temperature | — | –40 | — | 150 | °C |
| $F_{XTAL}$ | XOSC Crystal Frequency[10] | — | — | 40 | — | MHz |
| **AFE Bypass Modes Only** | | | | | | |
| **Single-Ended External Clock** | | | | | | |
| $EXTAL_{clk}$ | EXTAL external clock frequency | | | 40 | | MHz |
| $V_{inxoscjit}$ | EXTAL external clock Cycle to Cycle Jitter (RMS) | — | — | — | 3.5 | ps |
| $V_{inxoscclkvil}$ | EXTAL external clock input low voltage | — | 0 | — | 0.4 | V |
| $V_{inxoscclkvih}$ | EXTAL external clock input high voltage | — | 1 | — | 1.23 | V |
| $t_r/t_f$ | Rise/fall time of EXTAL external clock input | | | | 1 | ns |
| $t_{dc}$ | Duty Cycle of EXTAL external clock input | | 47 | 50 | 53 | % |

*Table continues on the next page...*

**Table 6. Device operating conditions (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| **Differential LVDS External Clock** | | | | | | |
| $LVDS_{clk}$ | LVDS external clock frequency | | | 40 | | MHz |
| $LVDSV_{inxosccclk}$ | LVDS external clock input voltage | | 0 | | 1.36 | V |
| $LVDSV_{inxosccclk(p-p)}$ | LVDS external clock input voltage (peak-peak) | Voltage driven, AC coupled Differential | 0.45 | 0.70 | 1.12 | V |
| $LVDSI_{inxosccclk}$ | LVDS external clock input current | Current driven, DC coupled. | 3.0 | 3.5 | 4.0 | mA |
| $LVDSV_{inxoscjit}$ | LVDS external clock Jitter (RMS) | | | | 3.5 | ps |
| $t_r$ /$t_f$ | Rise/fall time of LVDS external clock input | 20% - 80% | | | 1.5 | nS |
| $t_{dcLVDS}$ | Duty Cycle of LVDS external clock input | | 47 | 50 | 53 | % |

1. Full functionality cannot be guaranteed when voltages are out of the recommended operating conditions.
2. Min voltage takes into account the LVD variation.
3. Max voltage takes into account HVD variation.
4. The ground connection for the $V_{DD_HV_FLA}$ is shared with $V_{SS}$.
5. Supply range does not take into account HVD levels. Full range can be achieved after power-up, if HVD is disabled. See Voltage regulator electrical characteristics section for details.
6. For 141MAPBGA pacakge, VDD_HV_RAW and VDD_HV_DAC supplies share the same pin in the package.
7. On channels shared between ADC0 and 1, $V_{DD_HV_ADCREFx}$ is the lower of $V_{DD_HV_ADCREF0/1}$.
8. When determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is critical that the junction temperature specification is not exceeded under any condition
9. Full performance means Core1/2 running @ 240 MHz, SPT running @ 160 MHz, rich set of peripherals used.
10. Recommended Crystal 40 MHz (ESR≤30 Ω), 8 pF load capacitance.

## 4.4 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

**Table 7. Current consumption characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD_CORE}$ | Core current in run mode | All cores at max frequency. 1.31 V. Tj = 150°C | - | - | 1100[1] | mA |
| $I_{DD_HV_FLA}$ | Flash operating current | Tj = 150°C. $V_{DD_HV_FLA}$ = 3.6 V | - | 3[2] | 40[3] | mA |
| $I_{DD_LV_AURORA}$ | Aurora operating current | Tj = 150°C. $V_{DD_LV_AURORA}$ = 1.31 V. 4 TX lanes enabled. | - | - | 60 | mA |
| $I_{DD_HV_ADC}$ | ADC operating current | Tj = 150°C. $V_{DD_HV_ADC}$ = 3.6 V. 2 ADCs operating at 80 MHz. | - | 2 | 5 | mA |
| $I_{DD_HV_ADCREF}$ | Reference current per ADC[4] | Tj = 150°C. $V_{DD_HV_ADCREFx}$ = 3.6 V. ADC operating at 80 MHz. | - - | - - | 1.5 0.75 | mA |

*Table continues on the next page...*

**Table 7. Current consumption characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Reference current per temp sensor[5] | | | | | |
| $I_{DD_HV_RAW}$ | AFE and regulator operating current | Tj = 150°C. $V_{DD_HV_RAW}$ = 3.6 V. SD-PLL and AFE regulators enabled. | - | 13.4 [6] | 16 | mA |
| $I_{DD_HV_DAC}$ | AFE DAC operating current | Tj = 150°C. $V_{DD_HV_DAC}$ = 3.6 V. SD-PLL and DAC enabled. | - | 1.5 | 2 | mA |
| $I_{DD_HV_PMU}$ | PMU operating current | Tj = 150°C. VDD_HV_PMU = 3.6 V. Internal regulation enabled. | - | 2 | 10 | mA |
| $I_{DD_LV_DPHY}$ | MIPICSI2 DPHY operating current in HS-RX mode | Tj = 150°C, $V_{DD_LV_DPHY}$ =1.31 V | 8.7 | 14.9 | 23.2 | mA |

1. Strong dependence on use case, cache usage.
2. Measured during flash read.
3. Peak Flash current measured during read while write (RWW).
4. ADC0 and 1 on ADCREF0/1.
5. Temp sensor current when PMC_CTL_TD[TSx_AOUT_EN] = 1. TS0 on ADCREF0/1.
6. Typical number is approximately 12 mA for SD-PLL and 1 mA for the AFE regulators.

## 4.5 Voltage regulator electrical characteristics

**Table 8. Voltage regulator electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| POR-R | 1.25 V VDD core POR release | — | 0.97 | 1.02 | 1.06 | V |
| POR-E | 1.25 V VDD core POR engage | — | 0.93 | 0.98 | 1.02 | V |
| LVD12R | Low-Voltage Detection 1.25 V release (Core VDD supply, and PLL0/1 supply LVDs) | Untrimmed | 1.122 | 1.157 | 1.192 | V |
| LVD12R-trim | | Trimmed | 1.142 | 1.157 | 1.172 | V |
| LVD12E | Low-Voltage Detection 1.25 V engage (Core VDD supply and PLL0/1 supply LVDs) | Untrimmed | 1.102 | 1.137 | 1.172 | V |
| LVD12E-trim | | Trimmed | 1.122 | 1.137 | 1.152 | V |
| HVD12R-trim | High-Voltage Detection 1.25 V release (Core VDD) | Trimmed | 1.33 | 1.35 | 1.37 | V |
| HVD12E-trim | High-Voltage Detection 1.25 V engage (Core VDD supply) | Trimmed | 1.36 | 1.38 | 1.40 | V |
| LVD_MIPI12R-trim | Low-Voltage Detection 1.25V release (MIPICSI2 DPHY supply) | — | 1.130 | 1.157 | 1.184 | V |
| LVD_MIPI12E-trim | Low-Voltage Detection 1.25V engage (MIPICSI2 DPHY supply) | — | 1.111 | 1.137 | 1.163 | V |
| POR-R-VDD_HV_PMU | 3.3 V PMU supply voltage POR release threshold | — | 2.54 | 2.645 | 2.735 | V |
| POR-E-VDD_HV_PMU | 3.3 V PMU supply voltage POR engage threshold | — | 2.50 | 2.60 | 2.695 | V |
| LVD33R | 3.3V Low-Voltage Detection Release Threshold (PMC, FLASH, IO, ADC) | Untrimmed | 2.90 | 3.02 | 3.13 | V |
| LVD33R-trim | | Trimmed | 3.00 | 3.05 | 3.10 | V |

*Table continues on the next page...*

## Table 8. Voltage regulator electrical specifications (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| LVD33E | 3.3V Low-Voltage Detection Engage Threshold (PMC, FLASH, IO, ADC) | Untrimmed | 2.86 | 2.98 | 3.09 | V |
| LVD33E-trim | | Trimmed | 2.96 | 3.01 | 3.06 | V |
| HVD33R | 3.3V High-Voltage Detection Release Threshold (ADC) | Untrimmed | 3.45 | 3.61 | 3.75 | V |
| HVD33R-trim | | Trimmed | 3.47 | 3.53 | 3.58 | V |
| HVD33E | 3.3V High-Voltage Detection Engage Threshold (ADC) | Untrimmed | 3.51 | 3.65 | 3.79 | V |
| HVD33E-trim | | Trimmed | 3.51 | 3.57 | 3.62 | V |
| UVL30R | SMPS under-voltage lockout release threshold | Untrimmed | 2.75 | 2.90 | 3.05 | V |
| UVL25E | SMPS under-voltage lockout engage threshold | | 2.40 | 2.55 | 2.7 | V |
| DGLITCHE | Voltage Detector Deglitcher Filter Time - Engage | — | 2.0 | 3.5 | 5 | µs |
| DGLITCHR | Voltage Detector Deglitcher Filter Time - Release | — | 5 | 7 | 12 | µs |
| RSTDGLTC | VREG_POR_B Input Deglitch Filter Time | — | 200 | 320 | 500 | ns |
| RSTPUP | VREG_POR_B Pin Pull-up Resistance | — | 37 | 75 | 150 | kΩ |
| REGENPUP | VREG_SEL Pin Pull-up Resistance | — | 37 | 75 | 150 | kΩ |
| VSMPS | Internal switched regulator output voltage [1] | Load Current from 10 mA to 1.8 A | 1.19 | 1.255 | 1.35 | V |
| FSMPS | Internal switched regulator operating frequency without modulation | Untrimmed | 0.65 | 1.00 | 1.35 | MHz |
| | | Trimmed | 0.93 | 1.00 | 1.07 | MHz |
| FSMPS-M7.5 | Internal switched regulator frequency modulation | — | — | 7.5 | — | % |
| FSMPS-M15 | | — | — | 15 | — | % |
| FSMPS-M30 | | — | — | 30 | — | % |
| VREGSWPUP | Internal switched regulator gate-driver pull-up resistance[2] | — | — | — | — | — |
| VREF_BG_T | PMC bandgap reference voltage for SARADC | Trimmed | 1.20 | 1.22 | 1.237 | V |
| Vih (VREG_POR_B) | VREG_POR_B pin High Voltage level | — | 0.7 x VDD_HV_PMU | — | VDD_HV_PMU + 0.3 | V |
| Vil (VREG_POR_B) | VREG_POR_B pin Low Voltage level | — | -0.3 | — | 0.3 x VDD_HV_PMU | V |
| LVDAFER | Low Voltage Detection 3.3V Release (AFE VDD_HV_DAC and VDD_HV_RAW supplies) | | 2.75 | 2.80 | 2.90 | V |
| LVDAFEE | Low Voltage Detection 3.3V Engage (AFE VDD_HV_DAC and VDD_HV_RAW supplies) | | 2.68 | 2.77 | 2.86 | V |

1. Min/Max includes transient load conditions. Steady state voltage is within the core supply operating specifications.
2. There is a strong pull up from VREG_SWP to VDD_HV_REG3V8 which is connected when SMPS is disabled. The pullup has resistance less than 1 Kohm, therefore VREG_SWP should not be connected to ground if unused.

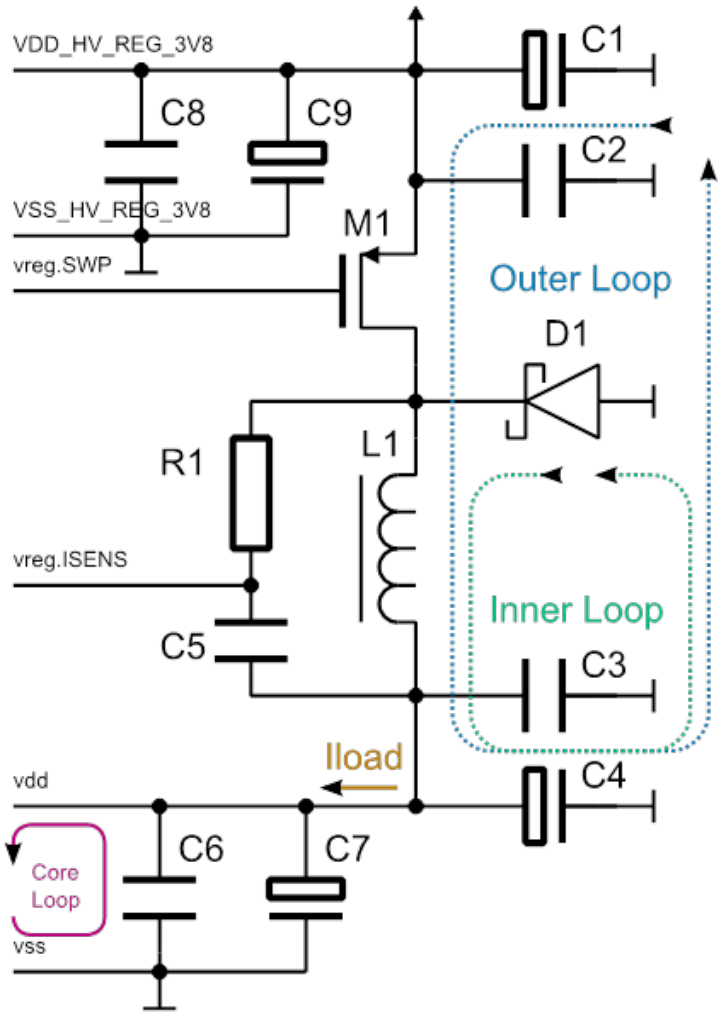



**Figure 3. SMPS External Components Configuration**

**Table 9. SMPS External Components**

| Ref | Description |
|---|---|
| M1 | SI3443, 2SQ2315 |
| L1 | 2.2 uH 3A < 100 mΩ series resistance (Ex. Bourns SRU8043-2R2Y) |
| D1 | SS8P3L 8A Schottcky Diode |
| R1 | 24 kΩ |
| C1 | 10 µF Ceramic |
| C2 | 100 nF Ceramic |
| C3 | 100 nF Ceramic (place close to inductor) |
| C4 | 10 uF Ceramic (place close to inductor) |
| C5 | 1 nF Ceramic |
| C6 | 4 x 100 nF + 4 x 10nF Ceramic (place close to MCU supply pins) |
| C7 | 4 x 10 µF Ceramic (place close to MCU supply pins) |
| C8 | 100 nF Ceramic |
| C9 | 1 µF Ceramic (Unless C1 is really close to the pin) |

**NOTE**

Internal DC-DC (SMPS) regulation mode is only supported in BGA257, for BGA141 an external 1.25 V (nominal) supply is required for device operation.

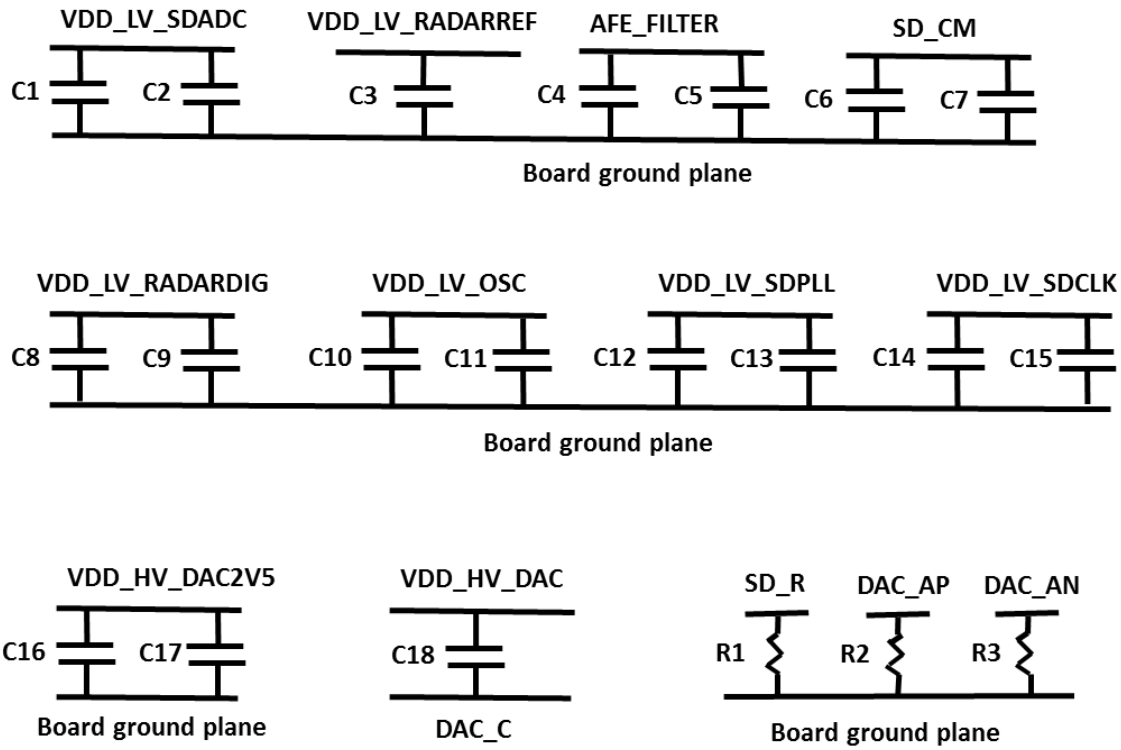



**Figure 4. Radar AFE External Components Configuration**

**Table 10. Radar AFE External Components**

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C1 | 0.47 µF | ±35% | 3 | — | — |
| C2 | 0.1 µF | ±35% | — | 1 | — |
| C3 | 1.0 µF | ±35% | 7 | — | — |
| C4 | 1.0 µF | ±35% | 2 | — | — |
| C5 | 0.1 µF | ±35% | — | 4 | — |
| C6 | 1.0 µF | ±35% | 8 | — | — |
| C7 | 0.1 µF | ±35% | — | 6 | — |
| C8 | 1.0 µF | ±35% | 6 | — | — |
| C9 | 0.1 µF | ±35% | — | 5 | — |
| C10 | 1.0 µF | ±35% | 4 | — | — |
| C11 | 0.1 µF | ±35% | — | 2 | — |
| C12 | 1.0 µF | ±35% | 5 | — | — |

*Table continues on the next page...*

**Table 10. Radar AFE External Components (continued)**

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C13 | 0.1 µF | ±35% | — | 3 | — |
| C14 | 1.0 µF | ±35% | 10 | — | — |
| C15 | 0.1 µF | ±35% | — | 8 | — |
| C16 | 1.0 µF | ±35% | 9 | — | — |
| C17 | 0.1µF | ±35% | — | 7 | — |
| C18 | 10 µF | — | 1 | — | X7R type |
| R1 | 40.2 kΩ | ±0.1% | — | — | tempco = 25ppm/C |
| R2 | 300 Ω | — | — | — | DAC RI See Table 1 |
| R3 | 300 Ω | — | — | — | DAC RI See Table 1 |
| Crystal | 40MHz | — | — | — | Connected between XOSC_EXTAL/ XOSC_XTAL, ESR ≤ 30Ω |

1. All Radar AFE external bypass capacitors should be placed as close as possible to the associated package pin. As shown in Radar AFE External Components Configuration figure, most pins have two values of bypass capacitor. Greater than 0.1 µF is referred to as the larger cap. 0.1 µF is referred to as the smaller cap

## 4.6 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

## 4.7 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × ($n$ + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**NOTE**

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room

temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 11. ESD ratings**

| No. | Symbol | Parameter | Conditions[1] | Class | Max value[2] | Unit |
|---|---|---|---|---|---|---|
| 1 | $V_{ESD(HBM)}$ | Electrostatic discharge (Human Body Model) | $T_A$ = 25 °C conforming to AEC-Q100-002 | H1C | 2000 | V |
| 2 | $V_{ESD(CDM)}$ | Electrostatic discharge (Charged Device Model) | $T_A$ = 25 °C conforming to AEC-Q100-011 | C3A | 500[3, 4, 5] 750 (corners) | V |

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.
3. 500 V for non-AFE pins, 250 V for AFE pins.
4. AFE pins for 257MAPBGA: balls C3-C4, D1-D2, D6, D8, E1-E2, F1-F4, G3-G4, H3-H4.
5. AFE pins for 141MAPBGA: balls A1, B1, C1-C3, D1-D3, E1.

# 5 I/O Parameters

## 5.1 I/O pad DC electrical characteristics

NMI, TCK, TMS, JCOMP are treated as GPIO.

**Table 12. I/O pad DC electrical specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.65*$V_{DD_HV_IO}$ | $V_{DD_HV_IO}$ + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | -0.3 | 0.35*$V_{DD_HV_IO}$ | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.55 * $V_{DD_HV_IO}$ | $V_{DD_HV_IO}$ + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | -0.3 | 0.40 * $V_{DD_HV_IO}$ | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.1 * $V_{DD_HV_IO}$ | — | V |
| $Vih_{TTL}$ | TTL Input high level voltage (All SAR_ADC input pins) | 2 | $V_{DD_HV_ADCREFx}$ + 0.3 | V |
| $Vil_{TTL}$ | TTL Input low level voltage (All SAR_ADC input pins) | -0.3 | 0.56 | V |
| $Vhyst_{TTL}$ | TTL Input hysteresis voltage (All SAR_ADC input pins) | 0.3 | — | V |
| Pull_Ioh | Weak Pullup Current[1] | 10 | 55 | µA |
| Pull_Iol | Weak Pulldown Current[2] | 10 | 55 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |

*Table continues on the next page...*

**Table 12. I/O pad DC electrical specifications (continued)**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Voh | Output High Voltage[3] | 0.8 * $V_{DD_HV_IO}$ | — | V |
| Vol | Output Low Voltage[4] | — | 0.2 * $V_{DD_HV_IO}$ | V |
| Ioh_f | Full drive Ioh[5] (ipp_sre[1:0] = 11) | 18 | 70 | mA |
| Iol_f | Full drive Iol[5] (ipp_sre[1:0] = 11) | 21 | 120 | mA |
| Ioh_h | Half drive Ioh[5] (ipp_sre[1:0] = 10) | 9 | 35 | mA |
| Iol_h | Half drive Iol[5] (ipp_sre[1:0] = 10) | 10.5 | 60 | mA |

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD_HV_IO}$
3. Measured when pad is sourcing 2 mA
4. Measured when pad is sinking 2 mA
5. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

## 5.2 I/O pad AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +150°C and for the full operating range of the $V_{DD_HV_IO}$ supply defined in Table 6.

**Table 13. Functional Pad electrical characteristics**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns)[2] | | Drive Load (pF) | SIUL2_MSCR[SRC] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| pad_sr_hv (output) | 2.5/2.5 | 8.25/7.5 | 0.7/0.6 | 3./3 | 50 | 11 |
| | 6.4/5 | 19.5/19.5 | 2.5/2.0 | 12/12 | 200 | |
| | 2.2/2.5 | 8/8 | 0.4/0.3 | 3.5/3.5 | 25 | 10 |
| | 2.9/3.5 | 12.5/11 | 1.0/0.8 | 6.5/6.5 | 50 | |
| | 11/8 | 35/31 | 6.5/3.0 | 25/21 | 200 | |
| | 8.3/9.6 | 45/45 | 4/3.5 | 25/25 | 50 | 01[3] |
| | 13.5/15 | 65/65 | 6.3/6.2 | 30/30 | 200 | |
| | 13/13 | 75/75 | 6.8/6 | 40/40 | 50 | 00[3] |
| | 21/22 | 100/100 | 11/11 | 51/51 | 200 | |
| pad_sr_hv (input)[4] | | 2/2 | | 0.5/0.5 | 0.5 | NA |

1. As measured from 50% of core side input to Voh/Vol of the output
2. Measured from 20% - 80% of output voltage swing
3. Slew rate control modes
4. Input slope = 2 ns

**NOTE**

Data based on characterization results, not tested in production.

**Table 14. Functional Pad AC Specifications**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| pad_sr_hv(Cp) | Parasitic Input Pin Capacitance | 4.5 | 4.7 | 5.0 | pF |

## 5.3 Aurora LVDS driver electrical characteristics

**NOTE**

The Aurora interface is AC coupled, so there is no common-mode voltage specification.

**Table 15. Aurora LVDS driver electrical characteristics**

| Symbol | Parameter[1] | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $F_{TXRX}$ | Data rate | — | — | 1.15 | Gbps |
| Transmitter Specifications | | | | | |
| $V_{diffout}$ | Differential output voltage swing (terminated) | +/- 400 | +/- 600 | +/- 800 | mV |
| $T_{rise}/T_{fall}$ | Rise/Fall time (10% - 90% of swing) | 60 | | | ps |
| Receiver Specifications | | | | | |
| $V_{diffin}$ | Differential voltage | +/- 100 | | +/- 800 | mV |
| Termination | | | | | |
| $R_{V_L}$ | Terminating Resistance (external) | 99 | 100 | 101 | Ohms |
| $C_P$ | Parasitic Capacitance (pad + bondwire + pin) | | | 1 | pF |
| $L_P$ | Parasitic Inductance | | | 7 | nH |
| STARTUP | | | | | |
| $T_{STRT_BIAS}$ | Bias startup time | — | — | 5 | µs |
| $T_{STRT_TX}$ | Transmitter startup time[2] | — | — | 5 | µs |
| $T_{STRT_RX}$ | Receiver startup time[2] | — | — | 5 | µs |
| LVDS_RXOUT[3] | Receiver o/p duty cycle | 30 | | 70 | % |

1. Conditions for these values are $V_{DD_LV_IO_AURORA}$ = 1.19V to 1.32V, $T_J$ = –40 / 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
3. Receiver o/p duty cycle is measured with 1.25 Gbps, 50% duty cycle, max 1 ns rise/fall time, 100 mV voltage swing signal applied at the receiver input.

## 5.4 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET_B pin.

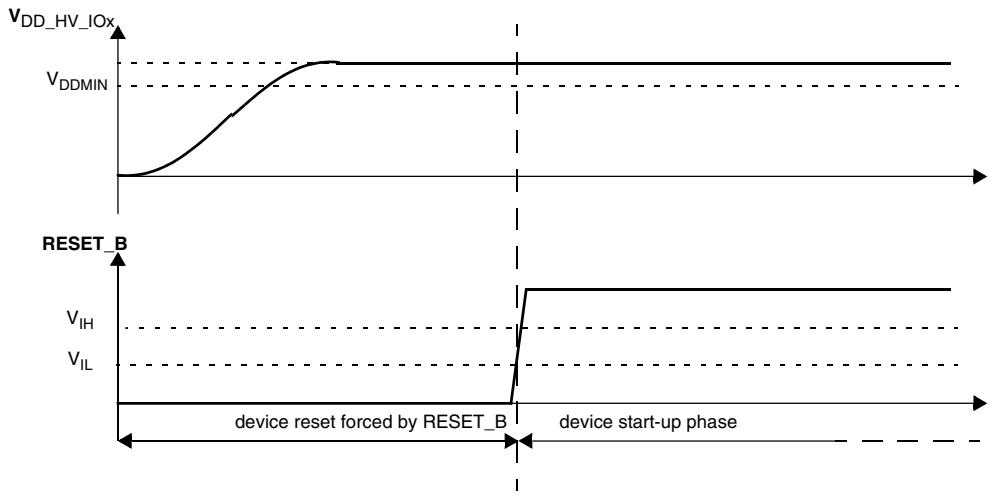



**Figure 5. Start-up reset requirements**

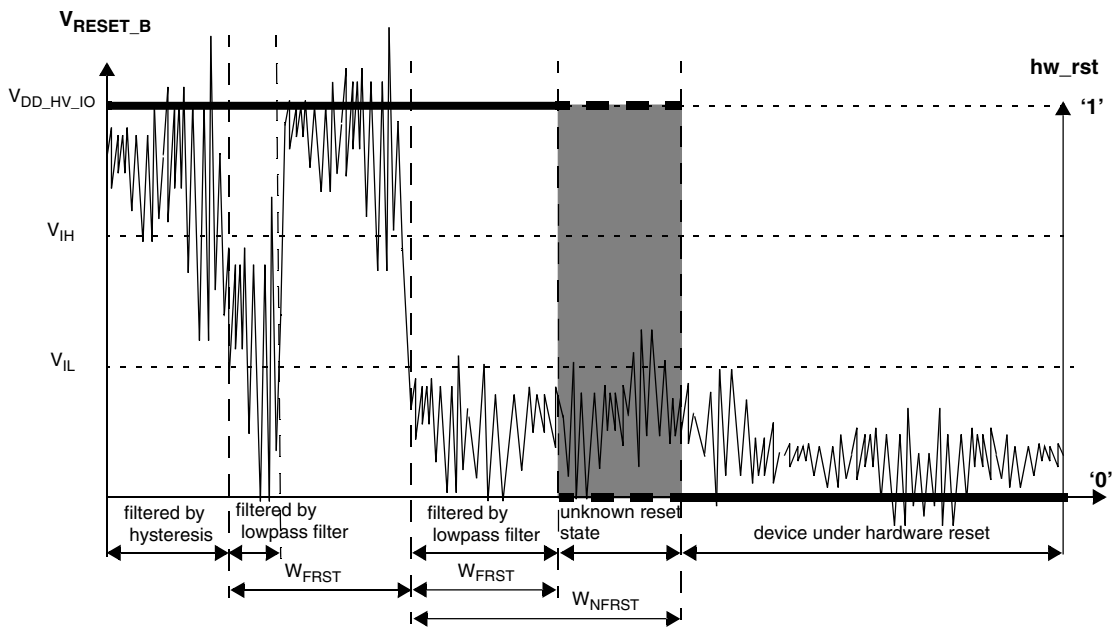



**Figure 6. Noise filtering on reset signal**

## Table 16. RESET_B electrical characteristics

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | Input high level TTL (Schmitt Trigger) | — | 2.0 | — | $V_{DD_HV_IOx}$ + 0.4 | V |
| $V_{IL}$ | Input low level TTL (Schmitt Trigger) | — | –0.4 | — | 0.56 | V |
| $V_{HYS}$[2] | Input hysteresis TTL (Schmitt Trigger) | — | 300 | — | — | mV |
| $I_{OL_R}$ | Strong pull-down current | Device under power-on reset<br>$V_{DD_HV_IO}$ = 1.2 V<br>$V_{OL}$ = 0.35 x $V_{DD_HV_IO}$ | 0.2 | — | — | mA |
| | | Device under power-on reset | 15 | — | — | mA |

*Table continues on the next page...*

**Table 16. RESET_B electrical characteristics (continued)**

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| | | $V_{DD_HV_IO}$=3.0 V<br>$V_{OL}$ = 0.35 x $V_{DD_HV_IO}$ | | | | |
| $W_{FRST}$ | RESET_B input filtered pulse | — | — | — | 500 | ns |
| $W_{NFRST}$ | RESET_B input not filtered pulse | — | 2400 | — | — | ns |
| $\|I_{WPD}\|$ | Weak pull-down current absolute value | $V_{IN}$ = $V_{DD_HV_IOx}$ | 30 | — | 100 | µA |

1. $V_{DD_HV_IOx}$ = 3.3 V -5%,+10%, $T_J$ = –40 / 150°C, unless otherwise specified.
2. Data based on characterization results, not tested in production.

# 6 Peripheral operating requirements and behaviors

## 6.1 Clocks and PLL Specifications

### 6.1.1 40 MHz Oscillator (XOSC) electrical characteristics

The device provides an oscillator/resonator driver.

**NOTE**

XTAL/EXTAL must not be directly used to drive external circuits.

**Table 17. XOSC electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $XOSC_{fout}$ | Oscillator frequency | | | 40 | | MHz |
| $t_{stab}$ | Oscillator start-up time | | | | 2 | ms |
| $t_{jitcc}$ | Cycle to cycle jitter (peak – peak) | | | | 2.5 | ps |
| | Output Duty Cycle | | 45 | 50 | 55 | % |
| Cin | Input Capacitance [1] | Extal and Xtal each | 3.0 | 4.0 | 5.0 | pF |
| $R_{inLVDS}$ | LVDS bypass mode input termination[2] | Between Extal and Xtal | 75 | 100 | 125 | ohm |
| $V_{CMLVDS}$ | LVDS Common Mode Voltage | Vdda/2 | 0.60 | 0.70 | 0.80 | V |

1. When using a 40 MHz crystal, the recommended load capacitance is 8 pF. Need quiet ground connection on the board and external crystal/load capacitor placement as close to the Extal and Xtal pins as possible to allow good jitter performance.

2. The Termination resistance is only active when the AFE is powered (VDD_HV_RAW, VDD_HV_DAC and the AFE regulators are powered up) and the XOSC is powered down (default case once device is out of reset) or the XOSC is configured in differential bypass mode.

## 6.1.2 FMPLL electrical characteristics

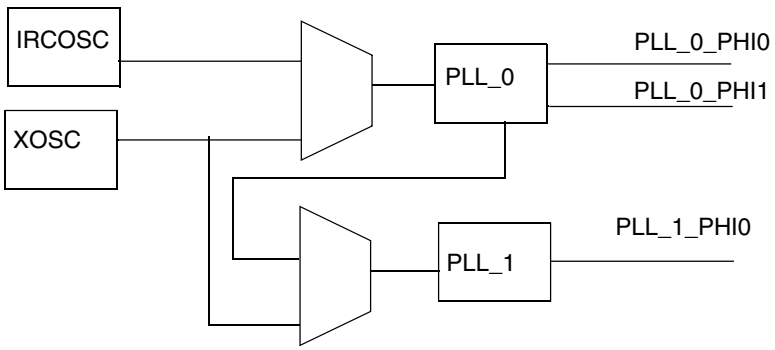



**Figure 7. PLL integration**

**Table 18. PLL0 electrical characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL0IN}$ | PLL0 input clock[2, 3] | — | 14 | — | 44 | MHz |
| $\Delta_{PLL0IN}$ | PLL0 input clock duty cycle[2] | — | 40 | — | 60 | % |
| $f_{PLL0VCO}$ | PLL0 VCO frequency | — | 600 | — | 1250 | MHz |
| $f_{PLL0PHI0}$ | PLL0 output clock PHI0 | — | 4.76 | — | 625[4] | MHz |
| $f_{PLL0PHI1}$ | PLL0 output clock PHI1 | — | 20 | — | 156 | MHz |
| $t_{PLL0LOCK}$ | PLL0 lock time | — | — | — | 100 | µs |
| $\Delta_{PLL0LTJ}$ | PLL0 long term jitter $f_{PLL0IN}$ = 8 MHz (resonator)[5] | $f_{PLL0PHI0}$ = 40 MHz, 1 µs | | | ± 1 | ns |
| | | $f_{PLL0PHI0}$ = 40 MHz, 13 µs | | | ± 1 | ns |
| $I_{PLL0}$ | PLL0 consumption | | — | — | 5 | mA |

1. $V_{DD_LV_PLL0}$ =1.25 V ± 5%, $T_J$ = -40 / 150 °C unless otherwise specified.
2. PLL0IN clock retrieved directly from either IRCOSC or external XOSC clock.
3. $f_{PLL0IN}$ frequency must be scaled down using PLLDIG_PLL0DV[PREDIV] to ensure the reference clock to the PLL analog loop is in the range 8 MHz-20 MHz
4. The maximum clock outputs are limited by the design clock frequency requirements as per recommended operating conditions.
5. $V_{DD_LV_PLL0}$ noise due to application in the range $V_{DD_LV_PLL0}$ = 1.25 V±5%, with frequency below PLL bandwidth (40 KHz) will be filtered.

**Table 19. FMPLL1 electrical characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PLL1IN}$ | PLL1 input clock[2] | — | 38 | — | 78 | MHz |
| $\Delta_{PLL1IN}$ | PLL1 input clock duty cycle[2] | — | 35 | — | 65 | % |
| $f_{PLL1VCO}$ | PLL1 VCO frequency | — | 600 | — | 1250 | MHz |
| $f_{PLL1PHI0}$ | PLL1 output clock PHI0 | — | 4.76 | — | 625 | MHz |

*Table continues on the next page...*

**Table 19. FMPLL1 electrical characteristics (continued)**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PLL1LOCK}$ | PLL1 lock time | — | — | — | 100 | µs |
| $f_{PLL1MOD}$ | PLL1 modulation frequency | — | — | — | 250 | kHz |
| $\|\delta_{PLL1MOD}\|$ | PLL1 modulation depth (when enabled) | Center spread | 0.25 | — | 2 | % |
| | | Down spread | 0.5 | — | 4 | % |
| $I_{PLL1}$ | PLL1 consumption | | — | — | 6 | mA |

1. $V_{DD_LV_PLL0}$ = 1.25 V ± 5%, $T_J$ = -40 / 150°C unless otherwise specified.
2. PLL1IN clock retrieved directly from either internal PLL0 or external XOSC clock.

## 6.1.3 16 MHz Internal RC Oscillator (IRCOSC) electrical specifications

**Table 20. Internal RC Oscillator electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{Target}$ | IRC target frequency | — | — | 16 | — | MHz |
| $F_{untrimmed}$ | IRC frequency (untrimmed) | — | 9.6 | — | 24 | MHz |
| $\delta F_{var}$ | IRC trimmed frequency variation[1] | — | -8 | — | 8 | % |
| $T_{startup}$ | Startup time | | — | — | 5 | µs |

1. The typical user trim step size (δfTRIM) is +48 KHz for frequencies trimmed above nominal and -40 KHz for frequencies trimmed below nominal.

## 6.1.4 320 MHz low-jitter PLL electrical characteristics

**Table 21. 320 MHz low-jitter PLL parameters**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $PLL_{fout}$ | Output Frequency | | — | 320 | — | MHz |
| $PLL_{fin}$ | Input Frequency | | — | — | 40 | MHz |
| $t_{cal}$ | Calibration Time [1] | LW64 = 1 | — | — | 150 | µs |
| | | LW64 = 0 | | | 500 | |
| $t_{lock}$ | Lock Time | after calibration | — | — | 75 | µs |
| $t_{jitcck}$ | Cycle to cycle jitter (peak – peak) | — | — | — | 10 | ps |
| — | Output duty cycle | — | 48 | 50 | 52 | % |

1. The LW64 bit sets the wait time before the PLL frequency is measured after each calibration step to allow for stabilization. If LW64 is '0', wait time of 256 reference clock cycles is used. If LW64 is'1', wait time of 64 reference clock cycles is used.

# 7 Analog

## 7.1 ADC electrical characteristics

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

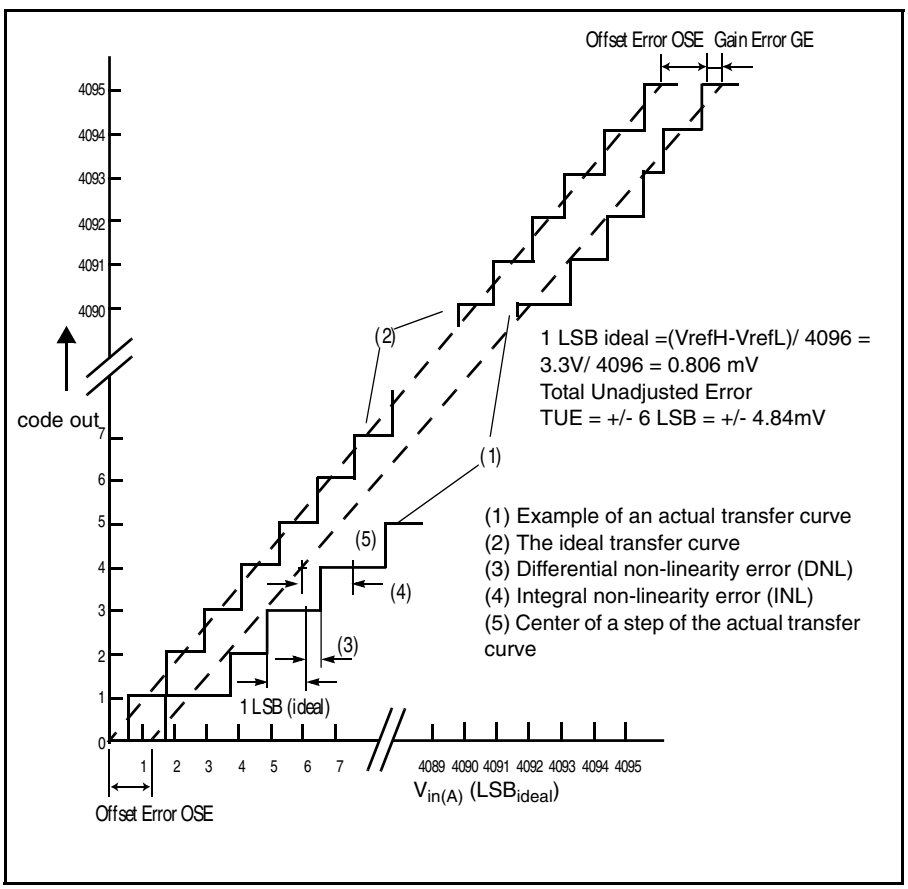



**Figure 8. ADC characteristics and error definitions**

## 7.1.1 Input equivalent circuit

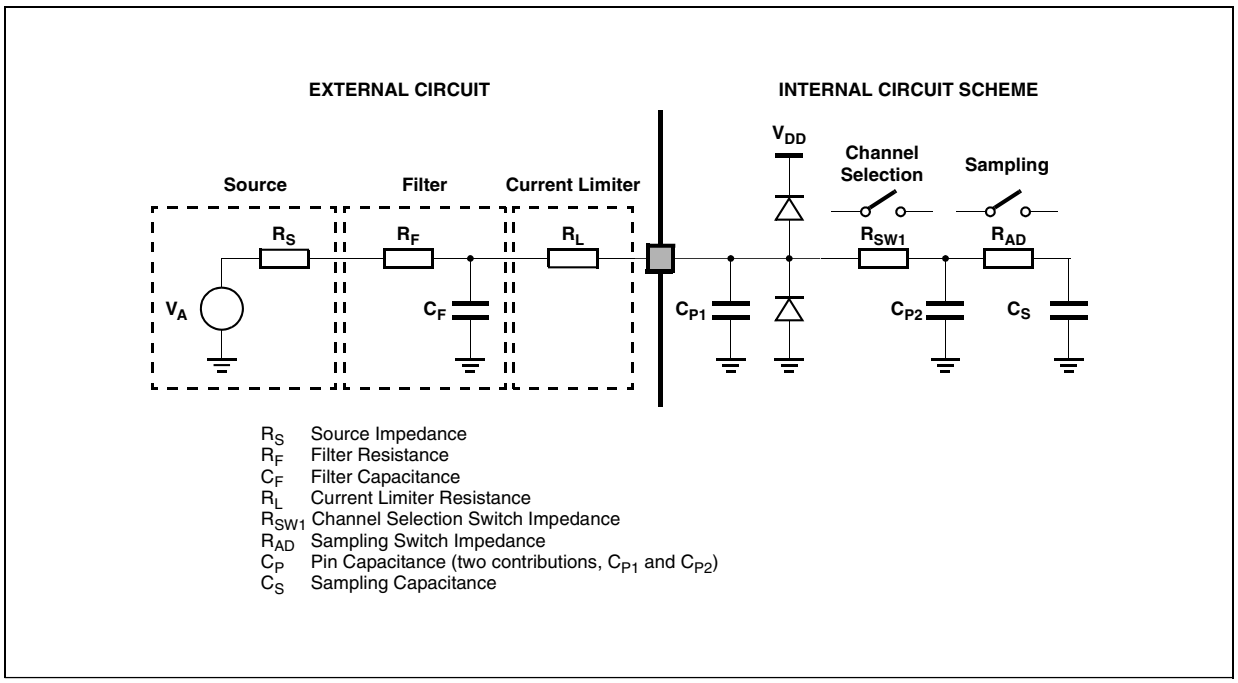



**Figure 9. Input equivalent circuit**

**Table 22. ADC conversion characteristics**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | ADC Clock frequency (depends on ADC configuration) (The duty cycle depends on AD_CK[2] frequency.) | — | 20 | 80 | 80 | MHz |
| $f_s$ | Sampling frequency | — | — | — | 1.00 | MHz |
| $t_{sample}$ | Sample time[3] | 80 MHz@ 200 ohm source impedance | 250 | — | — | ns |
| $t_{sampleC}$ | SAR selftest C-algorithm sample time | — | 300 | — | — | ns |
| $T_{sampleS}$ | SAR selftest S-algorithm sample time | — | 1 | — | — | µs |
| $T_{sampleBG}$ | Bandgap sample time | — | 1.87 | — | — | µs |
| $T_{sampleTS}$ | Temperature sensor sample time | — | 3.18 | — | — | µs |
| $t_{conv}$ | Conversion time[4] | 80 MHz | 675 | — | — | ns |
| $C_{S'}$ [5] | ADC input sampling capacitance | — | — | 3 | 5 | pF |
| $C_{P1}$[5] | ADC input pin capacitance 1 | — | — | — | 5 | pF |
| $C_{P2}$[5] | ADC input pin capacitance 2 | — | — | — | 0.8 | pF |
| $R_{SW1}$[5] | Internal resistance of analog source | $V_{REF}$ range = 3.0 to 3.6 V | — | — | 875 | Ω |
| $R_{AD}$[5] | Internal resistance of analog source | — | — | — | 825 | Ω |
| INL | Integral non-linearity | — | –2 | — | 2 | LSB |
| DNL | Differential non-linearity[6] | — | –1 | — | 1 | LSB |
| OFS | Offset error | — | –4 | — | 4 | LSB |
| GNE | Gain error | — | –4 | — | 4 | LSB |

*Table continues on the next page...*

**Table 22. ADC conversion characteristics (continued)**

| Symbol | Parameter | Conditions[1] | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $TUE_{IS1WINJ}$ | Total unadjusted error for IS1WINJ | | –6 | — | 6 | LSB |
| $TUE_{IS1WWINJ}$ | Total unadjusted error for IS1WWINJ | | –6 | — | 6 | LSB |
| IS1WINJ (pad going to one ADC) | (single ADC channel) | | | | | |
| | Max leakage | 150 °C | — | — | 250 | nA |
| | Max positive/negative injection | | –3 | — | 3[8] | mA |
| IS1WWINJ (pad going to two ADCs) | (double ADC channel) | | | | | |
| | Max leakage | 150 °C | — | — | 300 | nA |
| | Max positive/negative injection [7] | \|Vref_ad0 - Vref_ad1\| < 150 mV | –3.6 | — | 3.6 | mA |
| SNR | Signal-to-noise ratio | 3.3 V reference voltage | 67 | — | — | dB |
| THD | Total harmonic distortion | @ 50 KHz | 65 | — | — | dB |
| SINAD | Signal-to-noise and distortion | Fin < 50 KHz | 6.02 x ENOB + 1.76 | | | dB |
| ENOB | Effective number of bits | Fin < 50 KHz | 10.5 | — | — | bits |

1. $V_{DD_HV_ADC}$ = 3.3 V -5%,+10%, $T_J$ = –40 to +150°C, unless otherwise specified and analog input voltage from $V_{AGND}$ to $V_{DD_HV_ADCREFx}$.
2. AD_CK clock is always half of the ADC module input clock defined via the auxiliary clock divider for the ADC.
3. During the sample time the input capacitance $C_S$ can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within $t_{sample}$. After the end of the sample time $t_{sample}$, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock $t_{sample}$ depend on programming.
4. This parameter does not include the sample time $t_{sample}$, but only the time for determining the digital result and the time to load the result register with the conversion result.
5. See Figure 9
6. No missing codes.
7. ADC specifications are met only if injection is within these specified limits
8. Max injection current for all ADC IOs is ± 10 mA

**NOTE**

The ADC performance specifications are not guaranteed if two ADCs simultaneously sample the same shared channel. Aurora interface along with SAR-ADC would degrade SAR-ADC performance. General Purpose Input (GPI) functionality should not be used on any of the SAR-ADC channels when SARADC is functional.

# 8 Memory modules

## 8.1 Flash memory program and erase specifications

**NOTE**

All timing, voltage, and current numbers specified in this section are defined for a single embedded flash memory within

an SoC, and represent average currents for given supplies and operations.

Table 23 shows the estimated Program/Erase times.

**Table 23. Flash memory program and erase specifications**

| Symbol | Characteristic[1] | Typ[2] | Factory Programming[3, 4] | | Field Update | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Initial Max | Initial Max, Full Temp | Typical End of Life[5] | Lifetime Max[6] | | |
| | | | 20°C ≤$T_A$ ≤30°C | -40°C ≤$T_J$ ≤150°C | -40°C ≤$T_J$ ≤150°C | ≤ 1,000 cycles | ≤ 250,000 cycles | |
| $t_{dwpgm}$ | Doubleword (64 bits) program time | 43 | 100 | 150 | 55 | 500 | | µs |
| $t_{ppgm}$ | Page (256 bits) program time | 73 | 200 | 300 | 108 | 500 | | µs |
| $t_{qppgm}$ | Quad-page (1024 bits) program time | 268 | 800 | 1,200 | 396 | 2,000 | | µs |
| $t_{16kers}$ | 16 KB Block erase time | 168 | 290 | 320 | 250 | 1,000 | | ms |
| $t_{16kpgm}$ | 16 KB Block program time | 34 | 45 | 50 | 40 | 1,000 | | ms |
| $t_{32kers}$ | 32 KB Block erase time | 217 | 360 | 390 | 310 | 1,200 | | ms |
| $t_{32kpgm}$ | 32 KB Block program time | 69 | 100 | 110 | 90 | 1,200 | | ms |
| $t_{64kers}$ | 64 KB Block erase time | 315 | 490 | 590 | 420 | 1,600 | | ms |
| $t_{64kpgm}$ | 64 KB Block program time | 138 | 180 | 210 | 170 | 1,600 | | ms |
| $t_{256kers}$ | 256 KB Block erase time | 884 | 1,520 | 2,030 | 1,080 | 4,000 | — | ms |
| $t_{256kpgm}$ | 256 KB Block program time | 552 | 720 | 880 | 650 | 4,000 | — | ms |

1. Program times are actual hardware programming times and do not include software overhead. Block program times assume quad-page programming.
2. Typical program and erase times represent the median performance and assume nominal supply values and operation at 25 °C. Typical program and erase times may be used for throughput calculations.
3. Conditions: ≤ 150 cycles, nominal voltage.
4. Plant Programing times provide guidance for timeout limits used in the factory.
5. Typical End of Life program and erase times represent the median performance and assume nominal supply values. Typical End of Life program and erase values may be used for throughput calculations.
6. Conditions: -40°C ≤ $T_J$ ≤ 150°C, full spec voltage.

## 8.2 Flash memory Array Integrity and Margin Read specifications

**Table 24. Flash memory Array Integrity and Margin Read specifications**

| Symbol | Characteristic | Min | Typical | Max[1] | Units[2] |
|---|---|---|---|---|---|
| $t_{ai16kseq}$ | Array Integrity time for sequential sequence on 16 KB block. | — | — | 512 x Tperiod x Nread | — |

*Table continues on the next page...*

**Table 24. Flash memory Array Integrity and Margin Read specifications (continued)**

| Symbol | Characteristic | Min | Typical | Max[1] | Units[2] |
|---|---|---|---|---|---|
| $t_{ai32kseq}$ | Array Integrity time for sequential sequence on 32 KB block. | — | — | 1024 x Tperiod x Nread | — |
| $t_{ai64kseq}$ | Array Integrity time for sequential sequence on 64 KB block. | — | — | 2048 x Tperiod x Nread | — |
| tai256kseq | Array Integrity time for sequential sequence on 256 KB block. | — | — | 8192 x Tperiod x Nread | — |
| $t_{mr16kseq}$ | Margin Read time for sequential sequence on 16 KB block. | 73.81 | — | 110.7 | µs |
| $t_{mr32kseq}$ | Margin Read time for sequential sequence on 32 KB block. | 128.43 | — | 192.6 | µs |
| $t_{mr64kseq}$ | Margin Read time for sequential sequence on 64 KB block. | 237.65 | — | 356.5 | µs |
| $t_{mr256kseq}$ | Margin Read time for sequential sequence on 256 KB block. | 893.01 | — | 1,339.5 | µs |

1. Array Integrity times need to be calculated and is dependent on system frequency and number of clocks per read. The equation presented require Tperiod (which is the unit accurate period, thus for 200 MHz, Tperiod would equal 5e-9) and Nread (which is the number of clocks required for read, including pipeline contribution. Thus for a read setup that requires 6 clocks to read with no pipeline, Nread would equal 6. For a read setup that requires 6 clocks to read, and has the address pipeline set to 2, Nread would equal 4 (or 6 - 2).)
2. The units for Array Integrity are determined by the period of the system clock. If unit accurate period is used in the equation, the results of the equation are also unit accurate.

## 8.3 Flash memory module life specifications

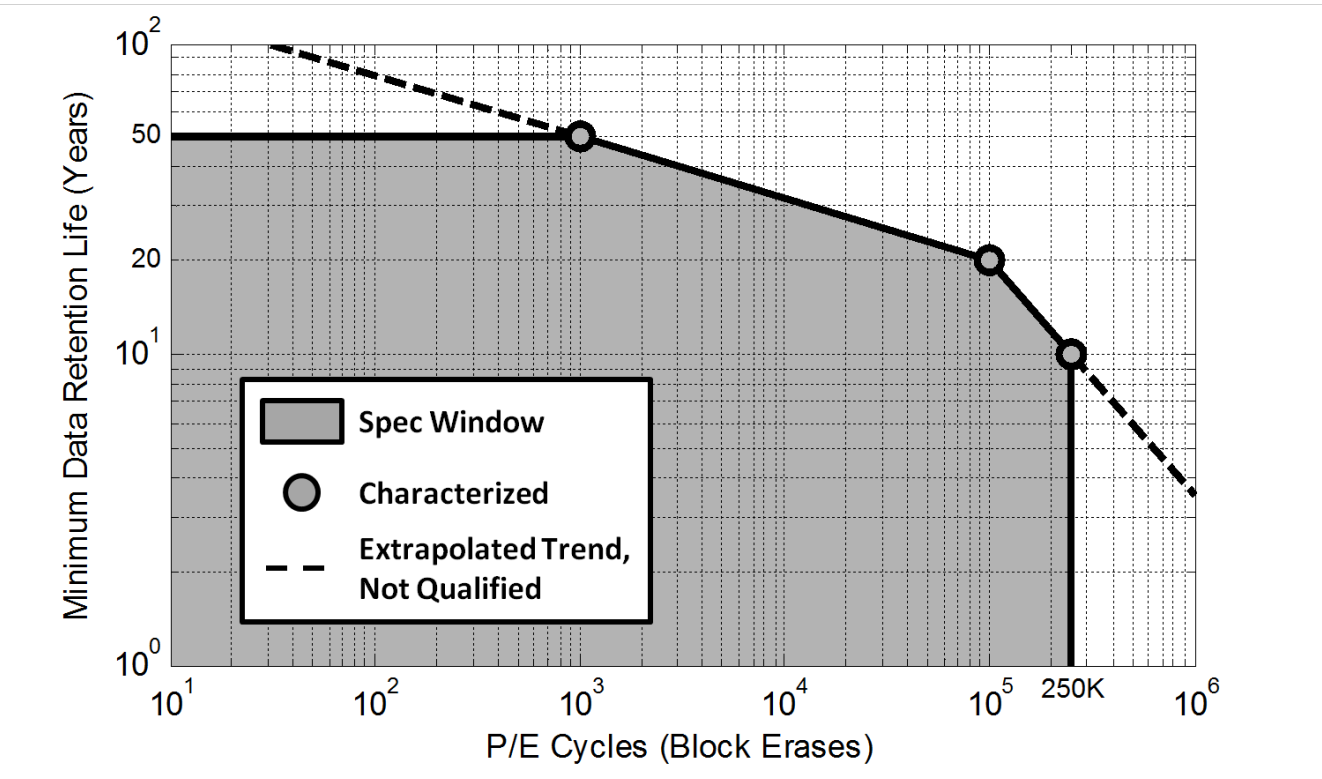
**Table 25. Flash memory module life specifications**

| Symbol | Characteristic | Conditions | Min | Typical | Units |
|---|---|---|---|---|---|
| Array P/E cycles | Number of program/erase cycles per block for 16 KB, 32 KB and 64 KB blocks.[1] | — | 250,000 | — | P/E cycles |
| | Number of program/erase cycles per block for 256 KB blocks.[2] | — | 1,000 | 250,000 | P/E cycles |
| Data retention | Minimum data retention. | Blocks with 0 - 1,000 P/E cycles. | 50 | — | Years |
| | | Blocks with 100,000 P/E cycles. | 20 | — | Years |
| | | Blocks with 250,000 P/E cycles. | 10 | — | Years |

1. Program and erase supported across standard temperature specs.
2. Program and erase supported across standard temperature specs.

## 8.4 Data retention vs program/erase cycles

Graphically, Data Retention versus Program/Erase Cycles can be represented by the following figure. The spec window represents qualified limits. The extrapolated dotted line demonstrates technology capability, however is beyond the qualification limits.




## 8.5 Flash memory AC timing specifications

**Table 26. Flash memory AC timing specifications**

| Symbol | Characteristic | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| $t_{psus}$ | Time from setting the MCR-PSUS bit until MCR-DONE bit is set to a 1. | — | 9.4<br>plus four system clock periods | 11.5<br>plus four system clock periods | µs |
| $t_{esus}$ | Time from setting the MCR-ESUS bit until MCR-DONE bit is set to a 1. | — | 16<br>plus four system clock periods | 20.8<br>plus four system clock periods | µs |

*Table continues on the next page...*

**Table 26. Flash memory AC timing specifications (continued)**

| Symbol | Characteristic | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| $t_{res}$ | Time from clearing the MCR-ESUS or PSUS bit with EHV = 1 until DONE goes low. | — | — | 100 | ns |
| $t_{done}$ | Time from 0 to 1 transition on the MCR-EHV bit initiating a program/erase until the MCR-DONE bit is cleared. | — | — | 5 | ns |
| $t_{dones}$ | Time from 1 to 0 transition on the MCR-EHV bit aborting a program/erase until the MCR-DONE bit is set to a 1. | — | 16 plus four system clock periods | 20.8 plus four system clock periods | µs |
| $t_{drcv}$ | Time to recover once exiting low power mode. | 16 plus seven system clock periods. | — | 45 plus seven system clock periods | µs |
| $t_{aistart}$ | Time from 0 to 1 transition of UT0-AIE initiating a Margin Read or Array Integrity until the UT0-AID bit is cleared. This time also applies to the resuming from a suspend or breakpoint by clearing AISUS or clearing NAIBP | — | — | 5 | ns |
| $t_{aistop}$ | Time from 1 to 0 transition of UT0-AIE initiating an Array Integrity abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Array Integrity suspend request. | — | — | 80 plus fifteen system clock periods | ns |
| $t_{mrstop}$ | Time from 1 to 0 transition of UT0-AIE initiating a Margin Read abort until the UT0-AID bit is set. This time also applies to the UT0-AISUS to UT0-AID setting in the event of a Margin Read suspend request. | 10.36 plus four system clock periods | — | 20.42 plus four system clock periods | µs |

## 8.6 Flash memory read wait-state and address-pipeline control settings

The following table describes the recommended settings of the Flash Memory Controller's PFCR1,2,3[RWSC] and PCRC1,2,3[APC] fields at various operating frequencies, based on specified intrinsic flash memory access timed of the Flash memory.

**Table 27. Flash read wait state and address pipeline control guidelines**

| Operating frequency (fsys) | RWSC | APC | Flash read latency on mini-cache miss (# of sys clock periods) | Flash read latency on mini-cache hit (# of sys clock periods) |
|---|---|---|---|---|
| 100 MHz | 2 | 1 | 5 | 1 |
| 120 MHz | 3 | 1 | 6 | 1 |

# 9 Communication modules

## 9.1 SPI timing specifications

The following table describes the SPI electrical characteristics.

MTEF=1 Mode timing values given below are only applicable when external SPI is in classic mode. Slave mode timing values given below are applicable when device is in MTFE=0.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured as SRE = 11.

**Table 28. SPI timing**

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{SCK}$ | SPI cycle time | Master (MTFE = 0) | 50 | — | ns |
| | | | Master (MTFE = 1) | 50 | — | |
| | | | Slave (MTFE = 0) | 50 | — | |
| | | | Slave Receive Only mode[1] | 16 | — | |
| 2 | $t_{CSC}$ | PCS to SCK delay | Master | 63.8[2] | — | ns |
| 3 | $t_{ASC}$ | After SCK delay | Master | 68.8[3] | — | ns |
| 4 | $t_{SDC}$ | SCK duty cycle | Master[4] | $t_{SCK}/2 - 1$ | $t_{SCK}/2 + 1$ | ns |
| | | | Slave[5] | — | — | ns |
| | | | Slave Receive only mode[6] | tSCK/2 – 0.750 | tSCK/2 + 0.750 | ns |
| 5 | $t_A$ | Slave access time | $\overline{SS}$ active to SOUT valid | — | 25 | ns |
| 6 | $t_{DIS}$ | Slave SOUT disable time | $\overline{SS}$ inactive to SOUT High-Z or invalid | — | 25 | ns |
| 7 | $t_{PCSC}$ | PCSx to $\overline{PCSS}$ time | — | 13[7] | — | ns |
| 8 | $t_{PASC}$ | $\overline{PCSS}$ to PCSx time | — | 13[8] | — | ns |
| 9 | $t_{SUI}$ | Data setup time for inputs | Master (MTFE = 0) | 15 | — | ns |
| | | | Slave | 2 | — | |
| | | | Slave Receive Mode | 2 | — | |
| | | | Master (MTFE = 1, CPHA = 0)[9] | 15-N x SPI IPG clock period[10] | — | |
| | | | Master (MTFE = 1, CPHA = 1) | 15 | — | |
| 10 | $t_{HI}$ | Data hold time for inputs | Master (MTFE = 0) | –2 | — | ns |
| | | | Slave | 4 | — | |
| | | | Slave Receive Mode | 4 | — | |
| | | | Master (MTFE = 1, CPHA = 0)[9] | -2 + N x SPI IPG clock period [10] | — | |

*Table continues on the next page...*

## Table 28. SPI timing (continued)

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| | | | Master (MTFE = 1, CPHA = 1) | –2 | — | |
| 11 | $t_{SUO}$ | Data valid (after SCK edge) | Master (MTFE = 0) | — | 7 [11] | ns |
| | | | Slave | — | 23 | |
| | | | Master (MTFE = 1, CPHA = 0)[12] | — | 7 + SPI IPG Clock Period | |
| | | | Master (MTFE = 1, CPHA = 1) | — | 7 | |
| 12 | $t_{HO}$ | Data hold time for outputs | Master (MTFE = 0) | –4 [11] | — | ns |
| | | | Slave | 3.8 | — | |
| | | | Master (MTFE = 1, CPHA = 0) [12] | -4 + SPI IPG Clock Period | — | |
| | | | Master (MTFE = 1, CPHA = 1) | –4 | — | |

1. Slave Receive Only mode can operate at a maximum frequency of 60 MHz. In this mode, the SPI can receive data on SIN, but no valid data is transmitted on SOUT.
2. For SPI_CTARn[PCSSCK] - 'PCS to SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[CSSCK] - 'PCS to SCK Delay Scaler' configuration is '2' (0000h).
3. For SPI_CTARn[PASC] - 'After SCK Delay Prescaler' configuration is '3' (01h) and SPI_CTARn[ASC] - 'After SCK Delay Scaler' configuration is '2' (0000h).
4. The numbers are valid when SPI is configured for 50/50 . Refer the Reference manual for the mapping of the duty cycle to each configuration. A change in duty cycle changes the parameter here. For example, a configuration providing duty cycle of 33/66 at SPI translates to min tSCK/3 - 1.5 ns and max tSCK/3 + 1.5 ns.
5. The slave mode parameters ($t_{SUI}$, $t_H$I, $t_{SUO}$ and $t_{HO}$) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing.
6. The slave receive only mode parameters ($t_{SUI}$ and $t_{HI}$) assume 50% duty cycle on SCK input. Any change in SCK duty cycle input must be taken care during the board design or by the master timing. However, there is additional restriction in the slave receive only mode that the duty cycle at the slave input should not go below $t_{sdc}$(min) corresponding to the $t_{sdc}$(min) for the slave receive mode.
7. In the master mode, this is governed by $t_{PCSSCK}$. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PCSSCK]= '0b01' (PCS to SCK delay prescalar of 3) or higher.
8. In the master mode, this is governed by $t_{PASC}$. Refer the SPI chapter in the Reference Manual for details. The minimum spec is valid only for SPI_CTARn[PASC]= '0b01' (after SCK delay prescalar of 3) or higher.
9. For SPI_CTARn[BR] - 'Baud Rate Scaler' configuration is >= 4.
10. N = Configured sampling point value in MTFE=1 Mode.
11. Same value is applicable for PCS timing in continuous SCK mode.
12. SMPL_PTR should be set to 1.

**NOTE**

For numbers shown in the following figures, see Table 28.

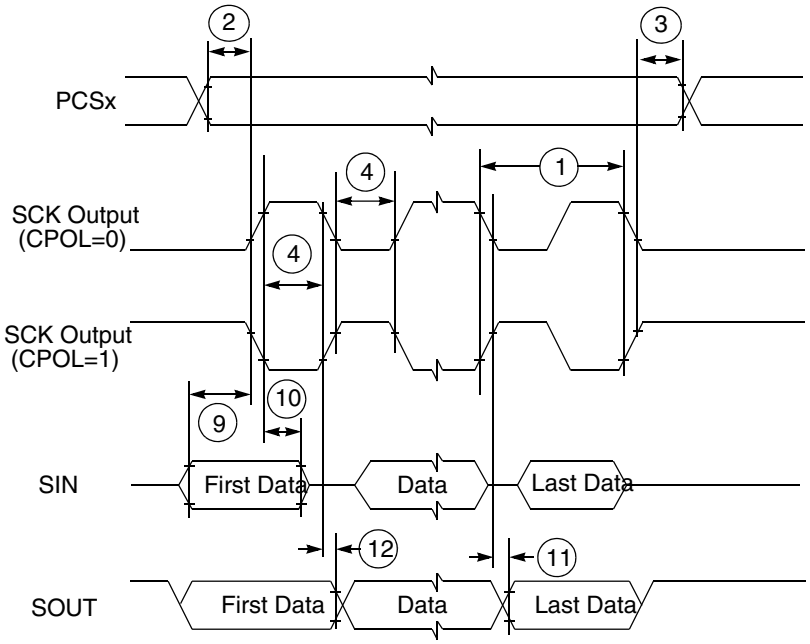



**Figure 10. SPI classic SPI timing — master, CPHA = 0**

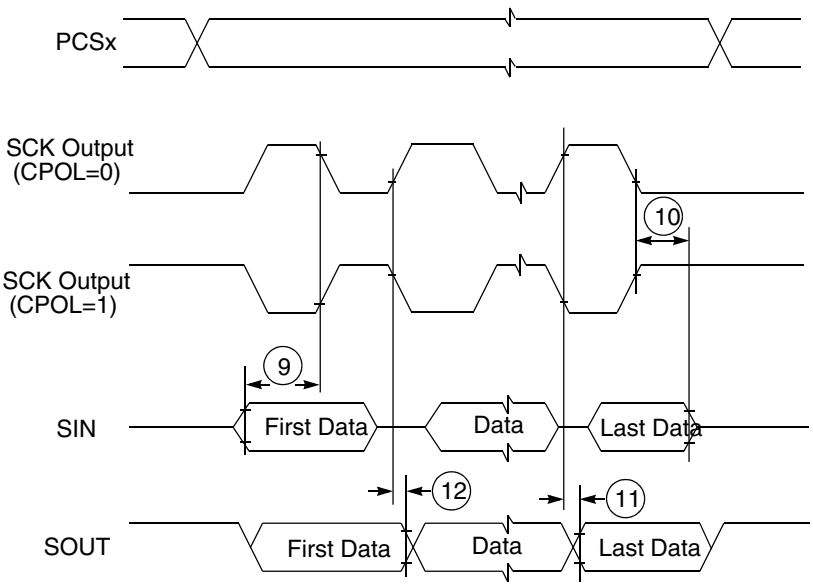



**Figure 11. SPI classic SPI timing — master, CPHA = 1**

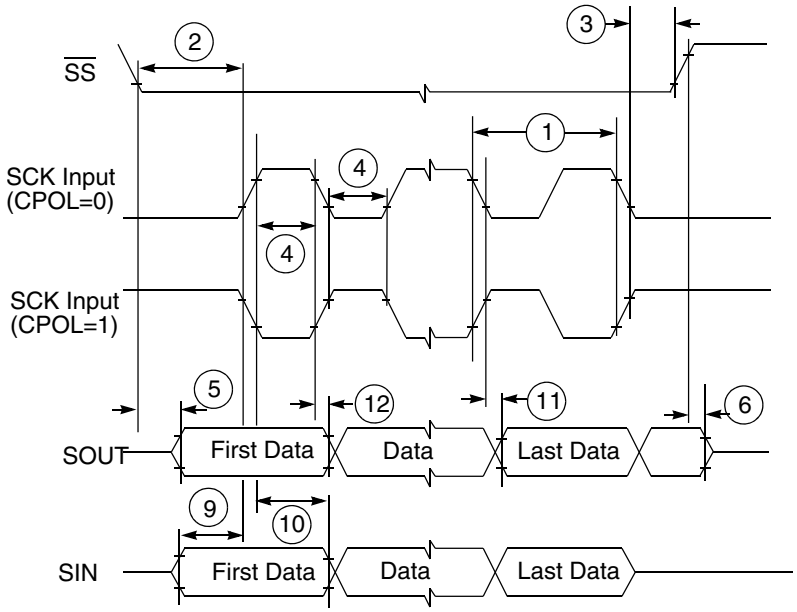



**Figure 12. SPI classic SPI timing — slave, CPHA = 0**

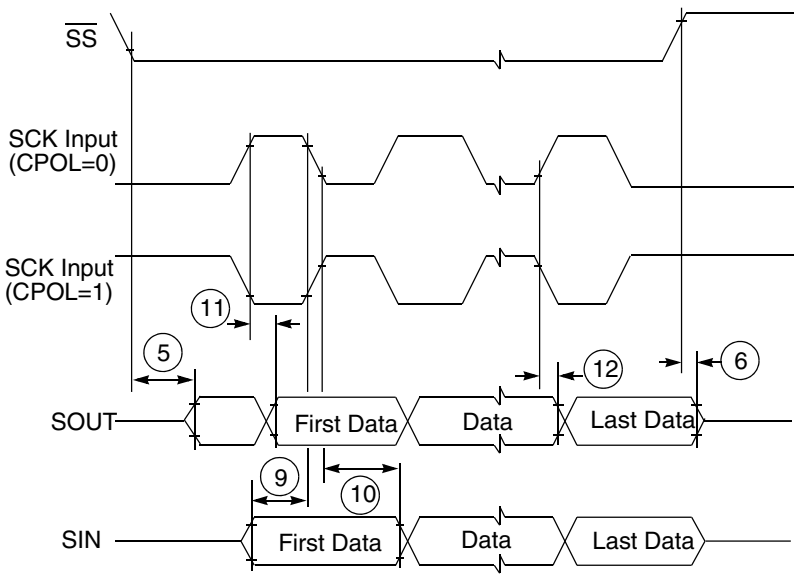



**Figure 13. SPI classic SPI timing — slave, CPHA = 1**

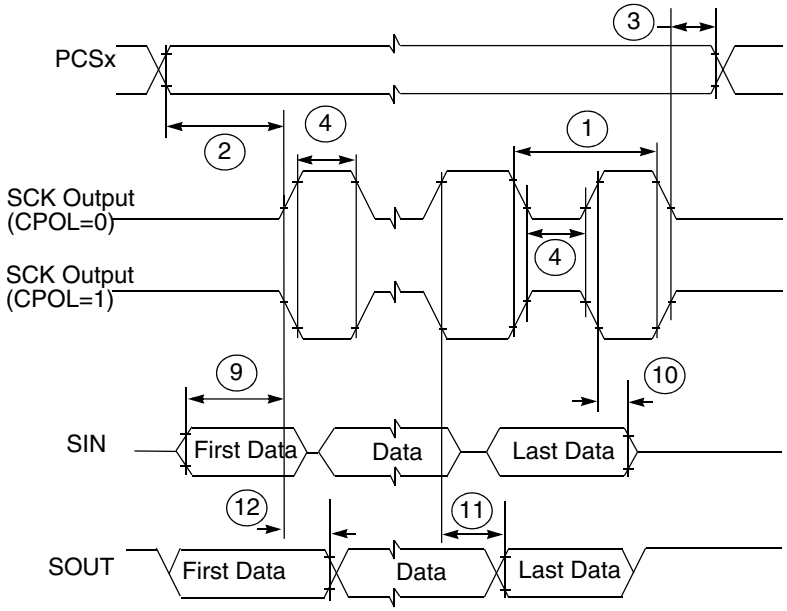



**Figure 14. SPI modified transfer format timing — master, CPHA = 0**

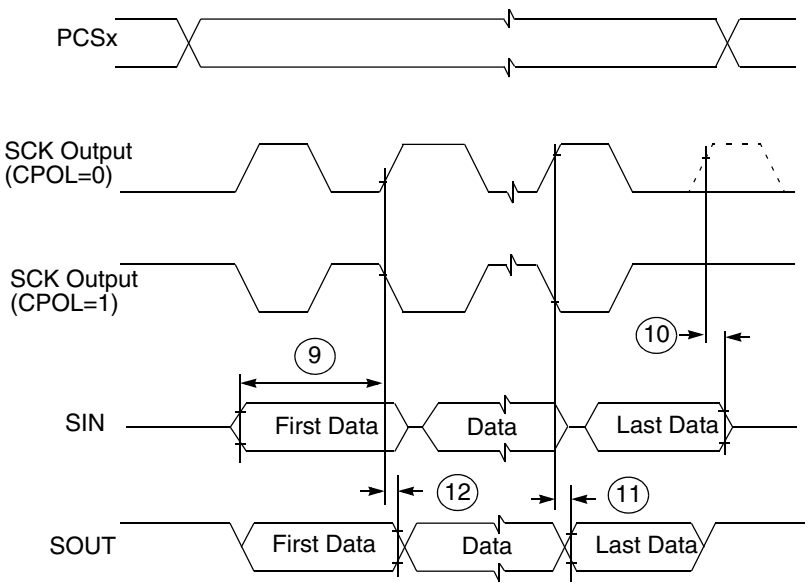



**Figure 15. SPI modified transfer format timing — master, CPHA = 1**

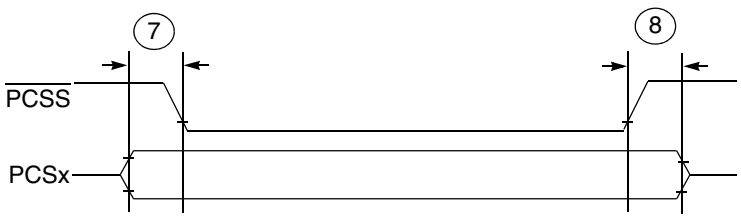



**Figure 16. SPI PCS strobe (PCSS) timing**

## 9.2 LINFlexD timing specifications

The maximum bit rate is 1.875 MBit/s.

## 9.3 I²C timing

**Table 29. I²C SCL and SDA input timing specifications**

| Number | Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | I_tHD:STA | Start Condition hold time | 2 | - | Peripheral clock |
| 2 | I_t_LOW | Clock low time | 8 | - | |
| 3 | I_tHD:DAT | Data hold time | 2 | - | |
| 4 | I_tHIGH | Clock high time | 4 | - | |
| 5 | I_tSU:DAT | Data setup time | 4 | - | |
| 6 | I_tSU:STA | Start condition setup time (for repeated start condition only) | 2 | - | |
| 7 | I_tSU:STOP | Stop condition setup time | 2 | - | |

**Table 30. I²C SCL and SDA output timing specifications**

| Number | Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| 1 | O_tHD:STA | Start condition hold time[1] | 6 | - | Peripheral clock |
| 2 | O_t_LOW | Clock low time[1] | 10 | - | |
| 3 | O_tHD:DAT | Data hold time[1] | 7 | - | |
| 4 | O_t_HIGH | Clock high time[1] | 10 | - | |
| 5 | O_tSU:DAT | Data setup time[1] | 2 | - | |
| 6 | O_tSU:STA | Start condition setup time (for repeated start condition only)[1] | 20 | - | |
| 7 | O_tSU:STOP | Stop condition setup time[1] | 10 | - | |
| 8 | O_tr | SCL/SDA rise time[2] | - | 99.6 | ns |
| 9 | O_tf | SCL/SDA fall time[1] | - | 99.6 | |

1. Programming IBFD (I²C Bus Frequency Divider Register) with the maximum frequency results in the minimum output timings listed. The I²C interface is designed to scale the data transition time, moving it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed in IBDR (I²C Bus Data I/O Register).
2. Serial data (SDA) and Serial clock (SCL) reaches peak level depending upon the external signal capacitance and pull up resistor values as SDA and SCL are open-drain type outputs which are only actively driven low by the I²C module.

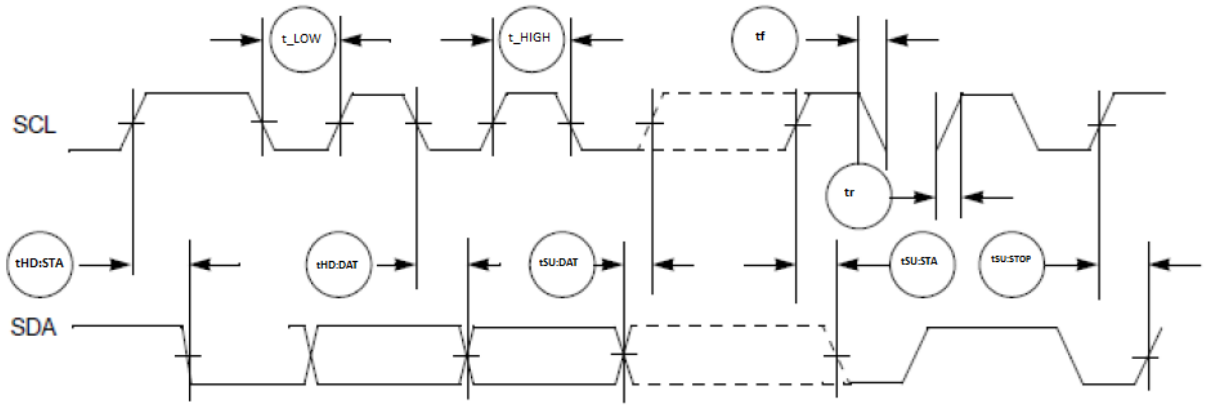



**Figure 17. I²C input/output timing**

# 10 Debug modules

## 10.1 JTAG/CJTAG interface timing

The following table lists JTAGC/CJTAG electrical characteristics.

- Measurements are with input transition of 1 ns, output load of 50 pF and pads configured with SRE=11.

**Table 31. JTAG/CJTAG pin AC electrical characteristics [1]**

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | $t_{JCYC}$ [2] | TCK Cycle Time (JTAG) | 36 | — | ns |
| | | TCK Cycle Time (CJTAG) | 50 | | |
| 2 | $t_{JDC}$ | TCK Clock Pulse Width | 40 | 60 | % |
| 3 | $t_{TCKRISE}$ | TCK Rise and Fall Times (40% - 70%) | — | 3 | ns |
| 4 | $t_{TMSS}$, $t_{TDIS}$ | TMS, TDI Data Setup Time | 5 | — | ns |
| 5 | $t_{TMSH}$, $t_{TDIH}$ | TMS, TDI Data Hold Time | 5 | — | ns |
| 6 | $t_{TDOV}$ | TCK Low to TDO/TMS Data Valid [3] | — | 15[4] | ns |
| 7 | $t_{TDOI}$ | TCK Low to TDO/TMS Data Invalid[3] | 0 | — | ns |
| 8 | $t_{TDOHZ}$ | TCK Low to TDO/TMS High Impedance[3] | — | 22 | ns |
| 9 | $t_{JCMPPW}$ | JCOMP Assertion Time | 100 | — | ns |
| 10 | $t_{JCMPS}$ | JCOMP Setup Time to TCK Low | 40 | — | ns |

*Table continues on the next page...*

## Table 31. JTAG/CJTAG pin AC electrical characteristics [1] (continued)

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 11 | $t_{BSDV}$ | TCK Falling Edge to Output Valid | — | 600[5] | ns |
| 12 | $t_{BSDVZ}$ | TCK Falling Edge to Output Valid out of High Impedance | — | 600 | ns |
| 13 | $t_{BSDHZ}$ | TCK Falling Edge to Output High Impedance | — | 600 | ns |
| 14 | $t_{BSDST}$ | Boundary Scan Input Valid to TCK Rising Edge | 15 | — | ns |
| 15 | $t_{BSDHT}$ | TCK Rising Edge to Boundary Scan Input Invalid | 15 | — | ns |

1. These specifications apply to JTAG boundary scan only.
2. This timing applies to TDI, TDO, TMS pins, however, actual frequency is limited by pad type for EXTEST instructions. Refer to pad specification for allowed transition frequency
3. TMS timing is applicable only in CJTAG mode
4. Timing includes TCK pad delay, clock tree delay, logic delay and TDO output pad delay.
5. Applies to all pins, limited by pad slew rate. Refer to IO delay and transition specification and add 20 ns for JTAG delay.

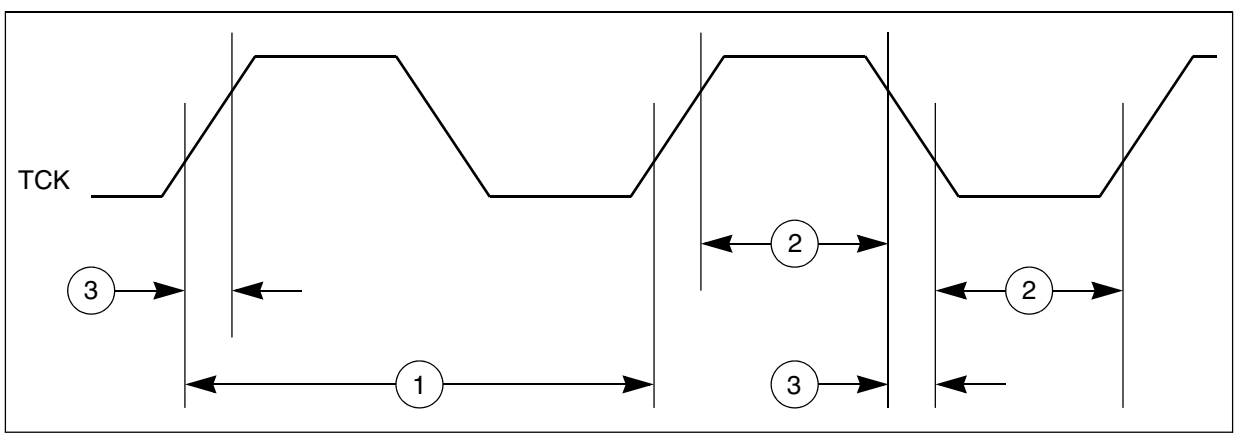



**Figure 18. JTAG test clock input timing**

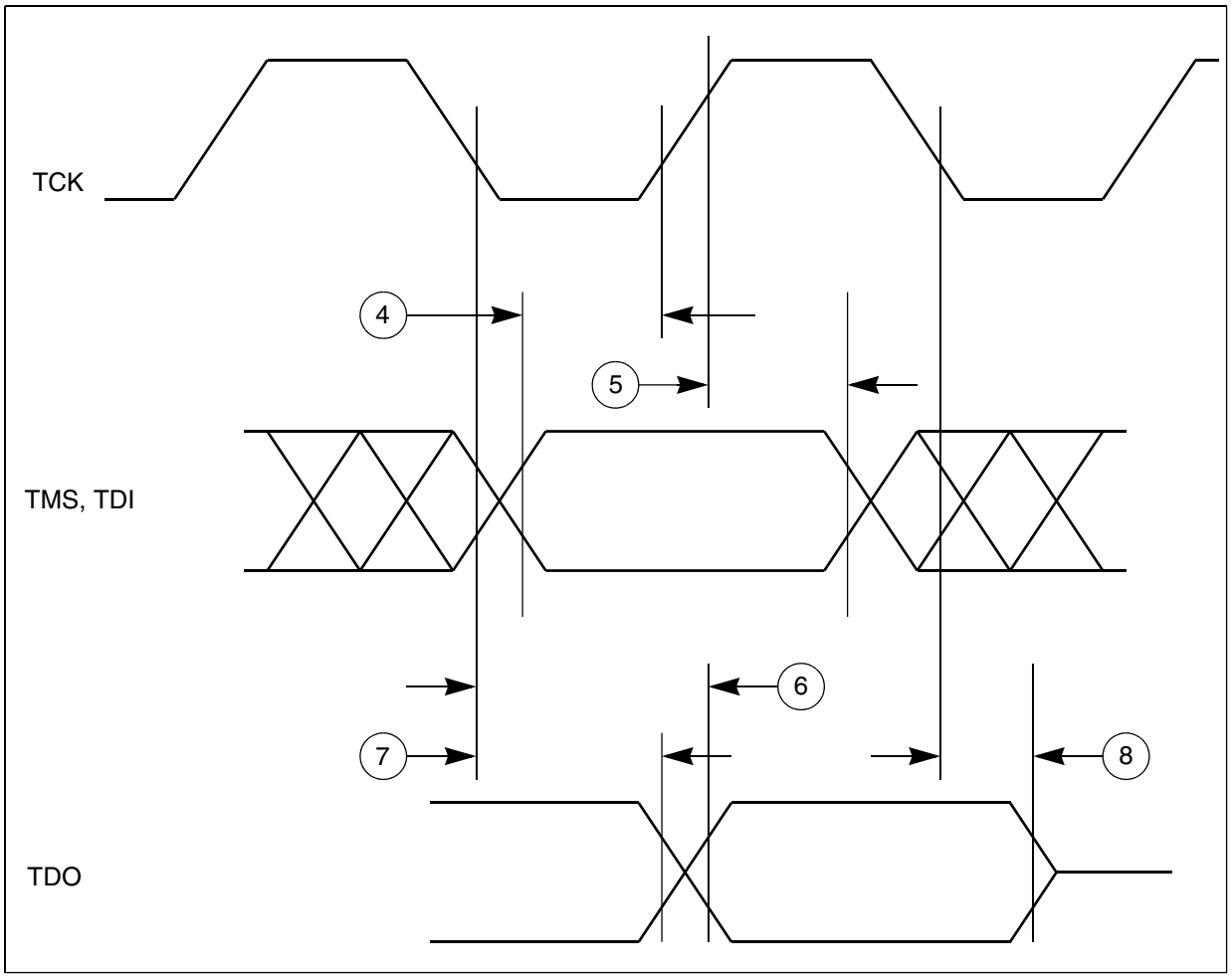



**Figure 19. JTAG test access port timing**

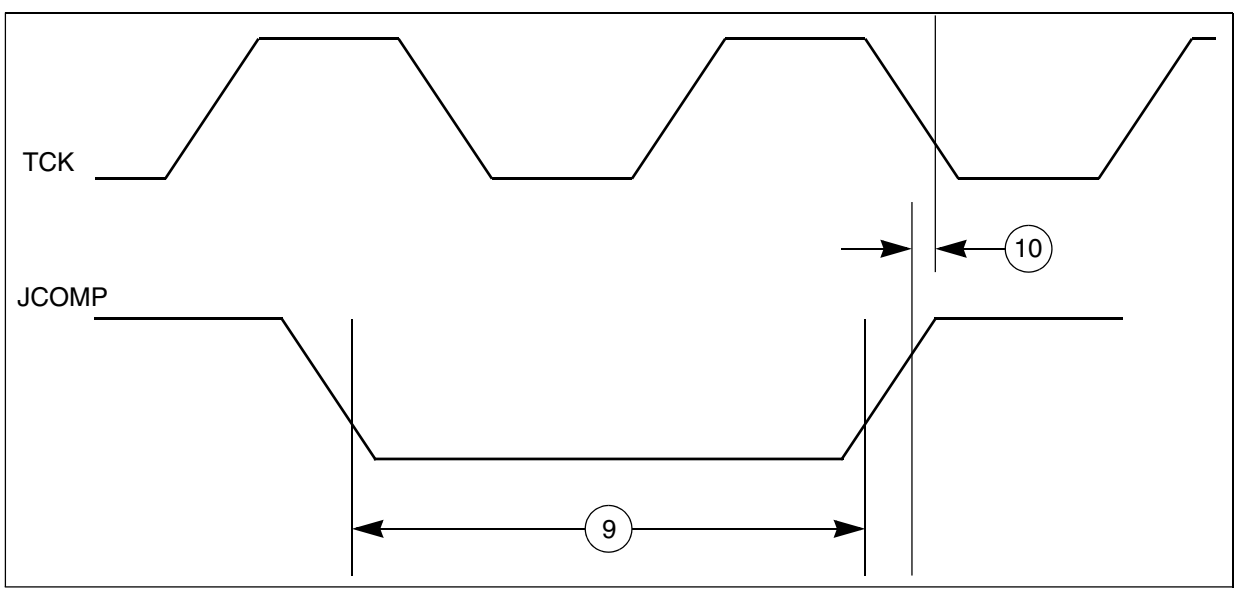



**Figure 20. JTAG JCOMP timing**

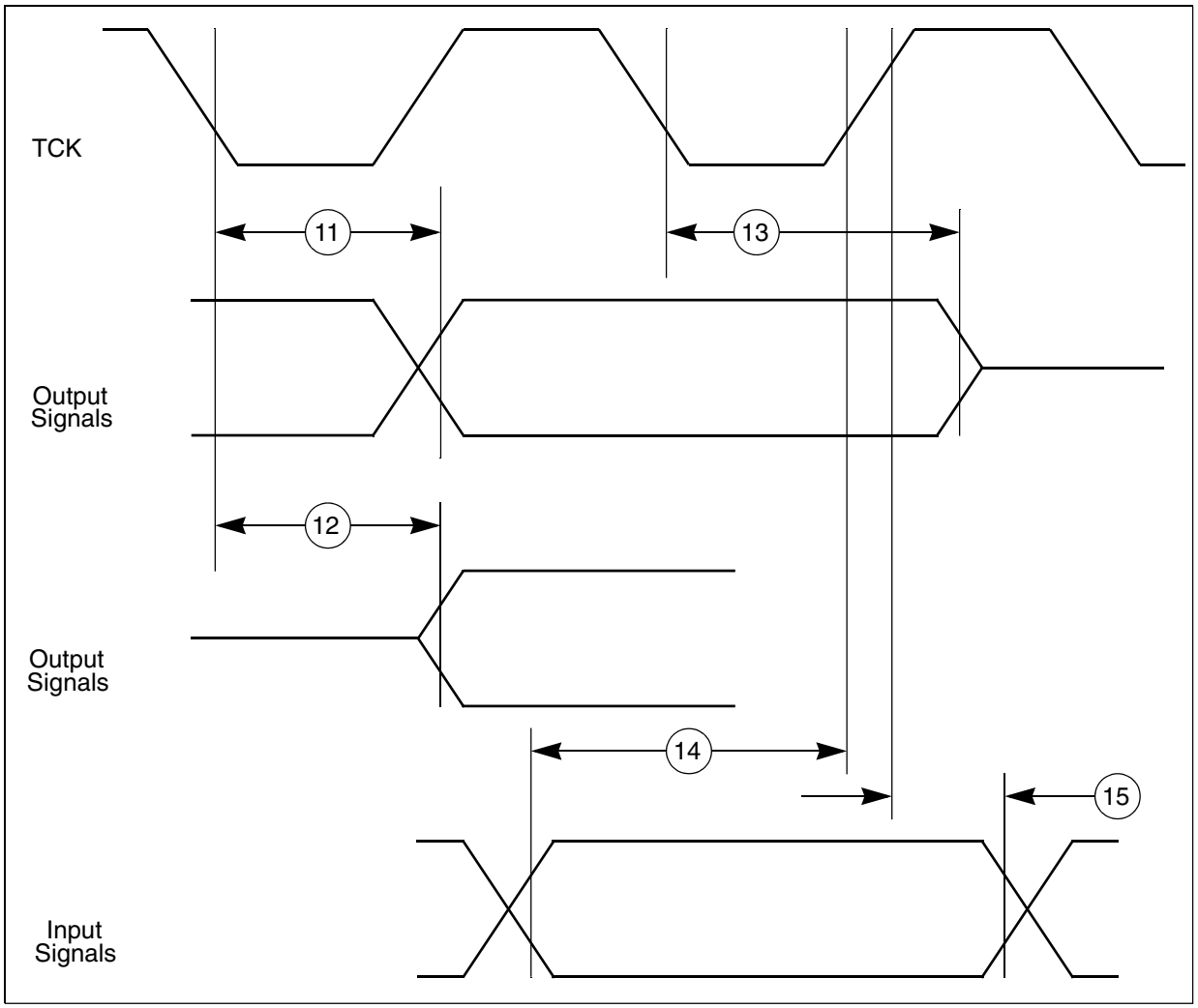



**Figure 21. JTAG boundary scan timing**

## 10.2 Nexus Aurora debug port timing

**Table 32. Nexus Aurora debug port timing**

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | $t_{REFCLK}$ | Reference clock frequency | 625 | 1250 | MHz |
| 1a | $t_{MCYC}$ | Reference Clock high/low time | — | 400 | ps |
| 2 | $t_{RCDC}$ | Reference Clock Duty Cycle | 45 | 55 | % |
| 3 | $J_{RC}$ | Reference Clock jitter | — | 40 | ps |
| 4 | $t_{STABILITY}$ | Reference Clock Stability | 50 | — | PPM |
| 5 | BER | Bit Error Rate | — | $10^{-12}$ | — |
| 6 | $t_{EVTIPW}$ | $\overline{\text{EVTI}}$ Pulse Width | 4.0 | — | $t_{TCYC}$ |
| 7 | $J_D$ | Transmit lane Deterministic Jitter | — | 0.17 | OUI |
| 8 | $J_T$ | Transmit lane Total Jitter | — | 0.35 | OUI |

*Table continues on the next page...*

**Table 32. Nexus Aurora debug port timing (continued)**

| # | Symbol | Characteristic | Min | Max | Unit |
|---|---|---|---|---|---|
| 9 | $S_O$ | Differential output skew | — | 20 | ps |
| 10 | $S_{MO}$ | Lane to lane output skew | — | 1000 | ps |
| 11 | OUI | Aurora lane Unit Interval | 800 | 800 | ps |

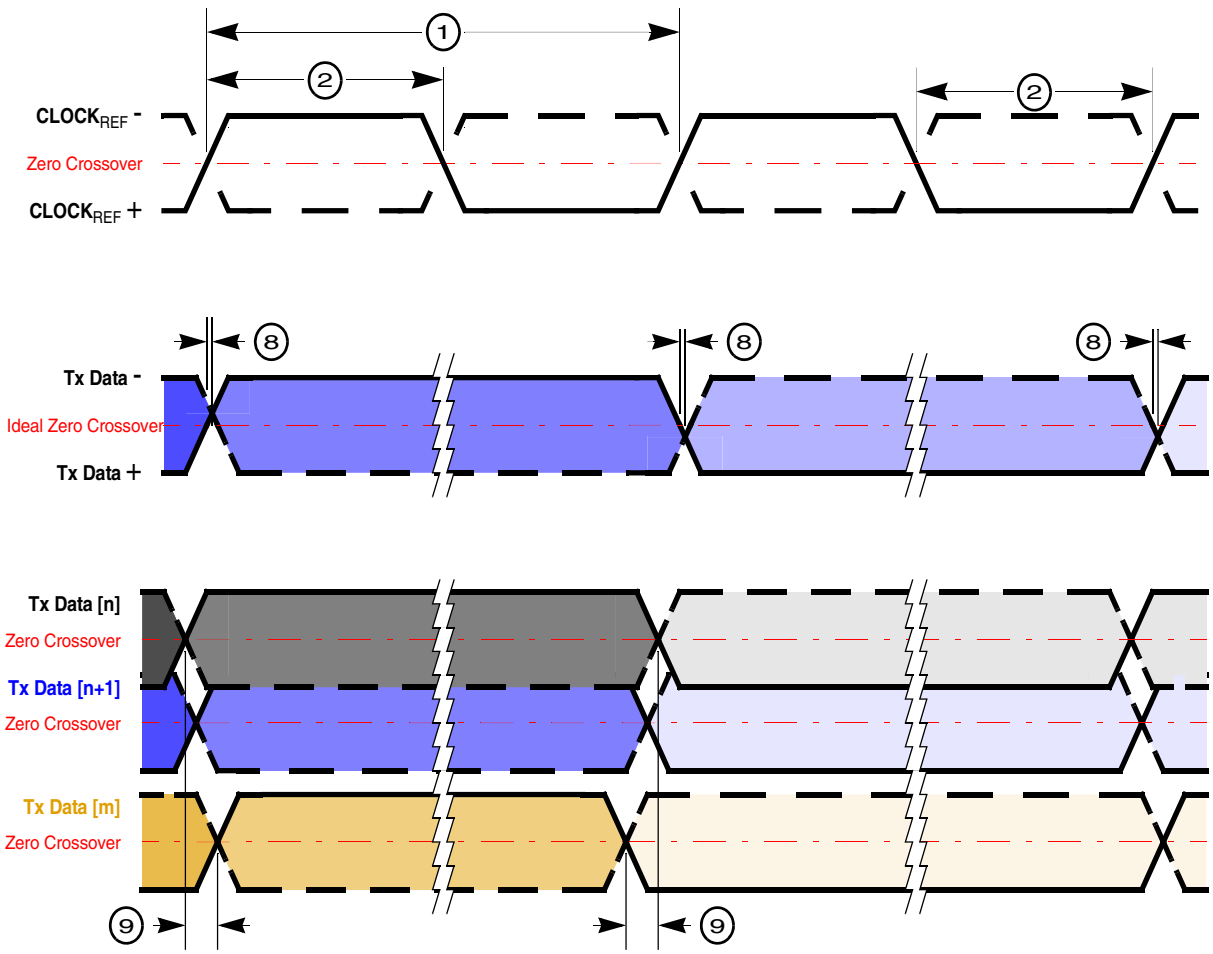



**Figure 22. Nexus Aurora timings**

# 11 WKPU/NMI timing specifications

**Table 33. WKPU/NMI glitch filter**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $W_{FNMI}$ | NMI pulse width that is rejected | — | — | 20 | ns |
| $W_{NFNMI}$ | NMI pulse width that is passed | 400 | — | — | ns |

# 12 External interrupt timing (IRQ pin)

**Table 34. External interrupt timing**

| No. | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | $t_{IPWL}$ | IRQ pulse width low | — | 3 | — | $t_{CYC}$ |
| 2 | $t_{IPWH}$ | IRQ pulse width high | — | 3 | — | $t_{CYC}$ |
| 3 | $t_{ICYC}$ | IRQ edge to edge time[1] | — | 6 | — | $t_{CYC}$ |

1. Applies when IRQ pins are configured for rising edge or falling edge events, but not both

**NOTE**

tCYC is equivalent to TCK (prescaled filter clock period) which is the IRC clock prescaled to the Interrupt Filter Clock Prescaler (IFCP) value. TCK = T(IRC) x (IFCP + 1) where T(IRC) is the internal oscillator period. Refer SIUL2 chapter of the reference manual for details.

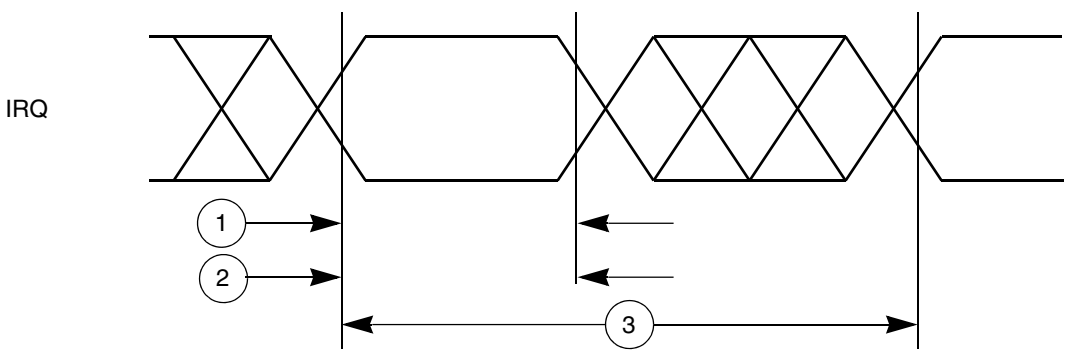



**Figure 23. External interrupt timing**

# 13 Temperature sensor electrical characteristics

The following table describes the temperature sensor electrical characteristics.

**Table 35. Temperature sensor electrical characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| — | Temperature monitoring range | | -40 | — | 150 | °C |
| $T_{SENS}$ | Sensitivity | | — | 5.18 | — | mV/°C |
| $T_{ACC}$ | Accuracy | $T_J$ = -40 to 150°C | 5 | — | 5 | °C |

# 14 Radar module

## 14.1 MIPICSI2 D-PHY electrical and timing specifications

This section describes MIPICSI2[1] D-PHY electrical specifications, compliant with MIPICSI2 version 1.1, D-PHY specification Rev. 1.0 (for MIPI sensor port x2 lanes).

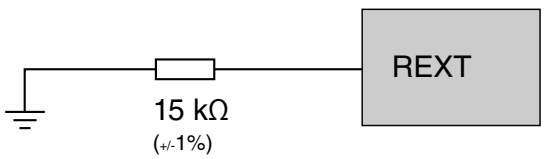



**Figure 24. MIPICSI2 circuit**

**Table 36. Calibrator specifications**

| Symbol | Parameters | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $R_{EXT}$ | External reference resistor, 1% accuracy (or better), for auto calibration | - | 15 | - | kΩ |
| $T_{cal}$ | Time from when PD signal goes low to when CALCOMPL goes high | - | 2.5 | 4.2 | µs |

### 14.1.1 Electrical and timing information

**Table 37. Electrical and timing information**

| Symbol | Parameters | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **HS Line Receiver DC Specifications** | | | | | |
| $V_{IDTH}$ | Differential input high voltage threshold | - | - | 70 | mV |
| $V_{IDTL}$ | Differential input low voltage threshold | -70 | - | - | mV |
| $V_{IHHS}$ | Single ended input high voltage | - | - | 460 | mV |
| $V_{ILHS}$ | Single ended input low voltage | -40 | - | - | mV |
| $V_{CMRXDC}$ | Input common mode voltage | 70 | - | 330 | mV |
| $V_{TERM-EN}$ | Single-ended threshold for HS termination enable | - | - | 450 | mV |
| $Z_{ID}$ | Differential input impedance | 80 | - | 125 | ohm |
| **LP Line Receiver DC Specifications** | | | | | |
| $V_{ILLP}$ | Input low voltage | - | - | 550 | mV |

*Table continues on the next page...*

1. All rights reserved. This material is reprinted with the permission of the MIPI Alliance, Inc. No part(s) of this document may be disclosed, reproduced or used for any purpose other than as needed to support the use of the products of NXP Semiconductors.

**Table 37. Electrical and timing information (continued)**

| Symbol | Parameters | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{IHLP}$ | Input high voltage | 880 | - | - | mV |
| $V_{HYST}$ | Input hysteresis | 25 | - | - | mV |

## 14.1.2 D-PHY signaling levels

The signal levels are different for differential HS mode and single-ended LP mode. The figure below shows both the HS and LP signal levels on the left and right sides, respectively. The HS signaling levels are below the LP low-level input threshold such that LP receiver always detects low on HS signals.

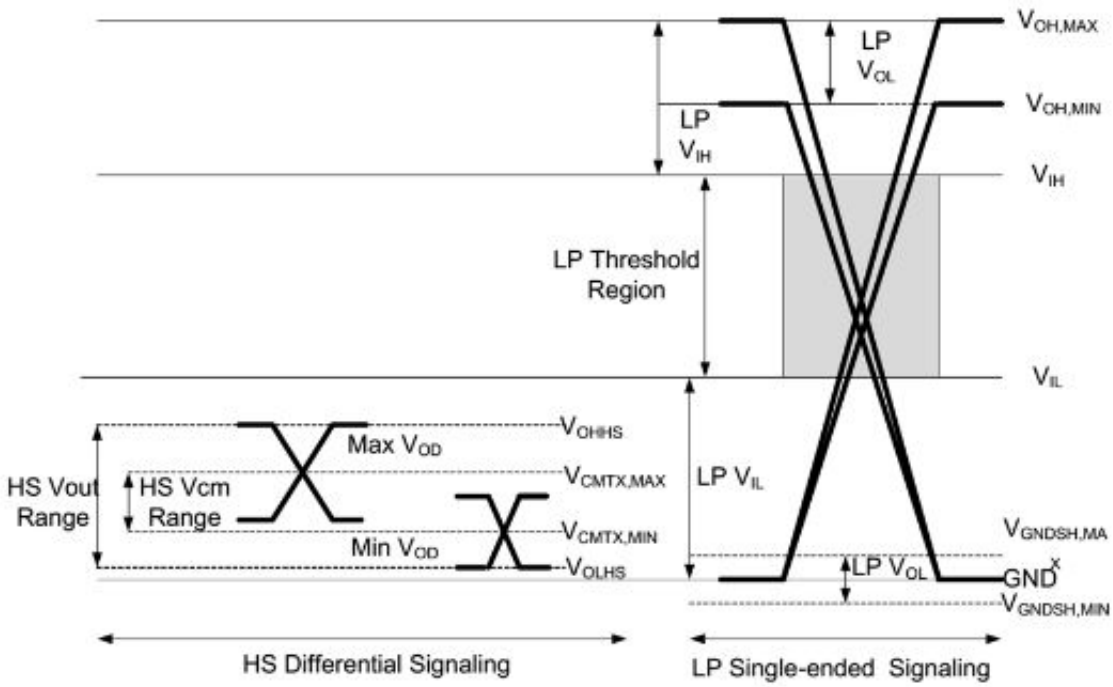



**Figure 25. D-PHY signaling levels**

## 14.1.3 D-PHY switching characteristics

**Table 38. D-PHY switching characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **HS Line Receiver AC Specifications** | | | | | | |
| - | Maximum serial data rate | On DATAP/N inputs. 80 Ohm<= RL <= 125 Ohm | 80 | - | 1000 | Mbps |

*Table continues on the next page...*

**Table 38. D-PHY switching characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ΔVCMRX(HF) | Common mode interference beyond 450 MHz | | - | - | 100 | mVpp |
| ΔVCMRX(LF) | Common mode interference between 50 MHz and 450 MHz | | -50 | - | 50 | mVpp |
| CCM | Common mode termination | | - | - | 60 | pF |
| **LP Line Receiver AC Specification** | | | | | | |
| $e_{SPIKE}$ | Input pulse rejection | | - | - | 300 | Vps |
| $T_{MIN}$ | Minimum pulse response | | 20 | - | - | ns |
| $V_{INT}$ | Pk-to-Pk interference voltage | | - | - | 200 | mV |
| $f_{INT}$ | Interference frequency | | 450 | - | - | MHz |

## 14.1.4 Low-power receiver timing

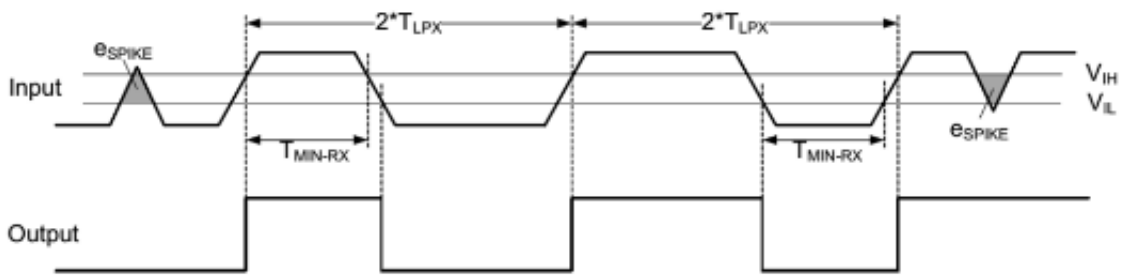



**Figure 26. Input Glitch Rejection of Low-Power Receivers**

### 14.1.5 Data to clock timing

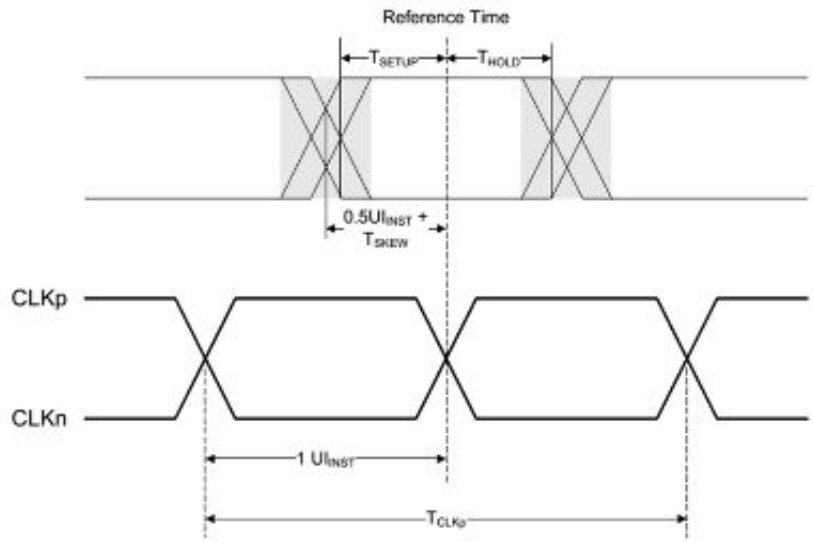



**Figure 27. Definition**

**Table 39. Data to clock timing specifications**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{CLKP}$ | Clock Period | 40 | - | 500 | MHz |
| $UI_{INST}$ | UI Instantaneuous | 1 | - | 12.5 | ns |
| $T_{SETUP}$ | Data to Clock Setup Time | 0.15 | - | - | $UI_{INST}$ |
| $T_{HOLD}$ | Clock to Data Hold Time | 0.15 | - | - | $UI_{INST}$ |

## 14.2 MIPICSI2 disclaimer

The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled by any of the authors or developers of this material or MIPI®. The material contained herein is provided on an “AS IS” basis and to the maximum extent permitted by applicable law, this material is provided AS IS AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of negligence.

All materials contained herein are protected by copyright laws, and may not be reproduced, republished, distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related trademarks, trade names, and other intellectual property are the exclusive property of MIPI Alliance and cannot be used without its express prior written permission.

ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL, CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL, WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document; and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance with the contents of this Document. The use or implementation of the contents of this Document may involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents, patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any IPR or claims of IPR as respects the contents of this Document or otherwise.

# 15 Thermal characteristics

**Table 40. 257MAPBGA package thermal characteristics**

| Symbol | Parameter | Conditions | 257MAPBGA | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient natural convection [1] | Single layer board - 1s | 45.4 | °C/W |
| | | Four layer board - 2s2p | 27.07 | |
| $R_{\theta JMA}$ | Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1] | Single layer board - 1s[2] | 35.67 | °C/W |

*Table continues on the next page...*

**Table 40. 257MAPBGA package thermal characteristics (continued)**

| Symbol | Parameter | Conditions | 257MAPBGA | Unit |
|---|---|---|---|---|
| | | Four layer board - 2s2p[3] | 22.7 | |
| $R_{\theta JB}$ | Thermal resistance junction-to-board[4] | — | 13.01 | °C/W |
| $R_{\theta JC}$ | Thermal resistance junction-to-case[5] | — | 7.95 | °C/W |
| $\Psi_{JT}$ | Junction-to-package-top natural convection[6] | Natural Convection | 0.2 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
5. Junction-to-Case at the top of the package determined using MIL-SPEC 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

**Table 41. 141MAPBGA package thermal characteristics**

| Symbol | Parameter | Conditions | 141MAPBGA | Unit |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal resistance, junction-to-ambient natural convection [1] | Single layer board - 1s | 66.6 | °C/W |
| | | Four layer board - 2s2p | 34.4 | |
| $R_{\theta JMA}$ | Thermal resistance, junction-to-ambient forced convection at 200 ft/min[1] | Single layer board - 1s[2] | 50.6 | °C/W |
| | | Four layer board - 2s2p[3] | 29.2 | |
| $R_{\theta JB}$ | Thermal resistance junction-to-board[4] | — | 13.4 | °C/W |
| $R_{\theta JC}$ | Thermal resistance junction-to-case[5] | — | 9.8 | °C/W |
| $\Psi_{JT}$ | Junction-to-package-top natural convection[6] | Natural Convection | 0.2 | °C/W |

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal
4. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. Board temperature is measured on the top surface of the board near the package.
5. Junction-to-Case at the top of the package determined using MIL-SPEC 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

## 15.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, $T_J$, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

$T_J = T_{BRD} + (R_{\theta JB} \times P_D)$

where:

- $T_A$ = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JB}$ = junction to board thermal resistance (°C/W)
- $T_{\theta BRD}$ = average board temperature just outside the package periphery (°C)
- $P_D$ = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard parameter that provides a quick and easy estimation of thermal performance. However, junction to board thermal resistance is more appropriate for tight enclosure spaces where board temperature should be used as reference temperature. Using 2s2p board with natural convection conditions, junction temperature is found to be less than 150°C . There are two parameters in common usage: the value determined on a single layer board and the value obtained on a board with two inner planes. For packages such as PBGA, these values can significantly differ. For customer board design with different number of layers and copper percentage content, these values must be appropriately interpolated in order to evaluate junction temperature. In general, the value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter ($\Psi_{JT}$) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$T_J = T_T + (\Psi_{JT} \times P_D)$

where:

- $T_T$ = thermocouple temperature on top of the package (°C)
- $\Psi_{JT}$ = thermal characterization parameter (°C/W)
- $P_D$ = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 15.2 References

Semiconductor Equipment and Materials International; 3081 Zanker Road; San Jose, CA 95134 USA; (408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the Web at http://www.jedec.org.

1. C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47–54.
2. G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications,” Electronic Packaging and Production, pp. 53–58, March 1998.
3. B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212–220.

# 16 Packaging

The S32R372 is offered in the following package types.

| If you want the drawing for this package | Then use this document number |
|---|---|
| 257-ball MAPBGA | 98ASA00081D |
| 141-ball MAPBGA | 98ASA01014D |

**NOTE**

For detailed information regarding package drawings, refer to www.nxp.com.

# 17 Reset sequence

This section describes different reset sequences and details the duration for which the device remains in reset condition in each of those conditions.

## 17.1 Reset sequence duration

Table 43 specifies the minimum and the maximum reset sequence duration for the five different reset sequences described in Reset sequence description.

**Table 43. RESET sequences**

| No. | Symbol | Parameter | $T_{Reset}$ | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max[1] | |
| 1 | $T_{DRB}$ | Destructive Reset Sequence, BIST enabled | 15 | | 50[2] | ms |
| 2 | $T_{DR}$ | Destructive Reset Sequence, BIST disabled | 400 | | 2000 | µs |
| 3 | $T_{ERLB}$ | External Reset Sequence Long, BIST enabled | 15 | | 50 | ms |
| 4 | $T_{FRL}$ | Functional Reset Sequence Long, BIST disabled | 400 | | 2000 | µs |
| 5 | $T_{FRS}$ | Functional Reset Sequence Short[3] | 1 | | 500 | µs |

1. The maximum value is applicable only if the reset sequence duration is not prolonged by an extended assertion of $\overline{\text{RESET}}$ by an external reset generator.
2. Max time is based on STCU BIST configuration execution time + max RESET time (TDR). For default STCU BIST configuration execution time.
3. BIST is not executed on short functional reset

## 17.2 Reset sequence description

The figures in this section show the internal states of the device during the five different reset sequences. The doted lines in the figures indicate the starting point and the end point for which the duration is specified in Table 43.

With the beginning of DRUN mode, the first instruction is fetched and executed. At this point, application execution starts and the internal reset sequence is finished.

The SMPS self test is always triggered during Phase3 after a destructive reset so that duration is included into Phase3 below.

In external regulation mode, the VREG_POR_B pin should be de-asserted only when all the design supplies are in operating range. Deassertion of VREG_POR_B pin triggers the start of reset sequence in internal as well as external regulation modes.

The following figures show the internal states of the device during the execution of the reset sequence and the possible states of the RESET_B signal pin.

**NOTE**

RESET_B is a bidirectional pin. The voltage level on this pin can either be driven low by an external reset generator or by the device internal reset circuitry. A high level on this pin can only be generated by an external pullup resistor which is strong enough to overdrive the weak internal pulldown resistor. The rising edge on RESET_B in the following figures indicates the time when the device stops driving it low. The reset sequence durations given in Table 43 are applicable only if the internal reset sequence is not prolonged by an external reset generator keeping RESET_B asserted low beyond the last Phase3.

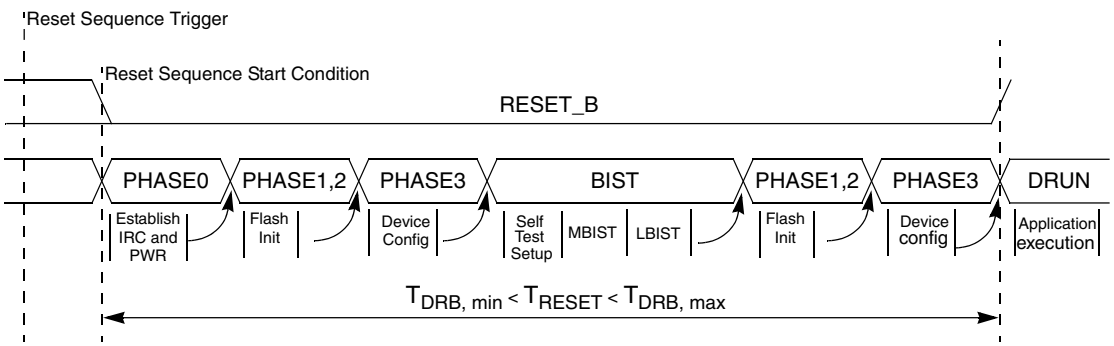



**Figure 28. Destructive reset sequence, BIST enabled**

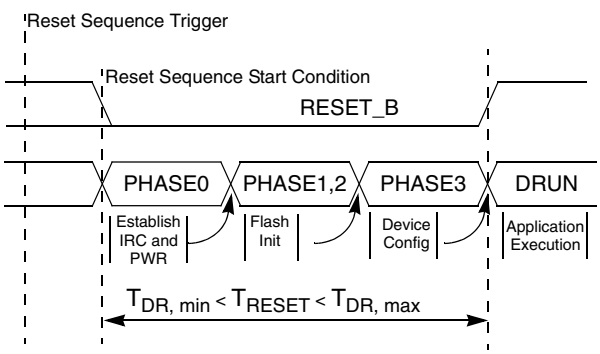



**Figure 29. Destructive reset sequence, BIST disabled**

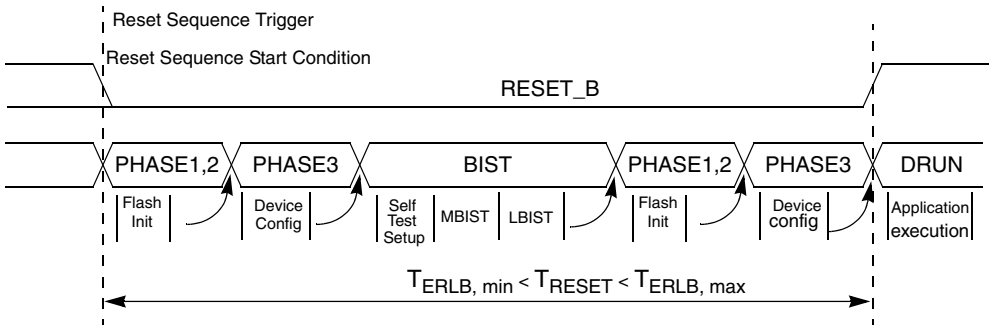



**Figure 30. External reset sequence long, BIST enabled**

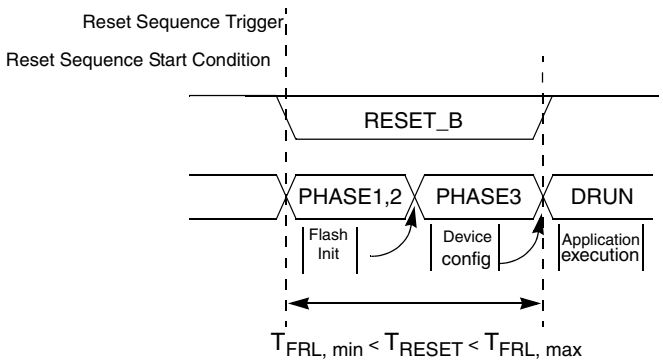



**Figure 31. Functional reset sequence long**

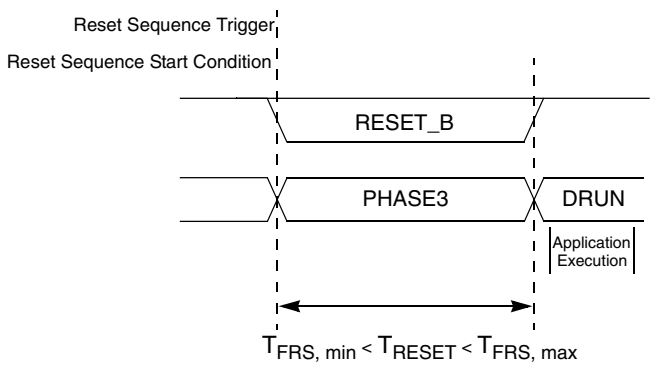



**Figure 32. Functional reset sequence short**

The reset sequences shown in Figure 31 and Figure 32 are triggered by functional reset events. $\overline{\text{RESET}}$ is driven low during these two reset sequences only if the corresponding functional reset source (which triggered the reset sequence) was enabled to drive RESET_B low for the duration of the internal reset sequence. See the RGM_FBRE register in the device reference manual for more information.

# 18 Power sequencing requirements

**NOTE**

Following table describes the power and ground groups that MUST be formed while designing the application board. "DC short" on board for a group of package pins mean that they should be powered through the same DC source, with appropriate passive filtering to ensure that required AC noise isolation is in place, but their DC supply levels remains the same for all practical purposes.

**Table 44. Power and ground grouping**

| BGA257 package connection | BGA257 Board Connection | BGA141 package connection | BGA141 Board Connection |
|---|---|---|---|
| $V_{DD}$ | DC short: $V_{DD_LV}$ | $V_{DD_LV}$ | DC short: $V_{DD_LV}$ |
| $V_{DD_LV_IO_AURORA}$ | | $V_{DD_LV_IO_AURORA}$ | |
| $V_{DD_LV_PLL0}$ | | $V_{DD_LV_PLL0}$ | |
| $V_{DD_LV_LFAST_PLL}$ | | | |
| $V_{DD_LV_DPHY}$, [1] | | $V_{DD_LV_DPHY}$ [1] | |
| $V_{DD_HV_IO}$ | DC short: $V_{DD_HV_DIG}$ | $V_{DD_HV_IO}$ | DC short: $V_{DD_HV_DIG}$ |
| $V_{DD_HV_IO_PWM}$ | | | |
| $V_{DD_HV_IO}$ | | | |
| $V_{DD_HV_FLA}$ | | $V_{DD_HV_FLA}$ | |
| $V_{DD_HV_PMU}$ | | $V_{DD_HV_PMU}$ | |
| $V_{DD_HV_REG3V8}$ | $V_{DD_HV_REG3V8}$ | | |
| $V_{DD_HV_ADCREF1}$ | $V_{DD_HV_ADCREF1}$ | $V_{DD_HV_ADCREF}$ | $V_{DD_HV_ADCREF}$ |
| $V_{DD_HV_ADCREF0}$ | $V_{DD_HV_ADCREF0}$ | | |
| $V_{DD_HV_ADC}$ | $V_{DD_HV_ADC}$ | $V_{DD_HV_ADC}$ | $V_{DD_HV_ADC}$ |
| $V_{DD_HV_RAW}$ | $V_{DD_HV_RAW}$ | $V_{DD_HV_RAW}$ | $V_{DD_HV_RAW}$ |
| $V_{DD_HV_DAC}$ | | | |
| $V_{DD_LV_RADARREF}$ | $V_{DD_LV_RADARREF}$ | $V_{DD_LV_RADARREF}$ | $V_{DD_LV_RADARREF}$ |
| $V_{DD_LV_SDPLL}$ | $V_{DD_LV_SDPLL}$ | $V_{DD_LV_SDPLL}$ | $V_{DD_LV_SDPLL}$ |
| $V_{DD_LV_OSC}$ | $V_{DD_LV_OSC}$ | $V_{DD_LV_OSC}$ | $V_{DD_LV_OSC}$ |
| $V_{DD_LV_SDCLK}$ | $V_{DD_LV_SDCLK}$ | $V_{DD_LV_SDCLK}$ | $V_{DD_LV_SDCLK}$ |
| $V_{SS_LV_COR}$ | DC short: $V_{SS}$ | $V_{SS_LV_COR}$ | DC short: $V_{SS}$ |
| $V_{SS_LV_PLL0}$ | | $V_{SS_LV_IO_AURORA}$ | |
| $V_{SS_LV_LFAST_PLL}$ | | | |
| $V_{SS_LV_PHY}$ | | | |
| $V_{SS_LV_IO_AURORA}$ | | | |
| $V_{SS_HV_IO}$ | | $V_{SS_LV_COR}$ | |

*Table continues on the next page...*

**Table 44. Power and ground grouping (continued)**

| BGA257 package connection | BGA257 Board Connection | BGA141 package connection | BGA141 Board Connection |
|---|---|---|---|
| $V_{SS_HV_IO_PWM}$ | | | |
| $V_{SS_LV_COR}$ | | | |
| $V_{SS_HV_REG3V8}$ | $V_{SS_HV_REG3V8}$ | | |
| $V_{SS_LV_COR}$ | DC short: $V_{SS}$ | | |
| $V_{SS_SUB_OUTPWB}$ | DC short: $V_{SS}$ | | |
| $V_{SS_HV_ADCREF1}$ | $V_{SS_HV_ADCREF1}$ | $V_{SS_HV_ADCREF}$ | $V_{SS_HV_ADCREF}$ |
| $V_{SS_HV_ADCREF0}$ | $V_{SS_HV_ADCREF0}$ | | |
| $V_{SS_HV_ADC}$ | DC short: $V_{SS_HV_ANA}$ | $V_{SS_HV_ADC}$ | DC short: $V_{SS_HV_ANA}$ |
| $V_{SS_HV_RAW}$ | | $V_{SS_AFE}$ | |
| $V_{SS_HV_DAC}$ | | | |
| $V_{SS_LV_RADARREF}$ | | | |
| $V_{SS_LV_SDPLL}$ | | | |
| $V_{SS_LV_OSC}$ | | | |
| $V_{SS_LV_SDCLK}$ | | | |
| $V_{SS_SUB_INPWB0}$ | | | |
| $V_{SS_SUB_INPWB1}$ | | | |

1. Refer to AN5251. Contact your NXP sales representative for details.

The device does not require any specific power sequencing as far as user follows recommendations in this section.

As mentioned in the previous section, it is expected that the external ASIC which powers up the device in external regulation mode deasserts VREG_POR_B pin only when all the power supplies to the design are in operating range.

It should be noted that LVD and HVD detectors on VDD supply are disabled by default in external regulation mode for preventing a conflict with external regulator operation but they can be enabled by software once design is powered up.

While designing the system, it is important to ensure that AFE supplies are powered up before data is sent on its input pads or the crystal oscillator pins EXTAL / XTAL are driven by an external clock source.

# 19 Package pinouts and signal descriptions

For package pinouts and signal descriptions, see the S32R372 Reference Manual.

# 20 Release Notes

**Table 45. Release notes**

| Revision | Date | Description |
|---|---|---|
| 1 | 28 Nov 2016 | Initial release |
| 2 | 15 Sep 2017 | • In Table 22 added rows for the symbols $t_{sampleC}$, $t_{sampleS}$, $t_{sampleBG}$, and $t_{sampleTS}$.<br>• In Table 6 changed the Max voltage of LVDS external clock input voltage parameter from 1.23 V to 1.36 V.<br>• In Nexus Aurora debug port timing, added spec for EVTI Pulse Width.<br>• In Table 6, updated $V_{inxosccclkvih}$ from 1.2V to 1.23V.<br>• In Table 17, updated $t_{jitcc}$ from 3.5ps to 2.5ps. |
| 3 | 14 May 2018 | • In Table 5 :<br>  • Changed Maximum value for $V_{INA}$ from $V_{DD_HV_ADCREFx}$ + 0.3 to 6.0.<br>  • Added footnote to $I_{INJPAD}$ to state "The maximum value limits of injection current and input voltage both must be followed together for proper device operation."<br>• In Table 6, changed $V_{INA}$ Maximum value from $V_{DD_HV_ADCREFx}$+ 0.3 to $V_{DD_HV_ADCREFx}$. |
| 3.1 | 09 July 2018 | • In Table 5, removed footnote on $I_{INJPAD}$. |
| 4 | 14 Aug 2018 | • On the first page, changed document classification from 'Advance Information' to 'Technical Data". |

***How to Reach Us:***

**Home Page:**
nxp.com

**Web Support:**
nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer’s technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer's applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, AltiVec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.

© 2017 NXP B.V.

Document Number S32R372
Revision 4, 08/2018