



PSMN025-80YL

N-channel 80 V, 25 mΩ logic level MOSFET in LPAK56

14 April 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in an LPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

2. Features and benefits

- Advanced TrenchMOS provides low $R_{DS(on)}$ and low gate charge
- Logic level gate operation
- Avalanche rated, 100% tested
- LPAK provides maximum power density in a Power SO8 package

3. Applications

- Synchronous rectification in power supply equipment
- Chargers & adaptors with $V_{out} < 10$ V
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

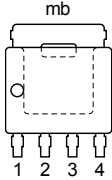
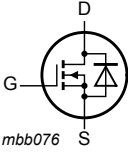
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	37	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	95	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	22.2	27	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 64\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14	-	5.8	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN025-80YL	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN025-80YL	025L80

8. Limiting values

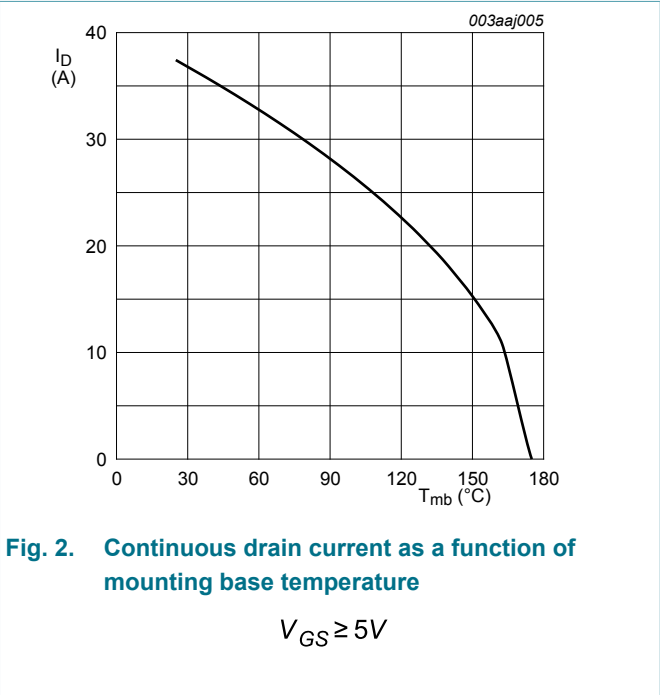
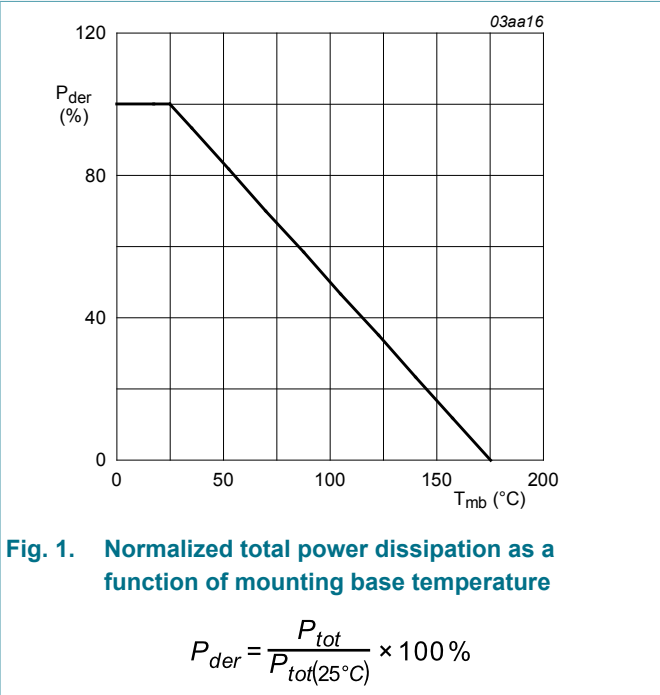
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	95	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	37	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	26.5	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	150	A
T_{stg}	storage temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	37	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	150	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 37 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[1] [2]	-	45.4	mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[2] Refer to application note AN10273 for further information.



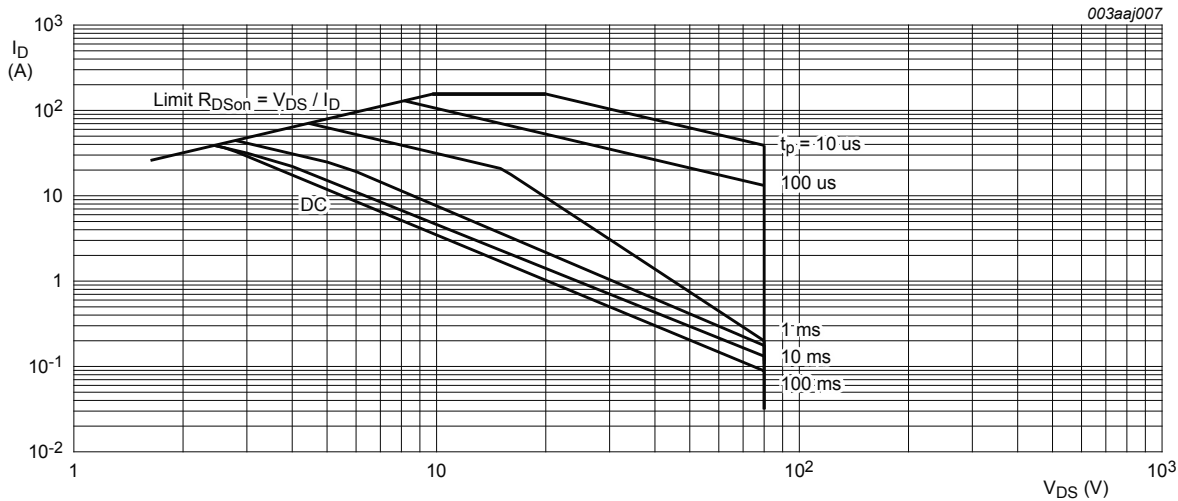


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

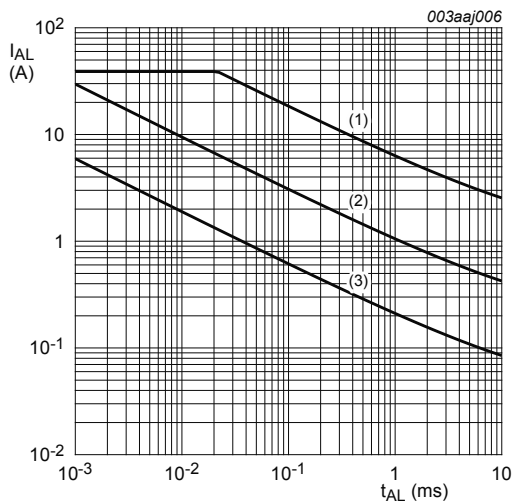


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(init)} = 25^{\circ}\text{C}$; (2) $T_{j(init)} = 150^{\circ}\text{C}$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	1.58	K/W

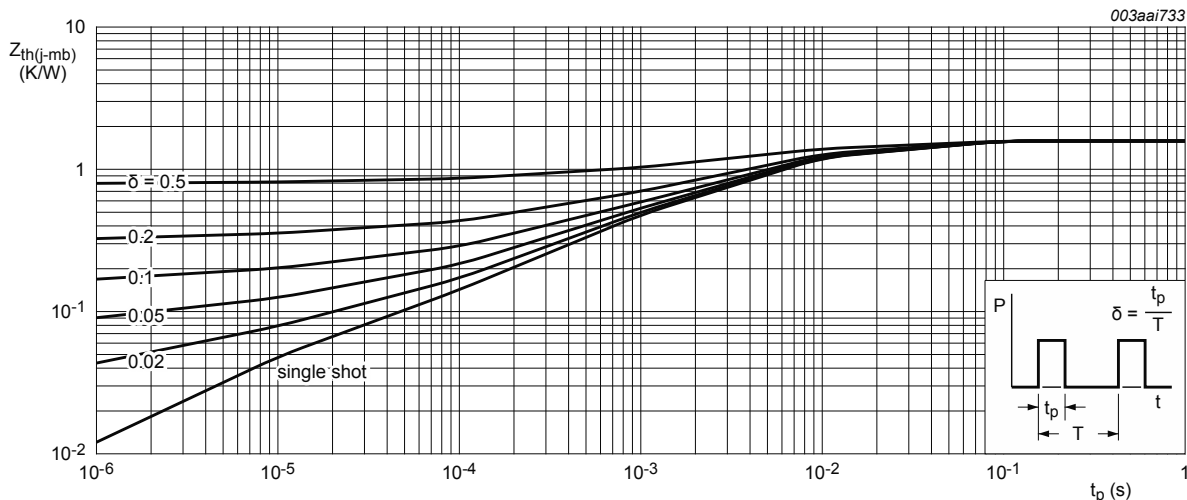


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$		80	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$		72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_j = 25\ ^\circ C$; Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_j = -55\ ^\circ C$; Fig. 9		-	-	2.45	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_j = 175\ ^\circ C$; Fig. 9		0.5	-	-	V
I_{DSS}	drain leakage current	$V_{DS} = 80\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$		-	0.1	1	μA
		$V_{DS} = 80\ V$; $V_{GS} = 0\ V$; $T_j = 175\ ^\circ C$		-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$		-	2	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$		-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\ V$; $I_D = 10\ A$; $T_j = 25\ ^\circ C$; Fig. 11		-	22.2	27	m Ω
		$V_{GS} = 10\ V$; $I_D = 10\ A$; $T_j = 25\ ^\circ C$; Fig. 11		-	20.5	25	m Ω
		$V_{GS} = 5\ V$; $I_D = 10\ A$; $T_j = 175\ ^\circ C$; Fig. 12 ; Fig. 11		-	-	67.8	m Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 10\ A$; $V_{DS} = 64\ V$; $V_{GS} = 5\ V$; $T_j = 25\ ^\circ C$; Fig. 13 ; Fig. 14		-	17.1	-	nC
		$I_D = 10\ A$; $V_{DS} = 64\ V$; $V_{GS} = 10\ V$; $T_j = 25\ ^\circ C$; Fig. 13 ; Fig. 14		-	34.3	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q _{GS}	gate-source charge	I _D = 10 A; V _{DS} = 64 V; V _{GS} = 5 V; T _J = 25 °C; Fig. 13 ; Fig. 14		-	5.2	-	nC
Q _{GD}	gate-drain charge			-	5.8	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 15		-	2032	2703	pF
C _{oss}	output capacitance			-	147	176	pF
C _{rss}	reverse transfer capacitance			-	75	103	pF
t _{d(on)}	turn-on delay time	V _{DS} = 60 V; R _L = 4.98 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	11.6	-	ns
t _r	rise time			-	17.2	-	ns
t _{d(off)}	turn-off delay time			-	23.9	-	ns
t _f	fall time			-	15.3	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 16		-	0.81	1.2	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V; T _J = 25 °C		-	23.8	-	ns
Q _r	recovered charge			-	27	-	nC

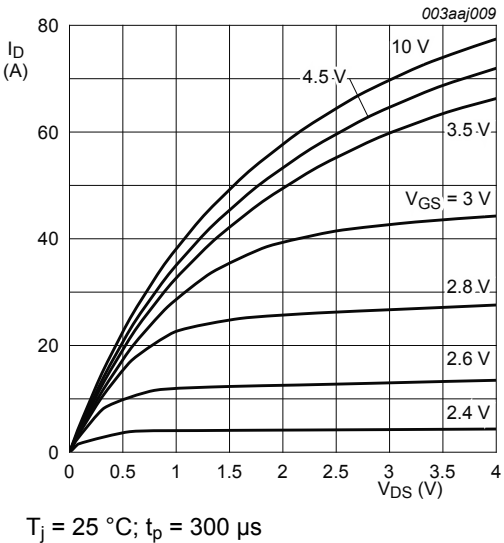


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

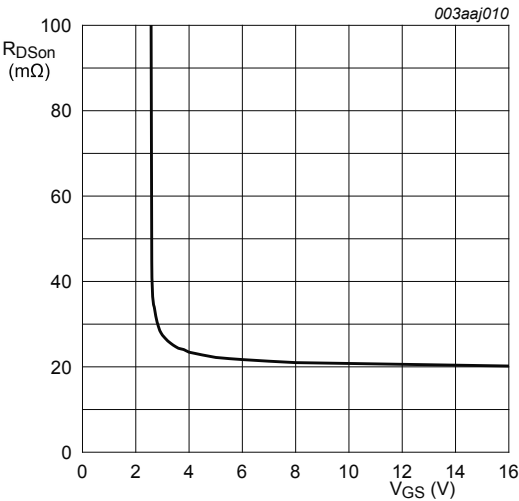


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ °C}$; $I_D = 10\text{ A}$

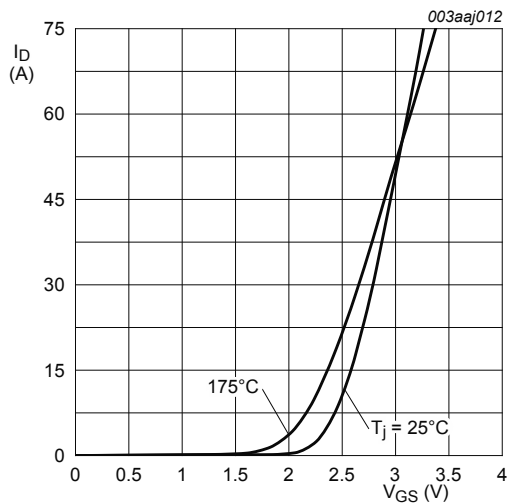


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

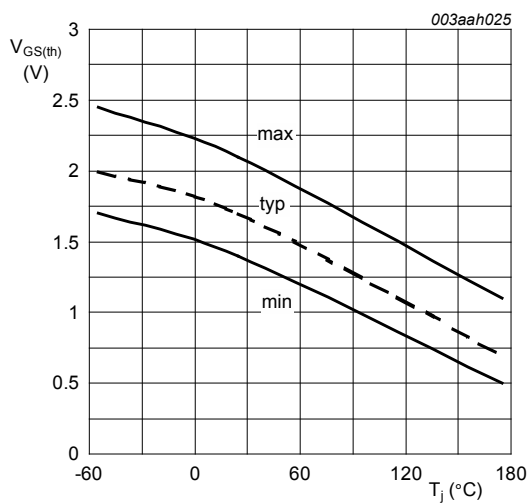


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

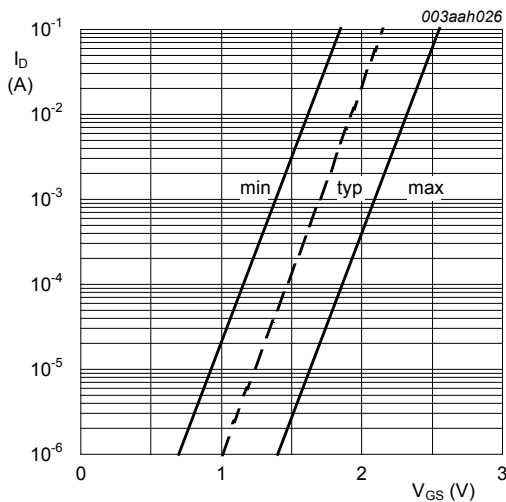
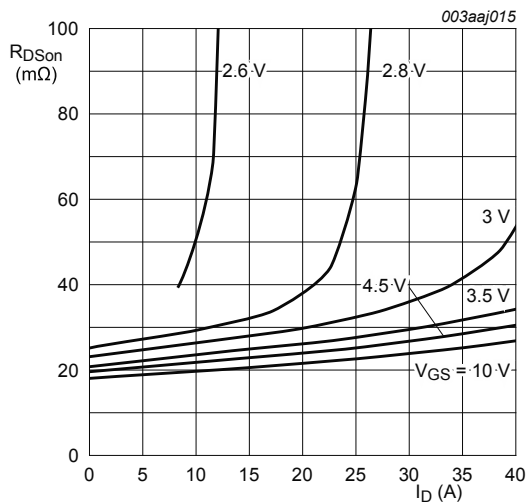


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$



$T_j = 25^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

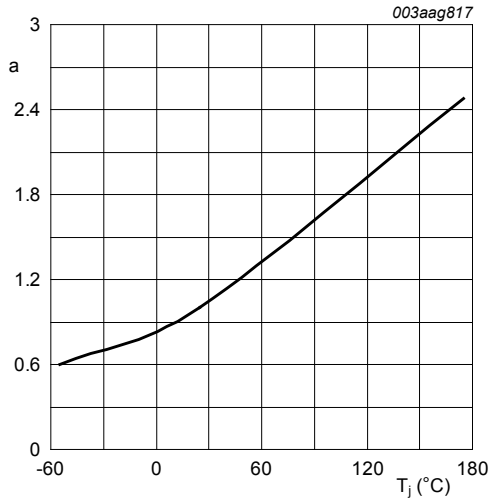


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

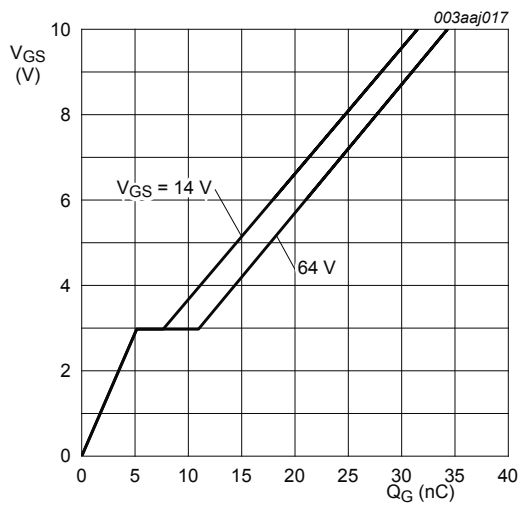


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 10\text{A}$$

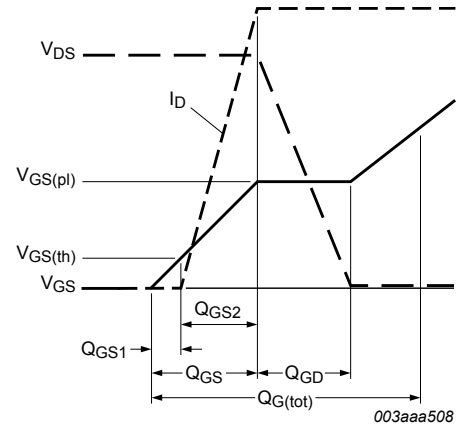


Fig. 13. Gate charge waveform definitions

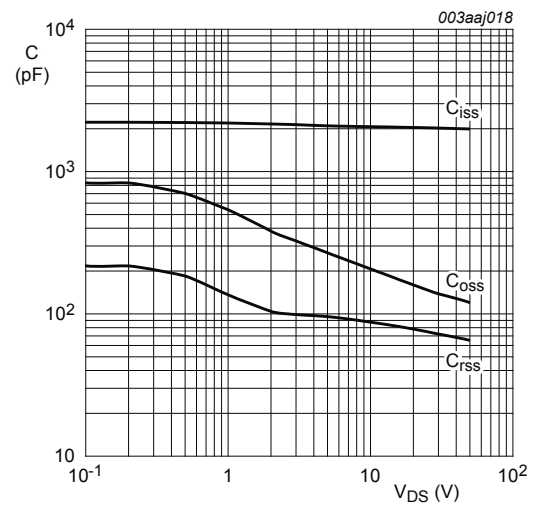


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

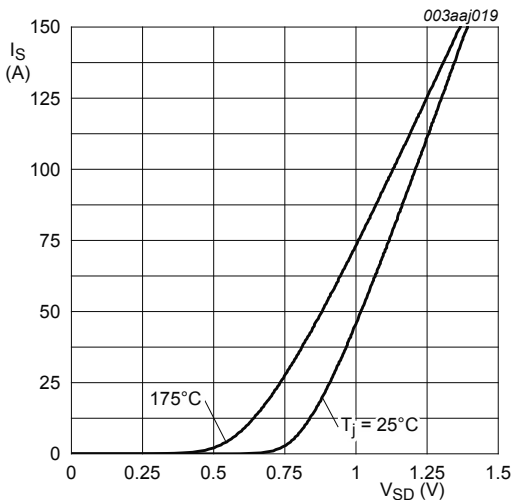


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values
 $V_{GS} = 0V$

11. Package outline

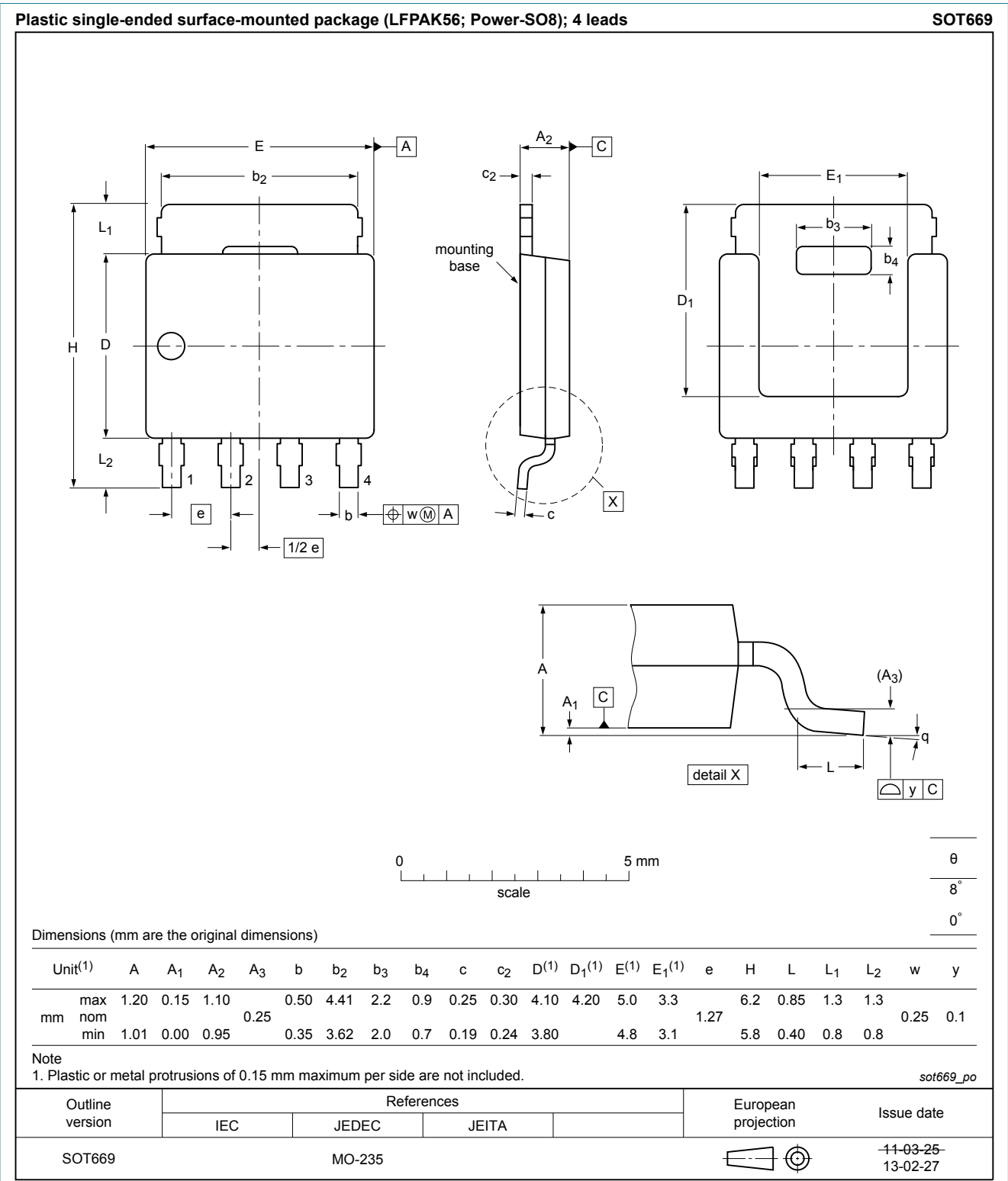


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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