



# BUK762R7-30B

N-channel TrenchMOS standard level FET

Rev. 04 — 8 June 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Q101 compliant
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

### 1.3 Applications

- 12 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

### 1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}; T_j \leq 175^\circ\text{C}$	-	-	30	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25^\circ\text{C};$ see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	[1]	-	-	75 A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	-	300	W
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $T_j = 25^\circ\text{C}$ ; see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	2.3	2.7	$\text{m}\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}; V_{sup} \leq 30\text{ V};$ $R_{GS} = 50\ \Omega; V_{GS} = 10\text{ V};$ $T_{j(init)} = 25^\circ\text{C}$ ; unclamped	-	-	2.3	J
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 10\text{ V}; I_D = 25\text{ A};$ $V_{DS} = 24\text{ V}; T_j = 25^\circ\text{C};$ see <a href="#">Figure 13</a>	-	29	-	nC

[1] Continuous current is limited by package.

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## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain <sup>[1]</sup>		
3	S	source		
mb	D	mounting base; connected to drain		
SOT404 (D2PAK)				

[1] It is not possible to make connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

Type number	Package			Version
	Name	Description		
BUK762R7-30B	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)		SOT404

## 4. Limiting values

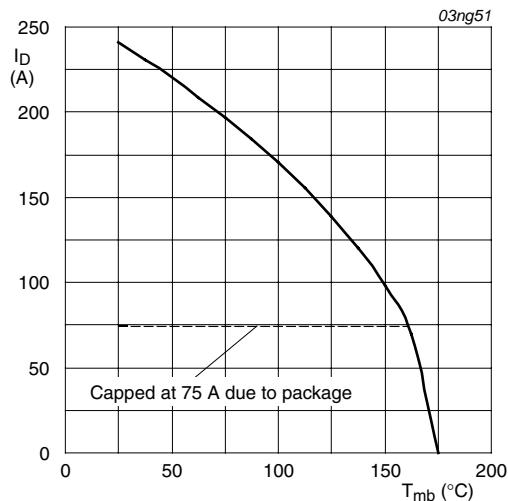
**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25^\circ\text{C}$ ; $T_j \leq 175^\circ\text{C}$	-	-	30	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	-	30	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$T_{mb} = 25^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; <a href="#">[1]</a>	-	-	241	A
		see <a href="#">Figure 3</a>				
		$T_{mb} = 100^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> <a href="#">[2]</a>	-	-	75	A
		$T_{mb} = 25^\circ\text{C}$ ; $V_{GS} = 10\text{ V}$ ; see <a href="#">Figure 1</a> ; <a href="#">[2]</a>	-	-	75	A
		see <a href="#">Figure 3</a>				
$I_{DM}$	peak drain current	$T_{mb} = 25^\circ\text{C}$ ; $t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; see <a href="#">Figure 3</a>	-	-	967	A
$P_{tot}$	total power dissipation	$T_{mb} = 25^\circ\text{C}$ ; see <a href="#">Figure 2</a>	-	-	300	W
$T_{stg}$	storage temperature		-55	-	175	°C
$T_j$	junction temperature		-55	-	175	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{mb} = 25^\circ\text{C}$	<a href="#">[1]</a> -	-	241	A
			<a href="#">[2]</a> -	-	75	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25^\circ\text{C}$	-	-	967	A
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 75\text{ A}$ ; $V_{sup} \leq 30\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25^\circ\text{C}$ ; unclamped	-	-	2.3	J

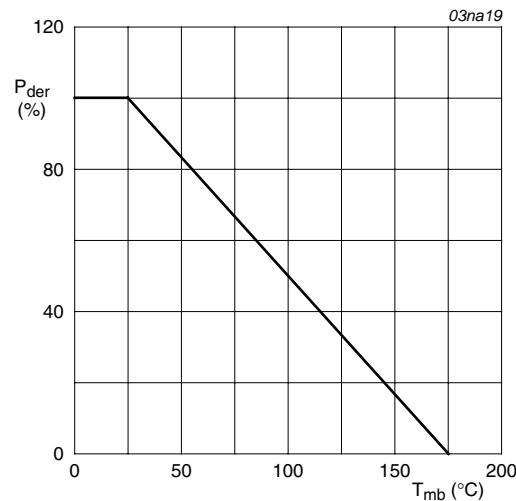
[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.



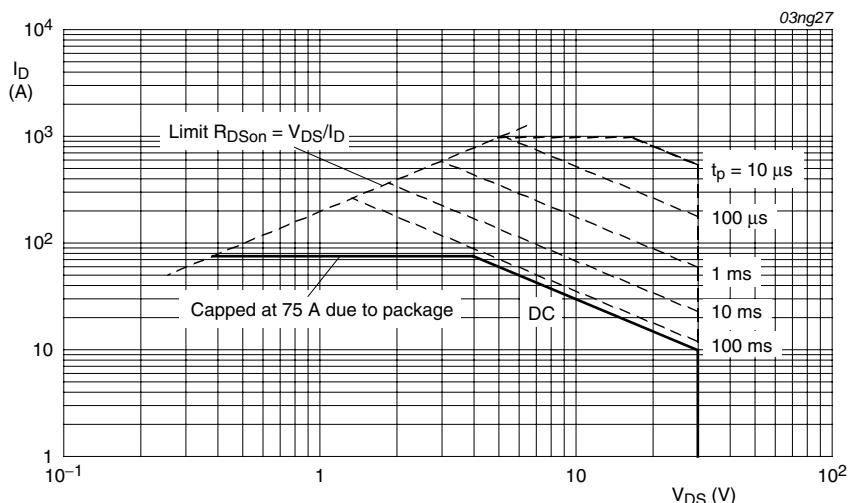
$$V_{GS} \geq 10V$$

**Fig 1.** Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot}(25^\circ\text{C})} \times 100 \%$$

**Fig 2.** Normalized total power dissipation as a function of mounting base temperature



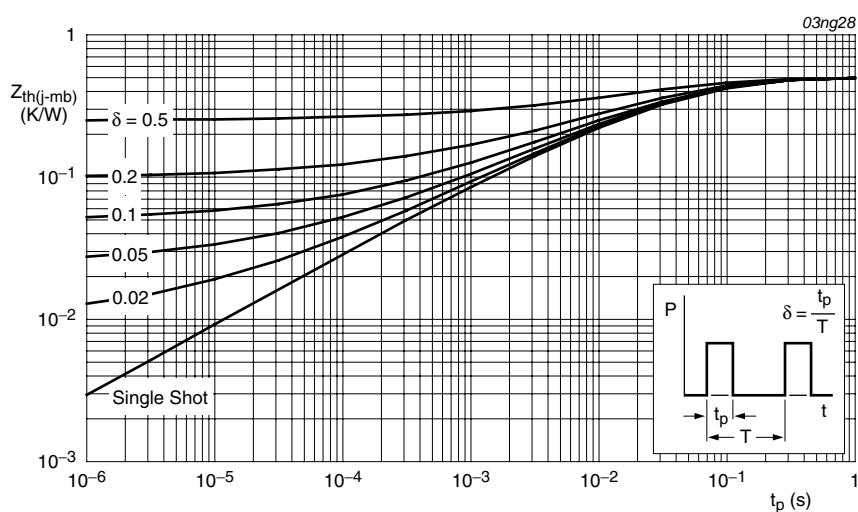
$$T_{mb} = 25^\circ\text{C}; I_{DM} \text{ is single pulse}$$

**Fig 3.** Safe operating area; continuous and peak drain currents as a function of drain-source voltage

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j\text{-}mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	0.5	K/W
$R_{th(j\text{-}a)}$	thermal resistance from junction to ambient	minimum footprint ; mounted on a printed-circuit board	-	50	-	K/W

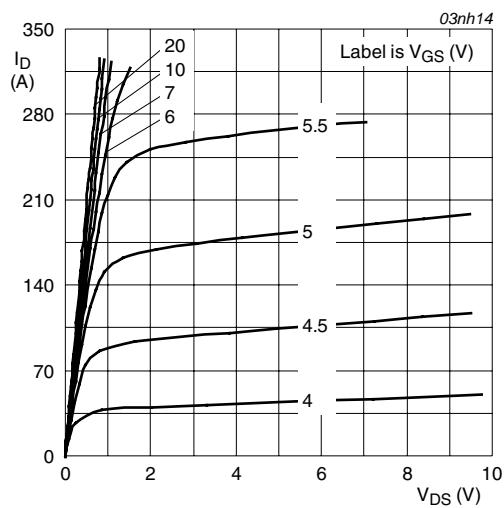


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

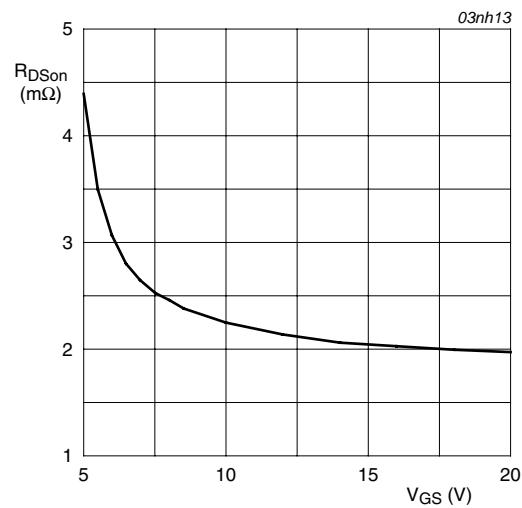
**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GS(\text{th})}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a> $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 10</a>	2	3	4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$ $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ $V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a> $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a> ; see <a href="#">Figure 12</a>	-	-	5.1	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 24 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>	-	91	-	nC
$Q_{GS}$	gate-source charge	$T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>	-	19	-	nC
$Q_{GD}$	gate-drain charge		-	29	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$	-	4659	6212	pF
$C_{oss}$	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 14</a>	-	1691	2029	pF
$C_{rss}$	reverse transfer capacitance		-	622	852	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 1.2 \text{ }\Omega; V_{GS} = 10 \text{ V};$ $R_{G(\text{ext})} = 10 \text{ }\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	31	-	ns
$t_r$	rise time		-	107	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	113	-	ns
$t_f$	fall time		-	118	-	ns
$L_D$	internal drain inductance	from drain lead 6 mm from package to center of die ; $T_j = 25 \text{ }^\circ\text{C}$ from upper edge of drain mounting base to centre of die ; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	-	nH
$L_S$	internal source inductance	from source lead to source bond pad ; $T_j = 25 \text{ }^\circ\text{C}$	-	7.5	-	nH
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 40 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$ $V_{GS} = -10 \text{ V}; V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	88	-	ns
$Q_r$	recovered charge		-	132	-	nC



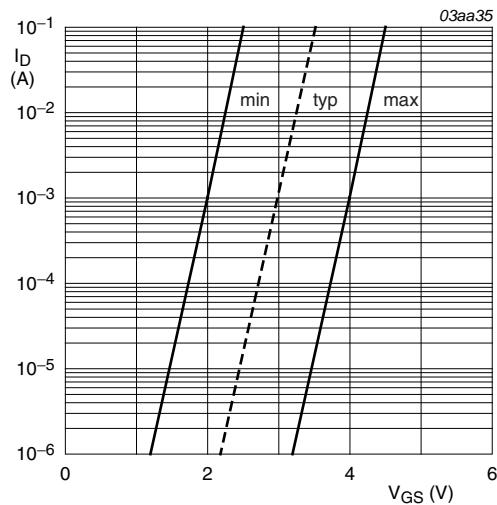
$T_j = 25^\circ C; t_p = 300\mu s$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



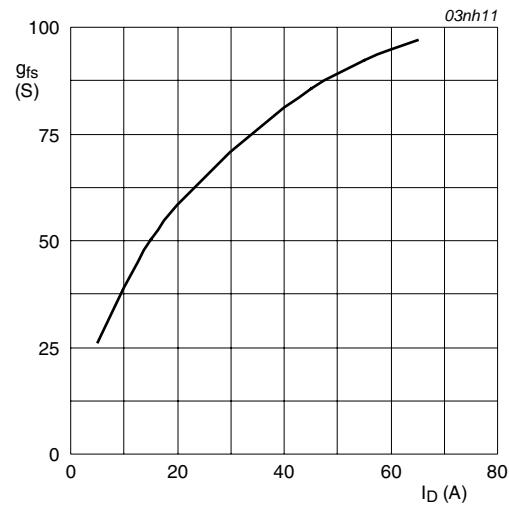
$T_j = 25^\circ C; I_D = 25A$

**Fig 6. Drain-source on-state resistance as a function of drain current; typical values**



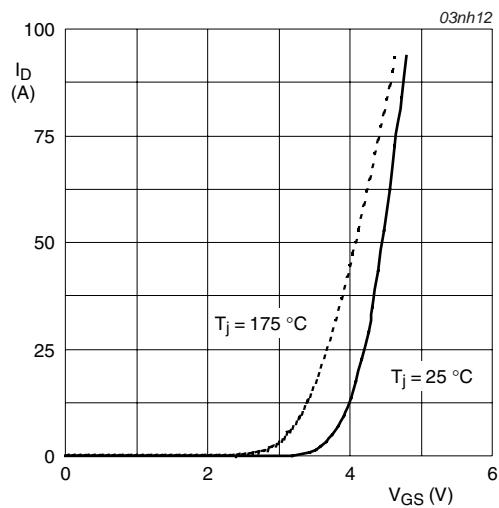
$T_j = 25^\circ C; V_{DS} = 5V$

**Fig 7. Sub-threshold drain current as a function of gate-source voltage**

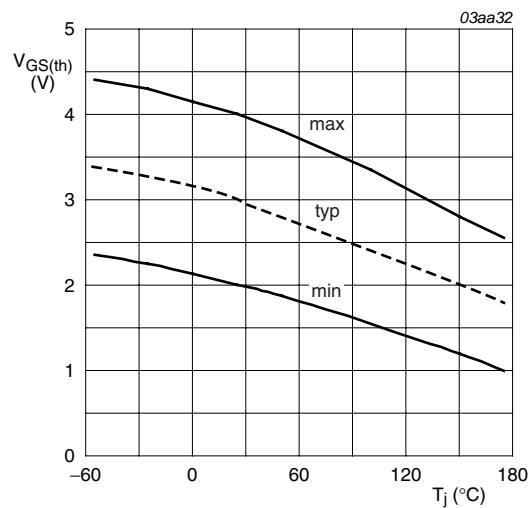


$T_j = 25^\circ C; V_{DS} = 25V$

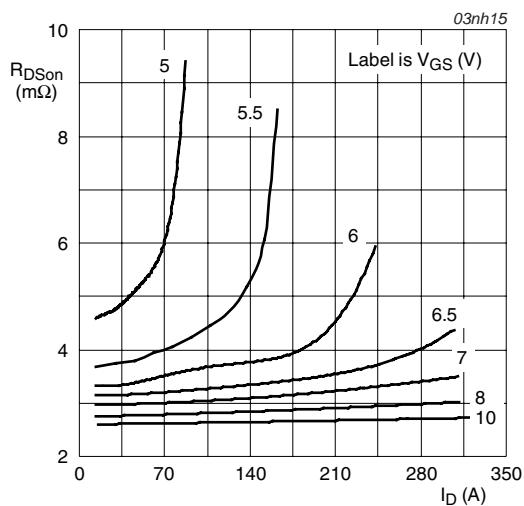
**Fig 8. Forward transconductance as a function of drain current; typical values**



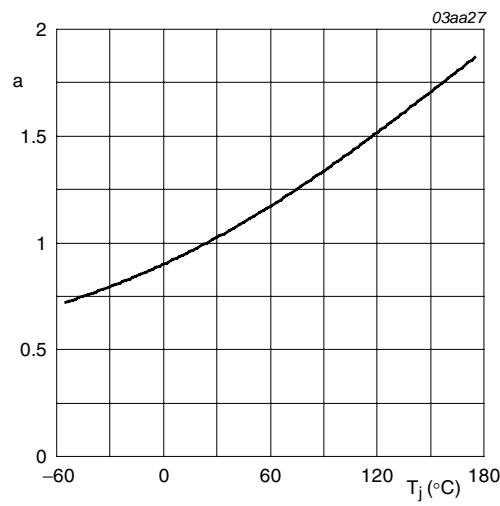
**Fig 9.** Transfer characteristics: drain current as a function of gate-source voltage; typical values



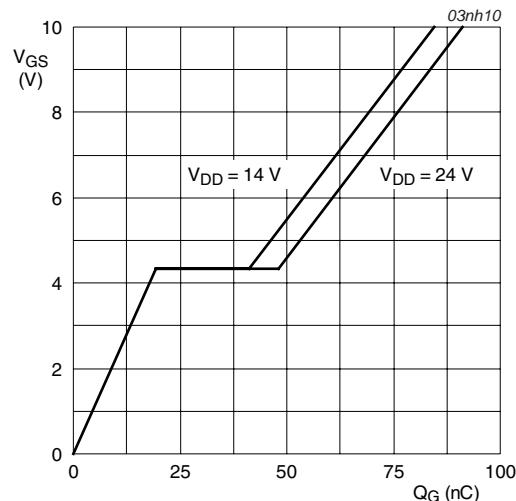
**Fig 10.** Gate-source threshold voltage as a function of junction temperature



**Fig 11.** Drain-source on-state resistance as a function of drain current; typical values

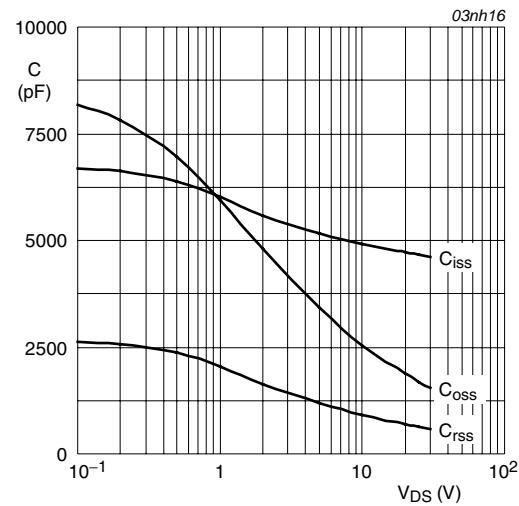


**Fig 12.** Normalized drain-source on-state resistance factor as a function of junction temperature



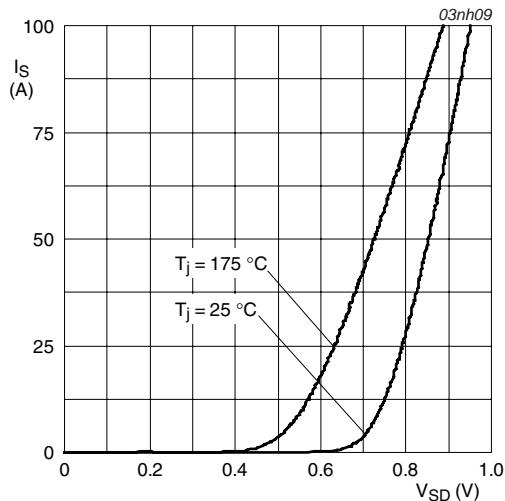
$T_j = 25^\circ\text{C}; I_D = 25\text{A}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



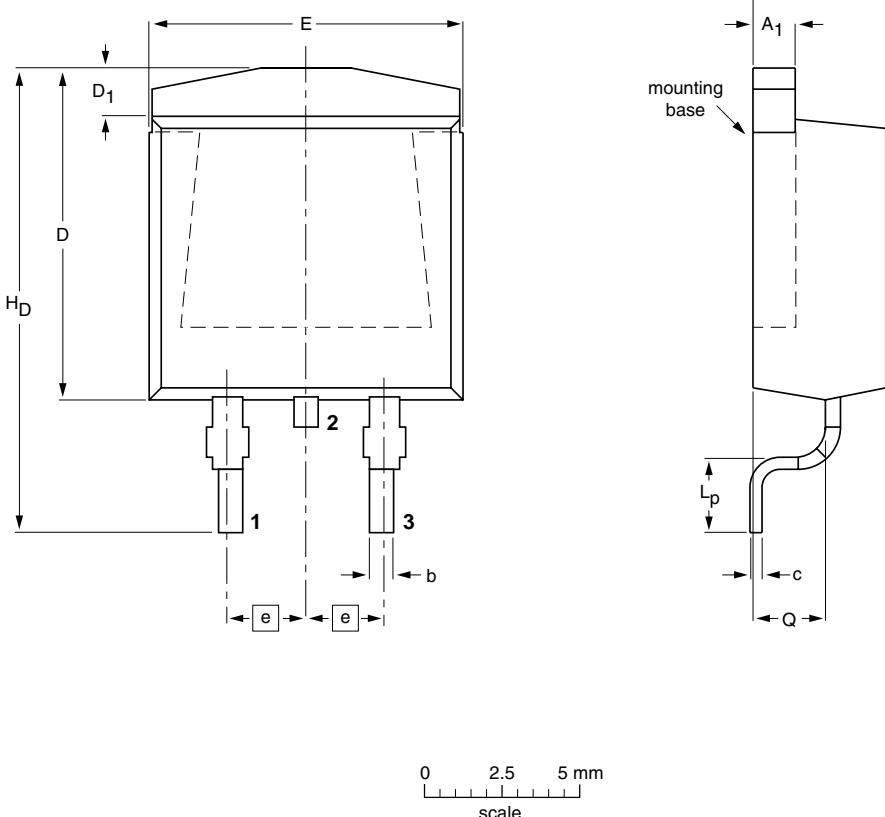
$V_{GS} = 0\text{V}$

**Fig 15. Source current as a function of source-drain voltage; typical values**

## 7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



### DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	c	D <sub>max.</sub>	D <sub>1</sub>	E	e	L <sub>p</sub>	H <sub>D</sub>	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 16. Package outline SOT404 (D2PAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK762R7-30B v.4	20100608	Product data sheet	-	BUK75_76_7E2R7_30B v.3
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number BUK762R7-30B separated from data sheet BUK75_76_7E2R7_30B v.3.</li></ul>			
BUK75_76_7E2R7_30B v.3 (9397 750 12048)	20031013	Product data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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