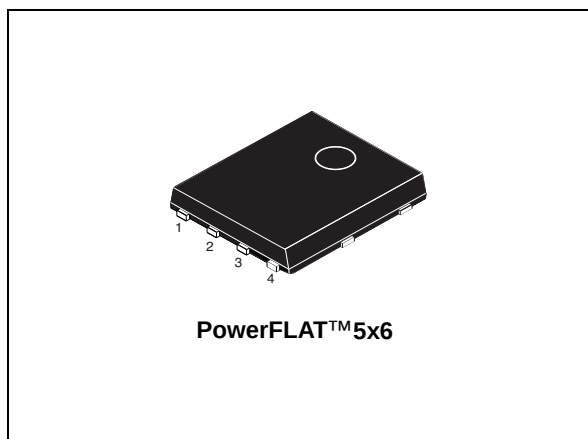


Automotive-grade N-channel 100 V, 0.008 Ω typ., 16 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data



Features

Order code	V_{DS}	$R_{DS(on)max}$	I_D	P_{TOT}
STL92N10F7AG	100 V	0.0095 Ω	16 A	5 W

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent figure of merit (FoM)
- Low C_{RSS}/C_{ISS} ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Figure 1. Internal schematic diagram

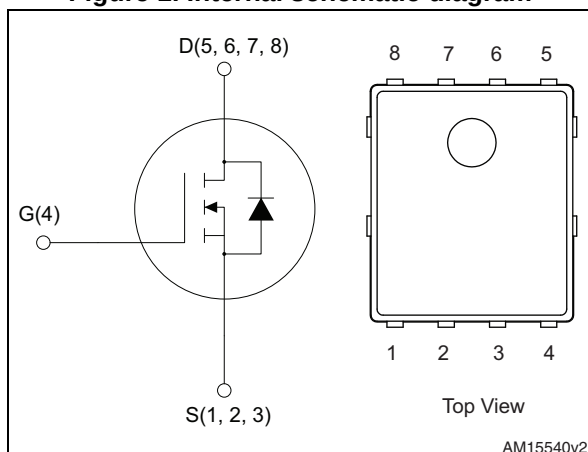


Table 1. Device summary

Order code	Marking	Package	Packaging
STL92N10F7AG	92N10F7	PowerFLAT™ 5x6	Tape and reel

Contents

1 **Electrical ratings** 3

2 **Electrical characteristics** 4

 2.1 Electrical characteristics (curves) 6

3 **Test circuits** 8

4 **Package mechanical data** 9

 4.1 PowerFLAT™ 5x6 WF type R package information 10

 4.2 PowerFLAT™ 5x6 packing information 13

5 **Revision history** 15



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	70	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	50	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	16	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	64	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	5	W
T_{stg}	Storage temperature	-55 to 175 $^\circ\text{C}$	$^\circ\text{C}$
T_j	Operating junction temperature		

1. This value is rated according to R_{thj-c}
2. This value is rated according to $R_{thj-pcb}$
3. Pulse width limited by safe operating area.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case max	1.5	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 100\text{ V}$			1	μA
		$V_{DS} = 100\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 8\text{ A}$		0.008	0.0095	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	3100	-	pF
C_{oss}	Output capacitance		-	700	-	pF
C_{rss}	Reverse transfer capacitance		-	45	-	pF
Q_g	Total gate charge	$V_{DD} = 50\text{ V}$, $I_D = 16\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14)	-	45	-	nC
Q_{gs}	Gate-source charge		-	18	-	nC
Q_{gd}	Gate-drain charge		-	13	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}$, $I_D = 8\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15 and Figure 18)	-	19	-	ns
t_r	Rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time		-	36	-	ns
t_f	Fall time		-	13	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16\text{ A}$, $V_{GS} = 0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 80\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	70		ns
Q_{rr}	Reverse recovery charge		-	125		nC
I_{RRM}	Reverse recovery current		-	3.6		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

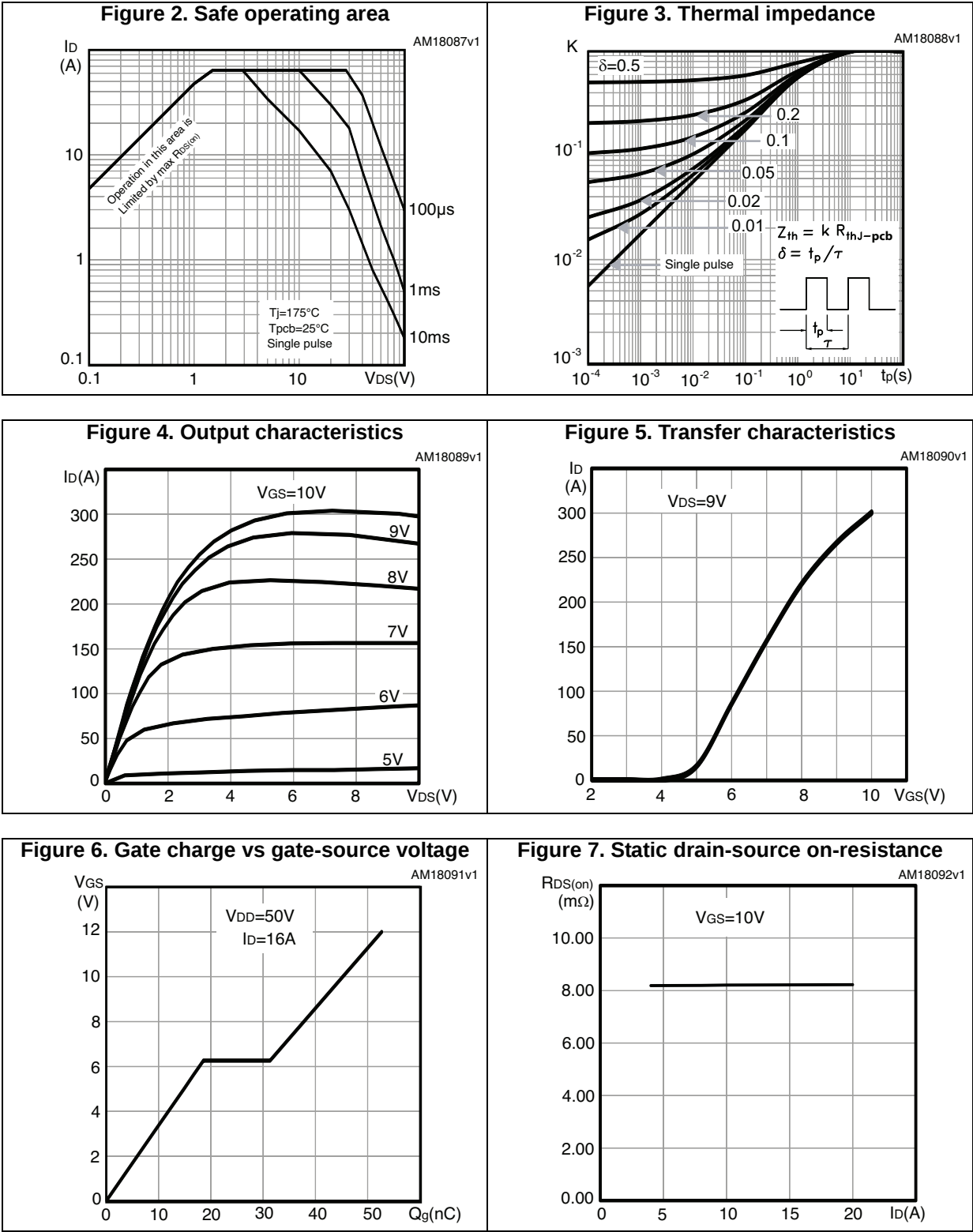


Figure 8. Capacitance variations

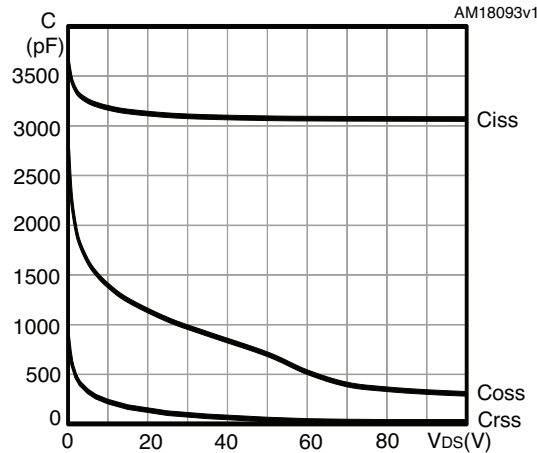


Figure 9. Normalized gate threshold voltage vs temperature

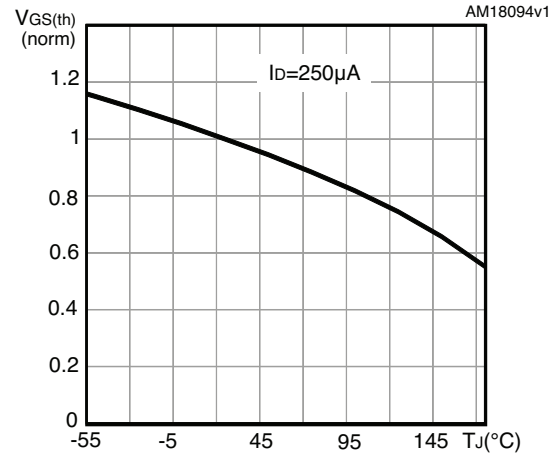


Figure 10. Normalized on-resistance vs temperature

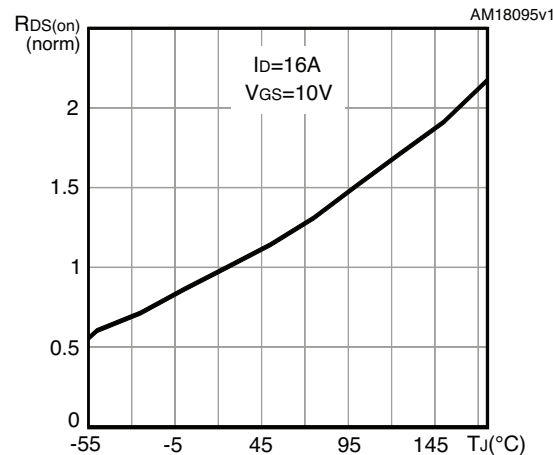


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

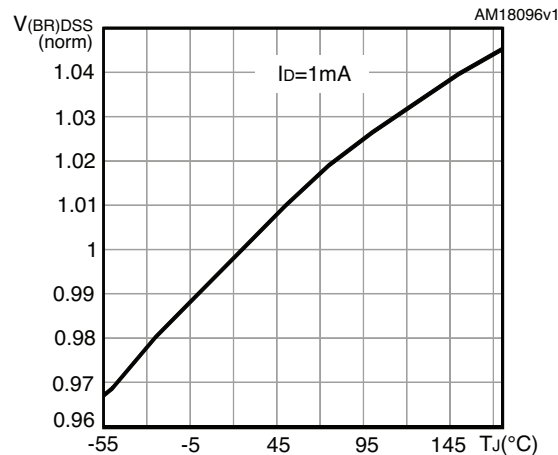
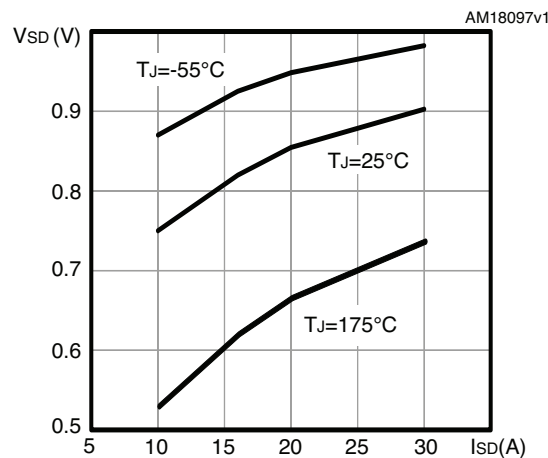


Figure 12. Source-drain diode forward characteristics



AM01468v1

AM01469v1

AM01470v1

AM01471v1

AM01472v1

AM01473v1

4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 19. PowerFLAT™ 5x6 WF type R package outline

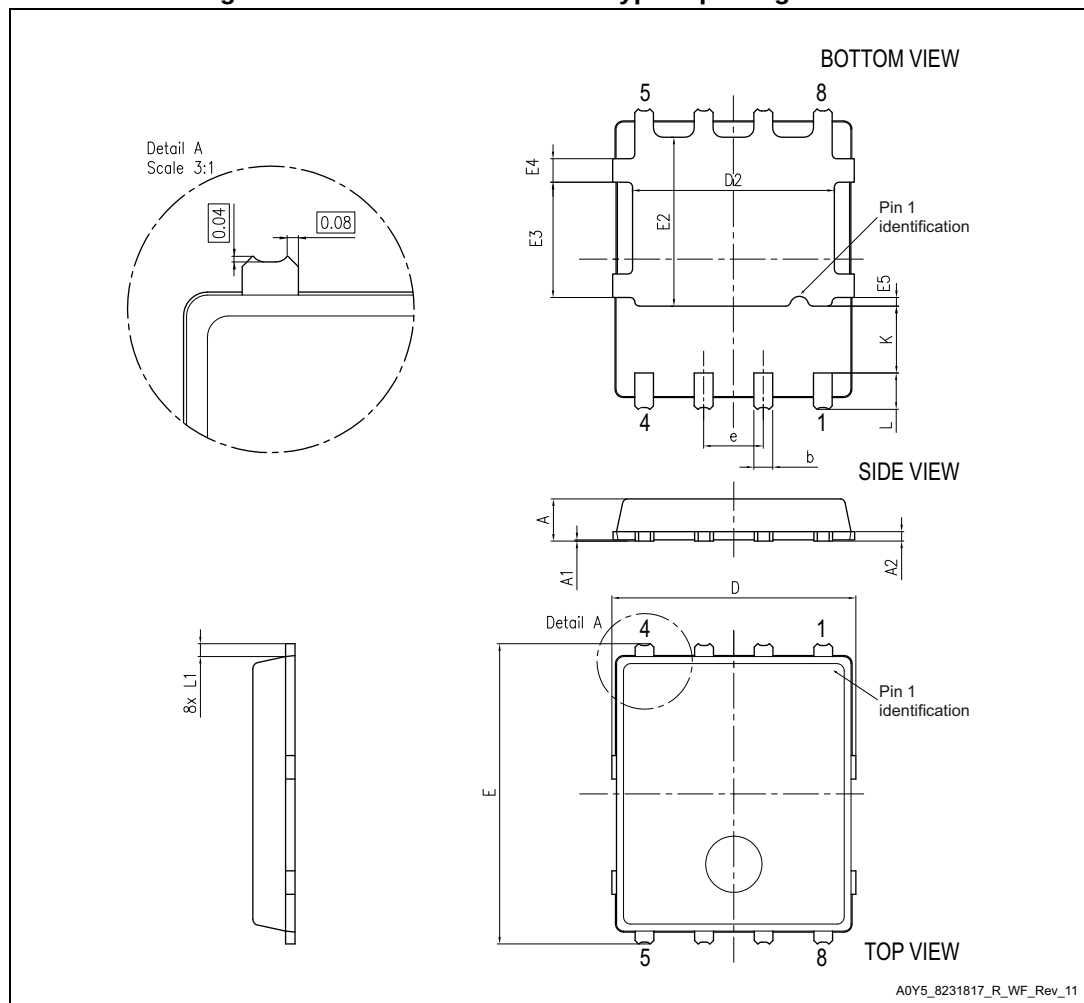
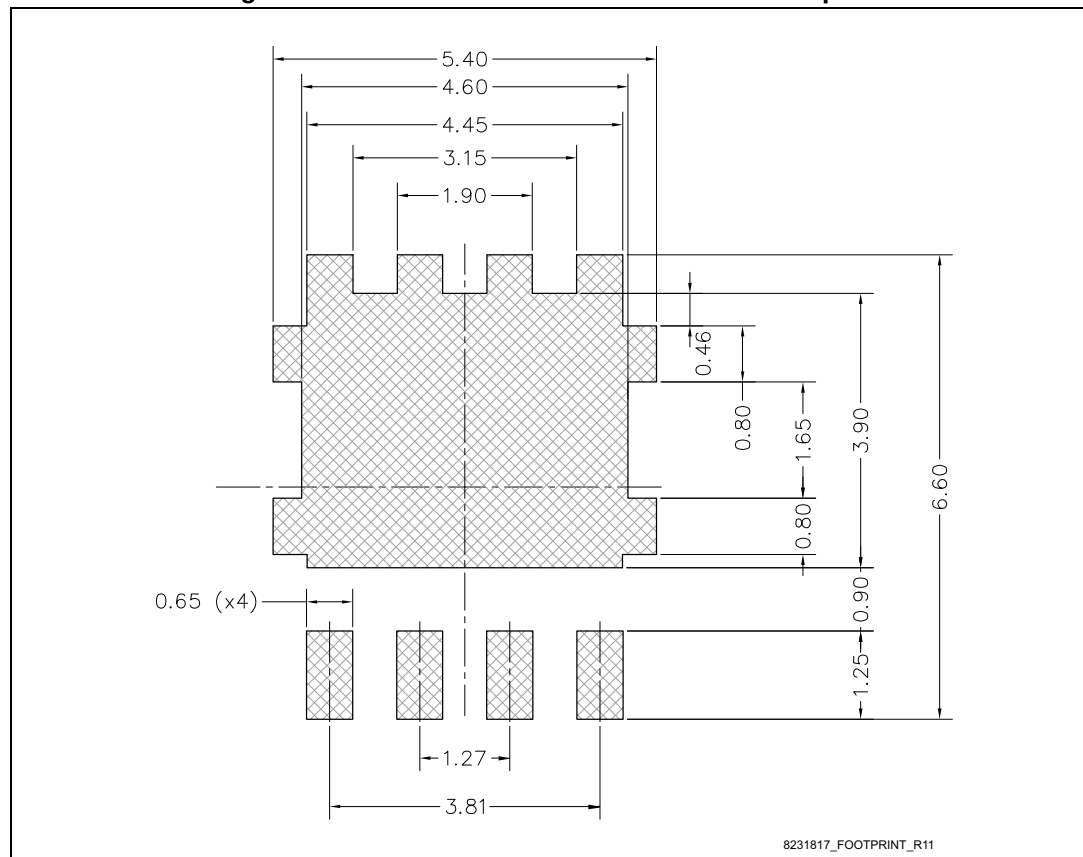


Table 8. PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	4.15		4.45
E2	3.50		3.70
e		1.27	
L	0.70		0.90
L1		0.275	
K	1.275		1.575
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20. PowerFLAT™ 5x6 recommended footprint



4.2 PowerFLAT™ 5x6 packing information

Figure 21. PowerFLAT™ 5x6 type WF tape^(a)

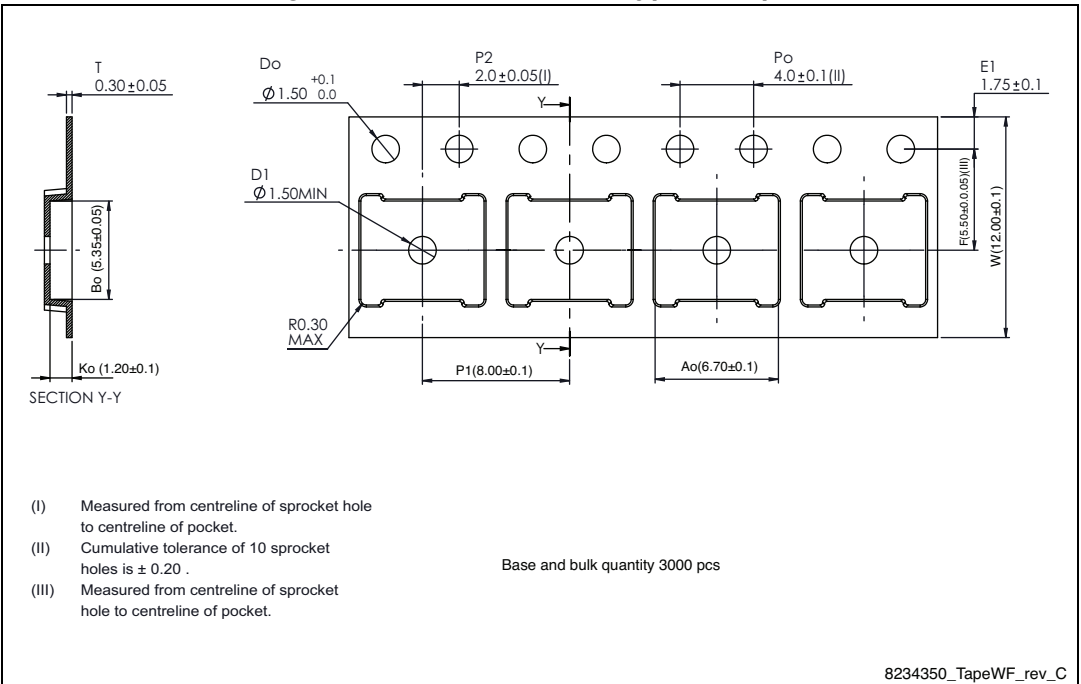
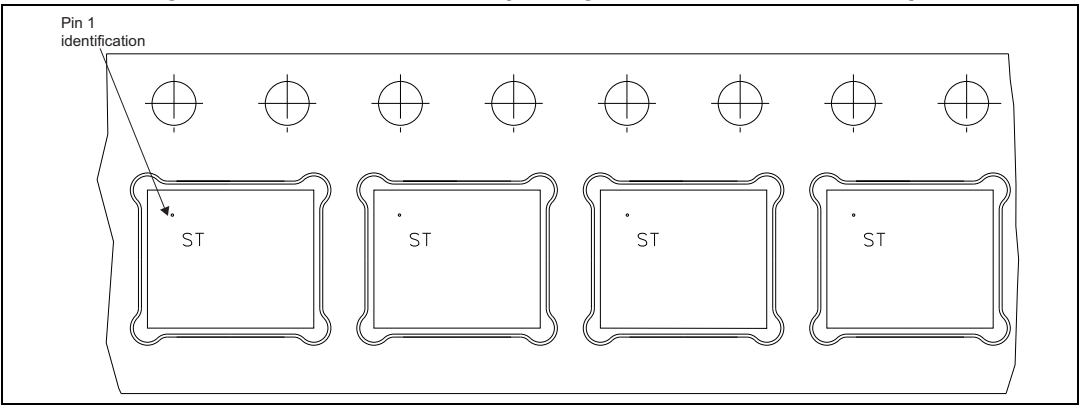


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Technical drawing of a circular ESD floor mat assembly, showing three views: Top View, Side View, and Core Detail.

Top View: A circular mat with a central hole. The outer diameter is 350 (+0/-4.0). The central hole has a diameter of 25.00. The distance from the center to the edge of the cutouts is 11.9/15.4. The mat features six rectangular cutouts arranged symmetrically. The distance between the cutouts is 18.4 (max). The mat is labeled "ESD LOGO".

Side View: Shows the mat's profile. The total thickness is 12.4 (+2/-0). The distance from the top surface to the bottom of the cutouts is 17.8 (+2.0). The distance from the bottom surface to the top of the cutouts is 1.90. The distance from the bottom surface to the top of the mat is 2.50. The mat is labeled "ESD LOGO".

Core Detail: A detailed view of the mat's core. The central hole has a diameter of 13.00. The core diameter is 13.00. The core thickness is 2.30. The core is labeled "CORE DETAIL".

Dimensions:

- Outer Diameter: 350 (+0/-4.0)
- Central Hole Diameter: 25.00
- Distance from Center to Edge of Cutouts: 11.9/15.4
- Distance between Cutouts: 18.4 (max)
- Mat Thickness: 12.4 (+2/-0)
- Distance from Top Surface to Bottom of Cutouts: 17.8 (+2.0)
- Distance from Bottom Surface to Top of Cutouts: 1.90
- Distance from Bottom Surface to Top of Mat: 2.50
- Core Diameter: 13.00
- Core Thickness: 2.30

All dimensions are in millimeters.

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Oct-2014	1	First release.
12-Oct-2015	2	Updated: Section 4.1: PowerFLAT™ 5x6 WF type R package information Datasheet promoted from preliminary data to production data Minor text changes

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved