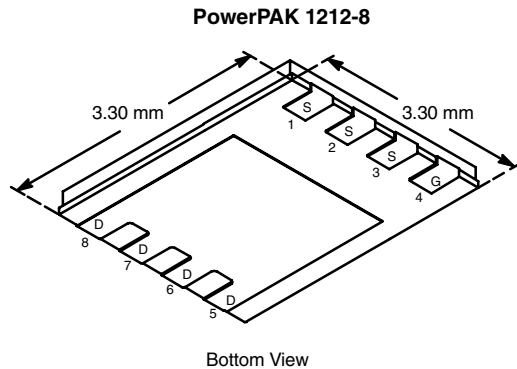


N-Channel 30-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ)
30	0.0075 @ $V_{GS} = 10$ V	18.3	12.5
	0.010 @ $V_{GS} = 4.5$ V	15.9	



Ordering Information: Si7114DN-T1
Si7114DN-T1—E3 (Lead (Pb)-Free)

FEATURES

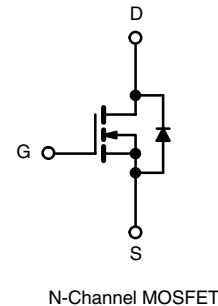
- TrenchFET® Gen II Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100% R_g Tested



RoHS
COMPLIANT
Available

APPLICATIONS

- Synchronous Rectification



ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	18.3	11.7	A
	T _A = 70°C		14.7	9.4	
Pulsed Drain Current		I _{DM}	60		
Continuous Source Current (Diode Conduction) ^a		I _S	3.2	1.3	
Single Avalanche Current	L = 0.1 mH	I _{AS}	29		A
Single Avalanche Energy		E _{AS}	42		mJ
Maximum Power Dissipation ^a	T _A = 25°C	P _D	3.8	1.5	W
	T _A = 70°C		2.0	0.8	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{b,c}			260		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	24	33	$^\circ\text{C/W}$
	Steady State		65	81	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.9	2.4	

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- See Solder Profile (<http://www.vishay.com/doc?73257>). The PowerPAK 1212-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

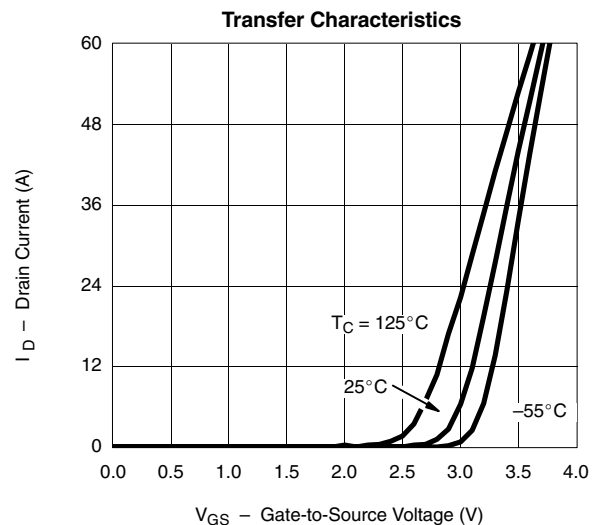
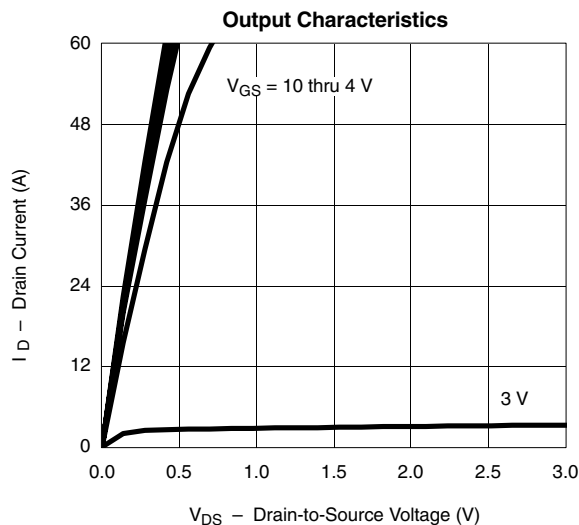
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}$, $V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$			1	μA
		$V_{DS} = 30\ \text{V}$, $V_{GS} = 0\ \text{V}$, $T_J = 55^\circ\text{C}$			5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\ \text{V}$, $V_{GS} = 10\ \text{V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 18.3\ \text{A}$		0.0062	0.0075	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 15.9\ \text{A}$		0.0081	0.010	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\ \text{V}$, $I_D = 18.3\ \text{A}$		77		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 3.2\ \text{A}$, $V_{GS} = 0\ \text{V}$		0.7	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 15\ \text{V}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 18.3\ \text{A}$		12.5	19	nC
Gate-Source Charge	Q_{gs}			6.3		
Gate-Drain Charge	Q_{gd}			3.6		
Gate-Resistance	R_g	$f = 1\ \text{MHz}$	0.7	1.4	2.1	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 15\ \Omega$ $I_D \cong 1\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_g = 6\ \Omega$		10	15	ns
Rise Time	t_r			10	15	
Turn-Off Delay Time	$t_{d(off)}$			45	70	
Fall Time	t_f			10	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.2\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		30	60	
Body Diode Reverse Recovery Charge	Q_{rr}	$I_F = 3.2\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$		19	38	nc

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

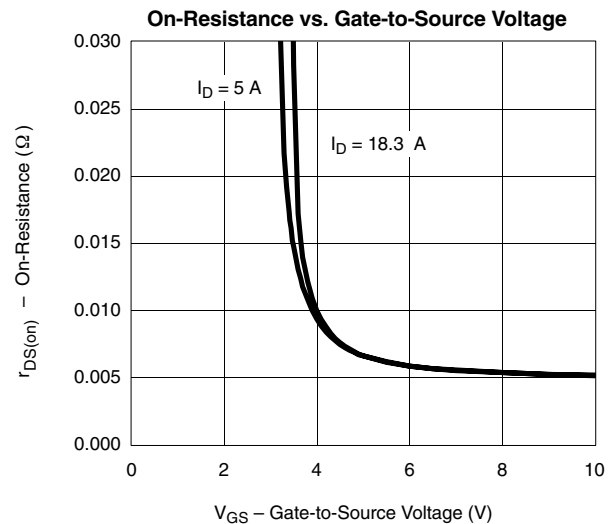
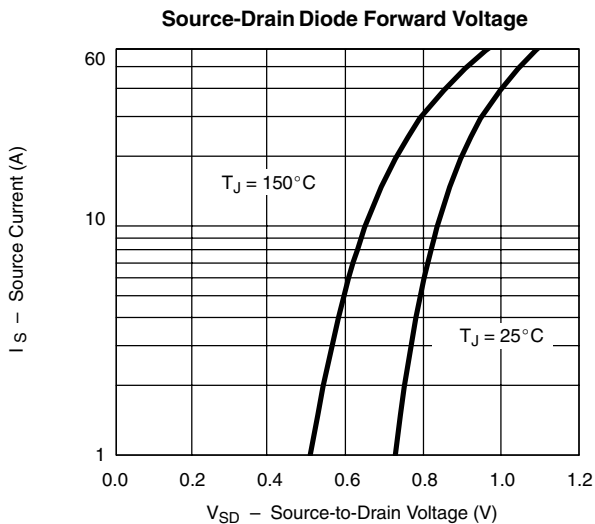
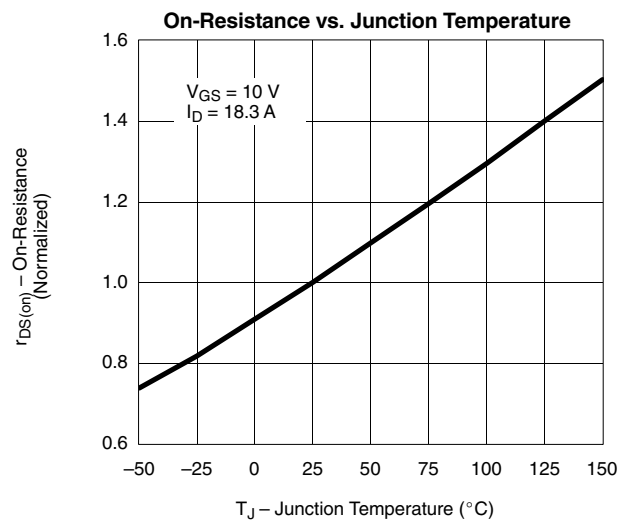
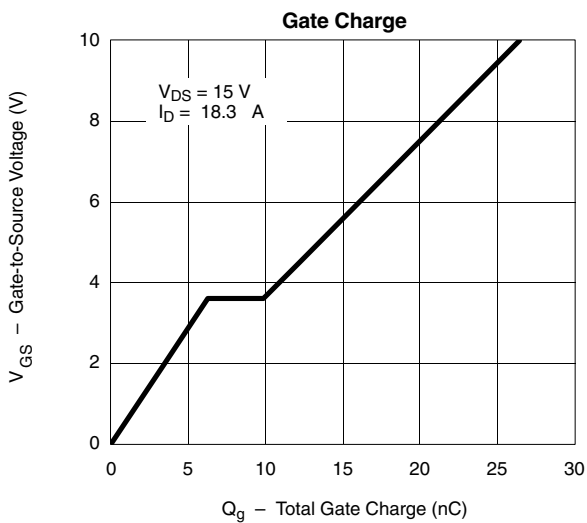
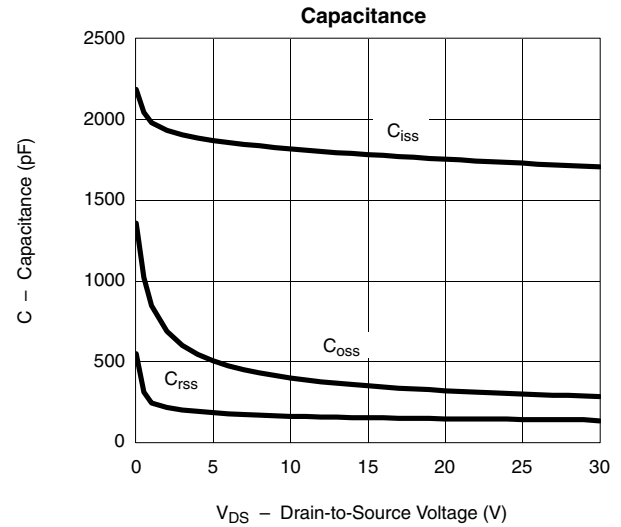
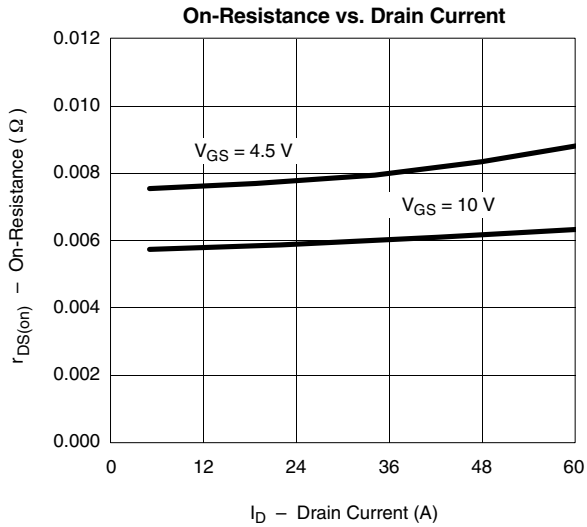
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

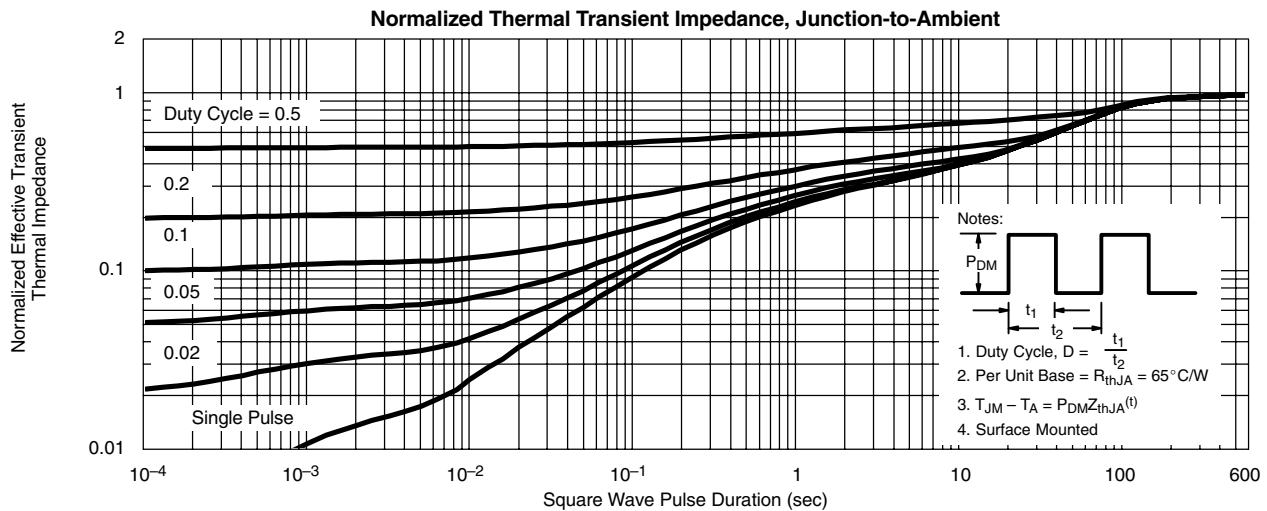
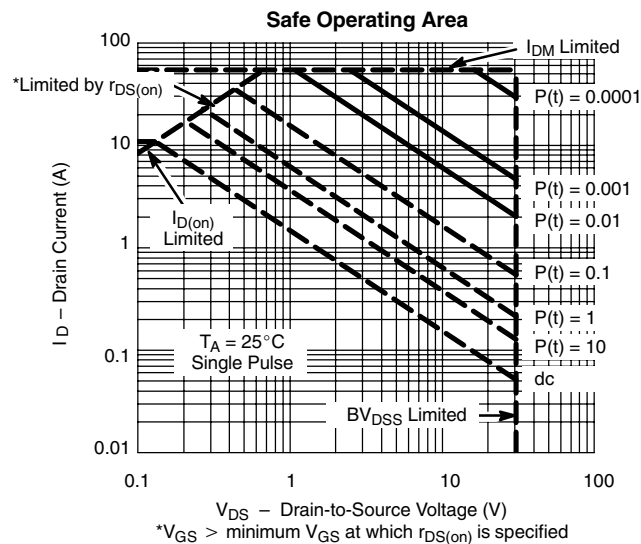
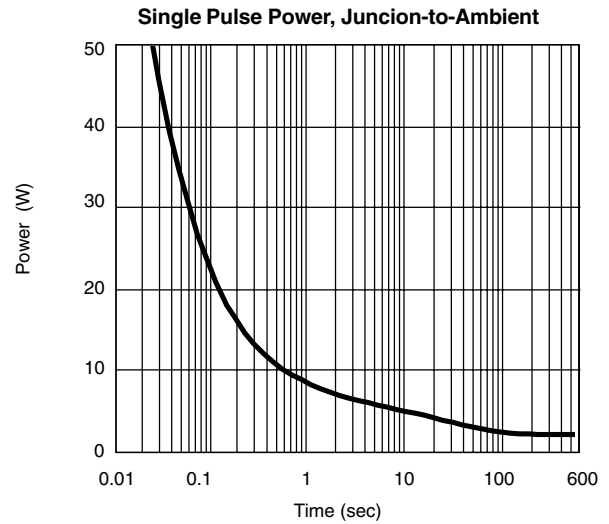
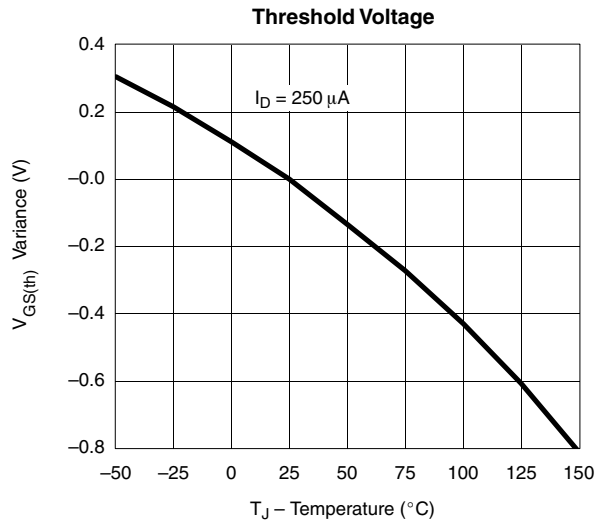




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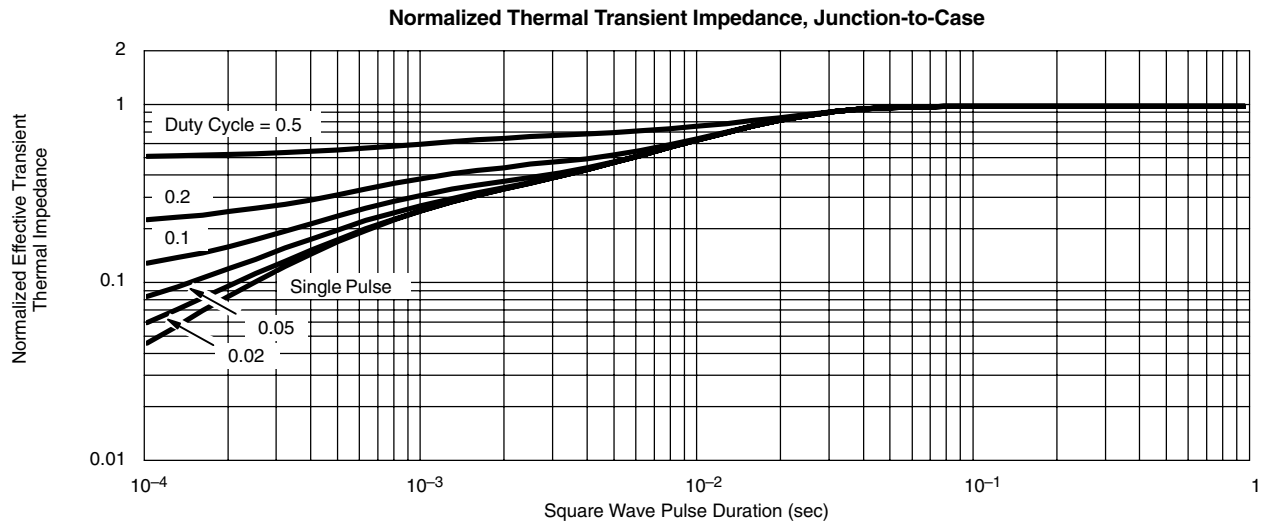


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?73039>.



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