QPF4518M

Wi-Fi Front End Module

Product Overview

The Qorvo® QPF4518M is an integrated front end module (FEM) designed for Wi-Fi 802.11a/n/ac systems. The compact form factor and integrated matching minimizes layout area in the application.

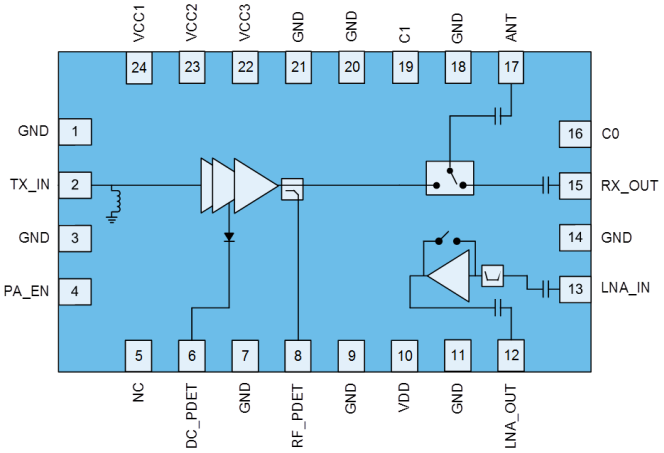
Performance is focused on optimizing the PA for a 5V supply voltage that conserves power consumption while maintaining the highest linear output power and leading edge throughput.

The receive path is pinned out so external filtering can be added in the optimal position. Integrated die level filtering for 2nd and 3rd harmonics as well as 2.4 GHz rejection for DBDC operation are included.

There are two options for power detect, a DC power detector which has voltage output and an RF power detector with an RF output from a directional coupler.

The QPF4518M integrates a 5 GHz power amplifier (PA), single pole two throw switch (SP2T) and bypassable low noise amplifier (LNA) into a single device

Functional Block Diagram



Top View

24 Pin 5x3 mm QFN Package

Key Features

- 5150 – 5925 MHz
- P_{OUT} = +23dBm MCS9 VHT80 -35dB Dynamic EVM
- P_{OUT} = +24.5dBm MCS7 HT20/40 -30dB Dynamic EVM
- P_{OUT} = +25dBm MCS0 HT20 Spectral Mask Compliance
- 160MHz Bandwidth and MCS11 Capable
- Optimized for +5 V Operation
- 32 dB Tx Gain
- 2 dB Noise Figure
- 16 dB Rx Gain & 6.5 dB Bypass Loss
- 25 dB 2.4 GHz Rejection on Rx Path
- Integrated RF Power Detector Coupler as well as DC Power Detector

Applications

- Access Points
- Wireless Routers
- Residential Gateways
- Customer Premise Equipment
- Internet of Things

Ordering Information

Part Number	Description
QPF4518MSB	Sample bag with 5 pieces
QPF4518MSQ	Sample bag with 25 pieces
QPF4518MSR	7” reel with 100 pieces
QPF4518MTR13	13” reel with 2,500 pieces
QPF4518MPCK401	Assembled Evaluation Board + 5 pcs

Absolute Maximum Ratings

Parameter	Conditions	Rating
DC Supply Voltage		-0.5 to +6 V
Control Voltage		-0.5 to +6 V
Storage Temperature		-40 to 150 °C
Junction Temperature	MTTF > $1.5x10^6$ hours MTTF > $1.0x10^6$ hours	160 °C 170 °C
RF Input Power at TX_IN	Into 50 Ω Load for 802.11a/n/ac (No Damage), Transmit Mode	+10 dBm
RF Input Power at ANT	(No Damage), Receive LNA On Mode	+15 dBm
RF Input Power at ANT	(No Damage), Receive Bypass Mode	+28 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. This is an InGaP device designed for high duty cycle applications with Tj>30 °C over ambient.

Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Frequency	5150		5850	MHz
Extended Operating Frequency	5150		5925	MHz
Device Voltage (V_{CC} & V_{DD})	+4.5	+5	+5.25	V
Control Voltage – High (PA_EN, C0 & C1)	+1.8	+3	V_{CC}	V
Control Voltage – Low (PA_EN, C0 & C1)	0		+0.4	V
$T_{OPERATING}$*	-40		+85	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions. * $T_{OPERATING}$ is temperature at package ground.

Electrical Specifications

Parameter	Conditions	Min.	Typ.	Max.	Units
Transmit (TX_IN-ANT) Mode	**Unless otherwise noted: V_{CC}=5V, T=+25ºC, PA_EN=High, C0=Low, C1=High, Only through path between RX_OUT and LNA_IN**				
11ac VHT80 Output Power	MCS11 1024QAM		20		dBm
Dynamic EVM				-40	dB
11ac VHT160 Output Power	MCS9 256QAM		22		dBm
				-35	dB
11ac VHT80 Output Power	MCS9 256QAM	22	23		dBm
Dynamic EVM				-35	dB
11n HT20/40 Output Power	MCS7 64QAM	23.5	24.5		dBm
Dynamic EVM				-30	dB
Margin to VHT80 Spectral Mask	P_{OUT} = +24 dBm, 11ac MCS0		6	3	dBc
Margin to VHT20 Spectral Mask	P_{OUT} = +25 dBm, 11n MCS0		6	3	dBc
Gain		30	32		dB

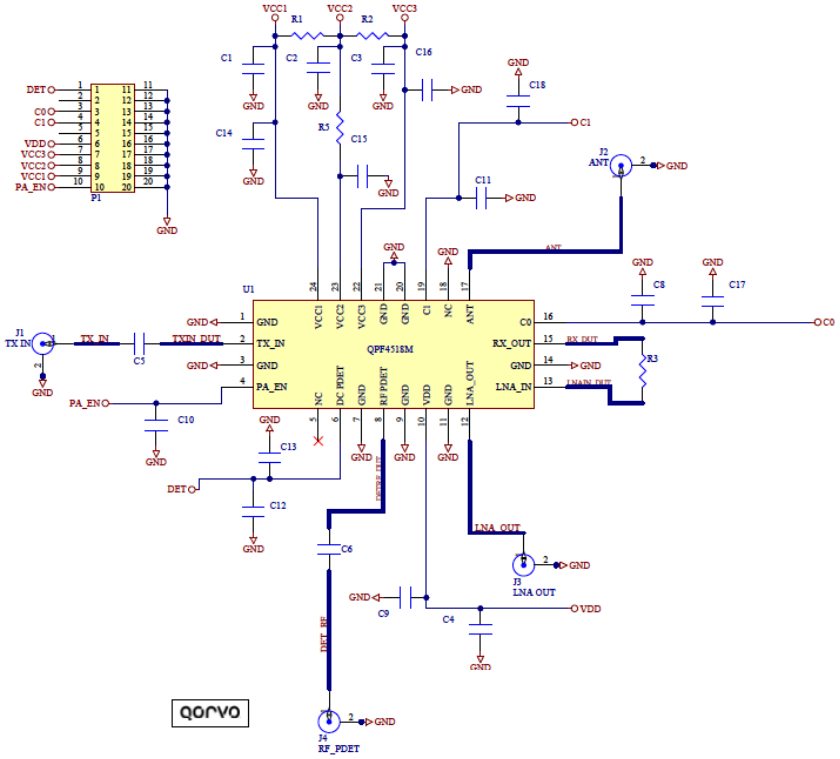
Parameter	Conditions	Min.	Typ.	Max.	Units
Gain Flatness	Across any 80 MHz Channel	-0.5		+0.5	dB
Out of Band Gain	*f* = 3300-3800MHz			-5	dB
	f > 7000MHz			7	dB
TX_IN Port Return Loss		6	10		dB
ANT Port Return Loss		7	10		dB
Quiescent Current	RF Off		140	155	mA
Operating Current	P_{OUT} = +23 dBm		280	320	mA
	P_{OUT} = +24.5 dBm		320	365	mA
2nd Harmonics	P_{OUT} = +27 dBm 802.11a 6 MBps		-50	-45	dBm/MHz
3rd Harmonics	P_{OUT} = +27 dBm 802.11a 6 MBps		-50	-45	dBm/MHz
ANT-LNA_OUT Isolation		35	40		dB
RF Power Detect Coupling		16	18		dB
DC Power Detect Voltage	RF Off		0.25		V
	P_{OUT} = +20 dBm		0.55		V
	P_{OUT} = +23 dBm		0.70		V
	P_{OUT} = +27 dBm		0.95		V
RECEIVE (ANT-LNA_OUT) LNA ON MODE	**Unless otherwise noted: V_{CC}=5V, T=+25ºC, PA_EN=Low, C0=High, C1=Low, Only through path between RX_OUT and LNA_IN**				
Gain		14	16		dB
Gain Flatness Across any 80 MHz Channel		-0.1		+0.1	dB
Out of Band Gain	*f* = 2400-2500 MHz		-25	-20	dB
Noise Figure			2	2.4	dB
LNA_OUT Port Return Loss		10	15		dB
ANT Port Return Loss		7	12		dB
Input P_{1dB}			-7		dBm
Input IP3		+3	+6		dBm
Rx Operating Current			15	25	mA
RECEIVE (ANT-LNA_OUT) BYPASS MODE	**Unless otherwise noted: V_{CC}=5V, T=+25ºC, PA_EN=Low, C0=High, C1=High, Only through path between RX_OUT and LNA_IN**				
Bypass Loss		5	6.5	8	dB
Loss Flatness Across any 80 MHz Channel		-0.1		+0.1	dB
Out of Band Gain	*f* = 2400-2500 MHz		-25	-20	dB
LNA_OUT Port Return Loss		10	14		dB
ANT Port Return Loss		7	10		dB
Input P_{1dB}		+25	+28		dBm
Input IP3		+33	+40		dBm
GENERAL SPECIFICATIONS	**Unless otherwise noted: V_{CC}=5V, T=+25ºC, Only through path between RX_OUT and LNA_IN**				
FEM Leakage Current			10	25	µA
Control Current - High			20	40	µA
Control Current - Low				1	µA
TX Output P_{1dB}	CW		+32		dBm
Ramp ON/OFF Time	10<->90% Ref from Control Voltage to RF Power		200		nS

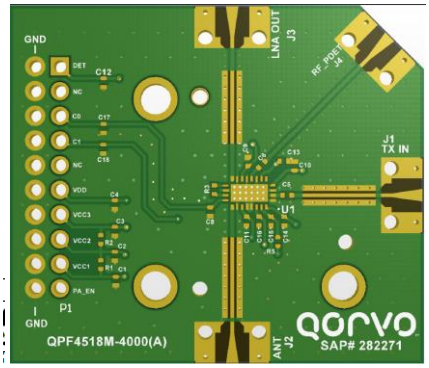
Parameter	Conditions	Min.	Typ.	Max.	Units
PA Stability - Output VSWR	CW No Spurious above -41.25dBm/MHz		10:1		
Output Power Range		0		27	dBm
Thermal Resistance, θ_{jc}	Junction to case		25		°C/W

Logic Truth Table

Mode	PA_EN	C0	C1
Standby	Low	Low	Low
Transmit	High	Low	High
LNA On	Low	High	Low
Bypass	Low	High	High

Evaluation Board Schematic and Layout

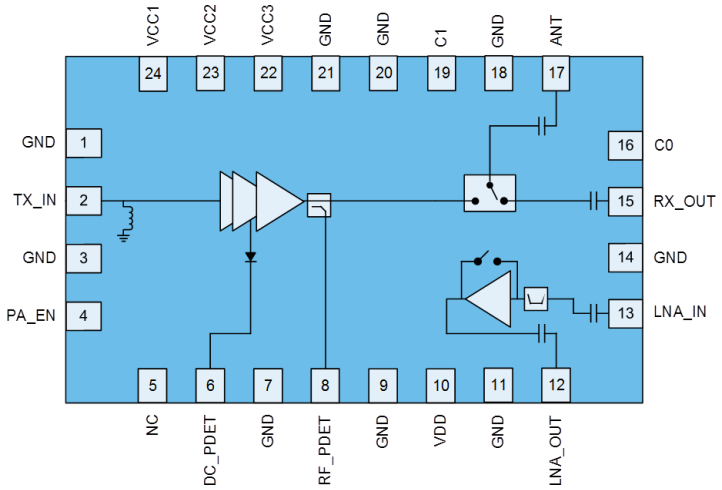




Bill of Material

Ref. Des.	Value	Description	Manuf.	Part number
-	-	Printed Circuit Board		
U1	-	5GHz Wi-Fi Front End Module	Qorvo	QPF4518M
C5, C6, C13	10 pF	Capacitor, Chip, 5%, 50V, C0G, 0402	Murata	GRM1555C1H100JA01D
C8,C9, C10, C11	1000 pF	Capacitor, Chip, 10%, 50V, X7R, 0402	Murata	GRM155R71H102KA01D
C14, C15, C16	2.2 µF	Capacitor, Chip, 10%, 6.3V, X5R, 0402	Taiyo Yuden	RM JMK105BJ225KV-F
R3, R5	0 Ω	Resistor, Chip, 5%, 1/10W, 0402	Kamaya	RMC1/16SJPTH
C1, C2, C3, C4, C12, C17, C18, R1, R2	-	Do Not Install		

Pin Configuration and Description

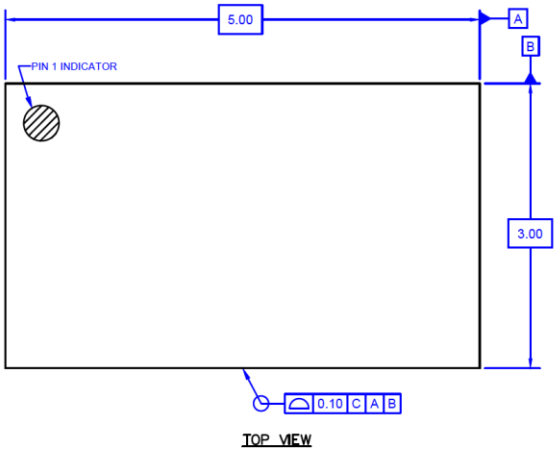


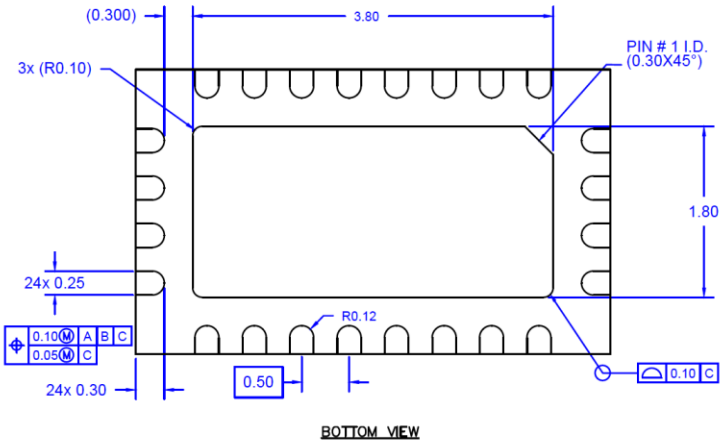
Top View

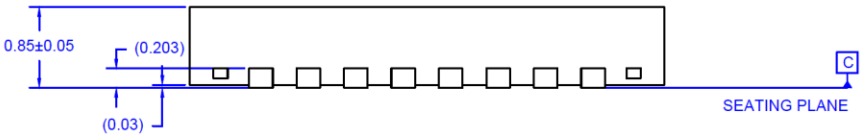
Pin Number	Label	Description
1	GND	Ground connection.
2	TX_IN	RF input. Internally matched to 50 Ω and DC Shorted.
3	GND	Ground connection.
4	PA_EN	Input enable bias voltage (Regulated internally)
5	NC	No electrical connection. It may be left floating or connected to ground.
6	DC_PDET	DC power detector. Provides an output voltage proportional to the RF output power level
7	GND	Ground connection.
8	RF_PDET	RF power detector. Provides an RF output proportional to the RF output power level
9	GND	Ground connection.
10	VDD	LNA supply voltage
11	GND	Ground connection.
12	LNA_OUT	RF output from the low noise amplifier. Internally matched to 50 Ω and DC blocked.
13	LNA_IN	RF input to the low noise amplifier. Internally matched to 50 Ω and DC blocked.
14	GND	Ground connection.
15	RX_OUT	RF output from the RX branch of the T/R switch. Internally matched to 50 Ω and DC blocked.
16	C0	Switch control pin 0
17	ANT	RF bi-directional antenna port. Internally matched to 50 Ω and DC blocked.
18	GND	Ground connection.
19	C1	Switch control pin 1
20	GND	Ground connection.
21	GND	Ground connection.
22	VCC3	3rd stage supply voltage
23	VCC2	2nd stage supply voltage
24	VCC1	1st stage supply voltage
Backside Paddle	GND	RF/DC ground. Use recommended via pattern to minimize inductance and thermal resistance. See PCB Mounting Pattern for suggested footprint.

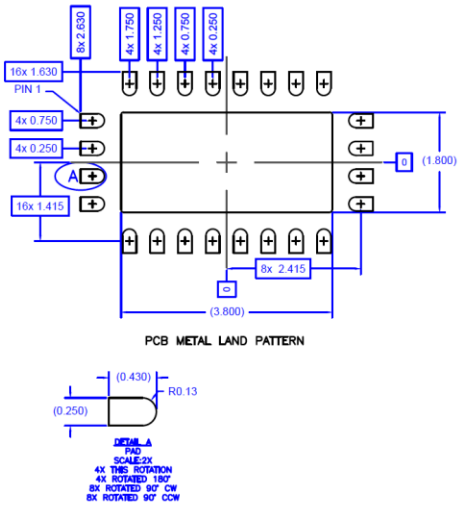
Mechanical Information

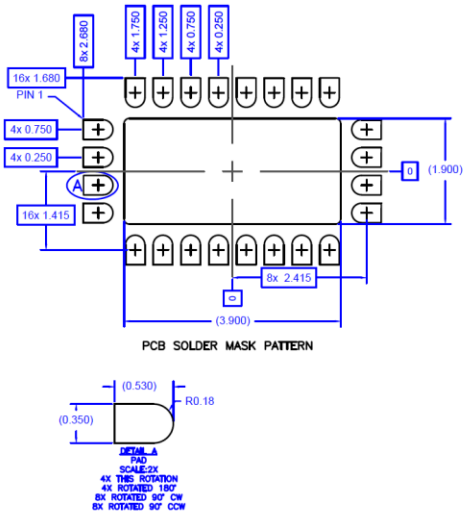
Dimensions and PCB Mounting Pattern

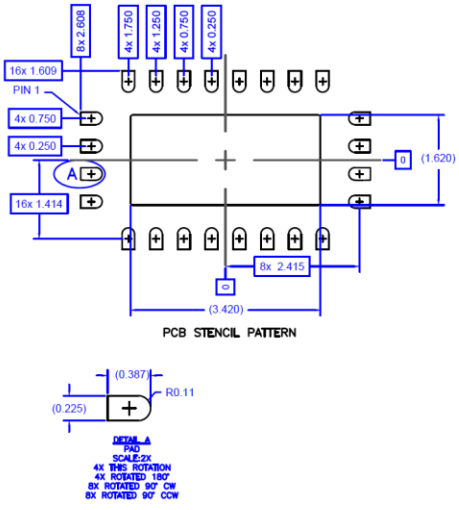












Thermal vias for center slug should be incorporated into the PCB design. The number and size of thermal vias will depend on the application, the power dissipation, and the electrical requirements. Example of the number and size of vias can be found on the evaluation board layout.

Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1B	JEDEC JS-002-214
ESD – Charged Device Model (CDM)	Class III	JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 2	JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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