TLE 8718 SA

Smart 18-Channel Lowside Switch with Micro Second Bus

Data Sheet

Rev. 1.1, 2012-07-31

Automotive Power

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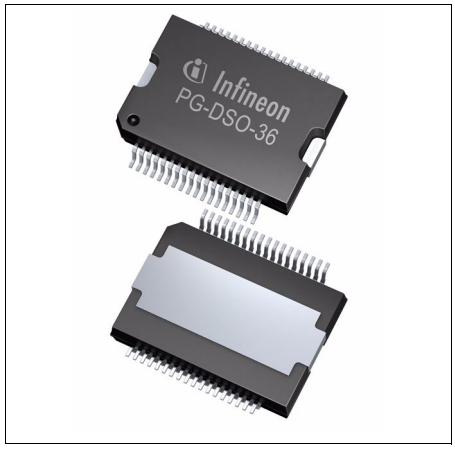
1 Overview



PG-DSO-36

Features

- Operating Conditions -40...150°C
- Over Temperature Warning
- ESD Capability 2/4KV HBM on-/off board Pins
- Short Circuit Protected for V_{BAT} = 36V
- Active Zener Clamping at typically 55V
- Open Load, Short to Ground, Short Circuit Diagnosis (2 bit/OUT)
- Output control, diagnostics and initialisation via high speed serial communication: Micro Second Channel [MSC]
- all Pins protected against ≤36V
- Over-Voltage and Under-Voltage Monitoring
- Two Output Channels operating during low supply voltage possible
- Programmable Short circuit behavior: switch off or current limitation
- Green Product (RoHS compliant)
- AEC Qualified

Application

- Automotive Engine Management Applications
- Driver IC for inductive and ohmic actuators, such as Injectors, Solenoids, Relays, Lambda Heater.

Table 1 Output Stage Overview and Product Summary

Output	Maximum current	RON_max at Tj = 150°C without clamping
OUT1, OUT3	8A	200mΩ
OUT2, OUT4	3A	350mΩ
OUT5...OUT8	2.2A	720mΩ
OUT9...OUT10	2.2A	470mΩ
OUT11...OUT14	2.2A	720mΩ
OUT15, OUT16	0.6A	2400mΩ
OUT17, OUT18	0.6A	2400mΩ
Operating Voltage	V_{DD_RES}	2.5V (defined behavior of the device)
	V_{DD_POR}	3...3.5V (OUT15,16 delayed switch-off)
	V_{DD}	4.5...5.5V (operating range)
Active Zener Voltage	$V_{DS\ (AZ)}$	50...60V

Type	Package	Marking
TLE8718SA	PG-DSO-36	TLE8718SA

1.1 Device Description

All stages are controlled by MSC interface. The MSC interface can be single ended or low voltage differential type.

Serial transmission of the error code (diagnostic) via MSC interface (upstream channel).

All power stages (PS) are protected against short circuit to battery voltage (SCB). All PS (OUT1...18) are equipped with switch off mode and current control mode in case of SCB (configurable).

Diagnosis of open load (OL), short-circuit to ground (SCG), short-circuit to battery voltage (SCB) and over temperature (DOT) individually for each PS.

The fault conditions SCB, SCG, OL and DOT are not stored until an integrated filtering time has expired. If, at one output, several errors occur in a sequence, always the last detected error is stored (after filtering time). All fault conditions are encoded in two bits per stage and stored in the corresponding MSC interface registers. Additionally there is one common diagnostic bit for fault occurrence (FAILURE_FLAG) at any output and one common diagnostic bit (COTW) for diagnosis over temperature (DOT). The diagnostic registers can be read via MSC interface. During the start-bit of a read out cycle the corresponding diagnostic register is cleared, nevertheless the status of the diagnostic register before the start-bit is send. Pull-down Diagnostic currents and Open Load OL can be switched off by configuration for OUT11...18; (CONREG3 and OUT1516).

Each stage (OUT1...14, 17, 18) is controlled with a separate bit of the data frame (downstream channel). The control bit is non inverting, i.e. if a control bit is ‘1’ the corresponding stage is off. Stages are disabled – i.e. switched off and switching on disabled if V_{DD} is too low (V_{DD} undervoltage or power on reset) or V_{DD} too high (V_{DD} overvoltage). The same applies when the MSC monitoring detects an error, micro controller reset is active (i.e. external signal on pin RST = low or external signal on Pin ABE is logical low level).

All outputs are designed with internal zener diodes for applications with inductive loads.

OUT1 and OUT3 are designed for normal operation with 4A and extended current of 8A for maximum of 200 seconds each vehicle driving cycle.

OUT5...OUT10 are disabled by active low level on pins DIS5_10 (with short delay).

OUT9 and OUT10 are designed for actuators with higher clamping energy.

OUT15 and OUT16 can be forced OFF with the higher thresholds of DELAYIN ($V_{DELAYIN_RES15_16_L}$ and $V_{DELAYIN_RES15_16_H}$) (see **Figure 8**). OUT15 and OUT16 can be configured to delayed reset behavior, in this case, the switching-off algorithm is delayed by internal filtering time (exception: power on reset (POR), RES15_16 and valid command frame to switch off stages is not delayed).

Parallel connection of stages (OUT1...14, 17, 18) is possible as the control bits that switch on and off these stages are all transmitted in the same data frame. OUT15 and OUT16 are only allowed to be connected to each other and not to other stages (see **Chapter 5.10**).

DELAYOUT is pulled active low to switch off external components by the lower thresholds of DELAYIN ($V_{DELAYIN_L}$ and $V_{DELAYIN_H}$), ABE or V_{DD} monitoring.

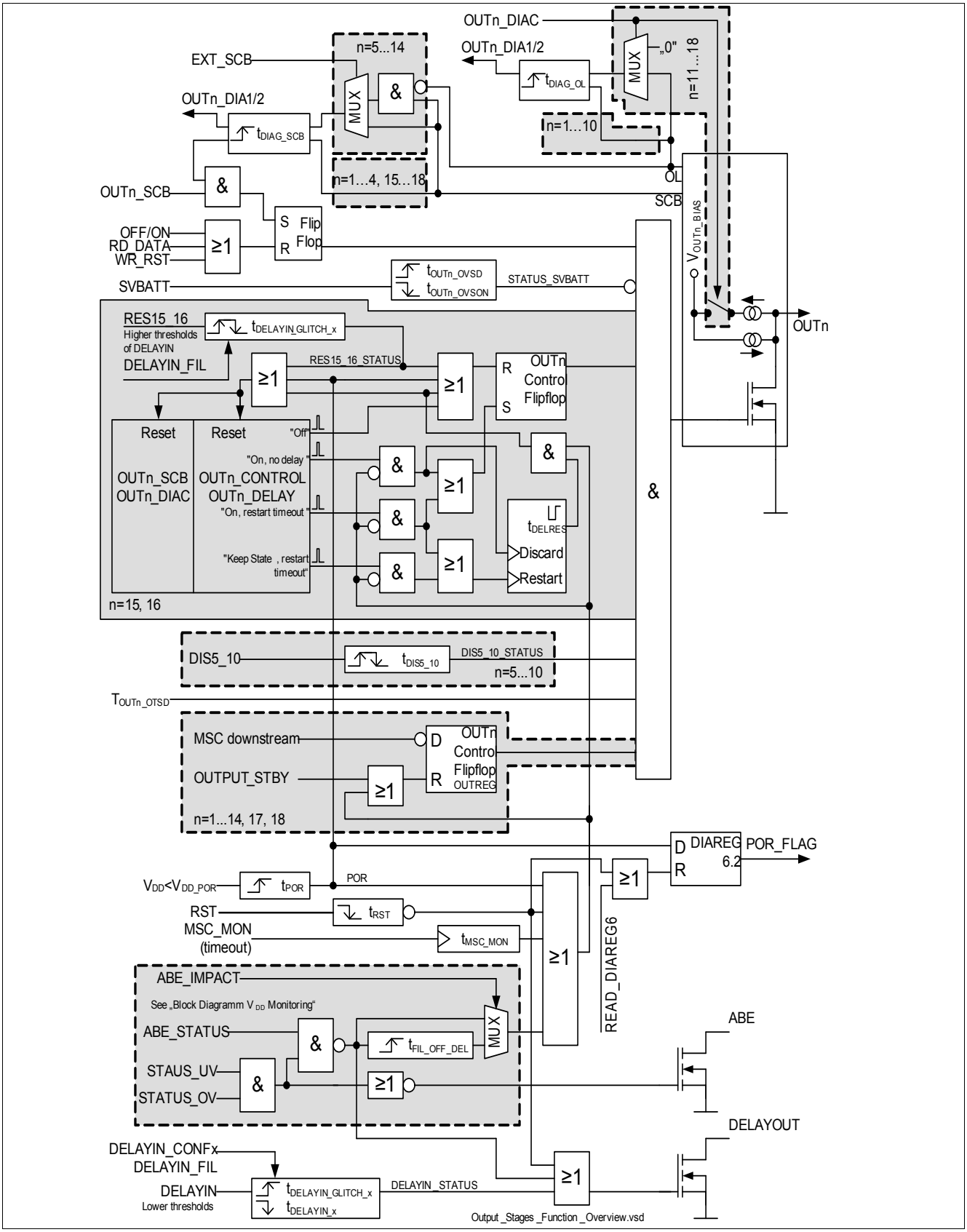


Figure 1 Output stages, functional schematic

2 Block Diagram

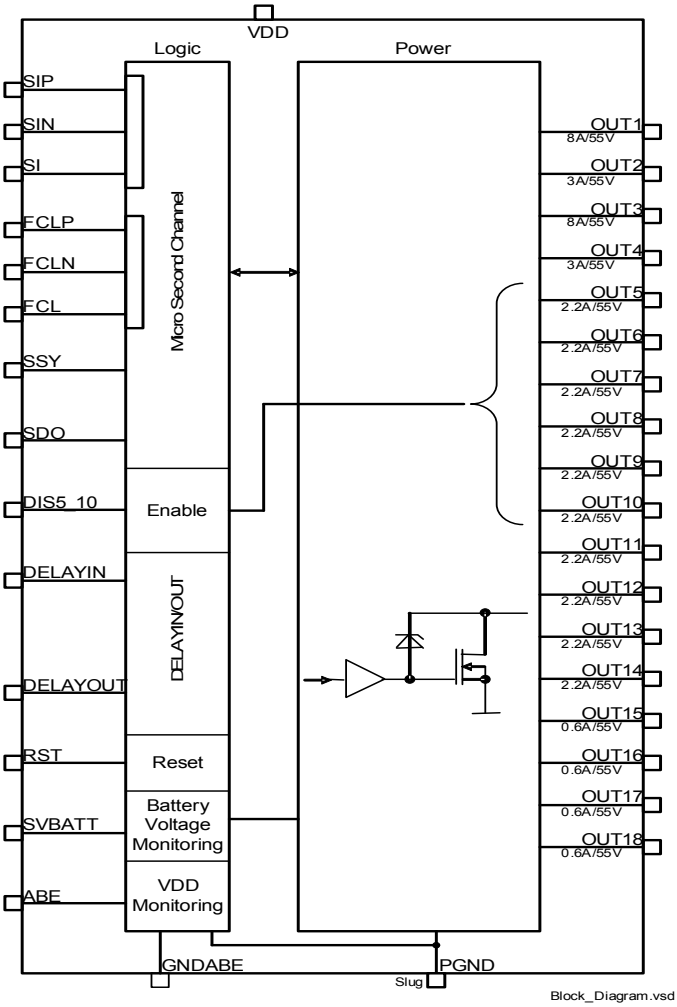


Figure 2 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

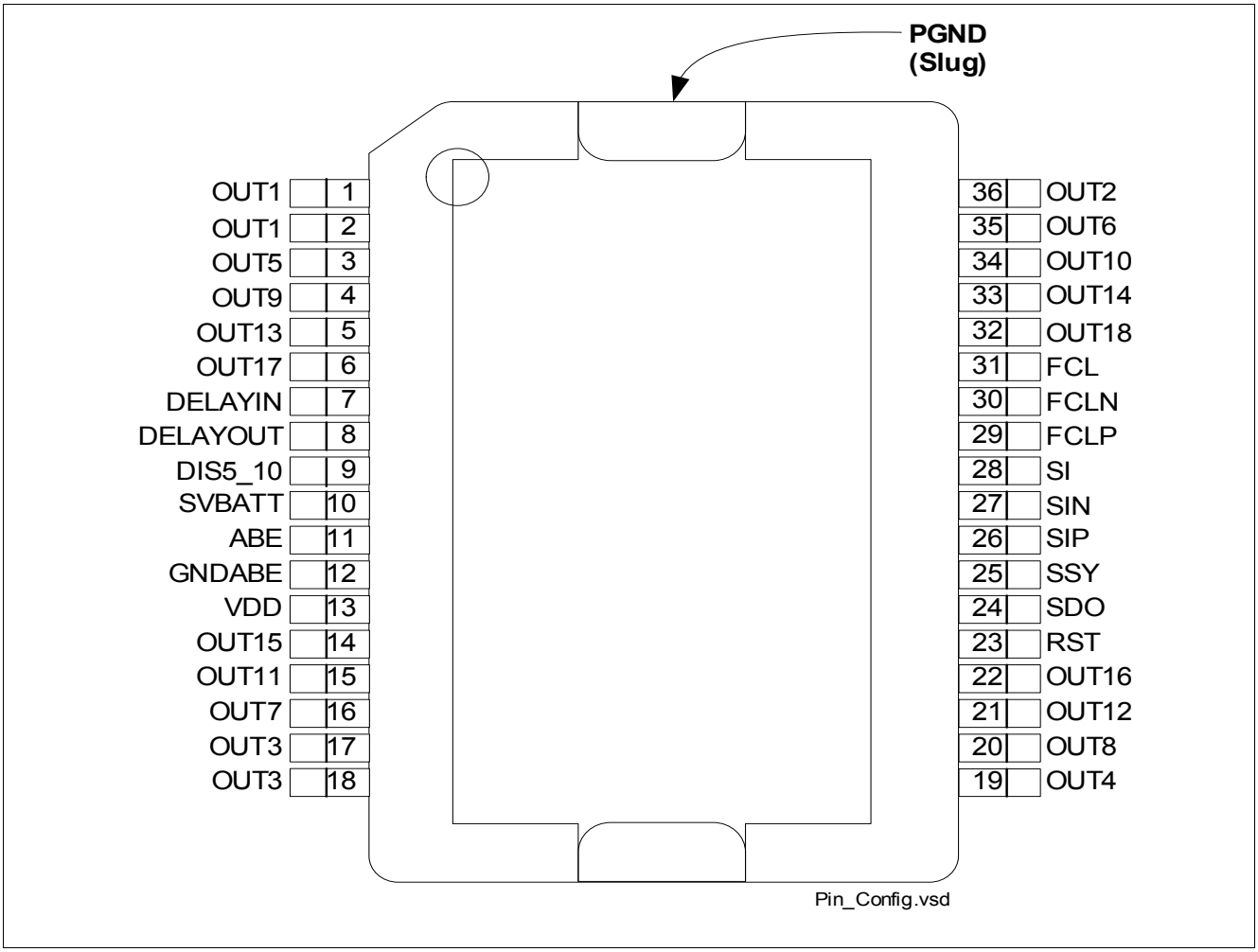


Figure 3 Pin Assignment

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1, 2	OUT1[1)]	Drain Connection of Power stage. Short circuit proof Individually protected against overtemperature diagnostic functions control via MSC Clamping of the output voltage by zener diodes
36	OUT2	
17, 18	OUT3[2)]	
19	OUT4	
3	OUT5	
35	OUT6	
16	OUT7	
20	OUT8	
4	OUT9	
34	OUT10	
15	OUT11	
21	OUT12	
5	OUT13	
33	OUT14	
14	OUT15	
22	OUT16	
6	OUT17	
32	OUT18	
9	DIS5_10	Disable pin for OUT5...OUT10 (low level disables OUT5...OUT10 after filtering time (t_{DIS5_10}) has expired). The thresholds are defined in **Chapter 7** (active low, internal pull-up)
7	DELAYIN	DELAYIN input (internal pull-down, active low): Disable pin for DELAYOUT after the configurable filtering time ($t_{DELAYIN}$) has expired and Reset pin for OUT15 and OUT16. The thresholds are defined in **Chapter 7**.
8	DELAYOUT	Open drain output generating active low level if DELAYIN is low level (below $V_{DELAYIN_L}$) and $t_{DELYAIN}$ has expired, input ABE disables stages or V_{DD} monitoring has detected a supply voltage failure. See **Chapter 7**.
11	ABE	Bidirectional pin (active low). Indicates VDD overvoltage and undervoltage condition by pulling ABE-pin low. If forced to low from externally all stages are turned off.
12	GNDABE	Sense ground. Reference ground for V_{DD} monitoring only. Connect this pin to ground.
13	VDD	Supply voltage 5V
24	SDO	MSC interface. Upstream data, open drain output
25	SSY	MSC interface. Chip select and synchronization strobe.
26	SIP	MSC interface. Downstream data positive for differential interface
27	SIN	MSC interface. Downstream data negative for differential interface
28	SI	MSC interface optional downstream data input for single ended interface
29	FCLP	MSC interface. Clock positive for differential interface
30	FCLN	MSC interface. Clock negative for differential interface
31	FCL	MSC interface optional clock input for single ended interface

Pin	Symbol	Function
23	RST	Reset input (active low, internal pull-up). Shuts down all stages regardless of their input signals. Clears the fault registers and resets the MSC interface registers (partially).
10	SVBATT	Sense Battery Voltage Monitoring Pin. Connect to V_{BAT}. Used to activate factory test mode. See **Chapter 6.4**.
Slug	PGND	Power Ground. Internally used as PGND. Analogue circuits except VDD-monitoring refer to PGND. Connect to Ground.

1) Pin1 and Pin2 have to be connected together without any parasitic resistor

2) Pin17 and Pin18 have to be connected together without any parasitic resistor in between.

3.3 Abbreviations

Table 2 Abbreviations

ABE	“ABschaltung Endstufen” (switch off output stages)
C	Command bit
CD	Command data bit
DC	Don´t care bit
DOT	Diagnosis overtemperature
LVDS	Low voltage differential signal
MSC	Micro Second Channel
NCB	Number of bits of the active phase of a command frame
NDB	Number of bits of the active phase of a data frame
OL	Open Load (diagnostic stage information)
OTSD	Over Temperature Shut Down (threshold to shut down stages for device self protection)
OTW	Over Temperature Warning (diagnostic information)
POR	Power On Reset, including filter time t_{POR}
PS	Power Stage(s)
RST	ReSeT input pin
SCB	Short Circuit to Battery (diagnostic stage information)
SCG	Short Circuit to Ground (diagnostic stage information)
SSY	Select / SYnc signal for MSC communication
SB	Selection bit
TC	Test coverage
UD	Upstream data bit

4 General Product Characteristics

4.1 Test coverage (TC) in series production

In the standard production flow not all parameters can be covered due to technical or economic reasons. Therefore the following test coverage classes are defined:

A) Parameter test (parameter is measured in production test)

B) Go/NoGo test (parameter within specified range is guaranteed by Go/NoGo-test in production)

C) Specified by design (covered by lab tests, not considered within the standard production flow)

The given supply voltage range is only valid as long as the related function is active. (e.g. the power stages are shut off if V_{BAT} > 28V. In that case, no function is available to be tested at V_{BAT} = 40V).

4.2 Absolute Maximum Ratings

The integrated circuit will not be damaged if maximum ratings are reached. Every maximum rating is allowed to be reached at the same time, as long as no other maximum rating is exceeded. But see **Item Note:**

Unless otherwise indicated all voltages are referred to PGND (all PGND and GNDABE are externally connected to each other) Positive current flows into the pin.

Table 3 Maximum Ratings

T_j = -40°C to +150°C, all voltages with respect to PGND, positive current flowing into pin, unless otherwise specified

Pos.	Parameter	Symbol	Values		Unit	TC	Conditions
			min.	max.			
Supply and Power Pins							
4.2.1	Supply Voltage Range pin VDD, static	V_{DD_MR}	-0.3	36	V	C	–
4.2.2	Battery Voltage stages output pins via load	V_{BAT_MR}	-1	40	V	C	–
4.2.3	Total current over the PGND	I_{PGND_MR}	-38	38	A	C	–
4.2.4	Ground Voltage Offset maximum permissible offset between GNDABE and the PGND	dV_{GND_MR}	-0.3	0.3	V	C	–
4.2.5	Output Stages static voltage OUTn (n=1...18)	V_{OUTn_MR}	-0.3	50	V	C	OUTn OFF
4.2.6	Short Circuit to V_{BAT} (single event)	V_{BAT_SC}	-0.3	36	V	C	OUTn (n=1...18), **Figure 4**
Interface and Logic							
4.2.7	Logic Input Pins SIP, SIN, SI, FCLP, FCLN, FCL, SSY, DIS5_10, RST	V_{SIP_MR}, V_{SIN_MR}, V_{SI_MR}, V_{FCLP_MR}, V_{FCLN_MR}, V_{FCL_MR}, V_{SSY_MR}, $V_{DIS5_10_MR}$, V_{RST_MR}	-0.3	36	V	C	–
4.2.8	Bidirectional Pin ABE	V_{ABE_MR}	-0.3	36	V	C	–
4.2.9	Output Pins DELAYOUT, SDO	$V_{DELAYOUT_MR}$, V_{SDO_MR}	-0.3	36	V	C	–

Table 3 Maximum Ratings

T_j = -40°C to +150°C, all voltages with respect to PGND, positive current flowing into pin, unless otherwise specified

Pos.	Parameter	Symbol	Values		Unit	TC	Conditions
			min.	max.			
4.2.10	Input Pins DELAYIN, SVBATT	$V_{DELAYIN_MR}$, V_{SVBATT_MR}	-0.3	40	V	C	–
4.2.11	Current into Pin SIP, SIN, SI, FCLP, FCLN, FCL, SSY, DIS5_10, RST, DELAYIN, SVBATT, SDO	I_{SIP_MR}, I_{SIN_MR}, I_{SI_MR}, I_{FCLP_MR}, I_{FCLN_MR}, I_{FCL_MR}, I_{SSY_MR}, $I_{DIS5_10_MR}$, I_{RST_MR}, $I_{DELAYIN_MR}$, I_{SVBATT_MR}, I_{SDO_MR}	-10	10	mA	C	1)
4.2.12	Current into Pin DELAYOUT, ABE	$I_{DELAYOUT_MR}$, I_{ABE_MR}	-10	15	mA	C	1)
Temperatures							
4.2.13	Junction Temperature	Tj	-40	150	°C	C	–
4.2.14	Storage Temperature	T_{STG}	-55	150	°C	C	–

1) Other maximum ratings (like **Item 4.2.7** to **Item 4.2.10** or **Item 4.2.13**) are not allowed to be exceeded.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous or repetitive operation.

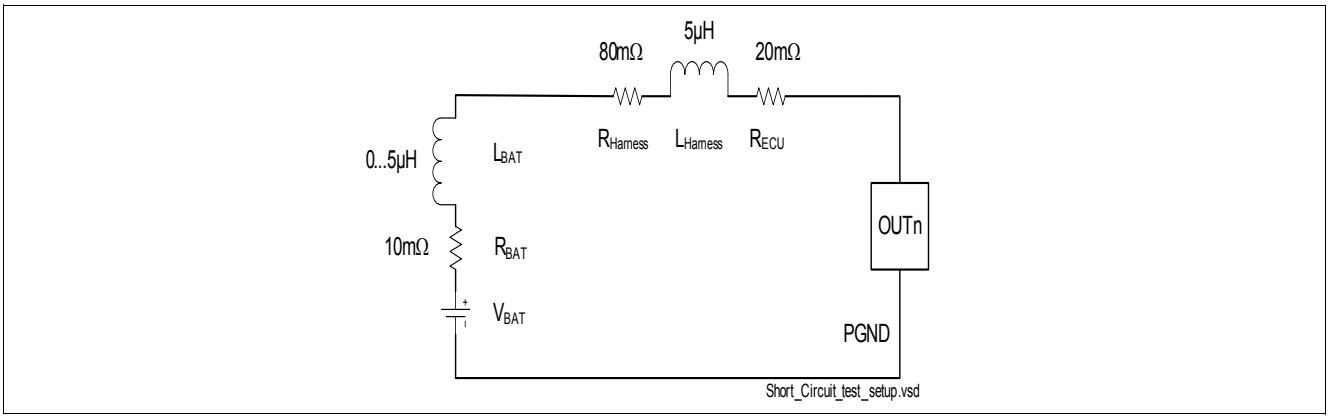


Figure 4 Short Circuit test set-up

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 4 Thermal Resistance

T_j = -40°C to +150°C, all voltages with respect to PGND, positive current flowing into pin, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
4.3.1	Junction to Case	R_{thJC}	–	–	2	K/W	C	1)
4.3.2	Junction to Ambient	R_{thJA}	–	25	–	K/W	C	see Figure 5 1)

1) Power dissipation Pv=3W distributed statically and homogeneously over all power stages. Resistive Load.

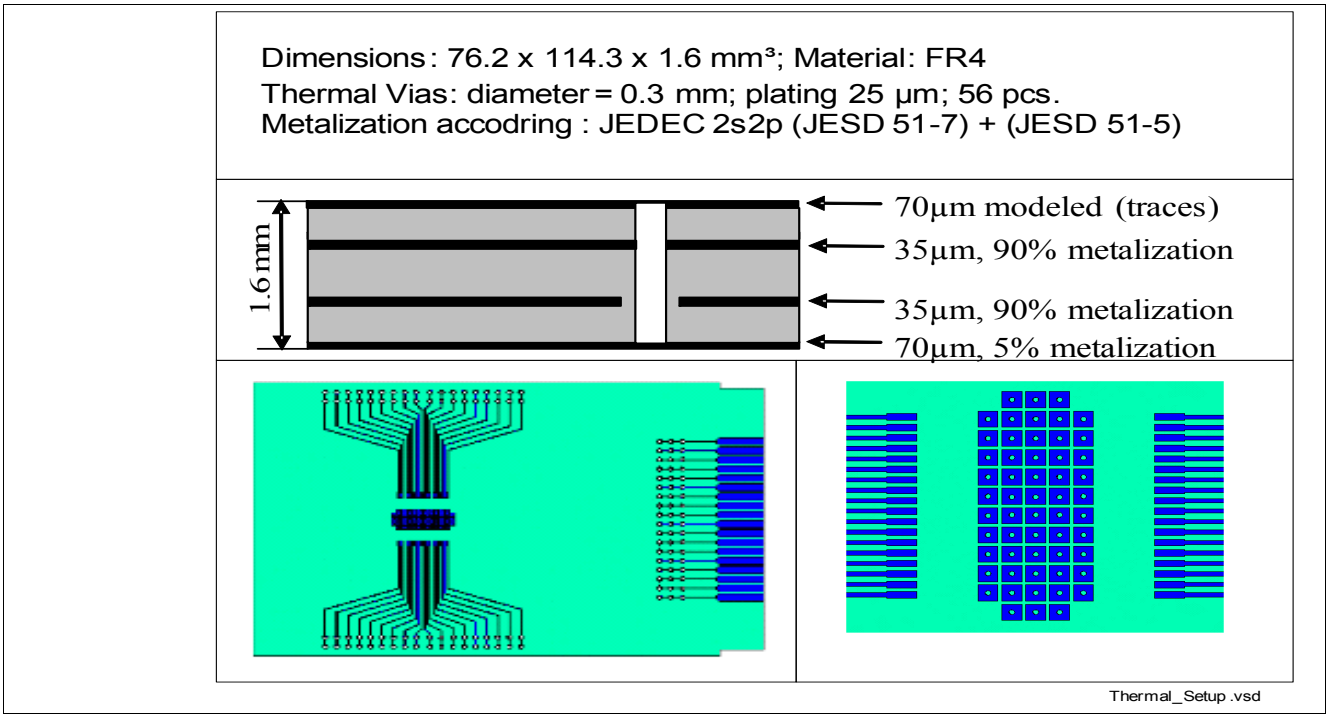


Figure 5 Thermal simulation - PCB setup

4.4 ESD

Of the various ESD models, the integrated circuit meets at least the “human body model” according to the requirements of the EIA/JESD22-A114-F. During manufacturing process, ESD pulses according to "charged device model" (EIA/JESD22-C101-D) may be exposed to each pin. ESD Specification Details in the following Table.

Table 5 ESD Susceptibility

T_j = -40°C to +150°C, all voltages with respect to PGND, positive current flowing into pin, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Standard Requirements for all Pins								
4.4.1	Electro Static Discharge Voltage “Human-Body-Model – HBM”	V_{ESD1}	-2	–	2	kV	C	All Pins
4.4.2	Electro Static Discharge Voltage “Charged-Device-Model – CDM”	V_{ESD2}	-500	–	500	V	C	All Pins
Pins with Extended Requirements								
4.4.3	Electro Static Discharge Voltage “Human-Body-Model – HBM”	V_{ESD3}	-6	–	6	kV	C	OUT1…14 vs. PGND
4.4.4	Electro Static Discharge Voltage “Human-Body-Model – HBM”	V_{ESD4}	-4	–	4	kV	C	OUT15…18 vs. PGND

4.5 Operating Range

Table 6 Operating Range

T_j = -40°C to +150°C, all voltages with respect to PGND, positive current flowing into pin, unless otherwise specified

Pos.	Parameter	Symbol	Values		Unit	TC	Conditions
			min.	max.			
Supply, Battery Voltage							
4.5.1	Supply Voltage Range	V_{DD}	4.5	5.5	V	C	–
4.5.2	Battery Voltage	$V_{BAT(typ)}$	13.5		V	C	–
4.5.3	Nominal Total PGND Current	$I_{PGND(typ)}$	-12	0	A	C	1)

1) Total PGND current influences e.g. the RON-measurement of the Power Stages or voltage thresholds of the input buffers because of common PGND bond wires. As basis for definition of the RON or the voltage thresholds, the defined PGND current is used.

5 Power Stages

5.1 Functional Description

The following general description is valid for the channel groups OUT1,3, OUT2,4, OUT5...8, OUT9,10, OUT11...14, OUT17,18. The specific function of the channel group OUT15,16 is described in **Chapter 5.7**.

The reset input of the OUTn-control flip-flop is active high and dominant, delivering a logic low level at the output of the OUTn-control flip-flop.Only in failure-free condition, output can be switched on by MSC downstream.

Disabling inputs DIS5_10 and DELAYIN have different input characteristics and delay ($t_{DELAYIN}$ >> t_{DIS5_10}). For details concerning DIS5_10, DELAYIN and DELAYOUT see **Chapter 7** and **Figure 1**.

5.2 Power Stages OUT1 and OUT3

Table 7 Electrical Characteristics Power Stages OUT1 and OUT3

n = 1 and 3, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin. T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Load Current								
5.2.1	Continuous Load Current	I_{OUTn}	–	–	4	A	C	
5.2.2	Extended Load Current	I_{OUTn_ex}	–	–	8	A	C	max 800h
5.2.3	Extended current time, Accumulated operating time	t_{OUTn_ec}	–	–	60	h	C	V_{BAT}≤14V, R_L≥0.88Ω
5.2.4	Maximum current, (short circuit limited current / switch off threshold)	I_{OUTn_max}	8	–	12.5	A	A	
ON-Resistance without clamping [1]								
5.2.5	On Resistance Tj=-40°C	R_{on-40_n}	–	–	120	mΩ	C	I_{OUTn}=4A
5.2.6	On Resistance Tj=25°C	R_{on+25_n}	–	–	148	mΩ	C	I_{OUTn}=4A
5.2.7	On Resistance Tj=150°C	R_{on+150_n}	–	–	200	mΩ	A	I_{OUTn}=4A
5.2.8	On Resistance Tj≤150°C	R_{on_n}	–	–	210	mΩ	C	I_{OUTn}<8A
ON-Resistance with clamping [2]								
5.2.9	On Resistance Tj=-40°C	R_{on-40_n}	–	–	156	mΩ	C	I_{OUTn}=4A
5.2.10	On Resistance Tj=25°C	R_{on+25_n}	–	–	193	mΩ	C	I_{OUTn}=4A
5.2.11	On Resistance Tj=150°C	R_{on+150_n}	–	–	260	mΩ	A	I_{OUTn}=4A
5.2.12	On Resistance Tj≤150°C	R_{on_n}	–	–	273	mΩ	C	I_{OUTn}<8A
Delay times, Slew rates (see **Figure 6**)								
5.2.13	Switch on delay	t_{don_n}	–	–	15	µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
5.2.14	Switch off delay	t_{doff_n}	–	–	15	µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
5.2.15	Difference of switch on and off delay t_{dif_n}=t_{don_n}-t_{doff_n}	t_{dif_n}	-8	–	8	µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
5.2.16	Switch on slew rates	s_{on_n}	0.5	1	2.5	V/µs	C	R_{Load}=5.9Ω, V_{BAT}=14V

Table 7 Electrical Characteristics Power Stages OUT1 and OUT3

n = 1 and 3, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin. T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
5.2.17	Switch off slew rates	s_{off_n}	0.5	1	2.5	V/µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
Leakage current								
5.2.18	Leakage current of the Output Stage	I_{l_OUTn}	–	–	5	µA	C	V_{OUTn}=14V, V_{DD}=0V, Tj=60°C
5.2.19	Leakage current of the Output Stage	I_{l_OUTn}	–	–	10	µA	C	V_{OUTn}=28V, V_{DD}=0V, Tj=60°C
5.2.20	Leakage current of the Output Stage	I_{l_OUTn}	–	–	30	µA	A	V_{OUTn}<28V, V_{DD}=0V, Tj=150°C
Clamping voltage								
5.2.21	Clamping voltage	V_{CL_n}	50	–	60	V	C	I_{OUTn}=3A
5.2.22	Clamping voltage	V_{CL_n}	50	–	60	V	A	I_{OUTn}=0.2A
Clamping energy [3]								
5.2.23	Standard operating range, max. 1000Mio cycles	E_{CL_OUTn}	–	–	25	mJ	C	$Tj_{(0)}$=125°C, $I_{OUTn(0)}$<2.8A
5.2.24	Jump Start, max. 0.01Mio cycles	E_{CL_OUTn}	–	–	27	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<5.6A
5.2.25	Load Dump, max. 10 pulses	E_{CL_OUTn}	–	–	90	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<8A
5.2.26	Load Dump, max. 10 pulses	E_{CL_OUTn}	–	–	26	mJ	C	$Tj_{(0)}$=150°C, $I_{OUTn(0)}$<8A
Reverse current through OUTn								
5.2.27	In operation mode, static, no destruction	$I_{R_S_OUTn}$	-3	–	–	A	C	Tj=150°C,V_{DD}=5V
5.2.28	Without supply voltage, possibly Leakage Current out of neighbor channels. 10ms after the reverse current disappears leakage current criteria are kept.	$I_{R_Soff_OUTn}$	-3	–	–	A	C	V_{DD}<1V
5.2.29	In operation mode, No unwanted switching of channels; No unwanted Reset, No unwanted change of Voltage Monitoring Thresholds; No unwanted communication errors or register changes beside diagnostic registers. Possibly unwanted diagnostic entries. Possibly Leakage Current out of neighbor channels.	$I_{R_S_OUTn}$	-1.5	–	–	A	C	Tj=150°C, V_{DD}=5V

1) **Item 5.2.5** to **Item 5.2.8** has to be considered for applications with resistive load or inductive load with external freewheeling.

2) **Item 5.2.9** to **Item 5.2.12** has to be considered for applications where clamping occurs.

3) Clamping energy, Linear decreasing current, fcl<67Hz.

5.3 Power Stages OUT2 and OUT4

Table 8 Electrical Characteristics Power Stages OUT2 and OUT4

n = 2 and 4, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Load Current								
5.3.1	Continuous Load Current	I_{OUTn}	–	–	3	A	C	
5.3.2	Extended Current time Accumulated Operating time	t_{OUTn_ec}	–	–	100	h	C	V_{BAT}≤14V, R_L≥1.98Ω
5.3.3	Maximum Current, (short circuit limited current / switch off threshold)	I_{OUTn_max}	3	–	6	A	A	
ON-Resistance without clamping [1]								
5.3.4	On Resistance Tj=-40°C	R_{on-40_n}	–	–	210	mΩ	C	I_{OUTn}=3A
5.3.5	On Resistance Tj=25°C	R_{on+25_n}	–	–	259	mΩ	C	I_{OUTn}=3A
5.3.6	On Resistance Tj≤150°C	R_{on_n}	–	–	350	mΩ	A	I_{OUTn}=3A
ON-Resistance with clamping [2]								
5.3.7	On Resistance Tj=-40°C	R_{on-40_n}	–	–	273	mΩ	C	I_{OUTn}=3A
5.3.8	On Resistance Tj=25°C	R_{on+25_n}	–	–	337	mΩ	C	I_{OUTn}=3A
5.3.9	On Resistance Tj≤150°C	R_{on_n}	–	–	455	mΩ	A	I_{OUTn}=3A
Delay times, Slew rates (see **Figure 6**)								
5.3.10	Switch on delay	t_{don_n}	–	–	15	µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
5.3.11	Switch off delay	t_{doff_n}	–	–	15	µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
5.3.12	Difference of switch on and off delay t_{dif_n}=t_{don_n}-t_{doff_n}	t_{dif_n}	-5	–	5	µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
5.3.13	Switch on slew rates	s_{on_n}	1.1	2.5	5.8	V/µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
5.3.14	Switch off slew rates	s_{off_n}	1.1	2.5	5.8	V/µs	C	R_{Load}=5.9Ω, V_{BAT}=14V
Leakage current								
5.3.15	Leakage current of the Output Stage	I_{l_OUTn}	–	–	5	µA	C	V_{OUTn}=14V, V_{DD}=0V, Tj=60°C
5.3.16	Leakage current of the Output Stage	I_{l_OUTn}	–	–	10	µA	C	V_{OUTn}=28V, V_{DD}=0V, Tj=60°C
5.3.17	Leakage current of the Output Stage	I_{l_OUTn}	–	–	30	µA	A	V_{OUTn}<28V, V_{DD}=0V, Tj=150°C
Clamping voltage								
5.3.18	Clamping voltage	V_{CL_n}	50	–	60	V	C	I_{OUTn}=3A
5.3.19	Clamping voltage	V_{CL_n}	50	–	60	V	A	I_{OUTn}=0.2A

Table 8 Electrical Characteristics Power Stages OUT2 and OUT4

n = 2 and 4, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Clamping energy [3]								
5.3.20	Standard operating range, max. 1000Mio cycles	E_{CL_OUTn}	–	–	22	mJ	C	$Tj_{(0)}$=125°C, $I_{OUTn(0)}$<1.05A
5.3.21	Jump Start, max. 0.01Mio cycles	E_{CL_OUTn}	–	–	18	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<2.1A
5.3.22	Load Dump, max. 10 pulses	E_{CL_OUTn}	–	–	76	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<3A
5.3.23	Load Dump, max. 10 pulses	E_{CL_OUTn}	–	–	19	mJ	C	$Tj_{(0)}$=150°C, $I_{OUTn(0)}$<3A
Reverse current through OUTn								
5.3.24	In operation mode, static, no destruction	$I_{R_S_OUTn}$	-3	–	–	A	C	Tj=150°C, V_{DD}=5V
5.3.25	Without supply voltage, possibly Leakage Current out of neighbor channels. 10ms after the reverse current disappears leakage current criteria are kept.	$I_{R_Soff_OUTn}$	-3	–	–	A	C	V_{DD}<1V
5.3.26	In operation mode, No unwanted switching of channels; No unwanted Reset, No unwanted change of Voltage Monitoring Thresholds; No unwanted communication errors or register changes beside diagnostic registers. Possibly unwanted diagnostic entries. Possibly Leakage Current out of neighbor channels.	$I_{R_S_OUTn}$	-1.1	–	–	A	C	Tj=150°C, V_{DD}=5V

1) **Item 5.3.4** to **Item 5.3.6** has to be considered for applications with resistive load or inductive load with external freewheeling.

2) **Item 5.3.7** to **Item 5.3.9** has to be considered for applications where clamping occurs.

3) Clamping energy, Linear decreasing current, fcl<67Hz.

5.4 Power Stages OUT5...OUT8

Table 9 Electrical Characteristics Power Stages OUT5...OUT8

n = 5...8, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Load Current								
5.4.1	Continuous Load Current	I_{OUTn}	–	–	2.2	A	C	–
5.4.2	Extended current time, Accumulated operating time	t_{OUTn_ec}	–	–	100	h	C	V_{BAT}≤14V, R_L≥2.78Ω
5.4.3	Maximum current, (short circuit limited current / switch off threshold)	I_{OUTn_max}	2.2	–	4	A	A	–
ON-Resistance								
5.4.4	On-resistance Tj=-40°C	R_{on-40_n}	–	–	432	mΩ	C	I_{OUTn}=2.2A
5.4.5	On-resistance Tj=25°C	R_{on+25_n}	–	–	533	mΩ	C	I_{OUTn}=2.2A
5.4.6	On-resistance Tj≤150°C	R_{on_n}	–	–	720	mΩ	A	I_{OUTn}=2.2A
Delay times, Slew rates (see Figure 6)								
5.4.7	Switch on delay	t_{don_n}	–	–	10	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.4.8	Switch off delay	t_{doff_n}	–	–	10	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.4.9	Difference of switch on and off delay t_{dif_n}=t_{don_n}-t_{doff_n}	t_{dif_n}	-5	–	5	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.4.10	Switch on slew rates	S_{on_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.4.11	Switch off slew rates	S_{off_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
Leakage current								
5.4.12	Leakage current of the Output Stage	I_{l_OUTn}	–	–	5	µA	C	V_{OUTn}=14V, V_{DD}=0V, Tj=60°C
5.4.13	Leakage current of the Output Stage	I_{l_OUTn}	–	–	10	µA	C	V_{OUTn}=28V, V_{DD}=0V, Tj=60°C
5.4.14	Leakage current of the Output Stage	I_{l_OUTn}	–	–	20	µA	A	V_{OUTn}<28V, V_{DD}=0V, Tj=150°C
Clamping voltage								
5.4.15	Clamping voltage	V_{CL_n}	50	–	60	V	C	I_{OUTn}=2.2A
5.4.16	Clamping voltage	V_{CL_n}	50	–	60	V	A	I_{OUTn}=0.2A
5.4.17	Clamping voltage, difference between outputs. OUTn with identical inductive loads	$V_{CL_dif_n}$	-3	–	3	V	A	I_{OUTn}=0.2A
Clamping energy [1]								
5.4.18	Standard operating range, max. 18Mio cycles	E_{CL_OUTn}	–	–	7.5	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<1.8A

Table 9 Electrical Characteristics Power Stages OUT5...OUT8

n = 5...8, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
5.4.19	Standard operating range, max. 648Mio cycles	E_{CL_OUTn}	–	–	4	mJ	C	$Tj_{(0)}$=125°C, $I_{OUTn(0)}$<1.4A
5.4.20	Standard operating range, max. 96Mio cycles	E_{CL_OUTn}	–	–	3	mJ	C	$Tj_{(0)}$=140°C, $I_{OUTn(0)}$<1A
5.4.21	Standard operating range, max. 4Mio cycles	E_{CL_OUTn}	–	–	3	mJ	C	$Tj_{(0)}$=150°C, $I_{OUTn(0)}$<1A
5.4.22	Generator defect, max. 0.5Mio cycles, or **Item 5.4.23**	E_{CL_OUTn}	–	–	9	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<2A
5.4.23	Generator defect, max. 0.5Mio cycles	E_{CL_OUTn}	–	–	5	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<1.5A
5.4.24	Jump start, max. 0.021Mio cycles, or **Item 5.4.25**	E_{CL_OUTn}	–	–	17.5	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<3A[2)]
5.4.25	Jump start, max. 0.021Mio cycles	E_{CL_OUTn}	–	–	10	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<2.3A[2)]
5.4.26	Load dump, max. 10 pulses, or **Item 5.4.27**	E_{CL_OUTn}	–	–	35	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<2.1A
5.4.27	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	20	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<2.1A
5.4.28	Load dump, max. 10 pulses, or **Item 5.4.29**	E_{CL_OUTn}	–	–	21	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<3.3A[2)]
5.4.29	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	18	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<2.4A[2)]
Reverse current through OUTn								
5.4.30	In operation mode, static, no destruction	$I_{R_S_OUTn}$	-2.2	–	–	A	C	Tj=150°C, V_{DD}=5V
5.4.31	Without supply voltage, possibly Leakage Current out of neighbor channels. 10ms after the reverse current disappears leakage current criteria are kept.	$I_{R_Soff_OUTn}$	-2.2	–	–	A	C	V_{DD}<1V
5.4.32	In operation mode, No unwanted switching of channels; No unwanted Reset, No unwanted change of Voltage Monitoring Thresholds; No unwanted communication errors or register changes beside diagnostic registers. Possibly unwanted diagnostic entries. Possibly Leakage Current out of neighbor channels.	$I_{R_S_OUTn}$	-1	–	–	A	C	Tj=150°C, V_{DD}=5V

1) Clamping energy, Linear decreasing current, fcl<67Hz.

2) PS might switch off to limit the current before reaching the given I_{OUTn} due to reaching I_{OUTn_max}.

5.5 Power Stages OUT9 and OUT10

Table 10 Electrical Characteristics Power Stages OUT9 and OUT10

n = 9 and 10, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Load Current								
5.5.1	Continuous Load Current	I_{OUTn}	–	–	2.2	A	C	–
5.5.2	Extended current time, Accumulated operating time	t_{OUTn_ec}	–	–	100	h	C	V_{BAT}≤14V, R_L≥2.78Ω
5.5.3	Maximum current, (short circuit limited current / switch off threshold)	I_{OUTn_max}	2.2	–	4	A	A	–
ON-Resistance								
5.5.4	On-resistance Tj=-40°C	R_{on-40_n}	–	–	282	mΩ	C	I_{OUTn}=2.2A
5.5.5	On-resistance Tj=25°C	R_{on+25_n}	–	–	348	mΩ	C	I_{OUTn}=2.2A
5.5.6	On-resistance Tj≤150°C	R_{on_n}	–	–	470	mΩ	A	I_{OUTn}=2.2A
Delay times, Slew rates (see Figure 6)								
5.5.7	Switch on delay	t_{don_n}	–	–	10	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.5.8	Switch off delay	t_{doff_n}	–	–	10	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.5.9	Difference of switch on and off delay t_{dif_n}=t_{don_n}-t_{doff_n}	t_{dif_n}	-5	–	5	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.5.10	Switch on slew rates	S_{on_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.5.11	Switch off slew rates	S_{off_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
Leakage current								
5.5.12	Leakage current of the Output Stage	I_{l_OUTn}	–	–	5	µA	C	V_{OUTn}=14V, V_{DD}=0V, Tj=60°C
5.5.13	Leakage current of the Output Stage	I_{l_OUTn}	–	–	10	µA	C	V_{OUTn}=28V, V_{DD}=0V, Tj=60°C
5.5.14	Leakage current of the Output Stage	I_{l_OUTn}	–	–	20	µA	A	V_{OUTn}<28V, V_{DD}=0V, Tj=150°C
Clamping voltage								
5.5.15	Clamping voltage	V_{CL_n}	50	–	60	V	C	I_{OUTn}=2.2A
5.5.16	Clamping voltage	V_{CL_n}	50	–	60	V	A	I_{OUTn}=0.2A
5.5.17	Clamping voltage, difference between outputs. OUTn with identical inductive loads	$V_{CL_dif_n}$	-3	–	3	V	A	I_{OUTn}=0.2A
Clamping energy [1]								
5.5.18	Standard operating range, max. 18Mio cycles	E_{CL_OUTn}	–	–	25	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<1.5A

Table 10 Electrical Characteristics Power Stages OUT9 and OUT10

n = 9 and 10, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
5.5.19	Standard operating range, max. 648Mio cycles	E_{CL_OUTn}	–	–	18	mJ	C	$Tj_{(0)}$=125°C, $I_{OUTn(0)}$<1.2A
5.5.20	Standard operating range, max. 96Mio cycles	E_{CL_OUTn}	–	–	15	mJ	C	$Tj_{(0)}$=140°C, $I_{OUTn(0)}$<1A
5.5.21	Standard operating range, max. 4Mio cycles	E_{CL_OUTn}	–	–	15	mJ	C	$Tj_{(0)}$=150°C, $I_{OUTn(0)}$<1A
5.5.22	Generator defect, max. 0.5Mio cycles; or **Item 5.5.23**	E_{CL_OUTn}	–	–	28	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<1.6A
5.5.23	Generator defect, max. 0.5Mio cycles	E_{CL_OUTn}	–	–	16	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<1.1A
5.5.24	Jump start, max. 0.021Mio cycles, or **Item 5.5.25**	E_{CL_OUTn}	–	–	50	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<2.2A
5.5.25	Jump start, max. 0.021Mio cycles	E_{CL_OUTn}	–	–	30	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<1.8A
5.5.26	Load dump, max. 10 pulses, or **Item 5.5.27**	E_{CL_OUTn}	–	–	120	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<2.4A[2)]
5.5.27	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	55	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<1.8A
5.5.28	Load dump, max. 10 pulses, or **Item 5.5.29**	E_{CL_OUTn}	–	–	80	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<3.5A[2)]
5.5.29	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	51	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<2A
Reverse current through OUTn								
5.5.30	In operation mode, static, no destruction	$I_{R_S_OUTn}$	-2.2	–	–	A	C	Tj=150°C, V_{DD}=5V
5.5.31	Without supply voltage, possibly Leakage Current out of neighbor channels. 10ms after the reverse current disappears leakage current criteria are kept.	$I_{R_Soff_OUTn}$	-2.2	–	–	A	C	V_{DD}<1V
5.5.32	In operation mode, No unwanted switching of channels; No unwanted Reset, No unwanted change of Voltage Monitoring Thresholds; No unwanted communication errors or register changes beside diagnostic registers. Possibly unwanted diagnostic entries. Possibly Leakage Current out of neighbor channels.	$I_{R_S_OUTn}$	-1	–	–	A	C	Tj=150°C, V_{DD}=5V

1) Clamping energy, Linear decreasing current, fcl<67Hz.

2) PS might switch off to limit the current before reaching the given I_{OUTn} due to reaching I_{OUTn_max}.

5.6 Power Stages OUT11...OUT14

Table 11 Electrical Characteristics Power Stages OUT11...OUT14

n = 11...14, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Load Current								
5.6.1	Continuous Load Current	I_{OUTn}	–	–	2.2	A	C	–
5.6.2	Extended current time, Accumulated operating time	t_{OUTn_ec}	–	–	100	h	C	V_{BAT}≤14V, R_L≥2.78Ω
5.6.3	Maximum current, (short circuit limited current / switch off threshold)	I_{OUTn_max}	2.2	–	4	A	A	–
ON-Resistance								
5.6.4	On-resistance Tj=-40°C	R_{on-40_n}	–	–	432	mΩ	C	I_{OUTn}=2.2A
5.6.5	On-resistance Tj=25°C	R_{on+25_n}	–	–	533	mΩ	C	I_{OUTn}=2.2A
5.6.6	On-resistance Tj≤150°C	R_{on_n}	–	–	720	mΩ	A	I_{OUTn}=2.2A
Delay times, Slew rates (see Figure 6)								
5.6.7	Switch on delay	t_{don_n}	–	–	10	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.6.8	Switch off delay	t_{doff_n}	–	–	10	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.6.9	Difference of switch on and off delay t_{dif_n}=t_{don_n}-t_{doff_n}	t_{dif_n}	-5	–	5	µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.6.10	Switch on slew rates	s_{on_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
5.6.11	Switch off slew rates	s_{off_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=7.68Ω, V_{BAT}=14V
Leakage current								
5.6.12	Leakage current of the Output Stage	I_{l_OUTn}	–	–	5	µA	C	V_{OUTn}=14V, V_{DD}=0V, Tj=60°C
5.6.13	Leakage current of the Output Stage	I_{l_OUTn}	–	–	20	µA	C	V_{OUTn}=14V, V_{DD}=5V (diagnosis current off, CONREG3), Tj=60°C
5.6.14	Leakage current of the Output Stage	I_{l_OUTn}	–	–	10	µA	C	V_{OUTn}=28V, V_{DD}=0V, Tj=60°C
5.6.15	Leakage current of the Output Stage	I_{l_OUTn}	–	–	25	µA	C	V_{OUTn}=28V, V_{DD}=5V (diagnosis current off, CONREG3), Tj=60°C
5.6.16	Leakage current of the Output Stage	I_{l_OUTn}	–	–	20	µA	A	V_{OUTn}<28V, V_{DD}=0V, Tj=150°C

Table 11 Electrical Characteristics Power Stages OUT11...OUT14

n = 11...14, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
5.6.17	Leakage current of the Output Stage	I_{l_OUTn}	–	–	35	µA	A	V_{OUTn}<28V, V_{DD}=5V (diagnosis current off, CONREG3), Tj=150°C
Clamping voltage								
5.6.18	Clamping voltage	V_{CL_n}	50	–	60	V	C	I_{OUTn}=2.2A
5.6.19	Clamping voltage	V_{CL_n}	50	–	60	V	A	I_{OUTn}=0.2A
Clamping energy [1]								
5.6.20	Standard operating range, max. 18Mio cycles	E_{CL_OUTn}	–	–	18	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<1.5A
5.6.21	Standard operating range, max. 520Mio cycles	E_{CL_OUTn}	–	–	9	mJ	C	$Tj_{(0)}$=125°C, $I_{OUTn(0)}$<1.2A
5.6.22	Standard operating range, max. 120Mio cycles	E_{CL_OUTn}	–	–	7	mJ	C	$Tj_{(0)}$=140°C, $I_{OUTn(0)}$<1A
5.6.23	Standard operating range, max. 13Mio cycles	E_{CL_OUTn}	–	–	7	mJ	C	$Tj_{(0)}$=150°C, $I_{OUTn(0)}$<1A
5.6.24	Generator defect, max. 0.25Mio cycles or **Item 5.6.25**	E_{CL_OUTn}	–	–	23	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<1.6A
5.6.25	Generator defect, max. 0.25Mio cycles	E_{CL_OUTn}	–	–	11	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<1.1A
5.6.26	Jump start, max. 0.02Mio cycles, or **Item 5.6.27**	E_{CL_OUTn}	–	–	35	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<2.2A
5.6.27	Jump start, max. 0.02Mio cycles	E_{CL_OUTn}	–	–	17	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<1.8A
5.6.28	Load dump, max. 10 pulses, or **Item 5.6.29**	E_{CL_OUTn}	–	–	50	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<2.3[2)]
5.6.29	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	30	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<1.3A
5.6.30	Load dump, max. 10 pulses, or **Item 5.6.31**	E_{CL_OUTn}	–	–	33	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<3.5A[2)]
5.6.31	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	18	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<2A

Table 11 Electrical Characteristics Power Stages OUT11...OUT14

n = 11...14, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Reverse current through OUTn								
5.6.32	In operation mode, static, no destruction	$I_{R_S_OUTn}$	-2.2	–	–	A	C	Tj=150°C,V_{DD}=5V
5.6.33	Without supply voltage, possibly Leakage Current out of neighbor channels. 10ms after the reverse current disappears leakage current criteria are kept.	$I_{R_Soff_OUTn}$	-2.2	–	–	A	C	V_{DD}<1V
5.6.34	In operation mode, No unwanted switching of channels; No unwanted Reset, No unwanted change of Voltage Monitoring Thresholds; No unwanted communication errors or register changes beside diagnostic registers. Possibly unwanted diagnostic entries. Possibly Leakage Current out of neighbor channels.	$I_{R_S_OUTn}$	-1	–	–	A	C	Tj=150°C, V_{DD}=5V

1) Clamping energy, Linear decreasing current, fcl<50Hz

2) PS might switch off to limit the current before reaching the given I_{OUTn} due to reaching I_{OUTn_max}.

5.7 Power Stages OUT15 and OUT16

Table 12 Electrical Characteristics Power Stages OUT15 and OUT16

n = 15 and 16, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Load Current								
5.7.1	Continuous Load Current	I_{OUTn}	–	–	0.6	A	C	–
5.7.2	Extended current time, Accumulated operating time.	t_{OUTn_ec}	–	–	100	h	C	V_{BAT}≤14V, R_L≥6.93Ω
5.7.3	Maximum current (short circuit limited current / switch off threshold).	I_{OUTn_max}	0.6	–	1.5	A	C	–
ON-Resistance								
5.7.4	On-resistance Tj=-40°C	R_{on-40_n}	–	–	1440	mΩ	C	3.5V<V_{DD}<5.5V, I_{OUTn}=0.6A
5.7.5	On-resistance Tj=25°C	R_{on+25_n}	–	–	1780	mΩ	C	3.5V<V_{DD}<5.5V, I_{OUTn}=0.6A
5.7.6	On-resistance Tj≤150°C	R_{on_n}	–	–	2400	mΩ	A	3.5V<V_{DD}<5.5V, I_{OUTn}=0.6A
Delay times, Slew rates (see **Figure 6**)								
5.7.7	Switch on delay	t_{don_n}	–	–	15	µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.7.8	Switch off delay	t_{doff_n}	–	–	15	µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.7.9	Difference of switch on and off delay t_{dif_n}=t_{don_n}-t_{doff_n}	t_{dif_n}	-5	–	5	µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.7.10	Switch on slew rates	s_{on_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.7.11	Switch off slew rates	s_{off_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
Leakage current								
5.7.12	Leakage current of the Output Stage	I_{l_OUTn}	–	–	5	µA	C	V_{OUTn}=14V, V_{DD}=0V, Tj=60°C
5.7.13	Leakage current of the Output Stage	I_{l_OUTn}	–	–	15	µA	C	V_{OUTn}=28V, V_{DD}=0V, Tj=60°C
5.7.14	Leakage current of the Output Stage	I_{l_OUTn}	–	–	35	µA	A	V_{OUTn}<28V, V_{DD}=5V (diagnosis current off, OUT1516), Tj=150°C
Clamping voltage								
5.7.15	Clamping voltage	V_{CL_n}	50	–	60	V	C	I_{OUTn}=0.6A
5.7.16	Clamping voltage	V_{CL_n}	50	–	60	V	A	I_{OUTn}=0.2A

Table 12 Electrical Characteristics Power Stages OUT15 and OUT16

n = 15 and 16, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Clamping energy [1]								
5.7.17	Standard operating range, max. 1.1Mio cycles	E_{CL_OUTn}	–	–	9	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.45A
5.7.18	Standard operating range, max. 40Mio cycles	E_{CL_OUTn}	–	–	6.5	mJ	C	$Tj_{(0)}$=125°C, $I_{OUTn(0)}$<0.3A
5.7.19	Standard operating range, max. 9Mio cycles	E_{CL_OUTn}	–	–	6.5	mJ	C	$Tj_{(0)}$=140°C, $I_{OUTn(0)}$<0.3A
5.7.20	Standard operating range, max. 1Mio cycles	E_{CL_OUTn}	–	–	6.5	mJ	C	$Tj_{(0)}$=150°C, $I_{OUTn(0)}$<0.3A
5.7.21	Generator defect, max. 0.02Mio cycles, or **Item 5.7.22**	E_{CL_OUTn}	–	–	11	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.5A
5.7.22	Generator defect, max. 0.02Mio cycles	E_{CL_OUTn}	–	–	8	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<0.35A
5.7.23	Jump start, max. 0.001Mio cycles, or **Item 5.7.24**	E_{CL_OUTn}	–	–	25	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.75A[2]
5.7.24	Jump start, max. 0.001Mio cycles	E_{CL_OUTn}	–	–	17	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<0.5A
5.7.25	Load dump, max. 10 pulses, or **Item 5.7.26**	E_{CL_OUTn}	–	–	50	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.8A[2]
5.7.26	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	30	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<0.4A
5.7.27	Load dump, max. 10 pulses, or **Item 5.7.28**	E_{CL_OUTn}	–	–	34	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<1A[2]
5.7.28	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	18	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<0.6A
Reverse current through OUTn								
5.7.29	In operation mode, static, no destruction	$I_{R_S_OUTn}$	-0.6	–	–	A	C	Tj=150°C, V_{DD}=5V
5.7.30	Without supply voltage, possibly Leakage Current out of neighbor channels. 10ms after the reverse current disappears leakage current criteria are kept.	$I_{R_Soff_OUTn}$	-0.6	–	–	A	C	V_{DD}<1V
5.7.31	In operation mode, No unwanted switching of channels; No unwanted Reset, No unwanted change of Voltage Monitoring Thresholds; No unwanted communication errors or register changes beside diagnostic registers. Possibly unwanted diagnostic entries. Possibly Leakage Current out of neighbor channels.	$I_{R_S_OUTn}$	-0.2	–	–	A	C	Tj=150°C, V_{DD}=5V

1) Clamping energy, Linear decreasing current, fcl<50Hz

2) PS might switch off to limit the current before reaching the given I_{OUTn} due to reaching I_{OUTn_max}.

5.8 Power Stages OUT17 and OUT18

Table 13 Electrical Characteristics Power Stages OUT17 and OUT18

n = 17 and 18, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Load Current								
5.8.1	Continuous Load Current	I_{OUTn}	–	–	0.6	A	C	–
5.8.2	Extended current time, Accumulated operating time.	t_{OUTn_ec}	–	–	100	h	C	V_{BAT}≤14V, R_L≥6.93Ω
5.8.3	Maximum current (short circuit limited current / switch off threshold).	I_{OUTn_max}	0.6	–	1.5	A	C	–
ON-Resistance								
5.8.4	On-resistance Tj=-40°C	R_{on-40_n}	–	–	780	mΩ	C	I_{OUTn}=0.6A
5.8.5	On-resistance Tj=25°C	R_{on+25_n}	–	–	962	mΩ	C	I_{OUTn}=0.6A
5.8.6	On-resistance Tj≤150°C	R_{on_n}	–	–	1300	mΩ	A	I_{OUTn}=0.6A
Delay times, Slew rates (see **Figure 6**)								
5.8.7	Switch on delay	t_{don_n}	–	–	10	µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.8.8	Switch off delay	t_{doff_n}	–	–	10	µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.8.9	Difference of switch on and off delay t_{dif_n}=t_{don_n}-t_{doff_n}	t_{dif_n}	-5	–	5	µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.8.10	Switch on slew rates	s_{on_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
5.8.11	Switch off slew rates	s_{off_n}	1.5	3.1	7.5	V/µs	C	R_{Load}=28.7Ω, V_{BAT}=14V
Leakage current								
5.8.12	Leakage current of the Output Stage	I_{l_OUTn}	–	–	5	µA	C	V_{OUTn}=14V, V_{DD}=0V, Tj=60°C
5.8.13	Leakage current of the Output Stage	I_{l_OUTn}	–	–	15	µA	C	V_{OUTn}=28V, V_{DD}=0V, Tj=60°C
5.8.14	Leakage current of the Output Stage	I_{l_OUTn}	–	–	35	µA	A	V_{OUTn}<28V, V_{DD}=5V (diagnosis current off, CONREG3), Tj=150°C
Clamping voltage								
5.8.15	Clamping voltage	V_{CL_n}	50	–	60	V	C	I_{OUTn}=0.6A
5.8.16	Clamping voltage	V_{CL_n}	50	–	60	V	A	I_{OUTn}=0.2A

Table 13 Electrical Characteristics Power Stages OUT17 and OUT18

n = 17 and 18, all channels ON or OFF, nominal load conditions, 4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Clamping energy [1]								
5.8.17	Standard operating range, max. 1.1Mio cycles	E_{CL_OUTn}	–	–	9	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.45A
5.8.18	Standard operating range, max. 40Mio cycles	E_{CL_OUTn}	–	–	6.5	mJ	C	$Tj_{(0)}$=125°C, $I_{OUTn(0)}$<0.3A
5.8.19	Standard operating range, max. 9Mio cycles	E_{CL_OUTn}	–	–	6.5	mJ	C	$Tj_{(0)}$=140°C, $I_{OUTn(0)}$<0.3A
5.8.20	Standard operating range, max. 1Mio cycles	E_{CL_OUTn}	–	–	6.5	mJ	C	$Tj_{(0)}$=150°C, $I_{OUTn(0)}$<0.3A
5.8.21	Generator defect, max. 0.02Mio cycles, or **Item 5.8.22**	E_{CL_OUTn}	–	–	11	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.5A
5.8.22	Generator defect, max. 0.02Mio cycles	E_{CL_OUTn}	–	–	8	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<0.35A
5.8.23	Jump start, max. 0.001Mio cycles, or **Item 5.8.24**	E_{CL_OUTn}	–	–	25	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.75A[2]
5.8.24	Jump start, max. 0.001Mio cycles	E_{CL_OUTn}	–	–	17	mJ	C	$Tj_{(0)}$=85°C, $I_{OUTn(0)}$<0.5A
5.8.25	Load dump, max. 10 pulses, or **Item 5.8.26**	E_{CL_OUTn}	–	–	50	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<0.8A[2]
5.8.26	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	30	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<0.4A
5.8.27	Load dump, max. 10 pulses, or **Item 5.8.28**	E_{CL_OUTn}	–	–	34	mJ	C	$Tj_{(0)}$=35°C, $I_{OUTn(0)}$<1A[2]
5.8.28	Load dump, max. 10 pulses	E_{CL_OUTn}	–	–	18	mJ	C	$Tj_{(0)}$=145°C, $I_{OUTn(0)}$<0.6A
Reverse current through OUTn								
5.8.29	In operation mode, static, no destruction	$I_{R_S_OUTn}$	-0.6	–	–	A	C	Tj=150°C, V_{DD}=5V
5.8.30	Without supply voltage, possibly Leakage Current out of neighbor channels. 10ms after the reverse current disappears leakage current criteria are kept.	$I_{R_Soff_OUTn}$	-0.6	–	–	A	C	V_{DD}<1V
5.8.31	In operation mode, No unwanted switching of channels; No unwanted Reset, No unwanted change of Voltage Monitoring Thresholds; No unwanted communication errors or register changes beside diagnostic registers. Possibly unwanted diagnostic entries. Possibly Leakage Current out of neighbor channels.	$I_{R_S_OUTn}$	-0.2	–	–	A	C	Tj=150°C, V_{DD}=5V

1) Clamping energy, Linear decreasing current, fcl<50Hz

2) PS might switch off to limit the current before reaching the given I_{OUTn} due to reaching I_{OUTn_max}.

5.9 Timing Diagram MSC to OUTn

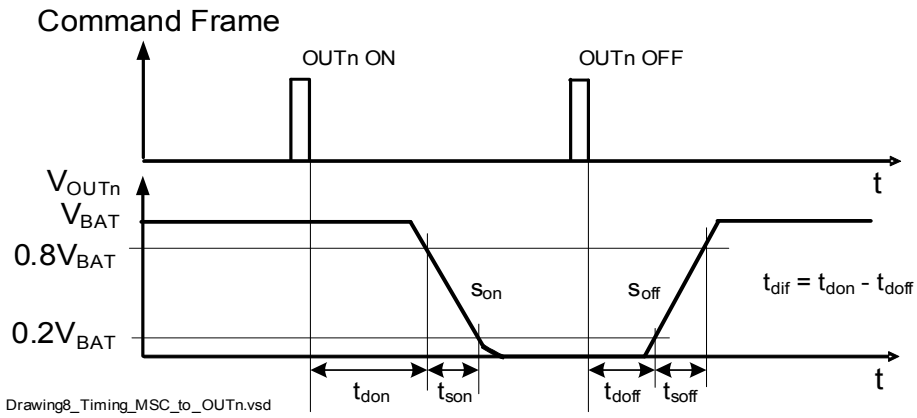


Figure 6 Timing diagram MSC to OUTn (not tested, overview only)

The timing starts with the end of the data frame.

5.10 Parallel connection of PS

All stages are switched on and off simultaneously as all data of the downstream frame becomes valid at the same time. The micro controller has to ensure that the stages which are connected in parallel have always the same state (on or off) and same configuration regarding current limitation (OUTn_SCB). Exceptions are OUT15 and OUT16 which are controlled by command. Therefor these two stages can only be connected in parallel with each other.

The application has to take into account that all maximum ratings are observed (e.g. in case of short circuit the ground current and the power dissipation has to be taken into account).

The Junction Temperature of the power stages which are switched in parallel has to be equal. No parasitic resistors between the parallel connected output channels are considered in **Table 14**. If channels are connected in parallel, they must be connected in parallel for the whole lifetime (no switching between “parallel connection” and “non parallel connection” allowed during lifetime for a single device).

Maximum current:

The maximum value of the maximum current I_{OUTpar_max}(max) of the parallel connected stages is the sum of the corresponding maximum current values I_{OUTn_max}(max). The minimum value of maximum current I_{OUTn_max}(min) is shown in **Table 14**.

ON-Resistance:

The maximum ON-Resistance at 150°C of a parallel connection R_{on_par} = 1 / Σ (1 / R_{on_n}) and the corresponding condition I_{OUTpar_max}(min) can be seen in **Table 14**.

Clamping Energy:

Only equivalent operating points could be added. The conditions ($Tj_{(0)}$, $I_{OUTn(0)}$) for parallel connected stages are the same as for a single stage. The clamping energy of parallel connected stages is
E_{CL_par}(max) = Clamping_energy_factor × Σ E_{CL_OUTn}(max) and shown in **Table 15**.

The performance during parallel connection of channels is specified by design and not subject to the production test. Only the combinations defined in **Table 14** and **Table 15** are supported for parallel connection.

Table 14 Parallel connection, definition of Maximum Current and ON Resistance[1)]

	OUT 1, 3	OUT 2, 4	OUT 5...8	OUT 9, 10	OUT 11...14	OUT 15,16	OUT 17,18	OUT 1, 3	OUT 2, 4	OUT 5...8	OUT 9, 10	OUT 11...14	OUT 15,16	OUT 17,18
	Maximum current for 2 stages [A][2)]							**ON Resistance for 2 stages [mΩ]**						
OUT1, 3	13.6	6.6	6.7	4.7	6.7	–	–	105[3)]	131	163	145	163	–	–
OUT2, 4	6.6	5.1	4.1	3.8	4.1	–	–	131	175	236	201	236	–	–
OUT5...8	6.7	4.1	3.7	3.1	3.7	–	–	163	236	360	284	360	–	–
OUT9, 10	5	3.8	3.1	3.7	3.1	–	–	145	201	284	235	284	–	–
OUT11...14	6.7	4.1	3.7	3.1	3.7	–	–	163	236	360	284	360	–	–
OUT15…16	–	–	–	–	–	1	–	–	–	–	–	–	1200	–
OUT17…18	–	–	–	–	–	–	1	–	–	–	–	–	–	650
	Maximum current for 3 stages [A][2)]							**ON Resistance for 3 stages [mΩ]**						
OUT5...8	–	–	5.2	–	–	–	–	–	–	240	–	–	–	–
OUT11...14	–	–	–	–	5.2	–	–	–	–	–	–	240	–	–
	Maximum current for 4 stages [A][2)]							**ON Resistance for 4 stages [mΩ]**						
OUT5...8	–	–	6.5	–	–	–	–	–	–	180	–	–	–	–
OUT11...14	–	–	–	–	6.5	–	–	–	–	–	–	180	–	–

1) The performance during parallel connection of the channels is specified by design and not subject to production test.
2) The defined current could be forced, without running into overcurrent shutdown. Nevertheless the metal lines on the PCB must be designed for ΣI_{OUTn_max} (max).
3) The defined ON Resistance is valid for operation without clamping (resistive load or inductive load with external freewheeling).

Table 15 Parallel connection, definition of Clamping_energy_factor[1)]

	OUT 5...8	OUT 9, 10	OUT 11...14	OUT 15,16	OUT 17,18
	Clamping_energy_factor for 2 stages				
OUT5...8	0.6	[2)]	[2)]		
OUT9, 10	[2)]	0.6	[3)]		
OUT11...14	[2)]	[3)]	0.6		
OUT15…16	–	–	–	0.6	–
OUT17…18	–	–	–	–	0.6
	Clamping_energy_factor for 3 stages				
OUT5...8	0.45	–	–	–	–
OUT11...14	–	–	0.45	–	–
	Clamping_energy_factor for 4 stages				
OUT5...8	0.4	–	–	–	–
OUT11...14	–	–	0.4	–	–

1) The performance during parallel connection of the channels is specified by design and not subject to production test.
2) The clamping energy of parallel connected stages is the same as clamping energy of a single OUT5...8 stage.
3) The clamping energy of parallel connected stages is the same as clamping energy of a single OUT11...14 stage.

6 Device Self Protection

6.1 Short Circuit Protection

All PS are short circuit protected - see **Chapter 4.2**.

In case of a short circuit to battery voltage the output current is limited by internal current control (OUT1...18).

After a delay time (t_{DIAG_SCB}) the output is turned off, if it´s configured in MSC register CONREG1, 2, OUT1516 to switch off (OUT1-18).

6.2 Over Temperature Shut Down

If critical overtemperature (overtemperature shut down threshold T_{OUTn_OTSD}) is detected in one stage the stage is switched off to protect the circuit against damage, see logic diagram, state D (**Chapter 8.3**).

All self protection circuits (Short Circuit to Battery and Over Temperature Shut Down) are functional in undervoltage and overvoltage condition from V_{DD_POR} up to V_{DD_MR}.

Registration of short circuit to battery (SCB) and overtemperature (DOT) in the diagnostic registers during undervoltage or overvoltage condition is not guaranteed. But the stage is switched off as defined in configuration register.

6.3 Battery Voltage Monitoring

The Battery Voltage Monitoring allows the detection of Over Voltage Conditions. In case of Over Voltage V_{SVBATT_OVSD}, the monitoring shuts down the Power Stages after a delay time t_{OUT_OVSD}. The Battery Voltage Monitoring acts as an Enable of the Output Stages and does not clear the control bits.

This functions supports the reduction of clamping energy to be dissipated in the power stage in case of over voltage conditions, such as Load Dumps.

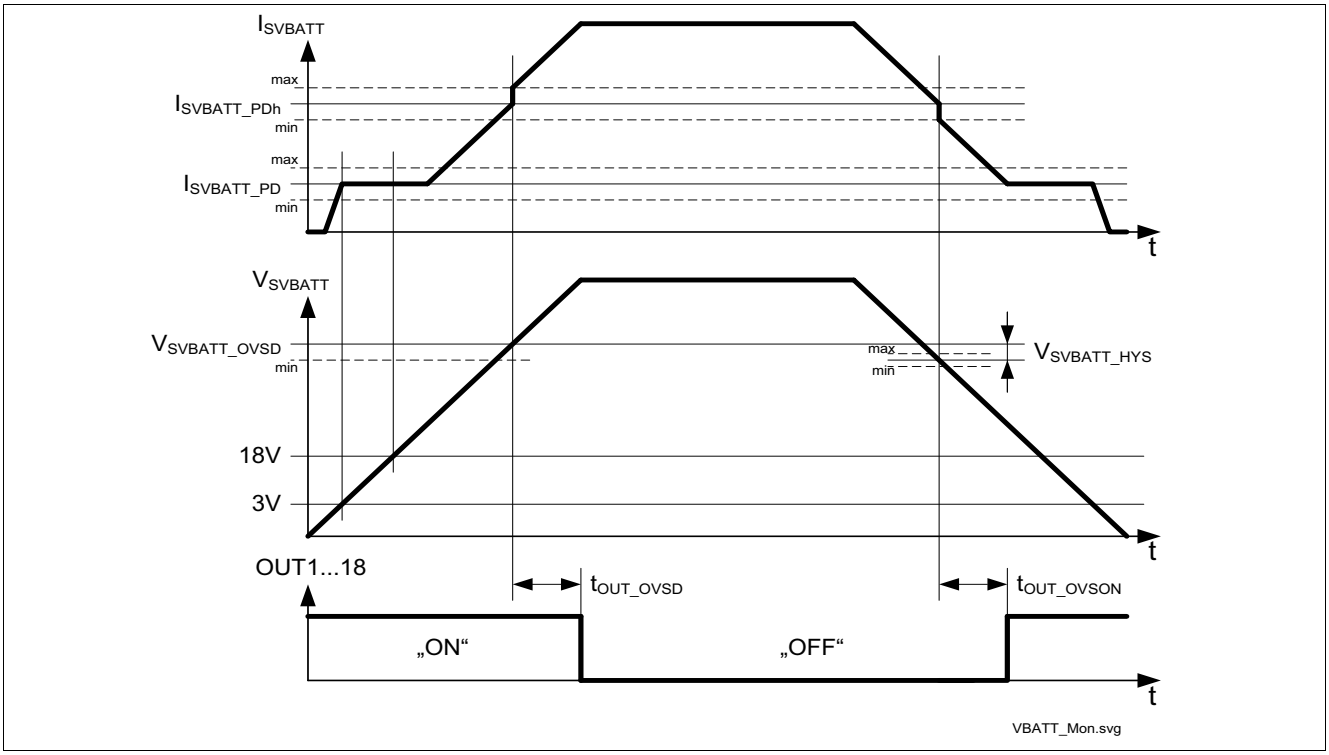


Figure 7 Battery Voltage Monitoring

6.4 Electrical Characteristics

Table 16 Self Protections

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Self Protection								
6.4.1	Self protection temperature threshold Junction temperature of OUTn (n=1...18)[1]	T_{OUTn_OTSD}	T_{OUTn_OTW}+0	–	T_{OUTn_OTW}+30	K	C	–
6.4.2	Self protection temperature hysteresis, OUTn (n=1...18)	$T_{OUTn_OTSDHYS}$	–	10	–	K	C	–
SVBATT Pin (Battery Voltage Monitoring Pin)								
6.4.3	SVBATT Pin Voltage, Battery Overvoltage Shut Down Threshold	V_{SVBATT_OVSD}	29	–	35	V	B	
6.4.4	SVBATT Pin Voltage, Battery Overvoltage Shut Down Hysteresis	V_{SVBATT_HYS}	0.25	–	1	V	C	
6.4.5	SVBATT Pin internal pull down current	I_{SVBATT_PD}	1	–	20	µA	C	3V<V_{SVBATT}<18V
6.4.6	SVBATT Pin internal pull down current	I_{SVBATT_PDh}	20	–	80	µA	C	[2]
6.4.7	SVBATT Pin internal pull down current	I_{SVBATT_PD}	1	–	500	µA	C	18V<V_{SVBATT}<40V
6.4.8	Filter time before Output Stages shut down in case of V_{SVBATT_OVSD} is exceeded	t_{OUT_OVSD}	5	–	20	µs	B	–
6.4.9	Filter time before Output Stages switch on again	t_{OUT_OVSON}	60	–	135	µs	B	–
6.4.10	Factory test mode activation	V_{SVBATT_TM}	–	–	-2	V	B	[3]

1) See **Chapter 8**, **Item 8.5.6** Diagnosis, Overtemperature warning diagnosis threshold.

2) V_{SVBATT}=V_{SVBATT_OVSD} during voltage increase, respectively V_{SVBATT}=V_{SVBATT_OVSD}-V_{SVBATT_HYS} during voltage decrease. See **Figure 7**.

3) Not intended to be used in application. Factory test mode entry condition violates Absolute Maximum Rating **Item 4.2.10**.

7 Supervisory (DIS5_10, DELAYIN, DELAYOUT)

Table 17 DIS5_10, DELAYIN, DELAYOUT

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Pin DIS5_10								
7.0.1	DIS5_10 input low level	$V_{DIS5_10_L}$	-0.3	–	1	V	B	–
7.0.2	DIS5_10 input high level	$V_{DIS5_10_H}$	2	–	36	V	B	–
7.0.3	DIS5_10 input hysteresis	$V_{DIS5_10_HYS}$	0.1	–	0.5	V	C	–
7.0.4	DIS5_10 input current	I_{DIS5_10}	-100	–	5	µA	C	-0.2V<V_{DIS5_10}< V_{DD}
7.0.5	DIS5_10 input current	I_{DIS5_10}	-400	–	–	µA	C	-0.3V<V_{DIS5_10}
7.0.6	DIS5_10 Input current	I_{DIS5_10}	–	–	100	µA	C	V_{DD}<V_{DIS5_10}< 36V
7.0.7	DIS5_10 pull-up current	I_{DIS5_10}	-100	–	-20	µA	A	0V<V_{DIS5_10}< V_{DD} – 1.5V
7.0.8	Filtering time before switching OUTn, high- or low-pulses on DIS5_10, n=5...10	t_{DIS5_10}	60	–	135	µs	C	–
Pin DELAYIN for DELAYOUT function (lower threshold)								
7.0.9	DELAYIN input low level for DELAYOUT	$V_{DELAYIN_L}$	-0.3	–	0.16*V_{DD}	V	B	–
7.0.10	DELAYIN input high level for DELAYOUT	$V_{DELAYIN_H}$	0.24*V_{DD}	–	36	V	B	–
7.0.11	DELAYIN input hysteresis for DELAYOUT	$V_{DELAYIN_HYS}$	0.02	–	0.1	V	C	–
7.0.12	DELAYIN input pull-down resistor	$R_{DELAYIN}$	168	–	312	kΩ	A	1V<$V_{DELAYIN}$<40V
7.0.13	DELAYIN input current	$I_{DELAYIN}$	-400	–	20	µA	C	-0.3V<$V_{DELAYIN}$ <1V
7.0.14	Rising edge long filter time before switching DELAYOUT or RES15_16	$t_{DELAYIN_GLITCH_long}$	7.5	–	24	ms	C	CONREG3.6='1'
7.0.15	Rising edge short filter time before switching DELAYOUT or RES15_16	$t_{DELAYIN_GLITCH_short}$	60	–	135	µs	C	CONREG3.6='0'
DELAYIN - Filtering time before switching DELAYOUT low								
7.0.16	Long delay for $t_{DELAYIN_x}$, default	$t_{DELAYIN_L}$	800	–	1600	ms	C	CONREG4.0='1', CONREG4.1='1'
7.0.17	Medium long delay for $t_{DELAYIN_x}$	$t_{DELAYIN_ML}$	400	–	800	ms	C	CONREG4.0='1', CONREG4.1='0'
7.0.18	Medium short delay for $t_{DELAYIN_x}$	$t_{DELAYIN_MS}$	200	–	400	ms	C	CONREG4.0='0', CONREG4.1='1'
7.0.19	Short delay for $t_{DELAYIN_x}$	$t_{DELAYIN_S}$	100	–	200	ms	C	CONREG4.0='0', CONREG4.1='0'

Table 17 DIS5_10, DELAYIN, DELAYOUT

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Pin DELAYIN for RES15_16 function (higher threshold)								
7.0.20	DELAYIN input low level for RES15_16	$V_{DELAYIN_RES15_16_L}$	-0.3	–	0.44*V_{DD}	V	B	–
7.0.21	DELAYIN input high level for RES15_16	$V_{DELAYIN_RES15_16_H}$	0.52*V_{DD}	–	36	V	B	–
7.0.22	DELAYIN input hysteresis for RES15_16	$V_{DELAYIN_RES15_16_HYS}$	0.02	–	0.1	V	C	–
Pin DELAYOUT								
7.0.23	DELAYOUT output low voltage	$V_{DELAYOUT_OUTL}$	–	–	0.7	V	A	V_{DD}=2.5V, $I_{DELAYOUT}$<2mA
7.0.24	DELAYOUT output low voltage	$V_{DELAYOUT_OUTL}$	–	–	1	V	A	2.5V<V_{DD}<36V, $I_{DELAYOUT}$<6.5mA
7.0.25	Maximum current (short circuit limited current)[1)]	$I_{DELAYOUT_max}$	15	–	–	mA	C	–
7.0.26	DELAYOUT passive output high voltage	$V_{DELAYOUT_OUTH}$	V_{DD} - 1.5	V_{DD}	–	V	A	no load
7.0.27	DELAYOUT pull-up current	$I_{DELAYOUT_INL}$	-50	–	-4	µA	A	0V<$V_{DELAYOUT}$< V_{DD}–1.5V, [2)]
7.0.28	DELAYOUT input current	$I_{DELAYOUT_INH}$	-10	–	10	µA	C	V_{DD}<$V_{DELAYOUT}$< 36V

1) Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous or repetitive operation. Application must take care, that current into this pin does not exceed 15mA.

2) DELAYOUT as Output is not active

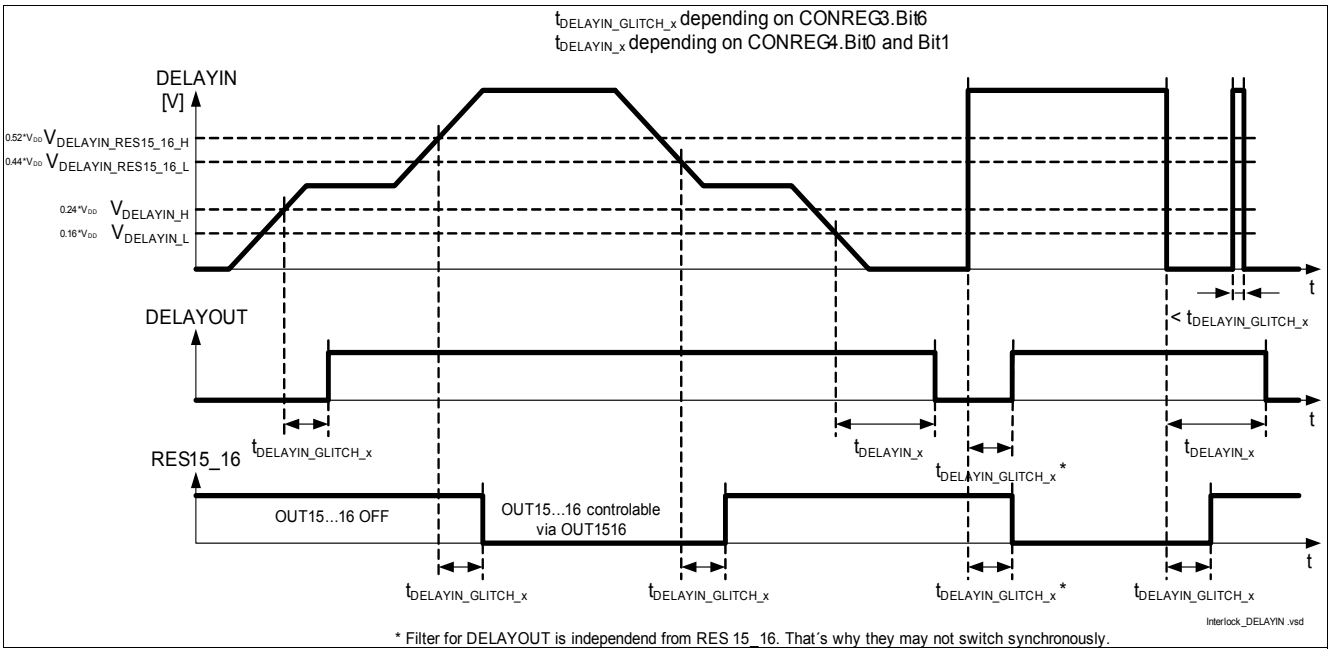


Figure 8 Timing DELAYIN

8 Diagnosis

8.1 Diagnostic Functions

All PS have fault diagnostic functions:

- short circuit to battery: (SCB) can be detected if stages are turned on
- short circuit to ground: (SCG) can be detected if stages are turned off
- open load: (OL) can be detected if stages are turned off
- Diagnosis overtemperature: (DOT) is set if Overtemperature Warning OTW occurs in ON-state or Overtemperature Shutdown OTSD occurs in any state

SCB is recognized if the output current reaches I_{OUTn_max} when the stage is switched on. If, after the filtering time (t_{DIAG_SCB}) has expired, the failure is still present, it is stored in the diagnostic register (DIAREG1...5). This may be caused by a short circuit to battery voltage (V_{BAT} up to V_{BAT_SC}) or by a load with too low impedance (e.g. load switched on under cold conditions).

In addition to this, there is the extended SCB behavior available, when CONREG3.EXT_SCB=”1”. In this case V_{OUTn} is checked in addition to I_{OUTn} and the diagnosis register SCB is only set, if I_{OUTn_max} and V_{OL} is reached for longer than t_{DIAG_SCB}. This feature is available for OUT5...14 only and shown in **Figure 9**.

A SCB condition is stored in the diagnosis register. It turns off the output dependent on configuration register (CONREG1, CONREG2, OUT1516). The output can be turned on again even if the SCB bit in the diagnosis registers have not been cleared yet (e.g. by polling the registers). Turning on the outputs won't clear the SCB bit.

The output current I_{OUTn} may overshoot before the current limiter reacts and limits the output current to I_{OUTn_max}. However, this overshoot (which depends on the external load) will not damage the device.

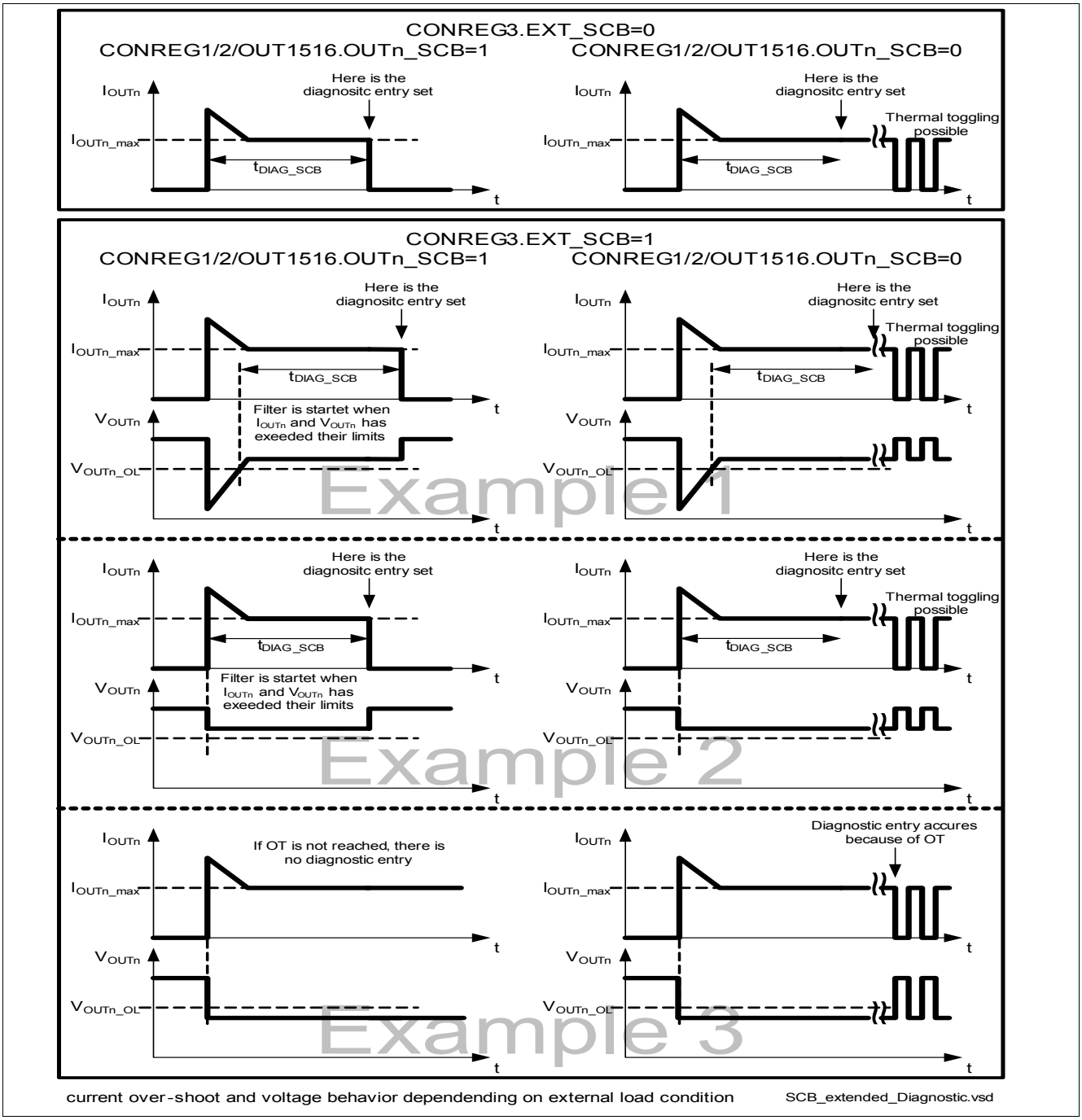


Figure 9 SCB Diagnosis function

Depending on the configuration of the stage (CONREG1, 2, OUT1516) the stage is switched off or remains functional in current limited mode with fault entry in the diagnostic register.

The OTSD threshold (T_{OUTn_OTSD}) has a hysteresis and switches off the channel (see **Chapter 6**); The OTW (T_{OUTn_OTW}) threshold has no hysteresis and is diagnosis only. The stage is not switched off by OTW. Only if temperature rises above shutdown threshold (T_{OUTn_OTSD}) the stage is disabled for device self protection. After this, the stage won´t be enabled again until temperature falls below Self protection temperature hysteresis ($T_{OUTn_OTSDHYS}$) (see **Chapter 6**).

Over Temperature Warning [T_{OTW}],
Over Temperature Shut Down [T_{OTSD}],
Over Temperature Shut Down Hysteresis [T_{OTSD_HYS}],
for OUT1...18

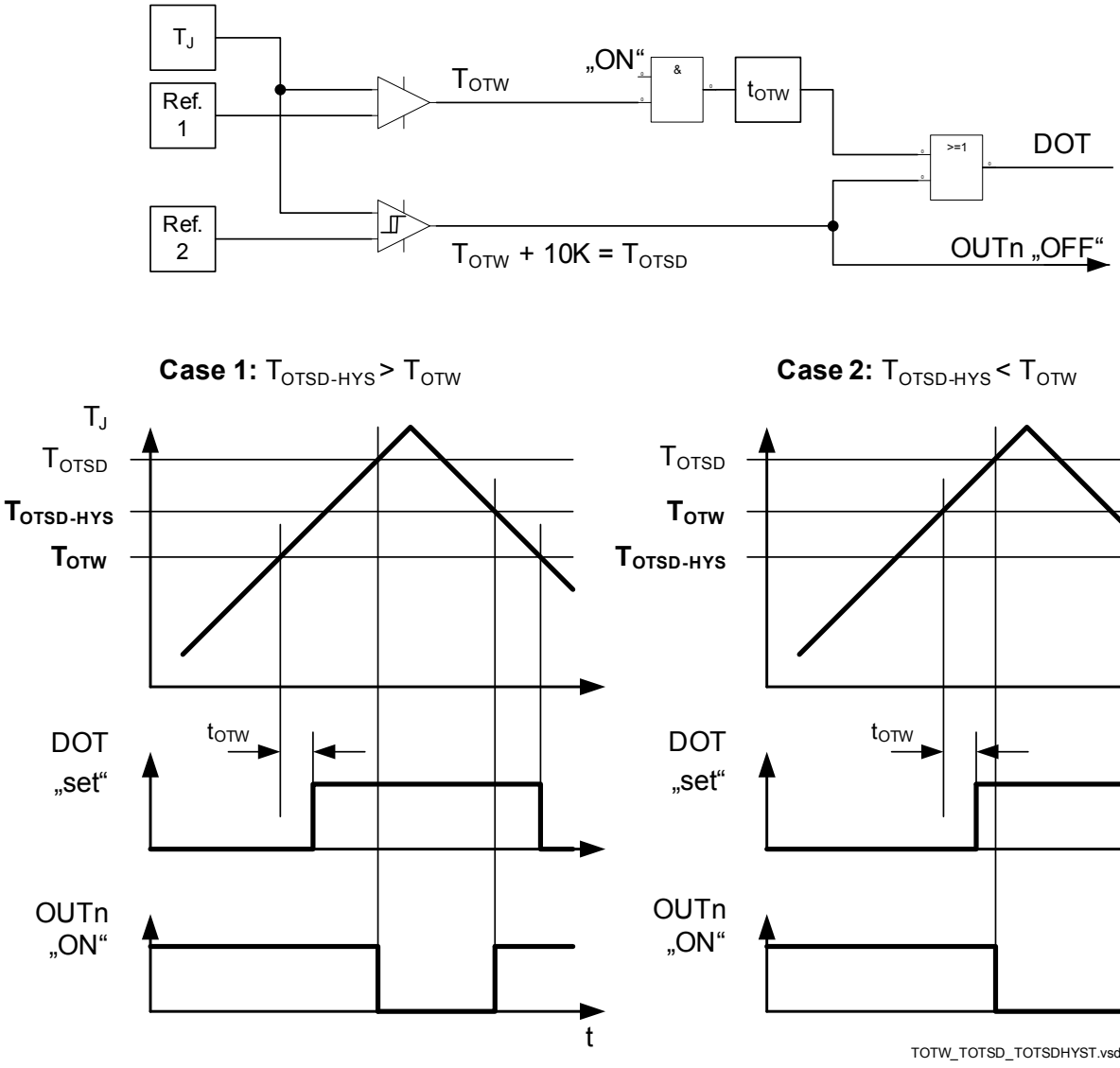


Figure 10 Temperature Thresholds (see also Chapter 6)

OL or SCG is recognized using two thresholds (V_{OUTn_SCG} and V_{OUTn_OL}) and a bias voltage source with current limit for each output.

For OUT11...OUT18 it is possible by configuration to switch off the internal diagnostic pull-down current source. In this case diagnosis of OL is deactivated, no entry of OL into diagnostic register, even if $V_{OUTn_SCG} < V_{OUTn} < V_{OUTn_OL}$. Diagnosis of SCG remains functional.

See **Chapter 8.3** for specified values of diagnostic currents and threshold voltages.

The fault conditions SCB, SCG, OL and DOT will not be stored until an integrated filtering time (t_{DIAG_SCB}, t_{DIAG_SCG}, t_{DIAG_OL}, t_{DIAG_OTW}) has expired. If at one output, several errors occur in a sequence, the newest detected error is stored to the diagnosis register (after filtering time).

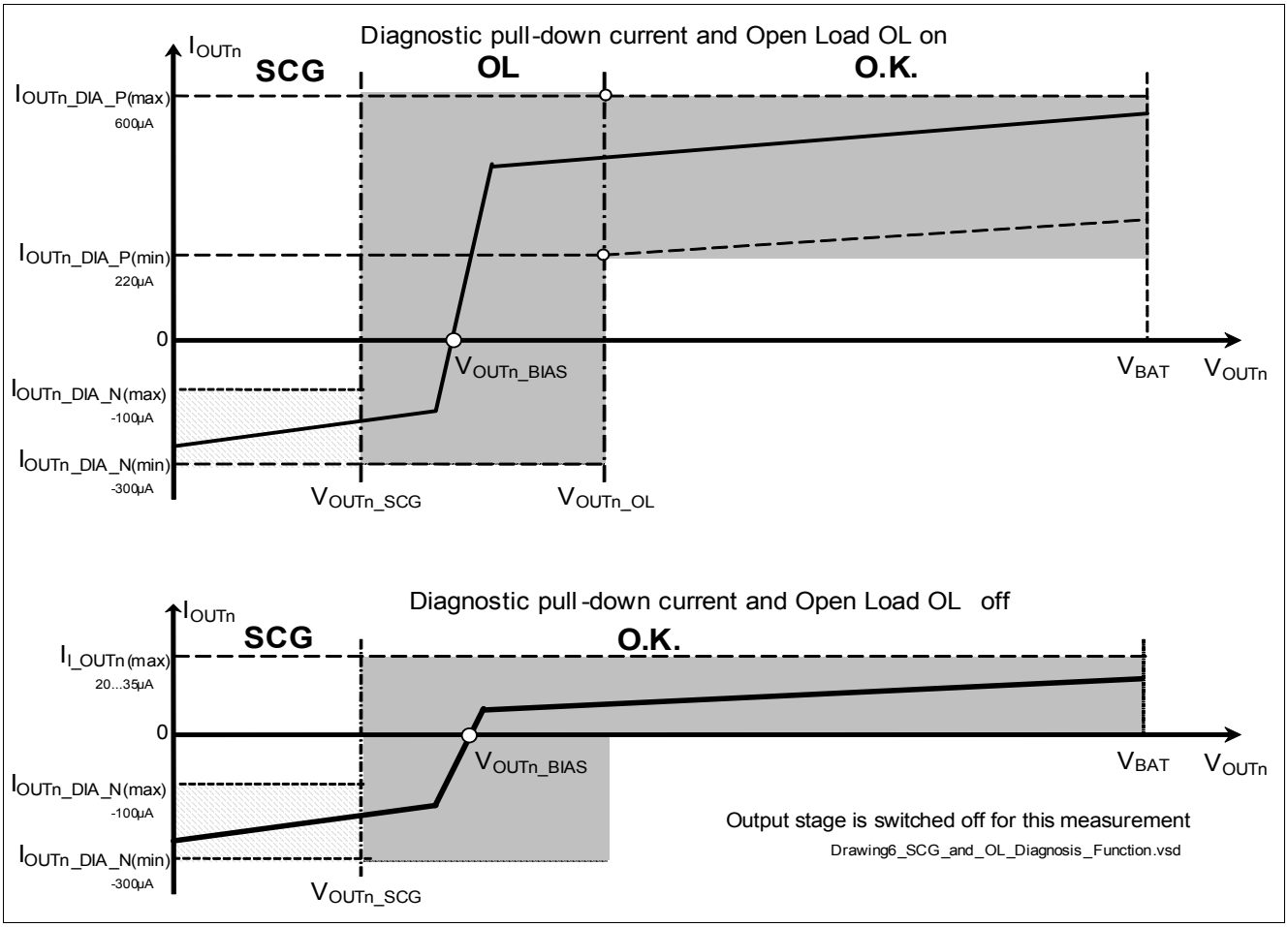


Figure 11 SCG and OL diagnosis function (not tested, overview only)

8.2 Encoding of Diagnostic Information

All fault conditions are encoded in two bits per stage and are stored in the corresponding registers (DIAREG1...5). Additionally there is one central diagnostic overtemperature bit (COTW) (this bit is set to ‘0’ if DOT occurred at any stage).

The common failure bit (DIAREG6, bit FAILURE_FLAG) is set to ‘0’ if SCB, SCG, OL or DOT is detected on any output stage (OUT1...18). Only if all the stage diagnostic bits are ‘1’, the FAILURE_FLAG bit is ‘1’.

The diagnosis registers can be read via MSC.

When a valid MSC read command (RD_DATA) is detected, the selected diagnosis register information is moved to a shift register for transmission (MSC upstream). At the same time the selected diagnosis register is cleared.

Table 18 Encoding of diagnosis information

Encoding of the diagnosis bits of the device		
OUTn_DIA2	OUTn_DIA1	description
1	1	Power stage ok
1	0	Short circuit to battery (SBC) or diagnostic overtemperature (DOT)
0	1	Open load (OL)
0	0	Short circuit to ground (SCG)

8.3 State Diagram of the Device Diagnosis

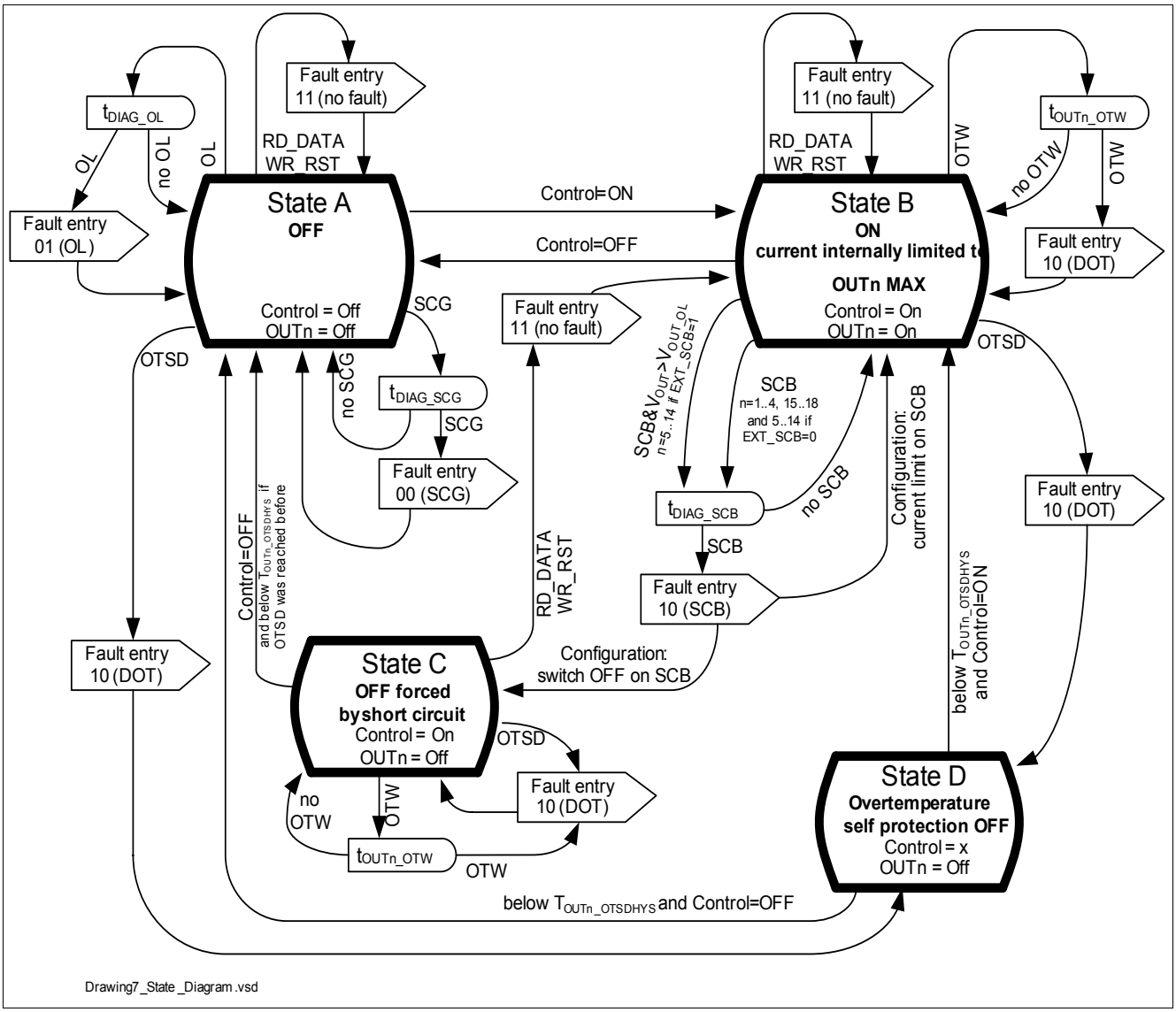


Figure 12 State diagram of the device diagnosis (not tested, overview only)

Outputs are switched inactive if V_{DD} is out of range or RST respectively ABE is externally pulled low. After a reset the stages start in state A (OFF state). If a stage is getting overheated above the overtemperature shutdown threshold (T_{OUTn_OTSD}, **Item 6.4.1**) it is entering state D (switched off for self protection) independent from its current state. Leaving this state is only possible if temperature falls below Self Protection Temperature Hysteresis ($T_{OUTn_OTSDHYS}$, **Item 6.4.2**).

8.4 Reset of the Diagnostic Information

The diagnostic registers are set to its reset value individually at readout by their RD_DATA command, or all together by WR_RST command, POR or RST.

At the same time, the filters t_{DIAG_SCB}, t_{DIAG_SCG}, t_{DIAG_OL} are re-set. The filter t_{DIAG_OTW} is not re-set.

In the case a stage is shut off because of SCB, by readout of the diagnostic information via RD_DATA instruction the DIAREGx entry is cleared and output is activated again. Because SCB could only be detected when the stage is switched on, the output is activated and shut off again after the shutoff delay, if SCB condition is still existent.

Some register bits are not cleared by read-out or reset, see tables in **Chapter 12.2**.

8.5 Electrical Characteristics

Table 19 Diagnosis

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Diagnosis filter time, delay time fault condition to switch off, OUTn (n=1...18)								
8.5.1	Overtemperature Warning	t_{DIAG_OTW}	15	–	30	µs	C	–
8.5.2	Short to Battery Voltage	t_{DIAG_SCB}	60	–	135	µs	B	–
8.5.3	Short to Ground	t_{DIAG_SCG}	60	–	135	µs	B	–
8.5.4	Open Load	t_{DIAG_OL}	60	–	135	µs	B	–
8.5.5	Diagnosis Fault entry delay, delay time after diagnosis filter time has expired until fault entry is stored in corresponding diagnostic register	t_{DIAG_DELAY}	0	–	5	µs	C	–
8.5.6	Overtemperature warning diagnosis threshold	T_{OUTn_OTW}	150	–	190	°C	C	–
8.5.7	Short circuit to ground diagnosis threshold	V_{OUTn_SCG}	0.6*V_{DD} -0.2	–	0.6*V_{DD} +0.2	V	B	–
8.5.8	Open load diagnosis threshold stage disabled	V_{OUTn_OL}	V_{DD}-0.2	–	V_{DD}+0.3	V	B	1)
8.5.9	Diagnostic bias voltage stage disabled	V_{OUTn_BIAS}	0.7*V_{DD} -0.2	–	0.7*V_{DD} +0.2	V	A	1)
Diagnostic current of OUTn 1)								
8.5.10	Diagnostic pull down current	$I_{OUTn_DIA_P}$	270	–	550	µA	A	V_{OUTn}=14V
8.5.11	Diagnostic pull down current	$I_{OUTn_DIA_P}$	220	–	550	µA	C	V_{OUTn_OL}< V_{OUTn}<V_{BAT}
8.5.12	Diagnostic pull up current	$I_{OUTn_DIA_N}$	-300	–	-100	µA	A	V_{OUTn}=0V
8.5.13	Diagnostic pull up current	$I_{OUTn_DIA_N}$	-300	–	-100	µA	C	0V<V_{OUTn} <V_{OUTn_SCG}

Table 19 Diagnosis

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Reverse Current Detection OUTn (n=1...18)								
8.5.14	Reverse Current detection voltage	V_{REVCUR}	-0.3	–	-0.03	V	C	–
8.5.15	Reverse Current filter time	t_{REVCUR}	26	–	60	µs	C	–

1) OUTn_DIAC='1'

8.6 Timing

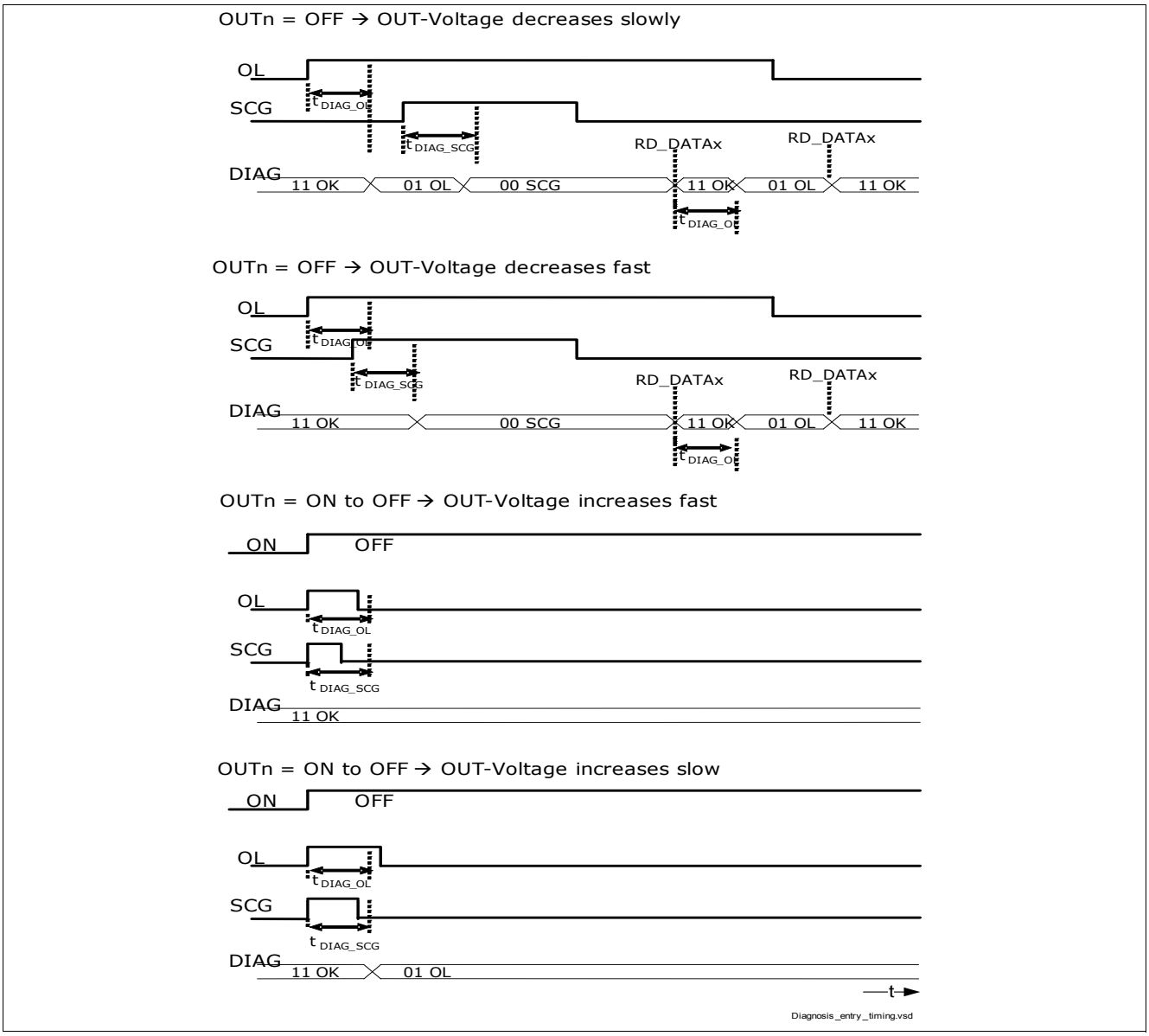


Figure 13 Timing and logic entry of diagnosis information to diagnosis register

9 Supply, V_{DD} Monitoring, Reset and ABE

9.1 General functions of V_{DD} Monitoring

V_{DD} -Monitoring is measured with reference to GNDABE. Power On Reset (POR) is measured with reference to PGND.

The state of V_{DD} monitoring is stored in DIAREG7 and can be read out via MSC.

V_{DD} monitoring detects supply voltage outside the specified range. It disables stages but does not reset registers CONREGx, DIAREGx

In case of V_{DD} failure, the stages must be switched off according CONREG4.ABE_IMPACT -setting, even if Pin ABE is high level because of external short circuit to V_{DD} or V_{BAT} (up to V_{BAT_SC}).

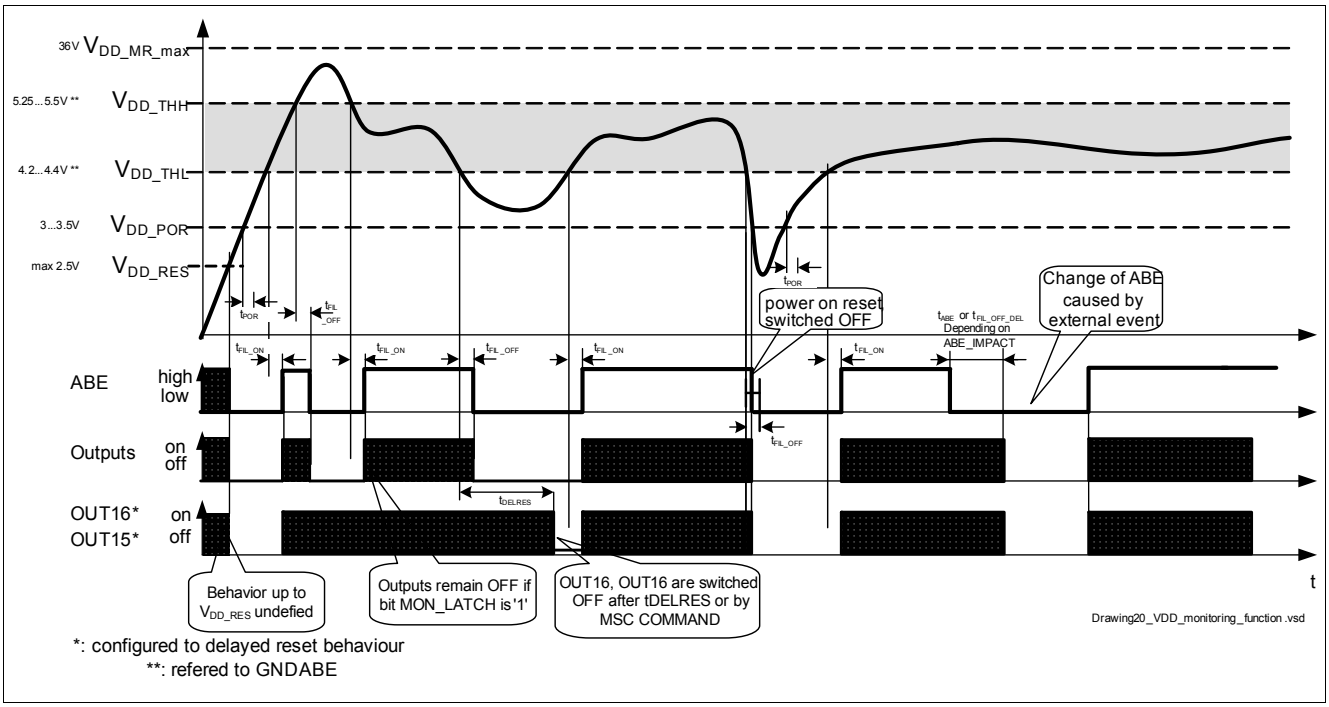


Figure 14 V_{DD} monitoring function (not tested, overview only)

Figure 14 explanation: In the “shaded” area of “Outputs”, the output channels may be switches ON or OFF by MSC DATA-Frame. In shaded area of “OUT15, OUT16” the output channels may be switched or remain ON or OFF dependent on the register settings OUT1516.

OUT15 and OUT16 can´t be switched on during over-, undervoltage, ABE, MSC_MON or RST. Switching off is possible (see **Figure 1**).

POR (V_{DD} < V_{DD_POR}) switches off all stages without delay.

9.2 V_{DD} Undervoltage

If the V_{DD} voltage is lower than the supply voltage supervisory lower threshold (V_{DD_THL}), all output stages are shut off after a filtering time (t_{FIL_OFF}) and active low signal is generated at the bi-directional pin ABE.

The only exception is OUT15 and OUT16, if configured to delayed reset behavior. These outputs then remain functional in undervoltage condition, until

- filtering time (t_{DELRES}) has expired, or
- stage is switched off by MSC command or
- V_{DD} falls below the power-on-reset threshold (V_{DD_POR}) or
- RES15_16 gets active.

OUT15 or OUT16 cannot be switched on by MSC command in undervoltage condition.

At the transition from undervoltage to normal voltage the signal at Pin ABE goes high after a filtering time (t_{FIL_ON}) has expired. Output registers are cleared to “1” (output stages remain off until switched on again via MSC data frame). During undervoltage condition no new fault conditions are written to diagnosis registers, the content is frozen. However, data and configuration registers still can be accessed (read and write) using MSC commands.

If V_{DD} falls below the power-on-reset supply voltage (V_{DD_POR}) all stages are shut off and ABE is switched active low.

When V_{DD} is rising above the power-on-reset supply voltage threshold (V_{DD_POR}) a power-on-reset is internally generated (t_{POR}), setting all registers to its default state (all stages switched off, all registers cleared to default).

9.3 V_{DD} Overvoltage

If the V_{DD} voltage is higher than the supply voltage supervisory upper threshold (V_{DD_THH}), all output stages are shut off after a filtering time (t_{FIL_OFF}) and active low signal is generated at the bi-directional Pin ABE.

The only exception is OUT15 and OUT16, if configured to delayed reset behavior. These outputs then remain functional in overvoltage condition, until

- filtering time (t_{DELRES}) has expired or
- stage is switched off by MSC command or
- RES15_16 gets active.

OUT15 or OUT16 cannot be switched on by MSC command in overvoltage condition.

The behavior of the ABE level and output stages on the return of VDD from overvoltage to the correct range is configured in CONREG4, bit MON_LATCH).

  – 1: ABE is latched and outputs remain off after overvoltage, t_{DELRES} continues to expire and switches off OUT15 and OUT16. Return to normal operation is only possible with power-on reset or by changing this bit via MSC command to “0”.
  – 0: ABE is inactive after V_{DD} returned to normal operating voltage and filtering time has expired.

At the transition from overvoltage to normal condition, output registers are cleared to “1” (output stages remain off until switched on again via MSC). During overvoltage condition no new fault conditions are written to diagnosis registers, the content is frozen. However, data and configuration registers still can be accessed (read and write) using MSC commands.

9.4 Thresholds

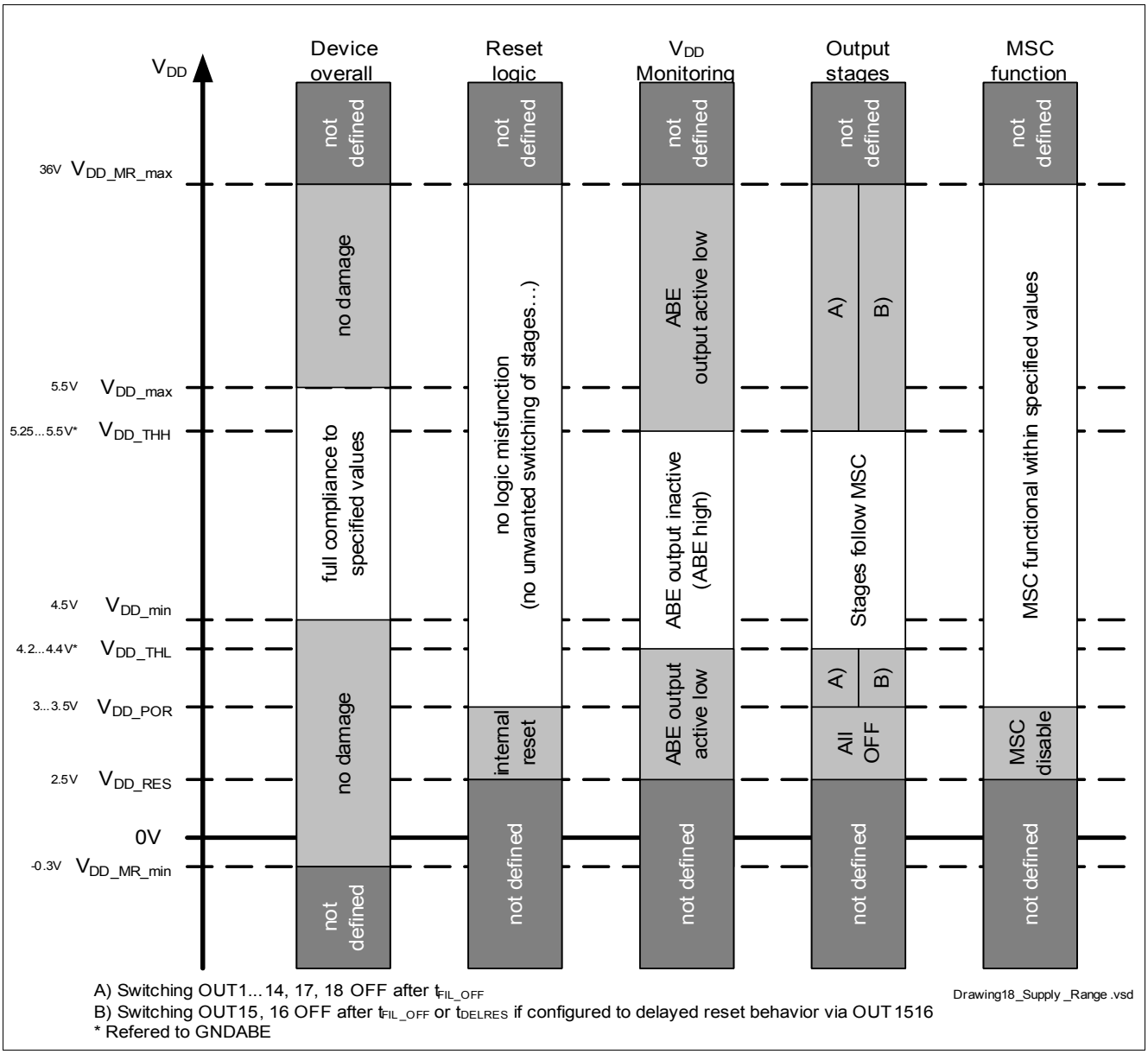


Figure 15 Operating Supply Range

9.5 ABE Pin

ABE is functional as input and output.

During a low on pin ABE (pulled low by the internal open drain device or forced low by an external source), the output registers are cleared to '1' switching off outputs OUT1…OUT14, OUT17, OUT18. Behavior of OUT15 and OUT16 depends on configuration register settings. Programmable filter times apply. See **Figure 1** and **Figure 16** for details.

9.6 Testing of V_{DD} Monitoring

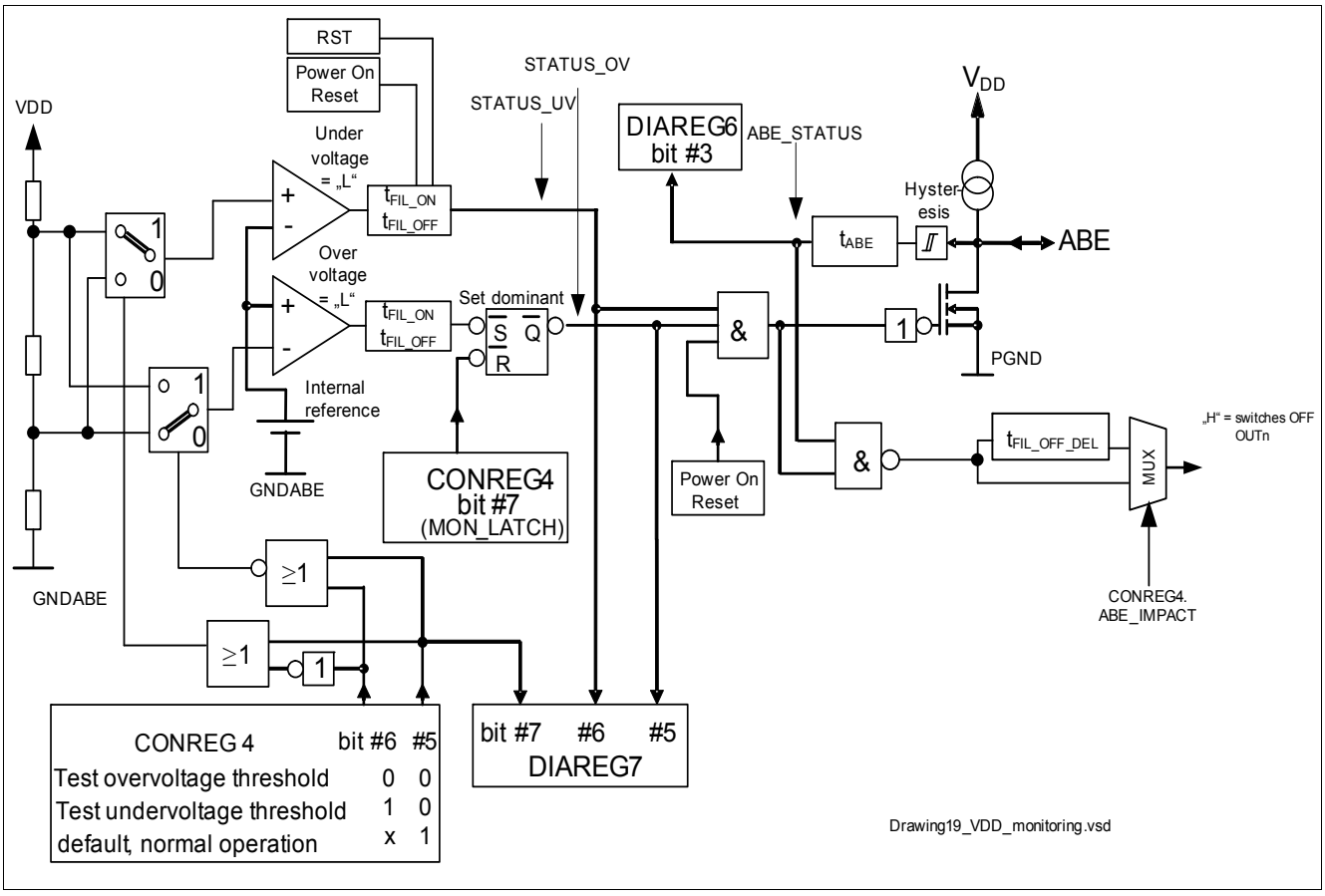


Figure 16 Block Diagram of V_{DD} Monitoring

The stages are switched off if under- or overvoltage is detected in any case OUT15,16 might be delayed, dependent on register OUT1516.

9.7 Testing procedure of V_{DD} Monitoring in the application

Testing upper threshold in application (VDD is 5V):

By writing xxxxx00xb into CONREG4, the overvoltage threshold is reduced to V_{TEST_THH}. In DIAREG7 bit 5 and 7 have to be LOW then. After writing xxxxx1x0b to CONREG4, bit 5 and 7 in DIAREG7 must be HIGH again.

Testing lower threshold in application (VDD is 5V):

By writing xxxxx01xb into CONREG4, the undervoltage threshold is increased to V_{TEST_THL}. In DIAREG7 bit 6 and 7 have to be LOW then. After writing xxxxx1xxb to CONREG4, bit 6 and 7 in DIAREG7 must be HIGH again.

9.8 Electrical Characteristics

Table 20 Power Supply, POR, V_{DD} Monitoring, ABE and RST

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Power Supply								
9.8.1	Operational Supply Current	I_{VDD}	–	18	25	mA	C	4.5V<V_{DD}<5.5V, All channels ON or OFF, nominal load conditions
9.8.2	Overvoltage Supply Current	I_{VDD_0V}	–	–	50	mA	C	5.5V<V_{DD}<36V, no damage
Power ON Reset								
9.8.3	Reset Circuit Functional, Internal reset active for V_{DD_RES}<V_{DD}<V_{DD_POR} All stages switched inactive and internal registers are cleared.	V_{DD_RES}	–	–	2.5	V	B	–
9.8.4	Power On Reset Threshold Below this threshold the device is in reset state, all registers are cleared. Device starts operation (V_{DD} monitoring forces stages off) after t_{POR}, when V_{DD} is rising above this threshold.	V_{DD_POR}	3	–	3.5	V	B	–
9.8.5	Power On Reset Extension Time	t_{POR}	180	–	360	µs	C	–
V_{DD} Monitoring								
9.8.6	Undervoltage threshold, ABE turns active low and stages are turned off when V_{DD} is below this threshold	V_{DD_THL}	4.1	–	4.4	V	B	1)
9.8.7	Overvoltage threshold, ABE turns active low and stages are turned off when V_{DD} is above this threshold	V_{DD_THH}	5.25	–	5.5	V	B	1)
9.8.8	Filtering time before switching off, V_{DD} is rising above V_{DD_THH} or falling below V_{DD_THL} all outputs except OUT15, OUT16 if configured to delayed reset	t_{FIL_OFF}	60	–	135	µs	C	–
9.8.9	Filtering time with delay before switching off if ABE is configured to delayed switching of stages by CONREG4, switching OFF because of VDD Monitoring or falling edge of ABE is de-bounced 2)	$t_{FIL_OFF_DEL}$	30	–	80	ms	C	–

Table 20 Power Supply, POR, V_{DD} Monitoring, ABE and RST

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
9.8.10	Delayed Reset for OUT15 and OUT16, if configuration bits are set to delayed reset	t_{DELRES}	400	–	800	ms	C	–
9.8.11	Filtering time before switching on, returning to V_{DD_THL}<V_{DD}<V_{DD_THH}	t_{FIL_ON}	60	–	135	µs	C	–
9.8.12	Test V_{DD} monitoring undervoltage, VDD monitoring test active	V_{TEST_THL}	5.15	–	5.6	V	B	1)
9.8.13	Test V_{DD} monitoring overvoltage, VDD monitoring test active	V_{TEST_THH}	4.1	–	4.5	V	B	1)
ABE as Input								
9.8.14	ABE input low level	V_{ABE_INL}	-0.3	–	0.3*V_{DD}	V	B	–
9.8.15	ABE input high level	V_{ABE_INH}	0.7*V_{DD}	–	36	V	B	–
9.8.16	ABE input hysteresis	V_{ABE_INHYS}	0.2	–	1	V	C	–
9.8.17	ABE input current	I_{ABE_INL}	-100	–	-20	µA	A	-0.2V<V_{ABE}<V_{DD}–1.5V3)
9.8.18	ABE input current	I_{ABE}	-400	–	–	µA	C	-0.3V<V_{ABE}3)
9.8.19	ABE input current	I_{ABE_INH}	-5	–	5	µA	A	V_{DD}<V_{ABE}<36V
9.8.20	ABE pulse width, ABE requires min. low level pulse width	t_{ABE}	0.5	–	3.5	µs	C	
ABE as Output								
9.8.21	ABE output low voltage	V_{ABE_OUTL}	–	–	1	V	A	2.5V<V_{DD}<V_{DD_THL}, I_{ABE}<6.5mA
9.8.22	ABE output low voltage	V_{ABE_OUTL}	–	–	1	V	A	V_{DD_THH}<V_{DD}<36V, I_{ABE}<7mA
9.8.23	ABE output low voltage	V_{ABE_OUTL}	–	–	0.7	V	A	V_{DD}=2.5V, I_{ABE}<2mA
9.8.24	Maximum current (short circuit limited current)4)	I_{ABE_max}	15	–	–	mA	C	
9.8.25	ABE passive output high voltage	V_{ABE_OUTH}	V_{DD}–1.5	V_{DD}	–	V	A	no load

Table 20 Power Supply, POR, V_{DD} Monitoring, ABE and RST

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Pin RST								
9.8.26	RST input low level	V_{RST_L}	-0.3	–	1	V	B	
9.8.27	RST input high level	V_{RST_H}	2	–	36	V	B	
9.8.28	RST input hysteresis	V_{RST_HYS}	0.1	–	0.5	V	C	
9.8.29	RST input current	I_{RST}	-120	–	20	µA	C	-0.2V<V_{RST}<V_{DD}
9.8.30	RST input current	I_{RST}	-10	–	1000	µA	C	V_{DD}<V_{RST}<36V
9.8.31	RST input current	I_{RST}	-400	–	–	µA	C	-0.3V<V_{RST}
9.8.32	RST pull-up current	I_{RST}	-50	–	-10	µA	A	0V<V_{RST}<V_{DD}–1.5V
9.8.33	Reset pulse width, RST requires min. low level pulse width	t_{RST}	0.5		3.5	µs	C	

1) Referred to GNDABE

2) In case of undervoltage of V_{DD}, specification is not fulfilled: e.g. proper operation of protection functions is not guaranteed (OUT= 1...14,17,18).

3) ABE as Output is not active

4) Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous or repetitive operation. Application must take care, that current into this pin does not exceed 15mA.

10 Device Logic Behavior

Table 21 Device Logic Behavior

	Registers				Output Stages			Others				
	DIAREG	CONREG	OUTREG	OUT1516	1...4, 11...14, 17, 18	5...10	15, 16	OUT1516 delay timer	MSC timeout counter	ABE output	DELAYOUT output	SDO output
MSC Communication												
Dataframe	–	–	data entry	–	ON/OFF depending on OUTREG		–	–	restart	–	–	–
RD_CONFIG	–	read out	–	–	–		–	–	–	–	–	send data
RD_DATA	read out & reset	–	1)	1)	1)		1)	–	–	–	–	send data
WR_RST	reset 2)	–	1)	1)	1)		1)	–	–	–	–	–
WR_CONREGx	–	data entry	–	–	–		–	–	–	–	–	–
WR_OUT1516	–	–	–	data entry	–		ON/OFF depending on OUT1516 3)	restart 3)	–	–	–	–
MON_TEST	x	data entry	x	x	x		x	–	–	x	x	–
Input pins												
DIS5_10	data entry	–	–	–	–	disable	–	–	–	–	–	–
lower thresholds of DELAYIN4)	data entry	–	–	–	–		–	–	–	–	pulled low	–
higher thresholds of DELAYIN5)	data entry	–	–	reset	–		reset	–	–	–	–	–
RST	reset	reset	reset	reset 6)	disable 7)		disable 6)	–	restart	pulled low	pulled low	disable 8)
ABE_STATUS	data entry	–	reset	reset 6)	disable 7)		disable 6)	–	–	–	–	–
Internally detected error cases												
STATUS_UV, STATUS_OV	data entry	–	reset	reset 6)	disable 7)		disable 6)	–	–	pulled low	pulled low	–
STATUS_SVBATT	data entry				disable		disable	–	–	–	–	–
POR	reset	reset	reset	reset	disable			restart	restart 9)	pulled low	pulled low	disable 8)
SCB	data entry	–	–	–	disable (defined in CONREGx and OUT1516)			–	–	–	–	–
OL	data entry	–	–	–	–		–	–	–	–	–	–
SCG	data entry	–	–	–	–		–	–	–	–	–	–

Table 21 Device Logic Behavior

	Registers				Output Stages		Others				
OTW	data entry	–	–	–	–	–	–	–	–	–	–
OTSD	10)	–	–	–	disable	disable	–	–	–	–	–
REVCUR_FLAG	data entry	–	–	–	–	–	–	–	–	–	–
Timeout counter expired											
MSC timeout counter	data entry	–	reset	reset 6)	disable 7)	disable 6)	–	expired	–	–	–
OUT1516 delay timer	–	–	–	reset 11)	–	disable 6)11)	expired	–	–	–	–

1) Outputs which have been switched off by SCB are switched on until SCB is detected again
2) Only DIAREG1...5 are reset, DIAREG6 and DIAREG7 remain unchanged
3) Switching on respectively restarting delay timer only in failure free condition
4) Thresholds $V_{DELAYIN_L}$ and $V_{DELAYIN_H}$
5) Thresholds $V_{DELAYIN_RES15_16_L}$ and $V_{DELAYIN_RES15_16_H}$
6) OUT1516 reset and stages are disabled after delay time (OUT15, OUT16 may be configured to long delay)
7) OUTREG reset and stages are disabled because control register is reset
8) communication stopped
9) before t_{MSC_mon} a data frame must be received, otherwise DIAREG6 must be read out to clear MSC_MON failure bit.
10) OTW still active in OTSD, no new diagnostic entry when changing from OTW to OTSD
11) Only if this timer has expired and failure occurs

Description:
– : no influence
x : influence possible, refer to corresponding chapter in this specification

11 Micro Second Channel MSC

Bidirectional micro second channel (MSC) is used for communication with micro controller.

Via MSC, the micro controller controls the outputs and logic of the stage device including the diagnosis and monitoring module. Diagnosis data is requested by micro controller via downstream and returned by the device via MSC upstream channel.

The MSC is a serial interface which is especially optimized to connect peripheral devices via serial link to micro controller. The serial communication link is built up by a fast synchronous downstream channel from micro controller to the stage device and an asynchronous upstream channel (referenced to downstream clock). The downstream interface can be “low voltage differential” (FCLN, FCLP, SIN, SIP) or “single ended” (FCL, SI, SSY).

Multiple “power devices” with MSC on downstream are possible. Downstream device is selected by SSY.

The MSC logic is supplied with V_{DD} and referenced to PGND.

If supply voltage of the device is below V_{DD_THL}, downstream communication is possible with reduced FCL clock frequency only. Power on reset (V_{DD}<V_{DD_POR}) disables the MSC interface.

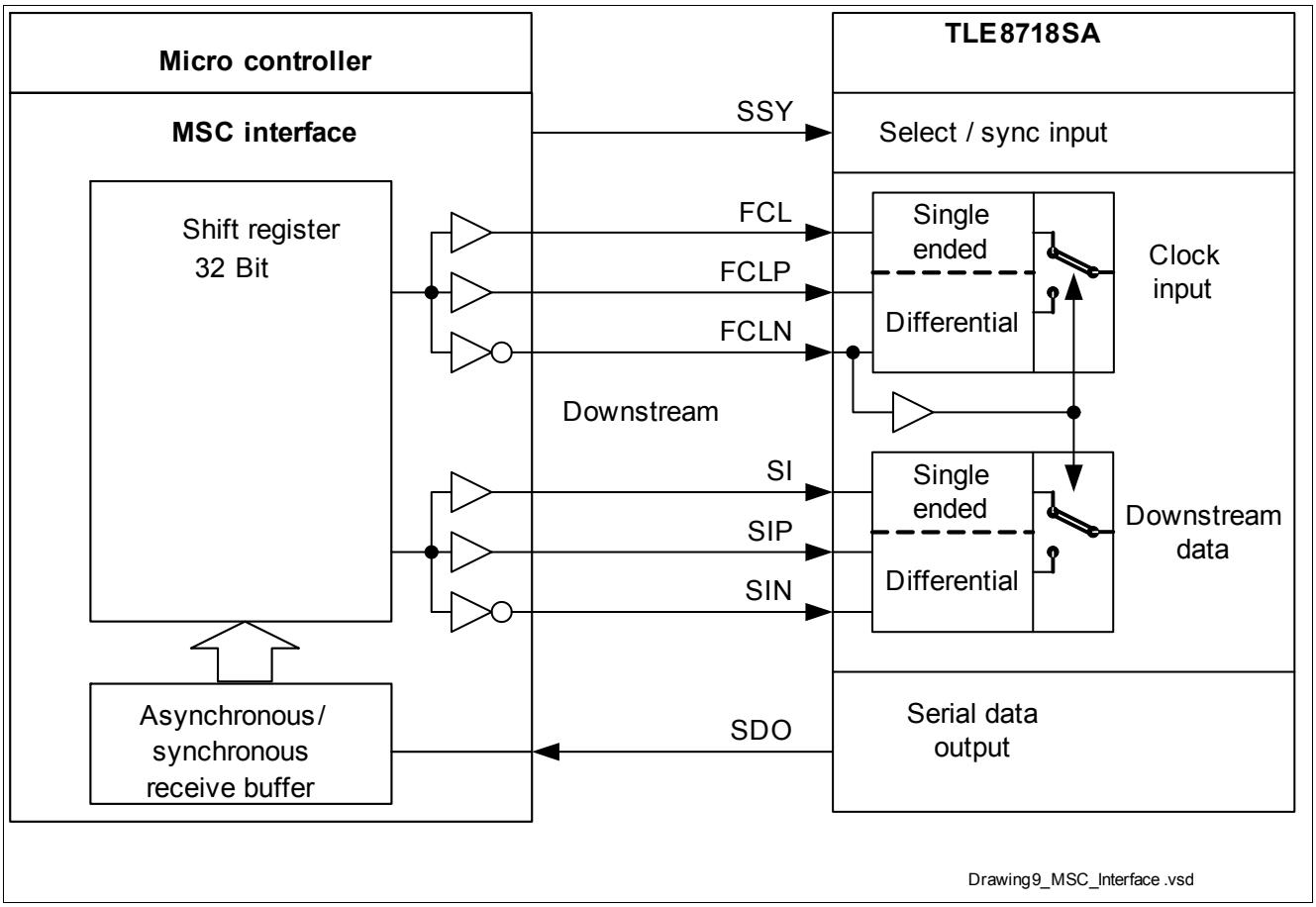


Figure 17 MSC Interface (not tested, overview only)

11.1 Downstream Communication

Downstream frames are synchronous serial frames with clock and data line.

The physical interface for downstream communication can be “low voltage differential” or “single ended” type. Both interface types are using individual pins (FCL and SI or FCLN, FCLP, SIN and SIP) and common pins (SSY and SO). To select the interface, FLCN has to be connected either to PGND (for single ended type) or to a voltage within the defined input voltage range (for low voltage differential type) (see **Item 11.5.7**). The unused pins are connected to PGND (FCLN, FCLP, FCL, SIP, SIN) or to VDD (SI).

Differential inputs for downstream data are SIP and SIN; the differential input signal SIP – SIN is the same logical signal as SI. The clock pins are FCLP and FCLN, the differential clock FCLP – FCLN is the same logical signal as FCL.

There is one input for select/sync at SSY, and one output for upstream data at SDO. The stage device is always the slave in this communication link.

The SSY signal enables receiver circuits automatically during a downstream frame transmission.

Two types of downstream frames are defined:

- Command frames (selection bit =“1”)
- Data frames (selection bit =“0”)

The device MSC uses non inverting polarity for SI and FCL: SI changes its state with the rising edge of FCL and is sampled with the falling edge; a logic ‘1’ is a ‘high level’ on SI, and a logic ‘0’ is a ‘low level’ on SI. Data at SI is latched by device on the falling edge of FCL.

The SSY input is active low during the active phases of command or data frames. An active enable signal validates the SI input signal. Outside the active phase (SSY line is at high level) data at SI is ignored.

By this way it is possible to drive multiple “power devices” with shared FCL and SI lines and individual SSY signal.

Command frames and data frames may be sent in any sequence (with a passive phase of at least 2 FCL-cycles after each frame).

Table 22 Execution of commands

Event on MSC downstream	upstream busy	upstream idle
valid read command frame	ignored	executed
valid write command frame	executed	executed
valid data frame	accepted	accepted
invalid command frame	ignored	ignored
invalid data frame	ignored	ignored

The serial clock FCL is active (toggling) continuously (“FCL continuous mode”) even when no command frame or data frame is transmitted. It is used to generate the upstream clock.

The clock period of FCL is defined as t_{FCL}, maximum downstream clock rate is f_{FCLmax}.

The active phase of a downstream frame starts with the falling edge of the signal on SSY and ends with the rising edge. SSY changes its state with the rising edge of clock FCL.

After a power-on-reset or RST returns to logical high level for device normal operation, the MSC interface is fully functional after a maximum of 8 clock pulses on FCL respectively FCLP and FCLN.

11.1.1 Voltage Level Diagrams of low voltage differential pins

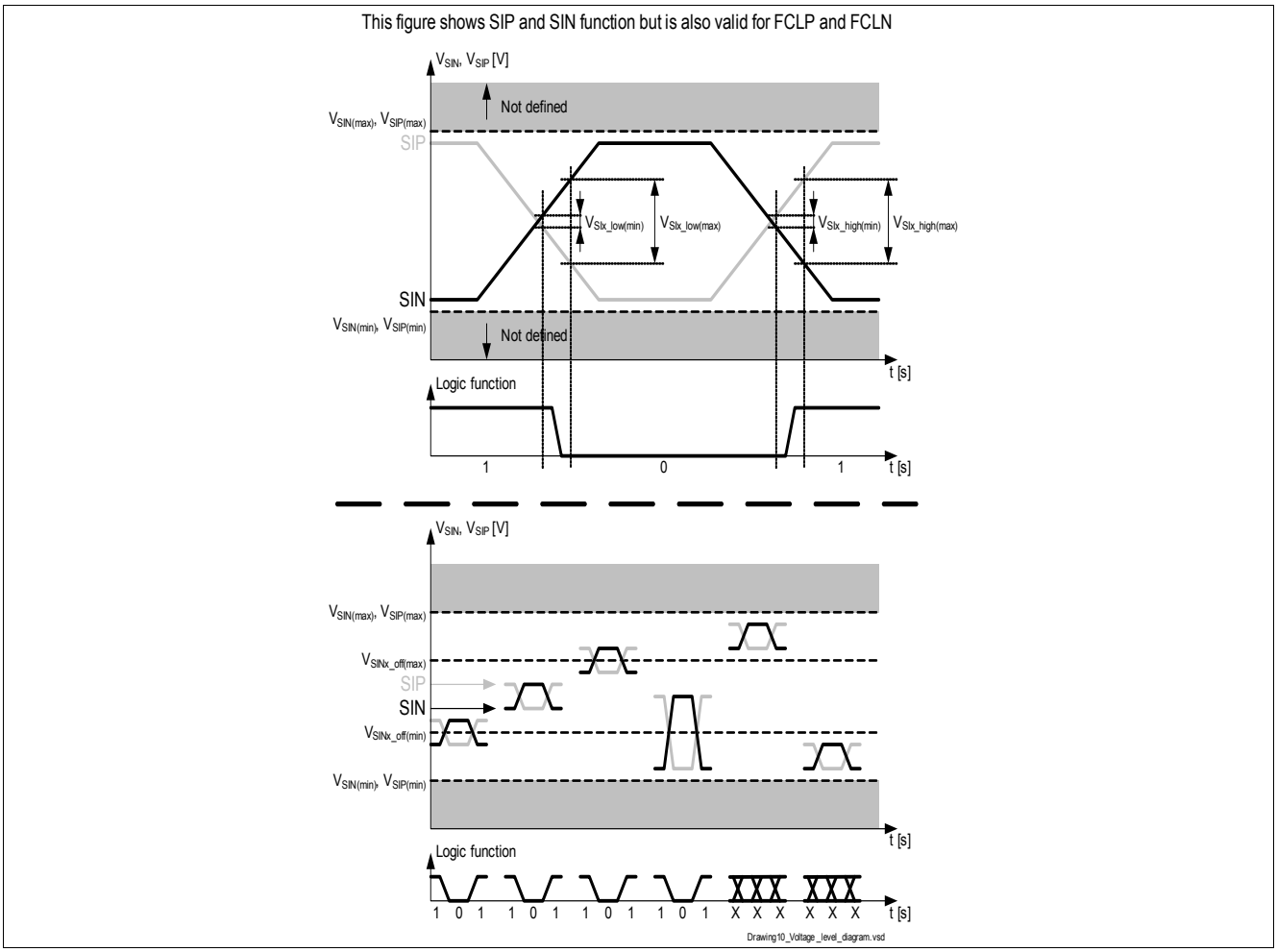


Figure 18 Voltage level diagram

11.1.2 Downstream Supervisory Functions

A command- or data frame is interpreted as valid, if it has the correct number of clock pulses (a frame has a length of 17 clock pulses). Clock pulses are counted at the falling edge of the signal.

There is no parity check.

If device receives no valid data frame for t > t_{MSC_mon}, the device will switch off the output stages (exception: OUT15 or OUT16 if configured to delayed reset behavior and set the bit MSC_MON in DIAREG6 to ‘0’.

11.1.3 Command Frame

A command frame always starts with a high level bit (command selection bit). The number of bits of the active phase of a command frame NCB is fixed to 17. A command is executed only if the number of the command bits is equal to NCB = 17.

The length of the command frame’s passive phase t_{CPP} must be a minimum of 2 * t_{FCL} (2 clock pulses).

Alternatively the passive phase can consist in t_{CPP} = t_{FCL} (1 clock pulse) followed by a frame of wrong length (4...8 bits, with or without SSY active low) and a second t_{CPP} = t_{FCL} (1 clock pulse).

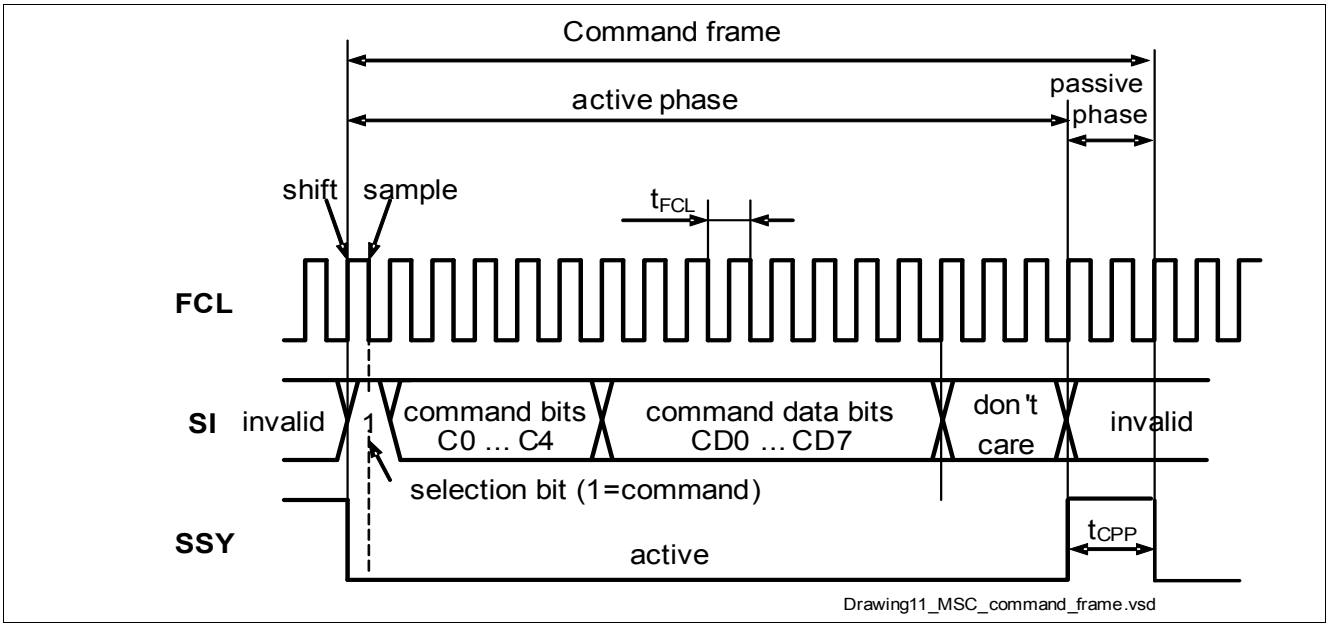


Figure 19 MSC command frame

Content of a command frame (LSB transmitted first)

Table 23 Command frame

Bit #	Description
0 (first bit)	= '1': command selection bit
1...5	Command [C0...C4]
6...13	Data for the command [CD0...CD7]
14...16	don't care 3 bits

The least significant (LSB) bit of a command is transmitted first.

11.1.4 Data Frame

A data frame always starts with a low level bit (data selection bit). The number of the bits of the active phase of a data frame NDB is fixed to 17 bit.

A data frame is accepted if the actual length is the expected length NDB.

MSC Monitoring t_{MSC_mon} is re-triggered by any data frame with correct length (no other error detection mechanism is implemented).

The length of the data frame's passive phase t_{DPP} must be a minimum of 2 * t_{FCL} (2 clock pulses).

Alternatively the passive phase can consist in t_{DPP} = t_{FCL} (1 clock pulse) followed by a frame of wrong length (4...8 bits, with or without SSY active low) and a second t_{DPP} = t_{FCL} (1 clock pulse).

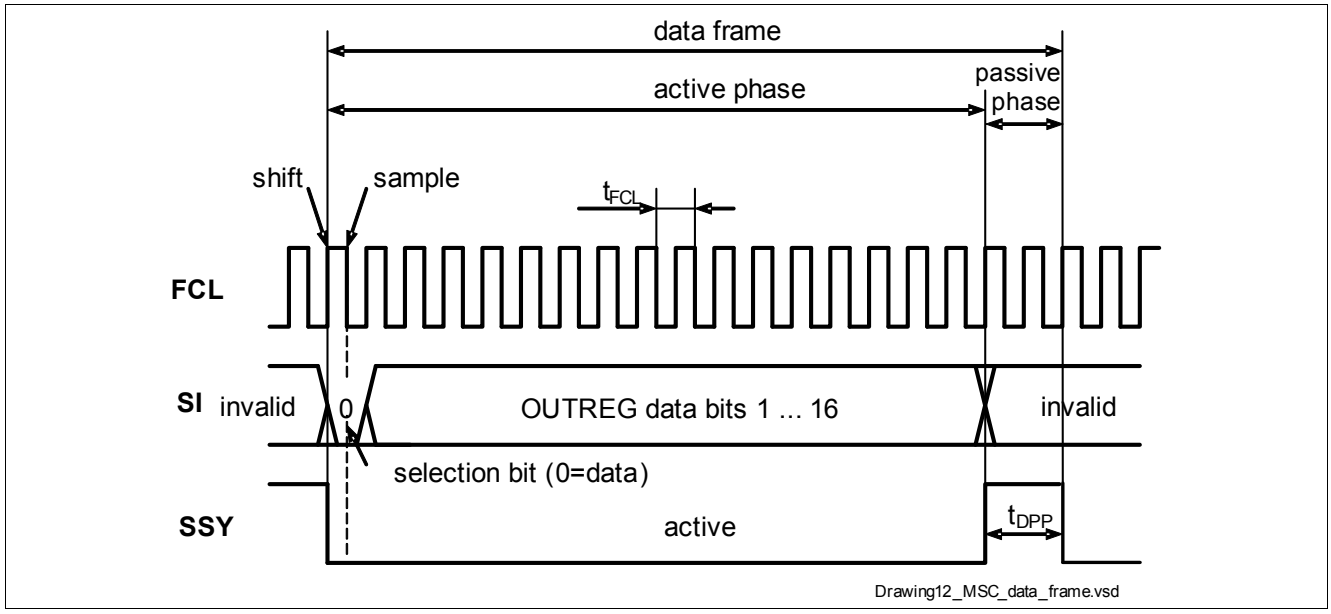


Figure 20 MSC data frame

There is no parity bit in the data frame.

Table 24 Data frame

OUTREG Bit	Description
0 (first bit)	= '0': data selection bit (R-A 1.5.3)
1	OUT1 stage data[1)]
2	OUT3 stage data[1)]
3	OUT5 stage data[1)]
4	OUT7 stage data[1)]
5	OUT9 stage data[1)]
6	OUT11 stage data[1)]
7	OUT13 stage data[1)]
8	OUT17 stage data[1)]
9	OUT2 stage data[1)]
10	OUT4 stage data[1)]
11	OUT6 stage data[1)]
12	OUT8 stage data[1)]
13	OUT10 stage data[1)]
14	OUT12 stage data[1)]
15	OUT14 stage data[1)]
16	OUT18 stage data[1)]

1) The control bit is non inverting, i.e. if a control bit is '1' the corresponding stage is off.

The stages OUT15 and OUT16 are accessed by command frame (WR_OUT1516) due to their optional special functions (delayed reset behavior on ABE, RST, ...).

The data is stored in register OUTREG.

11.2 Upstream Communication

The serial data output [SDO] is the synchronous serial data signal of the upstream channel.

The polarity for [SDO] is ‘non inverting polarity‘– i.e. a low level bit at [SDO] is stored in the micro controller as a logic ‘0‘, and a high level bit at [SDO] is stored in the micro controller as a logic ‘1‘.

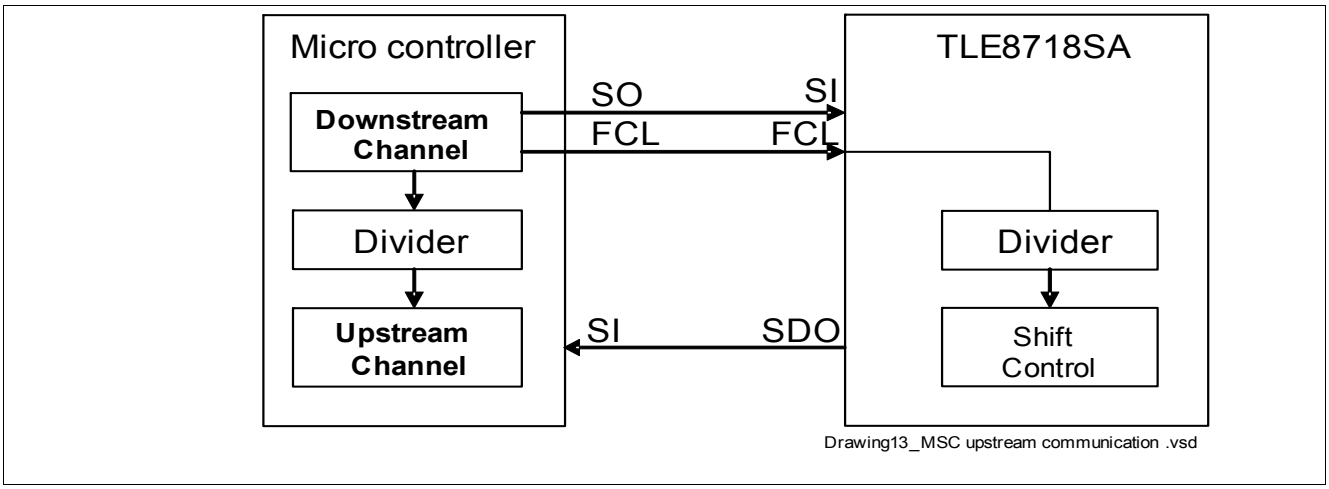


Figure 21 MSC upstream communication (not tested, overview only, Single Ended)

The serial data output (SDO) is single-ended.

The frequency for SDO is derived from FCL (or FCLN/FCLP) by an internal divider and can be configured via MSC.

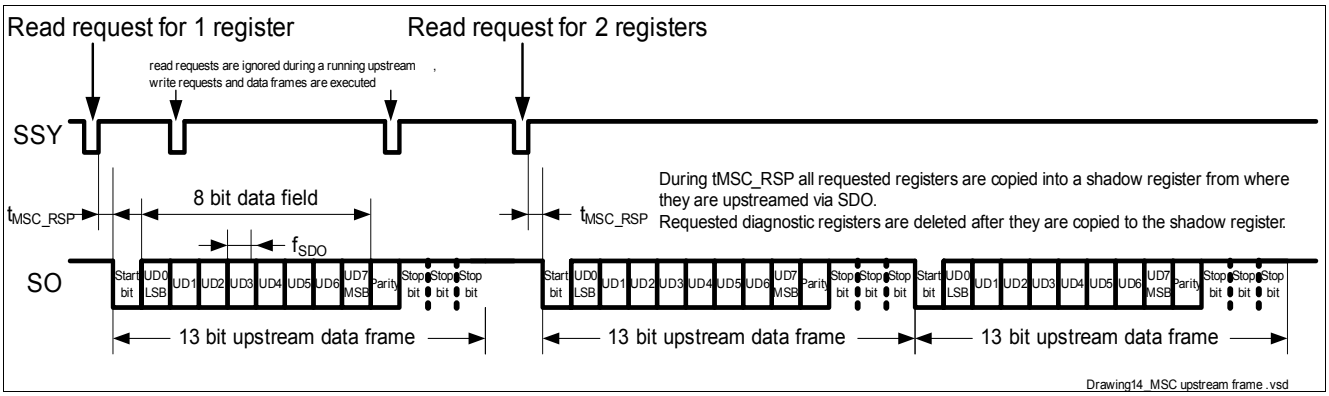


Figure 22 MSC upstream frame

Table 25 Upstream frame

Bit	description
0	start bit, always ‘0’
1-8	upstream data bits UD0...7
9	parity bit (The parity bit is set in order to achieve an even number of ‘1’ in Bits UD0...7+Parity)
10, 11, 12	stop bits, always ‘1’

Transmission of the registers via upstream starts within t_{MSC_RSP} after read command has been received. If a read command is received the device will ignore further read commands until the upstream data transfer is finished. A new read command is accepted if the rising edge SSY arrives after the last stop bit has been sent. Write commands or data frames are executed independently of ongoing read requests. If the write command is changing the register which is in transmission, the old register content will be sent (see **Figure 22**).

11.3 Timing Characteristics

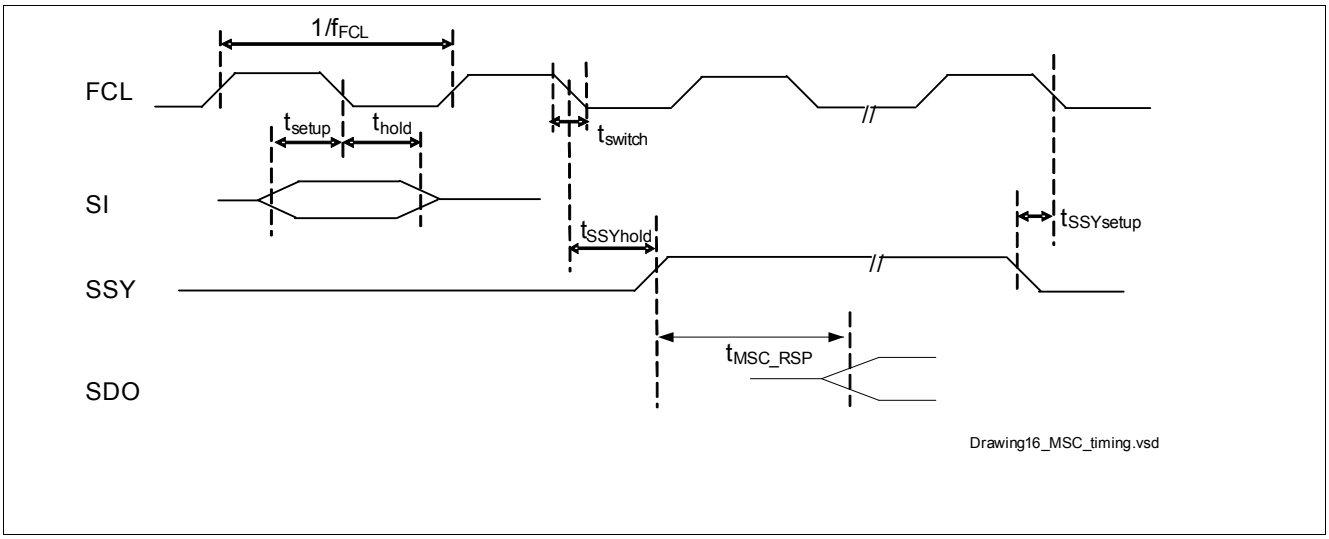


Figure 23 MSC timing

The downstream clock within the device is always running; each upstream data frame (i.e. each answer to a READ command) is synchronized with this clock.

The upstream response time t_{MSC_RSP} describes the time between end of read command (rising edge of SSY) to beginning of up-stream communication (falling edge of start bit).

11.4 Internal Clock Signal

The MSC interface is synchronously clocked by the external MSC clock signal (FCL or FCLN/FCLP). If this clock signal is missing the communication is halted.

All other functions of the circuit are available independently of an external MSC clock signal FCL or FCLN/FCLP.

The internal clock source is used for:

- Diagnosis filtering
- Self protection
- Reset extension
- MSC data stream supervisory
- Delayed reset behavior of OUT15 and OUT16
- Delayed disabling inputs (DIS5_10, DELAYIN)

The internal clock signal is generated independently from MSC clock (FCL or FCLN/FCLP).

The internal oscillator is functional in undervoltage V_{DD_THL} above V_{DD_POR}. By this way it is guaranteed that in undervoltage condition or during micro controller reset the diagnostic filters (e.g. stage shut off on SCB) and the delayed reset of OUT15 and OUT16 are functional.

11.5 Electrical Characteristics

Table 26 Micro Second Channel

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Internal Clock								
11.5.1	Frequency of internal clock	f_{INT}	0.7	–	1.1	MHz	C	-
Pin SSY								
11.5.2	Input comparator low level	V_{SSY_low}	-0.3	–	0.8	V	B	–
11.5.3	Input comparator high level	V_{SSY_high}	1.6	–	36	V	B	–
11.5.4	Input comparator hysteresis	V_{SSY_hys}	0.1	–	0.5	V	C	–
11.5.5	Input capacitance	C_{SSY}	–	–	10	pF	C	–
11.5.6	Input current Internal pull up current source to V_{DD}	I_{SSY}	-100	–	-10	µA	A	0V<V_{SSY}<2V
Pins FCLP, FCLN								
11.5.7	Input voltage range	V_{FCLP}, V_{FCLN}	0.8	–	1.6	V	C	–
11.5.8	Differential input high detection level, V_{FCLx_high}=V_{FCLP}–V_{FCLN}	V_{FCLx_high}	25	–	125	mV	C	–
11.5.9	Differential input low detection level, V_{FCLx_low}=V_{FCLP}–V_{FCLN}	V_{FCLx_low}	-125	–	-25	mV	C	–
11.5.10	Input voltage offset, V_{FCLx_off}=0.5*(V_{FCLP}+V_{FCLN})	V_{FCLx_off}	1.05	–	1.4	V	C	–
11.5.11	Differential capacitance between; FCLP and FCLN	C_{FCLx}	–	–	8	pF	C	–
11.5.12	FCLP Input pull up current; FCLP: internal pull up current source;	I_{FCLP}	-25	–	-3	µA	A	0V<V_{FCLP}<2V
11.5.13	FCLN Input pull down current; FCLN: internal pull down current source	I_{FCLN}	6	–	50	µA	A	1V<V_{FCLN}<V_{DD}
Single ended/Differential selection								
11.5.14	FCLN low level for MSC “single ended selection”	$V_{FCLN_sel_low}$	-0.3	–	0.4	V	B	–
11.5.15	FCLN high level for MSC “low voltage differential selection”	$V_{FCLN_sel_high}$	0.8	–	36	V	B	–
Pin FCL								
11.5.16	FCL input low voltage	V_{FCL_low}	-0.3	–	0.8	V	B	–
11.5.17	FCL input high voltage	V_{FCL_high}	1.6	–	36	V	B	–
11.5.18	FCL input hysteresis	V_{FCL_hys}	0.1	–	0.5	V	C	–
11.5.19	FCL Input current. Internal pull down current source to PGND;	I_{FCL}	10	–	100	µA	A	1V<V_{FCL}<V_{DD}
Clock Frequency								
11.5.20	FCLP, FCLN frequency	f_{FCLx}	4	–	23	MHz	B	V_{DD_POR}<V_{DD}< 5.5V

Table 26 Micro Second Channel

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
11.5.21	FCL frequency	f_{FCL}	4	–	12.5	MHz	B	V_{DD_POR}<V_{DD}< 5.5V
Pins SIP, SIN								
11.5.22	Input voltage range	V_{SIP}, V_{SIN}	0.8	–	1.6	V	C	–
11.5.23	Differential input high detection level, V_{SIx_high}=V_{SIP}–V_{NSI}	V_{SIx_high}	25	–	125	mV	C	–
11.5.24	Differential input low detection level, V_{SIx_low}=V_{SIP}–V_{SIN}	V_{SIx_low}	-125	–	-25	mV	C	–
11.5.25	Input voltage offset, V_{SIx_Off}=0.5*(V_{SIP}+V_{SIN})	V_{SIx_Off}	1.05	–	1.4	V	C	–
11.5.26	Differential capacitance between SIP and SIN	C_{SIx}	–	–	8	pF	C	–
11.5.27	Input pull up current; SIP: internal pull up current source	I_{SIP}	-25	–	-3	µA	A	0V<V_{SIP}<2V
11.5.28	Input pull down current; SIN: internal pull down current source to PGND	I_{SIN}	6	–	50	µA	A	1V<V_{SIN}<V_{DD}
Pin SI								
11.5.29	SI input low voltage	V_{SI_low}	-0.3	–	0.8	V	B	–
11.5.30	SI input high voltage	V_{SI_high}	1.6	–	36	V	B	–
11.5.31	SI input hysteresis	V_{SI_hys}	0.1	–	0.5	V	C	–
11.5.32	SI Input current; Internal pull up current source to V_{DD}	I_{SI}	-100	–	-10	µA	A	0V<V_{SI}<2V
Pin SDO								
11.5.33	SDO output low level	$V_{SDO_low;}$	–	–	0.8	V	C	I_{SDO}<4mA;
		V_{SDO_low}	–	–	0.4	V	A	I_{SDO}<1mA
11.5.34	SDO passive output high voltage	V_{SDO_high}	V_{DD} – 1.5	V_{DD}	–	V	C	no load
11.5.35	Maximum current (short circuit limited current)[1]	I_{SDO_max}	15	–	–	mA	C	–
11.5.36	SDO pull-up current source	I_{SDO_high}	-50	–	-10	µA	A	0V<V_{SDO}<2V, [2]
11.5.37	SDO (high level = inactive) pin capacity	C_{SDO}	–	–	10	pF	C	measured with bias voltage of 1V
11.5.38	SDO frequency; maximum upstream frequency with external pull-up	f_{SDO}	550	–	–	kHz	C	1kΩ and C_L=50pF

Table 26 Micro Second Channel

4.5V < V_{DD} < 5.5V, 4.5V < V_{BAT} < 40V, all voltages with respect to PGND, positive current flowing into pin., T_j = -40°C to +150°C, unless otherwise specified

Pos.	Parameter	Symbol	Values			Unit	TC	Conditions
			min.	typ.	max.			
Timing Characteristics [3]								
11.5.39	Data hold time	t_{hold}	10	–	–	ns	C	–
11.5.40	Data Setup time	t_{setup}	10	–	–	ns	C	–
11.5.41	Switching time	t_{switch}	–	–	3	ns	C	–
11.5.42	FCL low time	t_{FCLlow}	13	–	–	ns	C	–
11.5.43	FCL high time	$t_{FCLhigh}$	13	–	–	ns	C	–
11.5.44	SSY setup time	$t_{SSYsetup}$	5	–	–	ns	C	–
11.5.45	SSY hold time	$t_{SSYhold}$	17	–	–	ns	C	–
11.5.46	MSC data timeout monitoring	t_{MSC_mon}	60	–	135	µs	B	–
11.5.47	MSC upstream response time; up-stream divider independent (CONREG4_FCL_CONFx)	t_{MSC_RSP}	–	–	100	µs	C	f_{FCL} or f_{FCLx}=4MHz
11.5.48	Required idle time after command	t_{CPP}	$2/f_{FCL}$ (2 clock pulses)	–	–	s	C	–
11.5.49	Required idle time after data frame	t_{DPP}	$2/f_{FCL}$ (2 clock pulses)	–	–	s	C	–

1) Integrated protection functions are designed to prevent IC destruction under fault conditions. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous or repetitive operation. Application must take care, that current into this pin does not exceed 15mA.

2) SDO as Output is not active

3) See **Figure 19**, **Figure 20** and **Figure 23**.

12 Control of the device

12.1 Commands

Table 27 Command Overview

Command	SB	C0...4	CD0...7	DC	Description
–	1	00000	xxxx xxxx	xxx	Invalid command
WR_CONREG1	1	10000	CD0...7	xxx	Configuration of switch off or current control by SCB for OUT1...8
WR_CONREG2	1	01000	CD0...7	xxx	Configuration of switch off or current control by SCB for OUT9...14, 17, 18
–	1	11000	xxxx xxxx	xxx	Invalid command
WR_CONREG3	1	00100	CD0...7	xxx	Configuration of diagnostic pull-down current and Open Load OL of OUT11...14, 17, 18, DELAYIN_FIL and EXT_SCB
–	1	10100	xxxx xxxx	xxx	Invalid command
–	1	01100	xxxx xxxx	xxx	Invalid command
WR_OUT1516	1	11100	CD0...7	xxx	Configuration of OUT 15, 16, switch off or current control by SCB for OUT15, 16, configuration of diagnostic pull-down current and Open Load OL. Special behavior (time delay)
WR_RST	1	00010	xxxx xxxx	xxx	Soft reset via MSC (clear diagnostic registers)
–	1	10010	xxxx xxxx	xxx	Invalid command
–	1	01010	xxxx xxxx	xxx	Invalid command
WR_START	1	11010	xxxx xxxx	xxx	Enable OUT1...14, OUT17 and OUT18
–	1	00110	xxxx xxxx	xxx	Invalid command
WR_CONREG4	1	10110	CD0...7	xxx	Configuration of DELAYIN delay, upstream frequency divider and V_{DD} monitoring
WR_TESTREG	1	01110	CD0...7	xxx	For factory tests only. Do not use this command.
–	1	11110	xxxx xxxx	xxx	Invalid command
RD_CONFIG	1	00001	CD0...7	xxx	Request content of configuration registers CONREG1...4, OUT1516, TESTREG
–	1	10001	xxxx xxxx	xxx	Invalid command
–	1	01001	xxxx xxxx	xxx	Invalid command
RD_DATA	1	11001	CD0...7	xxx	Request content of diagnostic registers DIAREG1...7 and IDENTREG
–	1	00101	xxxx xxxx	xxx	Invalid command
–	1	10101	xxxx xxxx	xxx	Invalid command
–	1	01101	xxxx xxxx	xxx	Invalid command
–	1	11101	xxxx xxxx	xxx	Invalid command
–	1	00011	xxxx xxxx	xxx	Invalid command
–	1	10011	xxxx xxxx	xxx	Invalid command
WR_FUSE_SC	1	01011	CD0...7	xxx	Active during factory test mode only. For factory tests only. Do not use this command.
–	1	11011	xxxx xxxx	xxx	Invalid command

Table 27 Command Overview

Command	SB	C0...4	CD0...7	DC	Description
WR_SEL_THRES	1	00111	CD0...7	xxx	Active during factory test mode only. For factory tests only. Do not use this command.
–	1	10111	xxxx xxxx	xxx	Invalid command
–	1	01111	xxxx xxxx	xxx	Invalid command
–	1	11111	xxxx xxxx	xxx	Invalid command

12.1.1 WR_OUT1516

Table 28 Command WR_OUT1516

SB	C	CD0	CD1	CD2	CD3	CD4	CD5	CD6	CD7	DC
1	11100	OUT15_CONTROL	OUT15_DELAY	OUT15_DIAC	OUT15_SCB	OUT16_CONTROL	OUT16_DELAY	OUT16_DIAC	OUT16_SCB	xxx

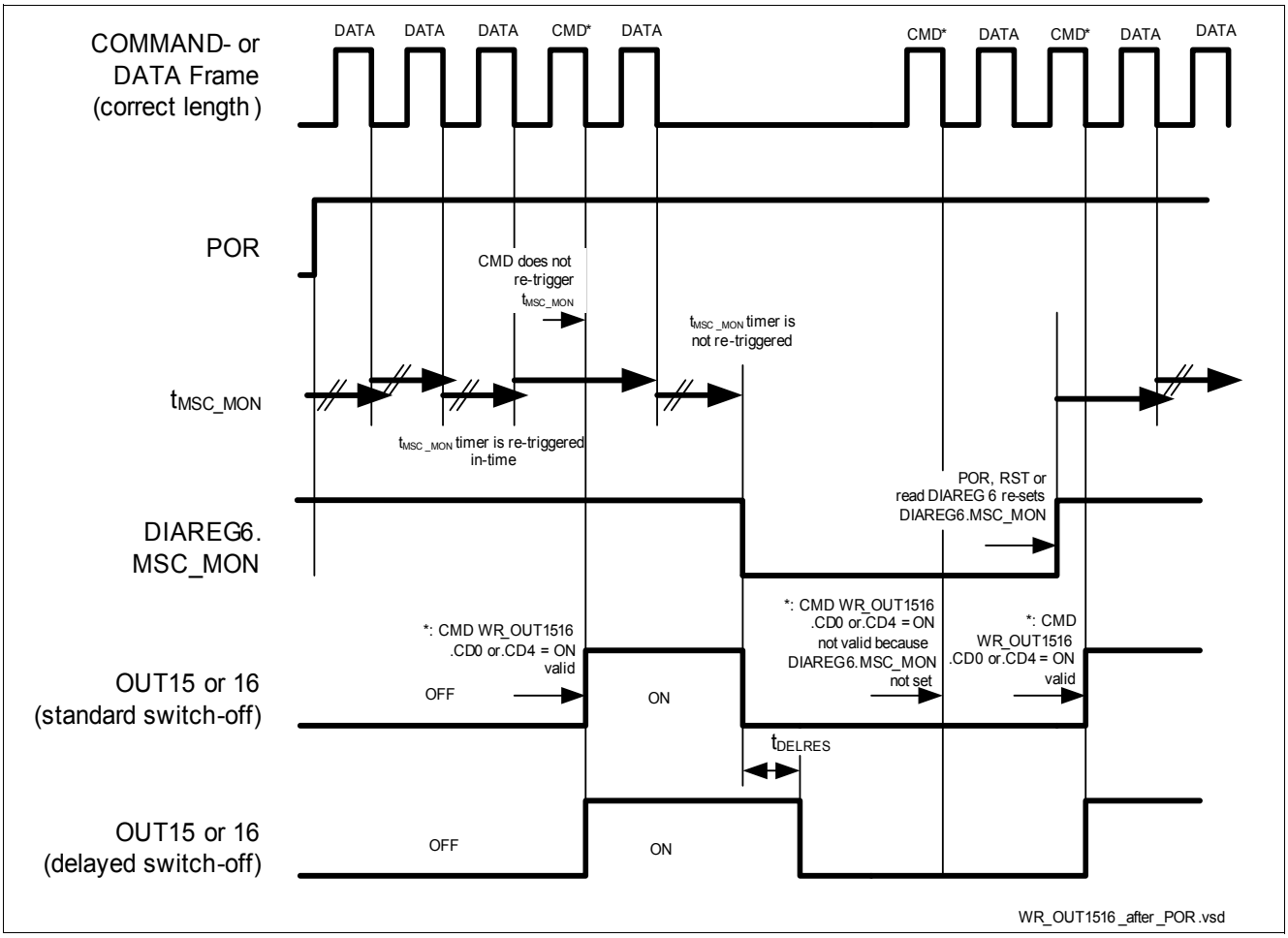


Figure 24 OUT1516 after Power ON (POR) and in dependency of t_{MSC_MON}

The MSC timeout counter is started from its initial state when POR and RST are released. The diagnosis flag DIAREG6.MSC_MON is initially set to '1'. Every valid data frame resets and restarts the MSC timeout counter as long as it has not expired. Hence data frames should be sent in intervals shorter than t_{MSC_mon}.

If no valid data frame is received within t_{MSC_mon}, the MSC timeout counter will expire, clear the DIAREG6.MSC_MON flag and switch off the output stages. An exception may be OUT15/16 which are switched off after t_{DELRES} if they are configured to delayed reset behavior. All other functions are not influenced by the MSC timeout, e.g. MSC upstream data transfer is not halted.

Once the MSC timeout counter has expired a data frame will neither restart the timeout counter nor set the diagnosis flag nor turn on any output. In order to enable the output stages again after an MSC timeout the following steps are necessary:

1) DIAREG6 must be read to set the DIAREG6.MSC_MON bit and restart the MSC timeout counter.

2) Subsequent data frames or WR_OUT1516 commands are needed to switch on the outputs again.

Command frames other than RD_DATA for DIAREG6 will neither influence the MSC timeout counter nor the DIAREG6.MSC_MON flag.

The WR_OUT1516 output is a 'high'-strobe after the command has been received. (See **Figure 1**)

The t_{DELRES} time-out counter generates a 'low' pulse of t_{DELRES} after the 'Restart' input has been activated by 'high' pulse. A 'high' pulse on input 'Discard' makes the timer expire without waiting for t_{DELRES}, the output then is 'high'-level (failure will reset OUTn control register).

The inputs of the OUTn-control flip-flop are active high and 'R' is dominant, output is non inverting.

OUT15 and OUT16 can be configured individually to delayed reset, only one timer (t_{DELRES}) is needed as both outputs are accessed in the same command frame and no independent restart is possible.

The functions are:

- switch OFF
- switch ON, no delay
- switch ON, restart timeout counter for delayed reset behavior
- keep state, restart timeout counter for delayed reset behavior

12.1.2 WR_RST

Table 29 Command WR_RST

SB	C0...4	CD0...7	DC
1	00010	xxxx xxxx	xxx

The command triggers a soft reset via MSC. Diagnostic registers are cleared.

If WR_RST command arrives during an up-stream burst, then all diagnostic registers are cleared. The incoming frame is sent with the uncleared content of the DIAREG and the rest of the frames are send with the cleared content.

12.1.3 WR_START

Table 30 Command WR_START

SB	C0...4	CD0...7	DC
1	11010	xxxx xxxx	xxx

The command clears the bit OUTPUT_STBY = ’0’. With OUTPUT_STBY =’1’ the output registers OUTREG of OUT1...14, 17, 18 are reset. Control of OUT15 and 16 is still possible by register OUT1516. The OUTPUT_STBY bit is set by power-on-reset or by active low signal on pin RST.

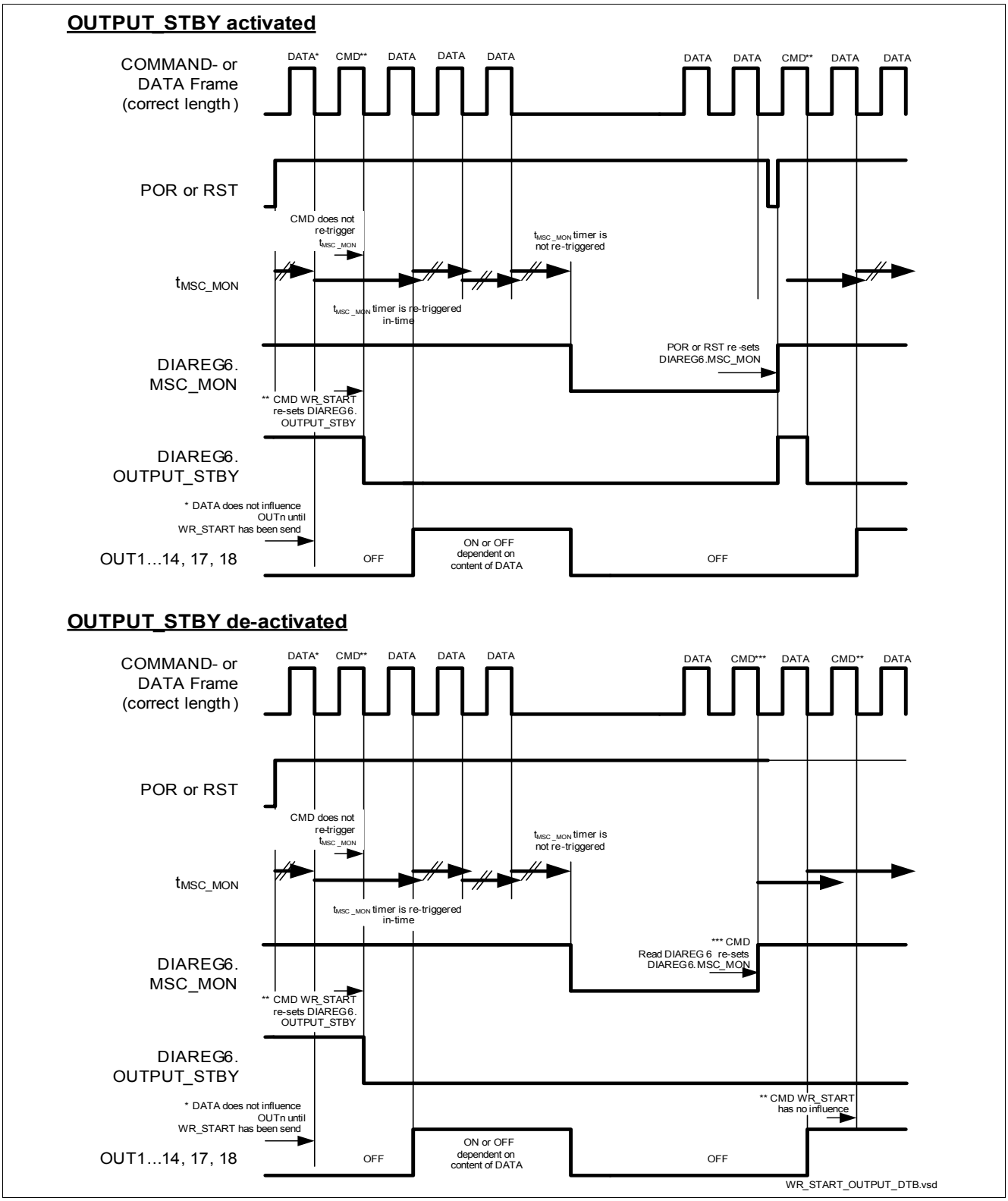


Figure 25 Impact of WR_START to OUTPUT_STBY

12.1.4 RD_CONFIG

Table 31 Command RD_CONFIG

Register	SB	C0...4	CD0...7	DC
CONREG1	1	00001	xxxx xxx1	xxx
CONREG2			xxxx xx1x	
CONREG3			xxxx x1xx	
CONREG4			xxxx 1xxx	
OUT1516			xxx1 xxxx	
not implemented			xx1x xxxx	
OUTREG_EVEN			x1xx xxxx	
OUTREG_ODD			1xxx xxxx	

The RD_CONFIG command requests the device to transmit configuration register content via MSC upstream. With the command data bit CD(0...7), it is masked which registers are to be transmitted.

If more than one register is requested the transmission is made from CD7 down to CD0 (upstream transmission of CONREG1 first, CONREG2 second and so on). The request for a not implemented register is ignored.

12.1.5 RD_DATA

Table 32 Command RD_DATA

Register	SB	C0...4	CD0...7	DC
DIAREG1	1	11001	xxxx xxx1	xxx
DIAREG2			xxxx xx1x	
DIAREG3			xxxx x1xx	
DIAREG4			xxxx 1xxx	
DIAREG5			xxx1 xxxx	
DIAREG6			xx1x xxxx	
DIAREG7			x1xx xxxx	
IDENTREG			1xxx xxxx	

The RD_DATA command requests the device to transmit diagnostic register content via MSC upstream. With the command data bit CD(0...7), it is masked which registers are to be transmitted.

If more than one register is requested the transmission is made from CD7 down to CD0 (upstream transmission of DIAREG1 first, IDENTREG last).

The Register which is sent on RD_DATA is deleted at the beginning of the transmission.

12.2 Registers

12.2.1 CONREG1

Table 33 CONREG1

Reset sources: RST, power-on-reset			
Controller read access: RD_CONFIG = ’1 00001xxxx xxx1 xxx’			
Controller write access: WR_CONREG1 = ’1 10000 CD0...CD7 xxx’			
UD/CD	**Name**	**Description**	**Reset value**
0	OUT1_SCB	‘1‘: OUTn is switched off in case of SCB ‘0‘: OUTn current limited mode in case of SCB	1
1	OUT2_SCB		1
2	OUT3_SCB		1
3	OUT4_SCB		1
4	OUT5_SCB		1
5	OUT6_SCB		1
6	OUT7_SCB		1
7	OUT8_SCB		1

12.2.2 CONREG2

Table 34 CONREG2

Reset sources: RST, power-on-reset			
Controller read access: RD_CONFIG = ’1 00001 xxxx xx1x xxx’			
Controller write access: WR_CONREG2 = ’1 01000 CD0...CD7 xxx’			
UD/CD	**Name**	**Description**	**Reset value**
0	OUT9_SCB	‘1‘: OUTn is switched off in case of SCB ‘0‘: OUTn current limited mode in case of SCB	1
1	OUT10_SCB		1
2	OUT11_SCB		1
3	OUT12_SCB		1
4	OUT13_SCB		1
5	OUT14_SCB		1
6	OUT17_SCB		1
7	OUT18_SCB		1

12.2.3 CONREG3

Table 35 CONREG3

Reset sources: RST, power-on-reset			
Controller read access: RD_CONFIG = ’1 00001 xxxx x1xx xxx’			
Controller write access: WR_CONREG3 = ’1 00100 CD0...CD7 xxx’			
UD/CD	**Name**	**Description**	**Reset value**
0	OUT11_DIAC	‘1‘: OUTn diagnostic pull-down current and Open Load OL on ‘0‘: OUTn diagnostic pull-down current and Open Load OL off	0
1	OUT12_DIAC		0
2	OUT13_DIAC		0
3	OUT14_DIAC		0
4	OUT17_DIAC		0
5	OUT18_DIAC		0
6	DELAYIN_FIL	‘1‘: Long filter time for $t_{DELAYIN_GLITCH_long}$ selected ‘0‘: Short filter time for $t_{DELAYIN_GLITCH_short}$ selected	1
7	EXT_SCB	‘1‘: Extended SCB behavior of OUT5...OUT14 active (I_{OUTn} and V_{OUTn} are taken into account) ‘0‘: Default SCB behavior (only I_{OUTn} is taken into account)	0

12.2.4 CONREG4

Table 36 CONREG4

Reset sources: RST, power-on-reset			
Controller read access: RD_CONFIG = ’1 00001 xxxx 1xxx xxx’			
Controller write access: WR_CONREG4 = ’1 10110 CD0...CD7 xxx’			
UD/CD	**Name**	**Description**	**Reset value**
0	DELAYIN_CONF0	See table below: configuration of DELAYIN delay	1
1	DELAYIN_CONF1	See table below: configuration of DELAYIN delay	1
2	FCL_CONF0	See table below: divider settings for upstream frequency	1
3	FCL_CONF1	See table below: divider settings for upstream frequency	0
4	ABE_IMPACT[1)]	1: ABE and VDD monitoring disables all Outputs with short delay 0: ABE and VDD monitoring disables all Outputs with long delay	1
5	MON_TEST	‘1‘: VDD monitoring test inactive ‘0‘: VDD monitoring test active	1
6	MON_THRES	‘1‘: Test undervoltage threshold ‘0‘: Test overvoltage threshold	1
7	MON_LATCH	‘1‘: Overvoltage failure will be latched. Normal operation after reset, POR or by setting this bit to ‘0’ ‘0‘: Device returns to normal operation after overvoltage	1

1)In case of undervoltage of V_{DD}, specification is not fulfilled: e.g. protection functions might not work. (OUT= 1...14,17,18)

Table 37 CONREG4, DELAYIN configuration

Configuration of $t_{DELAYIN_x}$ delay		
DELAYIN_CONF1	**DELAYIN_CONF0**	**Description**
1	1	Long delay $t_{DELAYIN_L}$, see **Item 7.0.16**
0	1	Medium long delay $t_{DELAYIN_ML}$, see **Item 7.0.17**
1	0	Medium short delay $t_{DELAYIN_MS}$, see **Item 7.0.18**
0	0	Short delay $t_{DELAYIN_S}$, see **Item 7.0.19**

Table 38 CONREG4, Upstream divider configuration[1)]

Configuration of upstream clock divider		
FCL_CONF1	**FCL_CONF0**	**Description**
1	0	Upstream clock is f_{FCL}/128
0	1	Upstream clock is f_{FCL}/64
0	0	Upstream clock is f_{FCL}/32
1	1	Upstream clock is f_{FCL}/16

1) Take care that **Item 11.5.38** f_{SDO} is not exceeded.

12.2.5 OUT1516

Table 39 OUT1516

Reset sources: RST, power-on-reset, ABE, over-/undervoltage, OUT1516 timeout [1)], MSC_MON, RES15_16			
Controller read access: RD_CONFIG = ’1 00001 xxx1 xxxx xxx’			
Controller write access: WR_ OUT1516 = ’1 11100 CD0...CD7 xxx’			
UD/CD	**Name**	**Description**	**Reset value**
0	OUT15_CONTROL	See table “Output stage switching” below	1[2)]
1	OUT15_DELAY	See table “Output stage switching” below	1[2)]
2	OUT15_DIAC	‘1‘:OUT15 diagnostic pull-down current and Open Load OL on ‘0‘:OUT15 diagnostic pull-down current and Open Load OL off	0
3	OUT15_ SCB	‘1‘: OUT15 is switched off in case of SCB ‘0‘: OUT15 current limited mode in case of SCB	1
4	OUT16_CONTROL	See table “Output stage switching” below	1[2)]
5	OUT16_DELAY	See table “Output stage switching” below	1[2)]
6	OUT16_DIAC	‘1‘:OUT16 diagnostic pull-down current and Open Load OL on ‘0‘:OUT16 diagnostic pull-down current and Open Load OL off	0
7	OUT16_ SCB	‘1‘: OUT16 is switched off in case of SCB ‘0‘: OUT16 current limited mode in case of SCB	1

1) Timeout t_{delres} only resets the register if another failure (RST, ABE, over-/undervoltage, MSC-timeout) is still present. POR and the filtered RES15_16 resets the register immediately.

2) After POR has occurred or RES15_16 is released OUT15, OUT16 starts in OFF- state. OUTn_DELAY, OUTn_CONTROL reset Values remain =’1’

Table 40 OUT1516, Delay configuration

Output stage switching		
OUTn_DELAY	**OUTn_CONTROL**	**Description**
1	1	keep state, restart timeout counter for delayed reset behavior
0	1	switch OFF
1	0	switch ON, restart timeout counter for delayed reset behavior
0	0	switch ON, no delay

12.2.6 OUTREG_EVEN

Table 41 OUTREG_EVEN

Reset sources: RST, power-on-reset, ABE, over-/undervoltage, MSC_MON, OUTPUT_STBY

Controller read access: RD_CONFIG = ’1 00001 x1xx xxxx xxx’

Controller write access: Data Frame = ’0 x UD0 x UD1 x UD2 x UD3 x UD4 x UD5 x UD6 x UD7’

UD	Name	Description	Reset value
0	OUT2	‘1‘: OUTREG of OUTn is set to “ON”[1)] ‘0‘: OUTREG of OUTn is set to “OFF”	0
1	OUT4		0
2	OUT6		0
3	OUT8		0
4	OUT10		0
5	OUT12		0
6	OUT14		0
7	OUT18		0

1) OUTREG_EVEN contains the inverted status of what is programmed via a data frame into OUTREG.

12.2.7 OUTREG_ODD

Table 42 OUTREG_ODD

Reset sources: RST, power-on-reset, ABE, over-/undervoltage, MSC_MON, OUTPUT_STBY

Controller read access: RD_CONFIG = ’1 00001 1xxx xxxx xxx’

Controller write access: Data Frame = ’0 UD0 x UD1 x UD2 x UD3 x UD4 x UD5 x UD6 x UD7 x’

UD	Name	Description	Reset value
0	OUT1	‘1‘: OUTREG of OUTn is set to “ON”[1)]‘0‘: OUTREG of OUTn is set to “OFF”	0
1	OUT3		0
2	OUT5		0
3	OUT7		0
4	OUT9		0
5	OUT11		0
6	OUT13		0
7	OUT17		0

1) OUTREG_ODD contains the inverted status of what is programmed via a data frame into OUTREG.

12.2.8 DIAREG1

Table 43 DIAREG1

Reset sources: RST, power-on-reset, WR_RST, RD_DATA = '1 11001 xxxx xxx1 xxx'			
Controller read access: RD_DATA = '1 11001 xxxx xxx1 xxx'			
Controller write access: -			
UD	**Name**	**Description**	**Reset value**
0	OUT1_DIA1	See **Table 44**	1
1	OUT1_DIA2		1
2	OUT2_DIA1		1
3	OUT2_DIA2		1
4	OUT3_DIA1		1
5	OUT3_DIA2		1
6	OUT4_DIA1		1
7	OUT4_DIA2		1

Table 44 Encoding of diagnosis information

Encoding of the diagnosis bits of the device		
OUTn_DIA2	**OUTn_DIA1**	**description**
1	1	Power stage ok
1	0	Short circuit to battery (SCB) or diagnostic overtemperature (DOT)
0	1	Open load (OL)[1)]
0	0	Short circuit to ground (SCG)

1) OL only available when OUTn_DIAC='1'

12.2.9 DIAREG2

Table 45 DIAREG2

Reset sources: RST, power-on-reset, WR_RST, RD_DATA = '1 11001 xxxx xx1x xxx'			
Controller read access: RD_DATA = '1 11001 xxxx xx1x xxx'			
Controller write access: -			
UD	**Name**	**Description**	**Reset value**
0	OUT5_DIA1	See **Table 44**	1
1	OUT5_DIA2		1
2	OUT6_DIA1		1
3	OUT6_DIA2		1
4	OUT7_DIA1		1
5	OUT7_DIA2		1
6	OUT8_DIA1		1
7	OUT8_DIA2		1

12.2.10 DIAREG3

Table 46 DIAREG3

Reset sources: RST, power-on-reset, WR_RST, RD_DATA = ’1 11001 xxxx x1xx xxx’			
Controller read access: RD_DATA = ’1 11001 xxxx x1xx xxx’			
Controller write access: -			
UD	**Name**	**Description**	**Reset value**
0	OUT9_DIA1	See **Table 44**	1
1	OUT9_DIA2		1
2	OUT10_ DIA1		1
3	OUT10_ DIA2		1
4	OUT11_ DIA1		1
5	OUT11_ DIA2		1
6	OUT12_ DIA1		1
7	OUT12_ DIA2		1

12.2.11 DIAREG4

Table 47 DIAREG4

Reset sources: RST, power-on-reset, WR_RST, RD_DATA = ’1 11001 xxxx 1xxx xxx’			
Controller read access: RD_DATA = ’1 11001 xxxx 1xxx xxx’			
Controller write access: -			
UD	**Name**	**Description**	**Reset value**
0	OUT13_DIA1	See **Table 44**	1
1	OUT13_DIA2		1
2	OUT14_DIA1		1
3	OUT14_DIA2		1
4	OUT15_DIA1		1
5	OUT15_DIA2		1
6	OUT16_DIA1		1
7	OUT16_DIA2		1

12.2.12 DIAREG5

Table 48 DIAREG5

Reset sources: RST, power-on-reset, WR_RST, RD_DATA = ’1 11001 xxx1 xxxx xxx’			
Controller read access: RD_DATA = ’1 11001 xxx1 xxxx xxx’			
Controller write access: -			
UD	**Name**	**Description**	**Reset value**
0	OUT17_DIA1	See **Table 44**	1
1	OUT17_DIA2		1
2	OUT18_DIA1		1
3	OUT18_DIA2		1
4	REVCUR_FLAG	‘1‘:Common Reverse Current Flag OUT1...18, no reverse current ‘0‘:Common Reverse Current Flag OUT1...18, Reverse current any stage for longer than t_{REVCUR}	1
5	OUT15_STATUS	‘0‘: OUT15 is ON[1)] ‘1‘: OUT15 is OFF	0[2)]
6	OUT16_STATUS	‘0‘: OUT16 is ON[1)] ‘1‘: OUT16 is OFF	0[2)]
7	RES15_16_STATUS	‘0‘: DELAYIN > $V_{RES15_16_H}$ for longer than $t_{DELAYIN_GLITCH_x}$ ‘1‘: DELAYIN < $V_{RES15_16_L}$	1[2)]

1) ’1’=OFF: Channel is currently either in OFF-state (State A, C or D, see **Figure 12**), during falling edge or in clamping
‘0‘=ON: Channel is currently either in ON-state (State B, see **Figure 12**), during rising edge or in current limitation.

2) Register data is asynchronously written and not latched by the device (status).

12.2.13 DIAREG6

Table 49 DIAREG6

Reset sources: RST, power-on-reset			
Controller read access: RD_DATA = ’1 11001 xx1x xxxx xxx’			
Controller write access: -			
UD	**Name**	**Description**	**Reset value**
0	OUTPUT_STBY	‘1‘: Outputs (1...14, 17, 18) disabled until command WR_START. ‘0‘: Output stages active, following MSC register data Bit can be set = ‘0’ by command WR_START only (see **Chapter 12.1.3**, **Figure 25**)	1
1	MSC_MON	‘1‘: No MSC monitoring timeout detected ‘0‘: Timeout: MSC monitoring has detected a transmission failure and power stages are switched off (see **Chapter 5.1**,**Table 21**, **Chapter 11.1.2**, **Item 11.5.46**) By activating the MSC communication this bit is not reset, only readout of DIAREG6 or power-on-reset (POR) or RST will enable output stages after MSC_MON has detected a failure.	1
2	POR_FLAG	‘1‘: Power-on-reset (POR) has happened. Bit is set by power-on-reset only ‘0‘: No POR since last readout. Bit is reset after RST or readout	RST and RD_DATA = ‘0’; POR = ‘1’
3	ABE_STATUS	‘1‘: ABE inactive ‘0‘: ABE active low disabling output stages	0[1)]
4	FAILURE_FLAG	‘1‘: Common failure flag OUT1...18, no failure ‘0‘: Common failure flag OUT1...18, any stage	1[1)]
5	COTW	‘1‘: Overtemperature flag OUT1...18, no DOT ‘0‘: Overtemperature flag OUT1...18, DOT any stage This bit is latched, remaining ’0’ after DOT disappears until register is reset by RST, POR or RD_DATA.	1
6	DIS5_10_STATUS	‘1‘: DIS5_10 > $V_{DIS5_10_H}$ for longer than t_{DIS5_10} ‘0‘: DIS5_10 < $V_{DIS5_10_L}$ for longer than t_{DIS5_10}	0[1)]
7	DELAYIN_STATUS	‘1‘: DELAYIN > $V_{DELAYIN_H}$ for longer than $t_{DELAYIN_GLITCH_x}$ ‘0‘: DELAYIN < $V_{DELAYIN_L}$ for longer than $t_{DELAYIN_x}$	0[1)]

1) Register data is asynchronously written and not latched by the device (status).

12.2.14 DIAREG7

Table 50 DIAREG7

Reset sources: -			
Controller read access: RD_DATA = ’1 11001 x1xx xxxx xxx’			
Controller write access: -			
UD	**Name**	**Description**	**Reset value**
0	not implemented		1
1			1
2			1
3	STATUS_SVBATT	‘1‘: No overvoltage detected by SVBATT monitoring ‘0‘: Overvoltage detected by SVBATT monitoring	1[1)]
4	TEST_ACTIVE	Device is currently ‘1’: in normal operation ‘0’: factory test mode is active	1[1)]
5	STATUS_OV	‘1‘: No overvoltage detected by VDD monitoring OV detection may be configured to be latched. ‘0‘: Overvoltage detected by VDD monitoring	1[1)2)]
6	STATUS_UV	‘1‘: No under voltage detected by VDD monitoring ‘0‘: Under voltage detected by VDD monitoring	0[1)]
7	MON_TEST	‘1‘: VDD monitoring test inactive ‘0‘: VDD monitoring test active	1[1)3)]

1) Register data is asynchronously written and not latched by the device (status).
2) Dependent on CONREG4, bit 7 setting, see **Figure 16**.
3) Same as CONREG4, bit 5

12.2.15 IDENTREG

Table 51 IDENTREG

Reset sources: -					
Controller read access: RD_DATA = ’ 1 11001 1xxx xxxx xxx’					
Controller write access: -					
UD	**Name**	**Description**			
		Software revision			
0	SW_REV0		SW_REV1	SW_REV0	
1	SW_REV1	A-step:	0	0	
		B-step:	0	1	
		C-step:	1	0	
		D-step:	1	1	
		Chip Revision			
2	CHIP_REV0		CHIP_REV2	CHIP_REV1	CHIP_REV0
3	CHIP_REV1	A-step:	0	0	0
4	CHIP_REV2	B-step:	0	0	1
		C-step:	0	1	0
		D-step	0	1	1
		E-step:	1	0	0
		Chip identifier			
5	IDENT0		IDENT2	IDENT1	IDENT0
6	IDENT1	TLE8718SA:	1	0	0
7	IDENT2				

CHIP_REV is increased for “major” design changes. SW_REV is increased for “minor” changes within each CHIP_REV separately.

12.2.16 TESTREG

For factory tests only. Do not use this command.

Table 52 TESTREG

Reset Sources: RST, power-on-reset			
Controller read access: -			
Controller write access: WR_TESTREG = ’1 01110 CD0...CD7 xxx’			
CD	**Name**	**Description**	**Reset value**
0	TEST1	reserved for factory test mode	1
1	TEST2		1
2	TEST3		1
3	TEST4		1
4	TEST5		1
5	TEST6		1
6	TEST7		1
7	TEST8		1

To enter in the test mode, a negative voltage on SVBATT (see **Item 6.4.10**) has to be applied together with a WR_TESTREG. To leave the test mode, a RST or POR has to be performed.

12.2.17 SEL_THRES

Table 53 SEL_THRES

Reset Sources: RST, power-on-reset			
Controller read access: -			
Controller write access: WR_SEL_THRESH = ’1 00111 CD0...CD7 xxx’			
CD	**Name**	**Description**	**Reset value**
0	SEL_TRESH0	active only during factory test mode	1
1	SEL_TRESH1		1
2	SEL_TRESH2		1
3	SEL_TRESH3		1
4	SEL_TRESH4		1
5	SEL_TRESH5		1
6	SEL_TRESH6		1
7	SEL_TRESH7		1

12.2.18 FUSE_SC

Table 54 FUSE_SC

Reset Sources: RST, power-on-reset			
Controller read access: -			
Controller write access: WR_FUSE_SC = ’1 01011 CD0...CD7 xxx’			
CD	**Name**	**Description**	**Reset value**
0	FUSE_SC0	active only during factory test mode	0
1	FUSE_SC1		0
2	FUSE_SC2		0
3	FUSE_SC3		0
4	FUSE_SC4		0
5	FUSE_SC5		0
6	FUSE_SC6		0
7	FUSE_SC7		0

13 Application Information

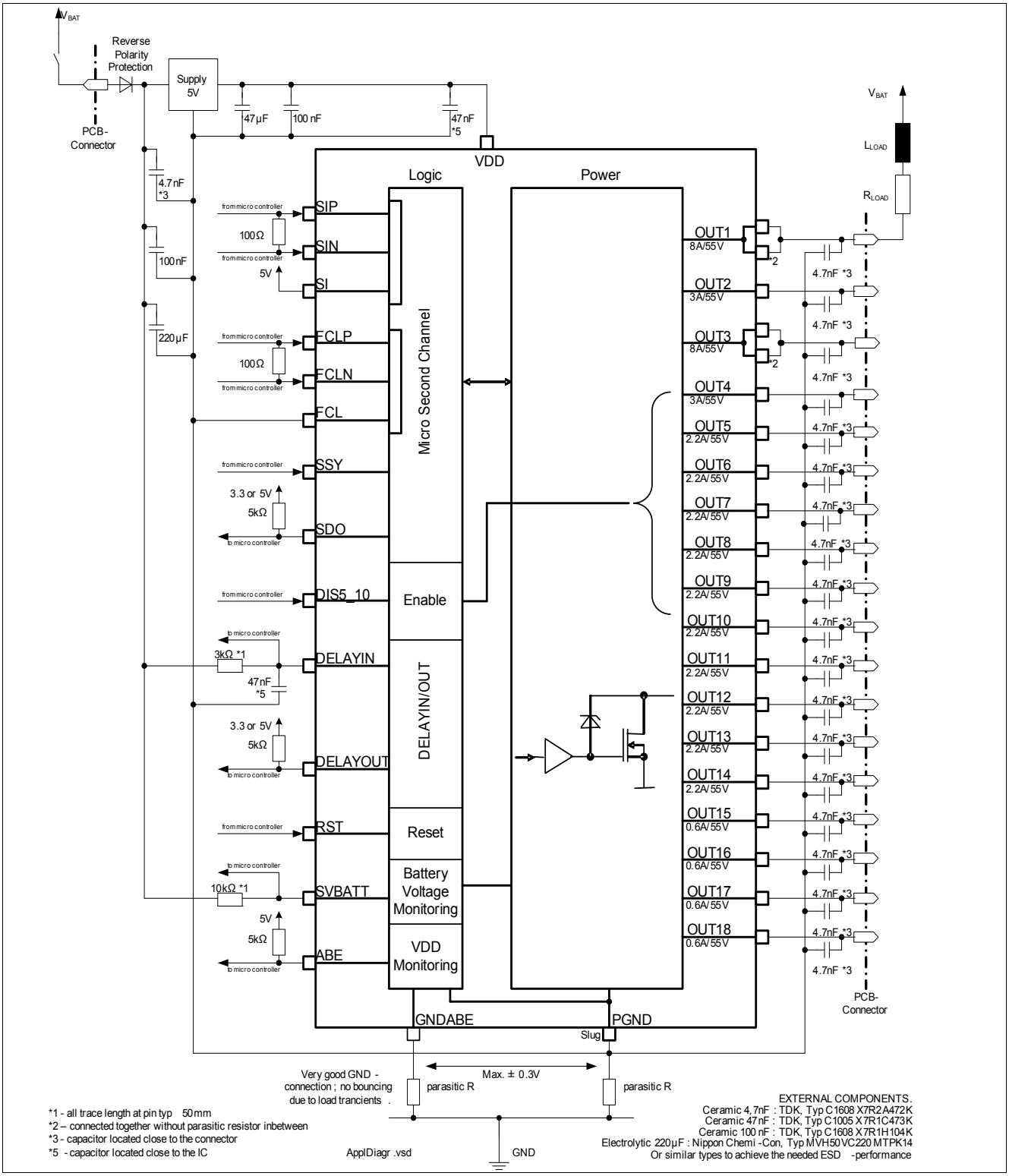


Figure 26 Application Diagram (LVDS configuration)

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

Note: The information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

14 Package Outlines

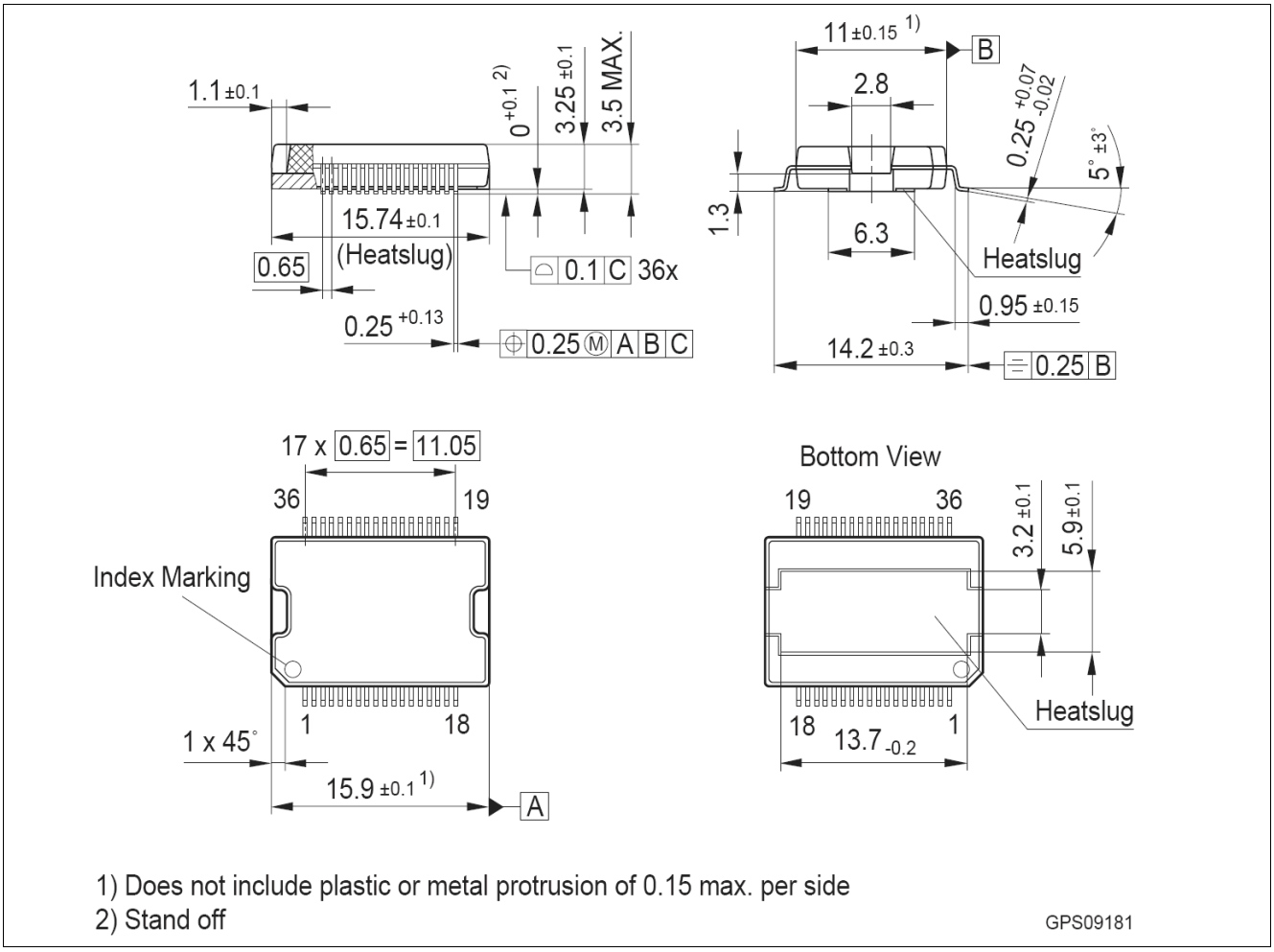


Figure 27 PG-DSO-36

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

15 Revision History

Revision	Date	Changes	1)
V1.0	2011-04-21	Datasheet created.	n
V1.1	2012-07-31	IDENTREG in **Table 51** changed from “101x xxxx“ to “100x xxxx“.	y
		Temperature Profile Table removed from **Chapter 4.5**	n

1) Functional Change

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