



# PMCM6501VPE

12 V, P-channel Trench MOSFET

10 August 2015

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a 6 bumps Wafer Level Chip-Size Package (WLCSP) using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Ultra small package:  $0.98 \times 1.48 \times 0.35$  mm
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection  $> 2$  kV HBM

## 3. Applications

- Battery switch
- High-speed line driver
- Low-side loadswitch
- Switching circuits

## 4. Quick reference data

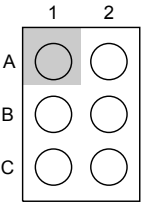
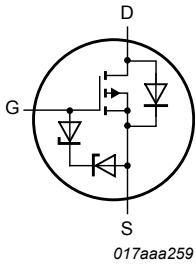
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-12	V
$V_{GS}$	gate-source voltage			-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}$ ; $T_{amb} = 25\text{ °C}$ ; $t \leq 5\text{ s}$	[1]	-	-	-8.2	A
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}$ ; $I_D = -3.0\text{ A}$ ; $T_j = 25\text{ °C}$		-	19	25	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
A1	G	gate	 <p>Transparent top view <b>WLCSP6 (OL-PMCM6501VPE)</b></p>	 <p>017aaa259</p>
A2	S	source		
B1	S	source		
B2	S	source		
C1	D	drain		
C2	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCM6501VPE	WLCSP6	WLCSP6: wafer level chip-size package; 6 bumps (3 x 2)	OL-PMCM6501VPE

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCM6501VPE	AD

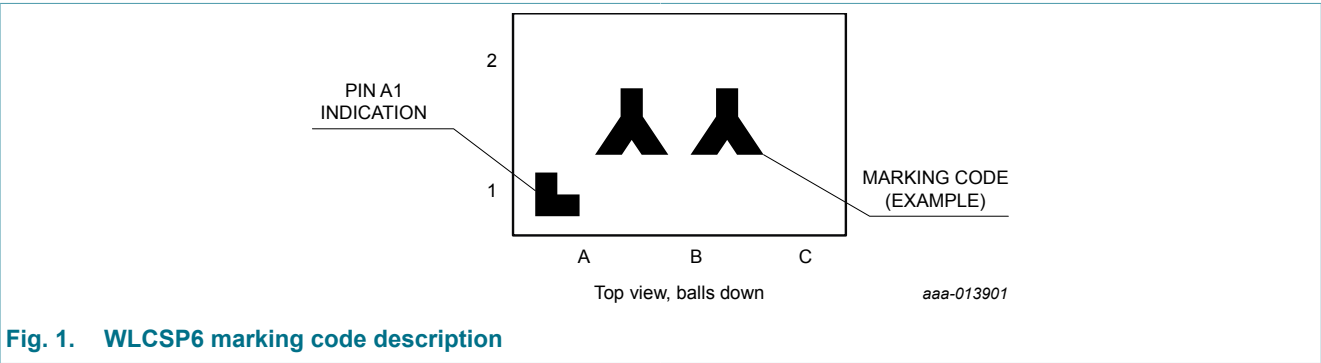


Fig. 1. WLCSP6 marking code description

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	-12	V
$V_{GS}$	gate-source voltage			-8	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-8.2	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-6.2	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-4	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-25	A
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	556	mW
			[1]	-	1300	mW
		$T_{sp} = 25\text{ °C}$		-	12500	mW
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-1.2	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

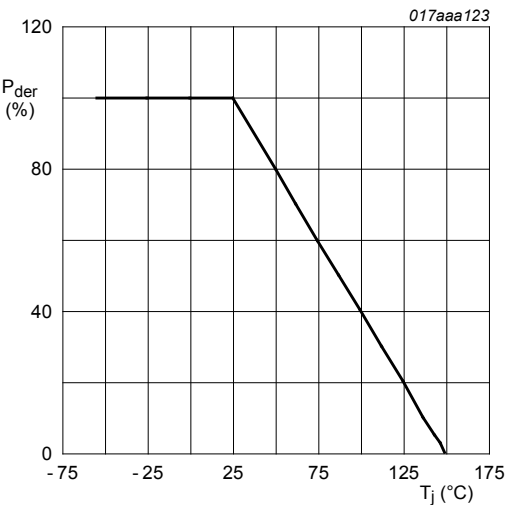


Fig. 2. MOSFET transistor: Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

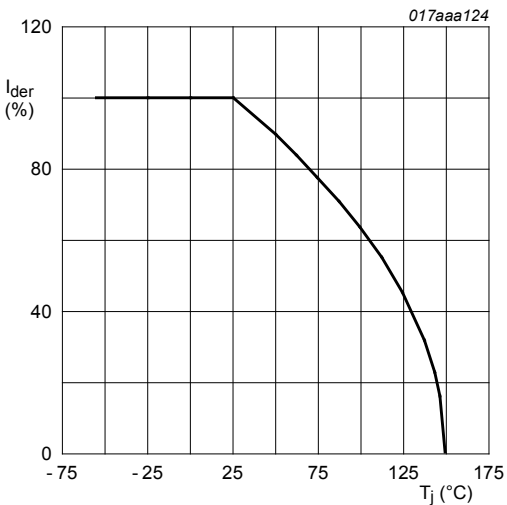
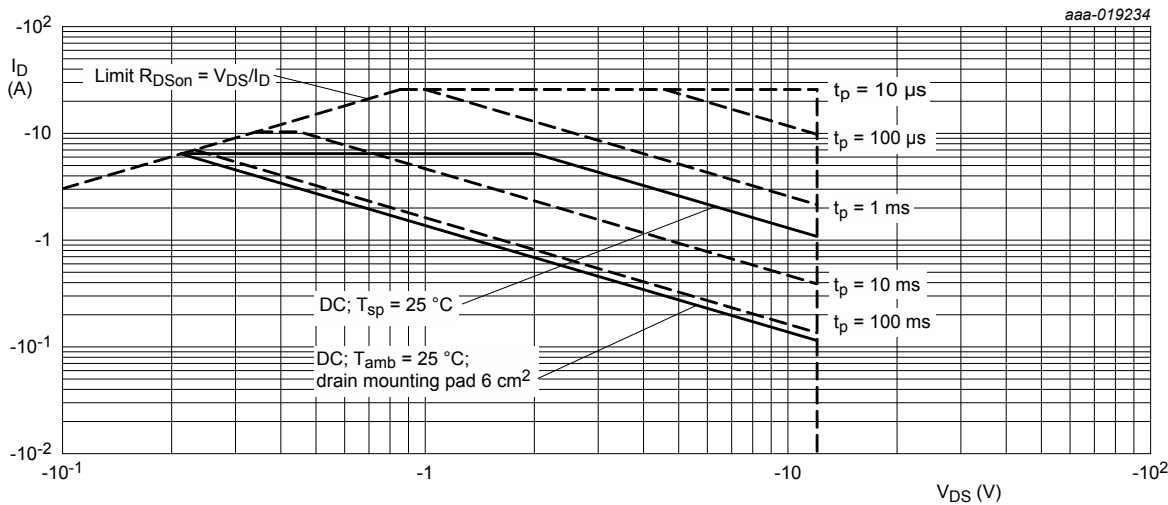


Fig. 3. MOSFET transistor: Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$



$I_{DM}$  = single pulse

Fig. 4. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	180	225	K/W
			[2]	-	65	85	K/W
			[3]	-	75	95	K/W

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		in free air; $t \leq 5$ s	[3]	-	45	55	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 4-layer 1 cm<sup>2</sup>.
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

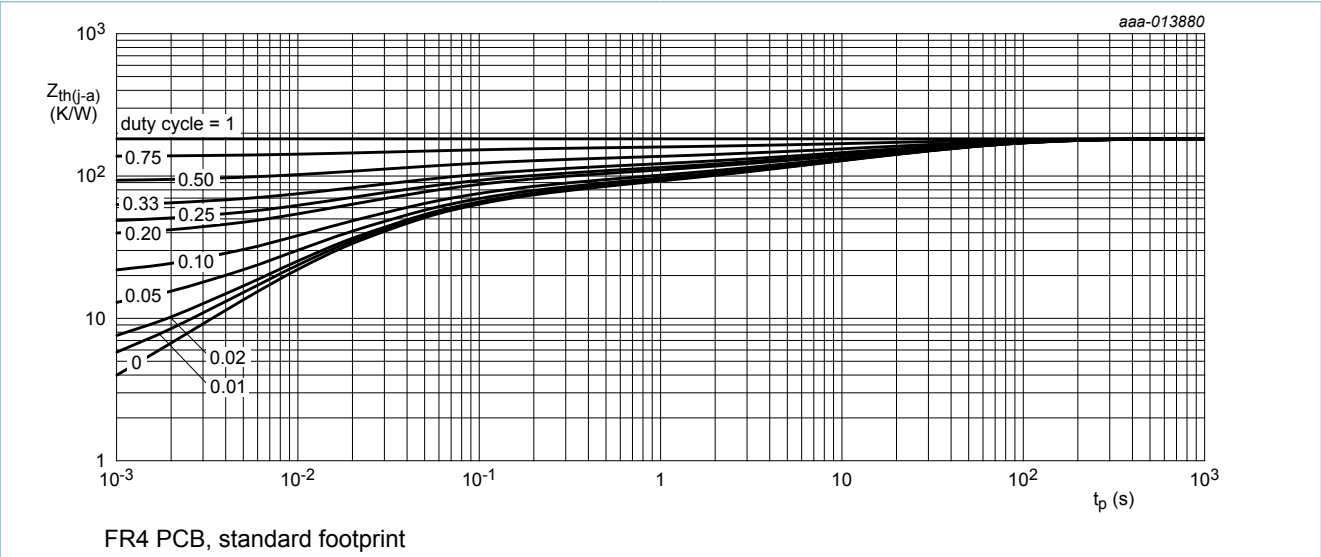


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

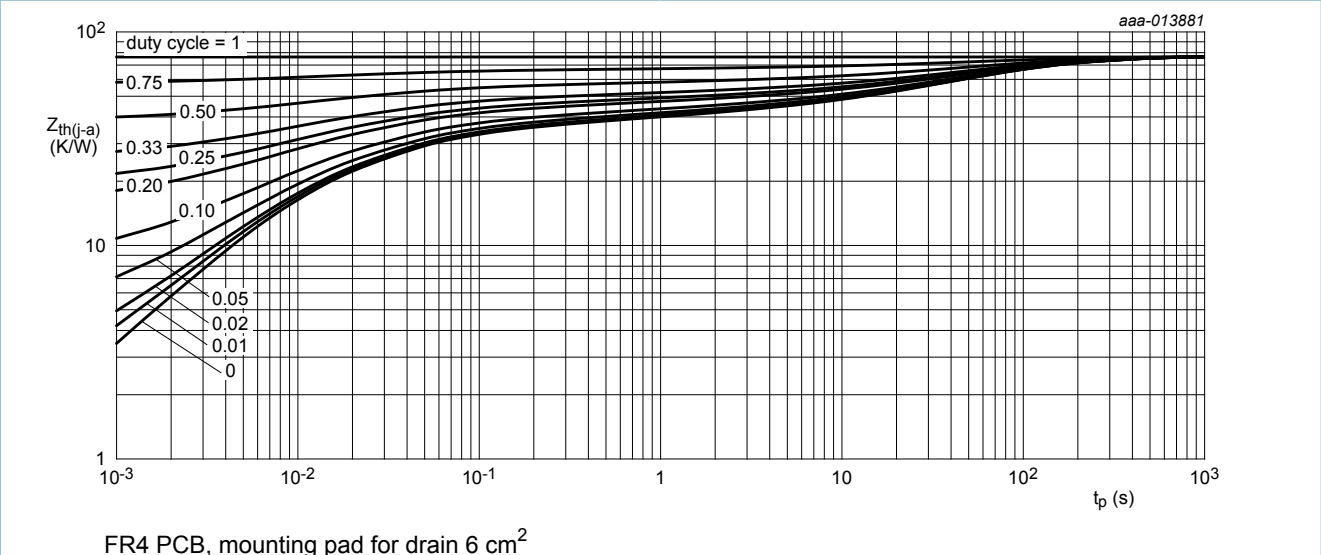


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = -250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-12	-	-	V
V <sub>GSth</sub>	gate-source threshold voltage	I <sub>D</sub> = -250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C		-0.4	-0.6	-0.9	V
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = -12 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = -8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-10	μA
		V <sub>GS</sub> = 8 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	10	μA
		V <sub>GS</sub> = -4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-1	μA
		V <sub>GS</sub> = 4.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	1	μA
		V <sub>GS</sub> = -2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	-200	nA
		V <sub>GS</sub> = 2.5 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-	200	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -3.0 A; T <sub>j</sub> = 25 °C		-	19	25	mΩ
		V <sub>GS</sub> = -4.5 V; I <sub>D</sub> = -3.0 A; T <sub>j</sub> = 150 °C		-	26	34	mΩ
		V <sub>GS</sub> = -2.5 V; I <sub>D</sub> = -3.0 A; T <sub>j</sub> = 25 °C		-	25	33	mΩ
		V <sub>GS</sub> = -1.8 V; I <sub>D</sub> = -1.0 A; T <sub>j</sub> = 25 °C		-	37	60	mΩ
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = -6.0 V; I <sub>D</sub> = -3.0 A; T <sub>j</sub> = 25 °C		-	13	-	S
R <sub>G</sub>	gate resistance	f = 1 MHz		-	12.6	-	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	V <sub>DS</sub> = -6 V; I <sub>D</sub> = -3 A; V <sub>GS</sub> = -4.5 V; T <sub>j</sub> = 25 °C		-	19.6	29.4	nC
Q <sub>GS</sub>	gate-source charge			-	2.7	-	nC
Q <sub>GD</sub>	gate-drain charge			-	5	-	nC
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = -6 V; f = 1 MHz; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	1400	-	pF
C <sub>oss</sub>	output capacitance			-	430	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	400	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = -6 V; I <sub>D</sub> = -6 A; V <sub>GS</sub> = -4.5 V; R <sub>G(ext)</sub> = 6 Ω; T <sub>j</sub> = 25 °C		-	8	-	ns
t <sub>r</sub>	rise time			-	51	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	72	-	ns
t <sub>f</sub>	fall time			-	62	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = -1.2 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C		-	-0.9	-1.2	V

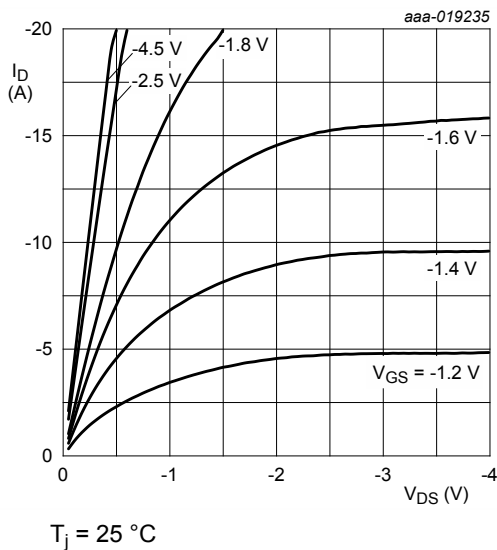


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

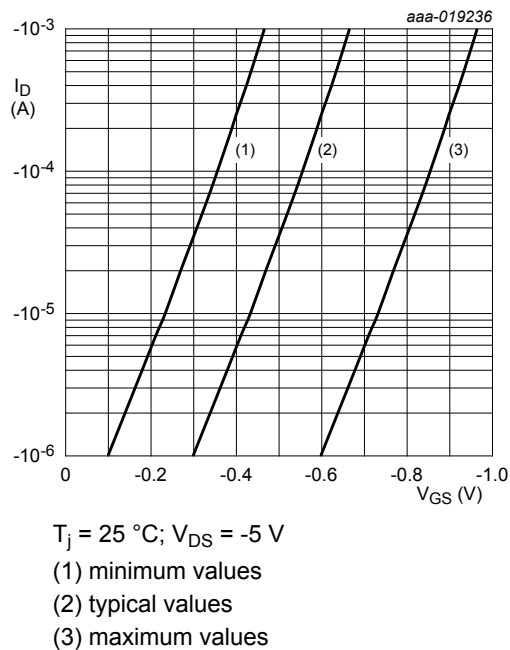


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

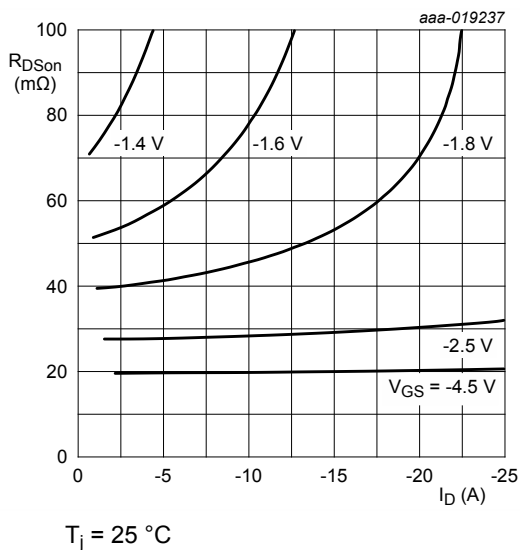


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

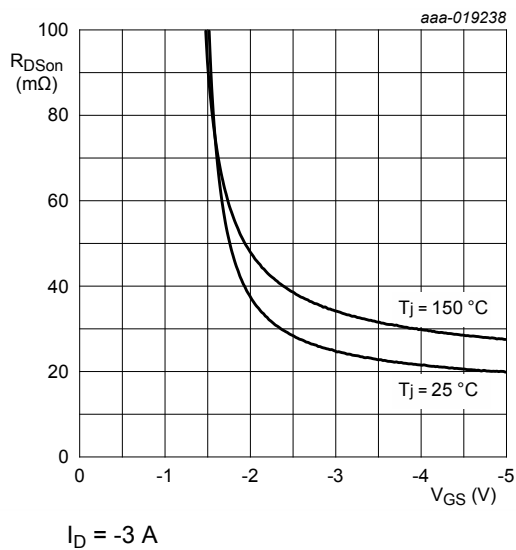
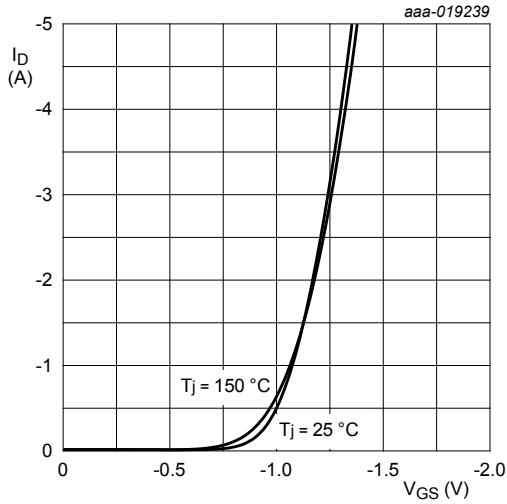
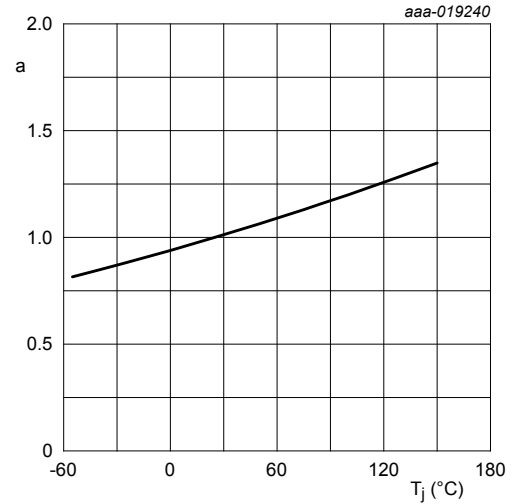


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

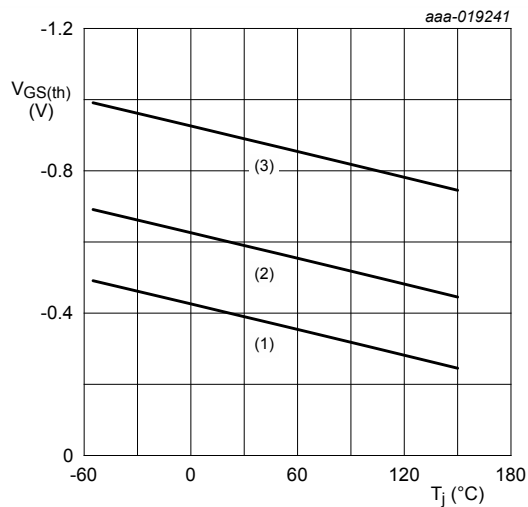


**Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



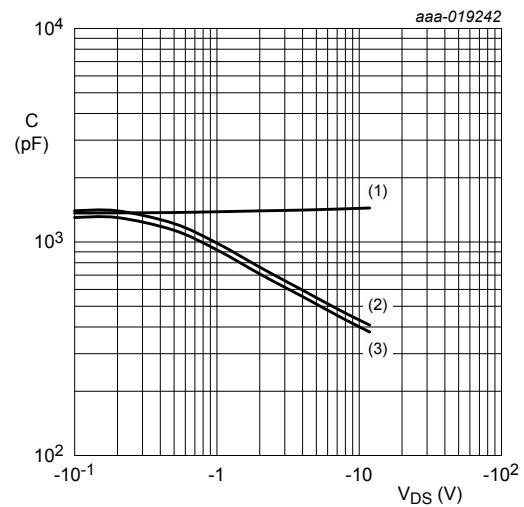
**Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$



$I_D = -0.25 \text{ mA}$ ;  $V_{DS} = V_{GS}$   
 (1) minimum values  
 (2) typical values  
 (3) maximum values

**Fig. 13. Gate-source threshold voltage as a function of junction temperature**



$f = 1 \text{ MHz}$ ;  $V_{GS} = 0 \text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

**Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



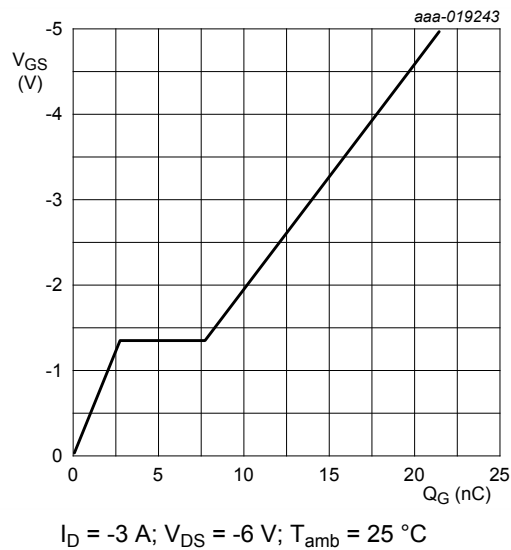


Fig. 15. Gate-source voltage as a function of gate charge; typical values

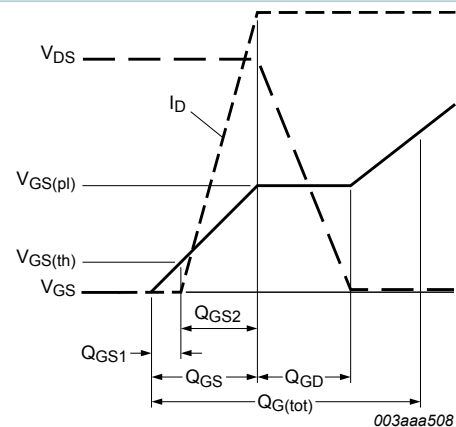


Fig. 16. MOSFET transistor: Gate charge waveform definitions

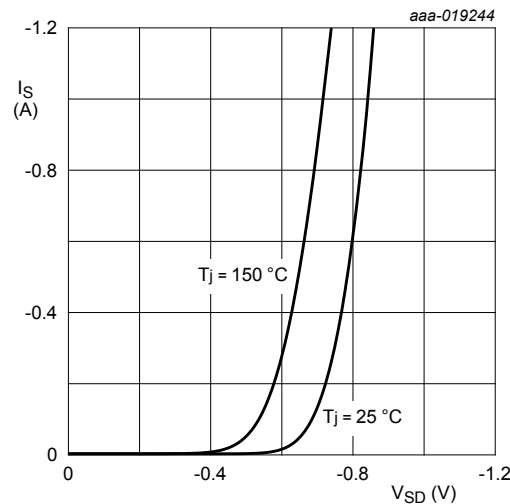


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

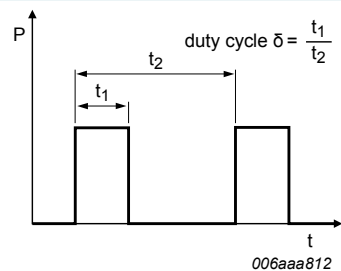


Fig. 18. Duty cycle definition

12. Package outline

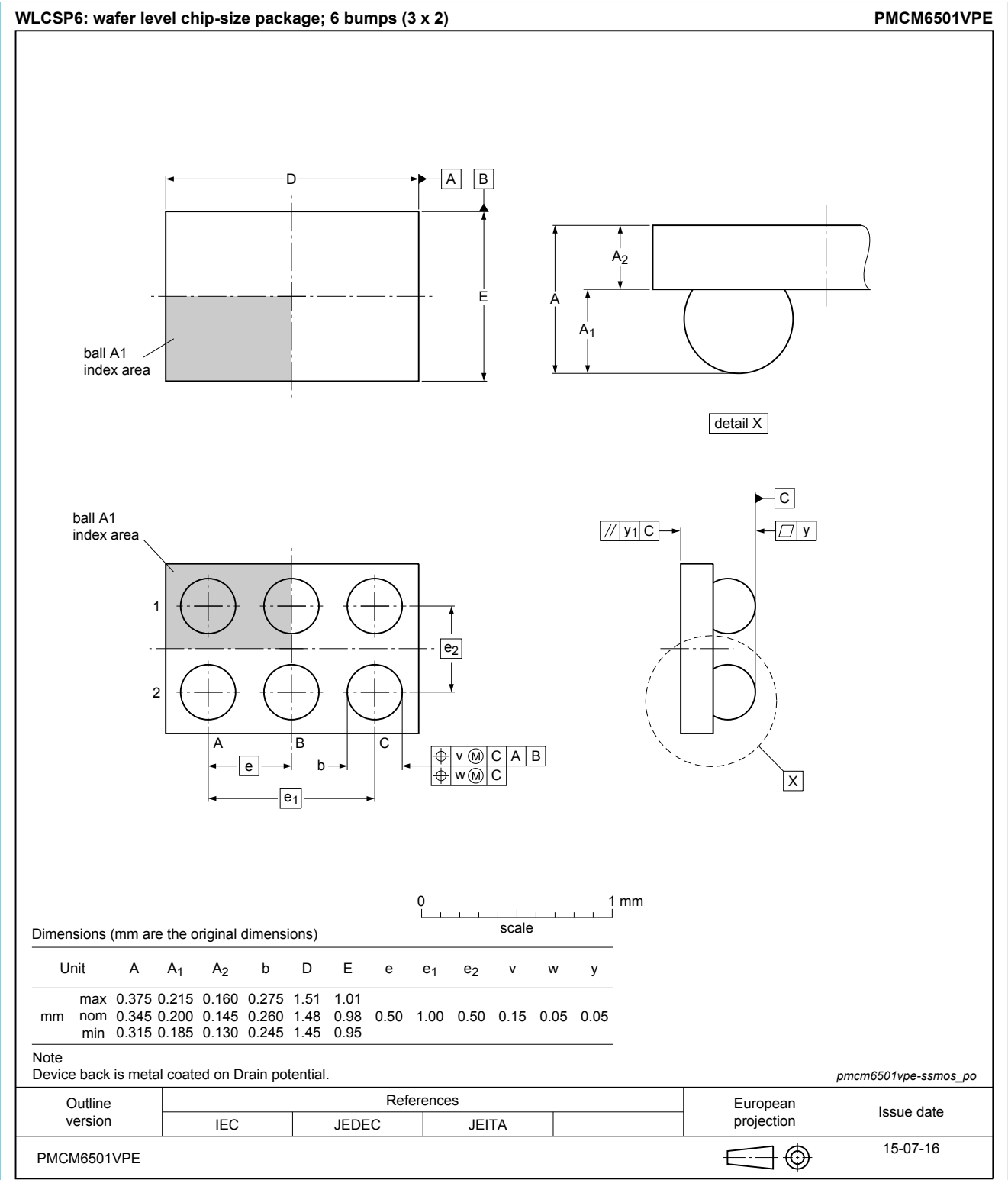
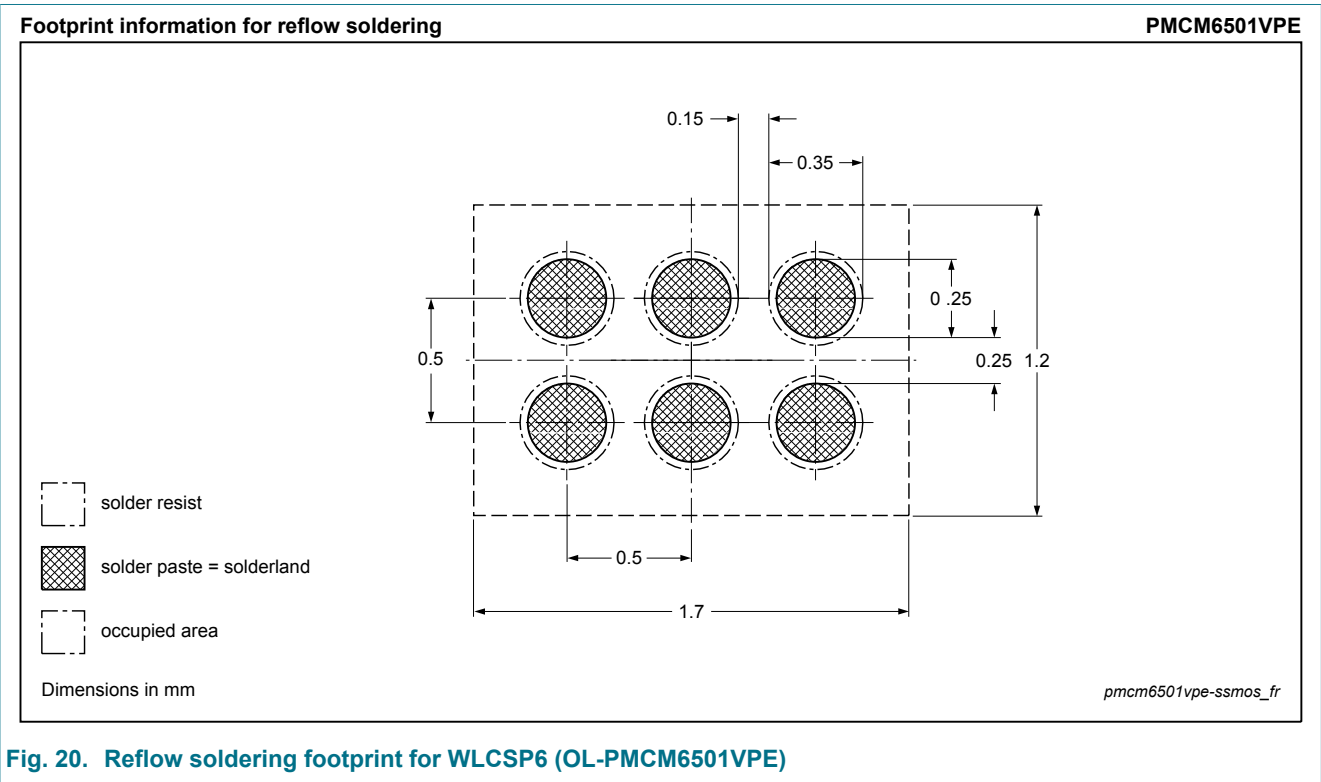


Fig. 19. Package outline WLCSP6 (OL-PMCM6501VPE)

13. Soldering



## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCM6501VPE v.1	20150810	Product data sheet	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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