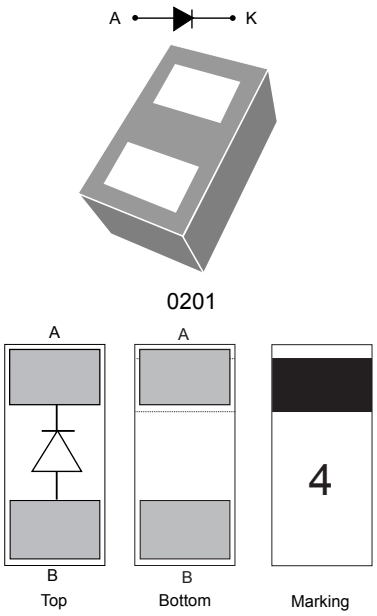
BAT30F4

Datasheet

30 V signal Schottky diode



Features

- Very low conduction losses
- Negligible switching losses
- 0201 package
- Low capacitance diode
- ECOPACK®2 and RoHS compliant

Applications

- Reverse polarity protection
- Fingerprint module
- Camera module
- Bluetooth wireless earbud
- Biometric computer card

Description

The BAT30F4 uses 30 V Schottky barrier diodes in a 0201 package. This device is intended to be used in smartphones, and is especially suited for rail to rail protection where its low forward voltage drop will help designers to get an efficient protection of their ICs.

Product status link
BAT30F4

Product summary	
V_{RRM}	30 V
T_j (max)	85 °C
I_F	300 mA

1 Characteristics

Table 1. Absolute ratings (limiting values, at 25 °C, unless otherwise specified)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		30	V
I_F	Continuous forward current		300	mA
I_{FSM}	Surge non repetitive forward current	t_p = 10 ms sinusoidal	4	A
P_D (1)	Power dissipation		200	mW
T_{stg}	Storage temperature range		-55 to + 150	°C
T_{OP}	Operating junction temperature range		-40 to +85	°C
T_j	Maximum junction temperature in DC forward mode		150	°C
T_L	Maximum soldering temperature during 10 s		260	°C

1. *On epoxy printed circuit board with minimum recommended footprint*

Table 2. Thermal resistance parameter

Symbol	Parameter	Value (Typ.)	Unit
$R_{th(j-a)}$	Junction to ambient (1)	450	°C/W

1. *On epoxy printed circuit board with minimum recommended footprint*

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
I_R (1)	Reverse leakage current	T_j = 25 °C	V_R = 10 V	-	2.2	6.0	µA
		T_j = 85 °C		-		300	
		T_j = 25 °C	V_R = 30 V	-	18		
		T_j = 85 °C		-		1600	
V_F (2)	Forward voltage drop	T_j = 25 °C	I_F = 5 mA	-		0.285	V
		T_j = 85 °C		-		0.205	
		T_j = 25 °C	I_F = 10 mA	-	0.27	0.31	
		T_j = 85 °C		-		0.24	
		T_j = 25 °C	I_F = 100 mA	-	0.39	0.44	
		T_j = 85 °C		-		0.40	
		T_j = 25 °C	I_F = 300 mA	-	0.55	0.625	
		T_j = 85 °C		-		0.64	

1. *Pulse test: t_p = 5 ms, δ < 2%*
2. *Pulse test: t_p = 380 µs, δ < 2%*

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C	Diode capacitance	V_R = 1 V, F = 1 MHz	-	10	14	pF

1.1 Characteristics (curves)

Figure 1. Reverse leakage current versus reverse applied voltage (typical values)

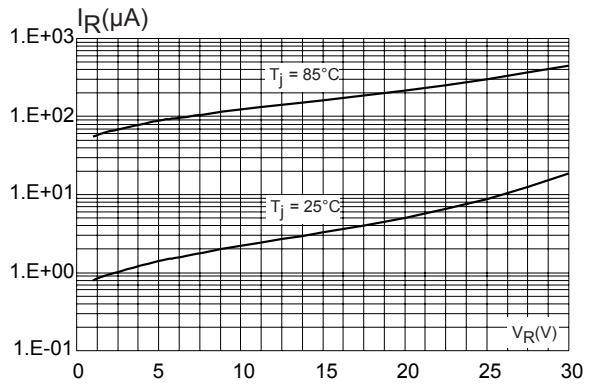


Figure 2. Forward voltage drop versus forward current (typical values)

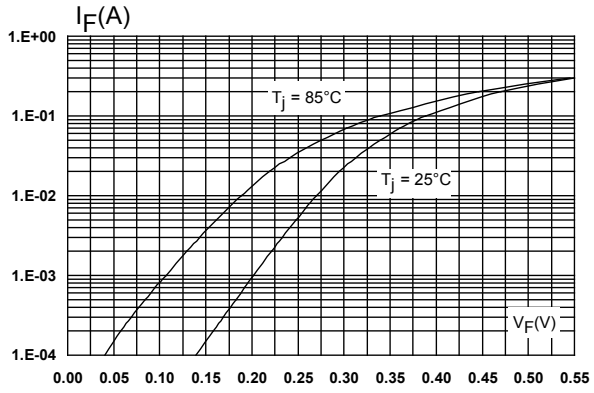


Figure 3. Relative variation of reverse leakage current versus junction temperature

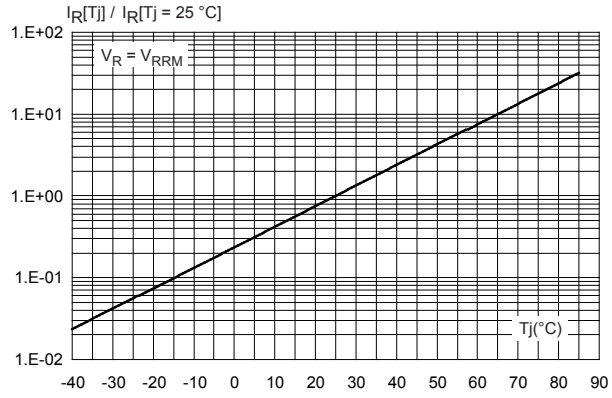


Figure 4. Junction capacitance versus reverse applied voltage (typical values)

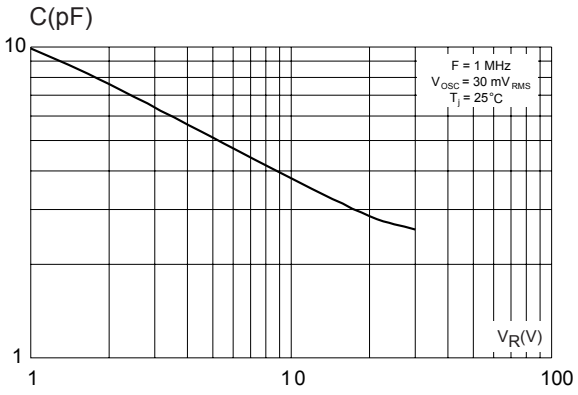
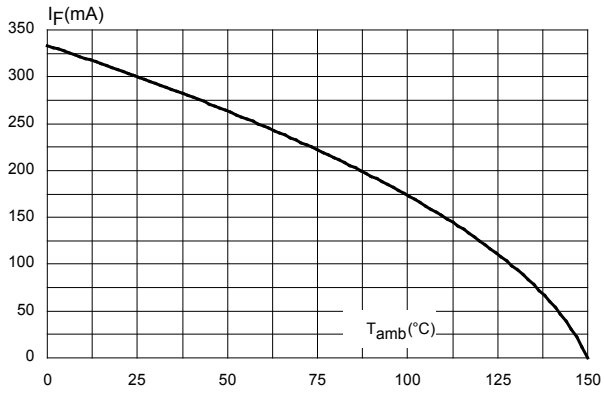


Figure 5. Continuous forward current versus ambient temperature



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

2.1 0201 package information

Figure 6. 0201 package outline

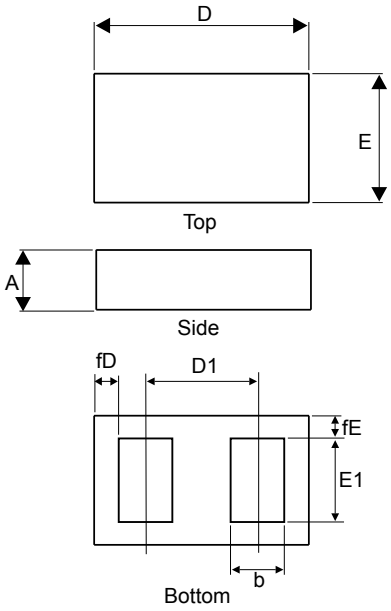


Table 5. 0201 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches (for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.28	0.30	0.32	0.0110	0.0118	0.0126
b	0.125	0.14	0.155	0.0049	0.0055	0.0061
D	0.57	0.60	0.63	0.0224	0.0236	0.0248
D1		0.35			0.0138	
E	0.27	0.30	0.33	0.0106	0.0118	0.0130
E1	0.175	0.19	0.205	0.0069	0.0075	0.0081
fD	0.040	0.055	0.070	0.0015	0.0021	0.0027
fE	0.040	0.055	0.070	0.0015	0.0021	0.0027

Figure 7. **Footprint in mm (inches)**

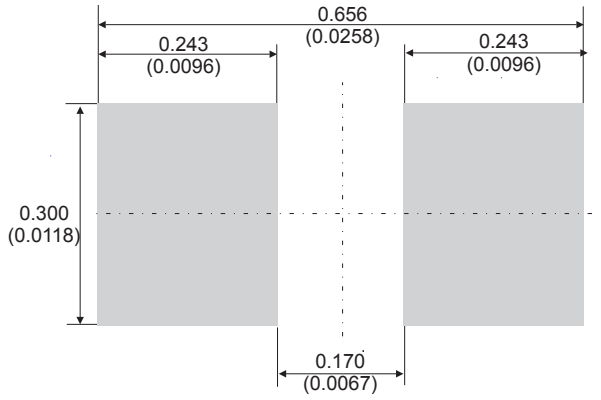
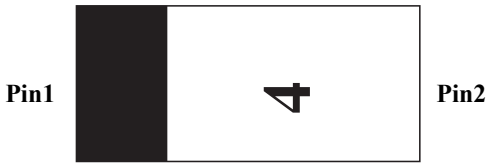
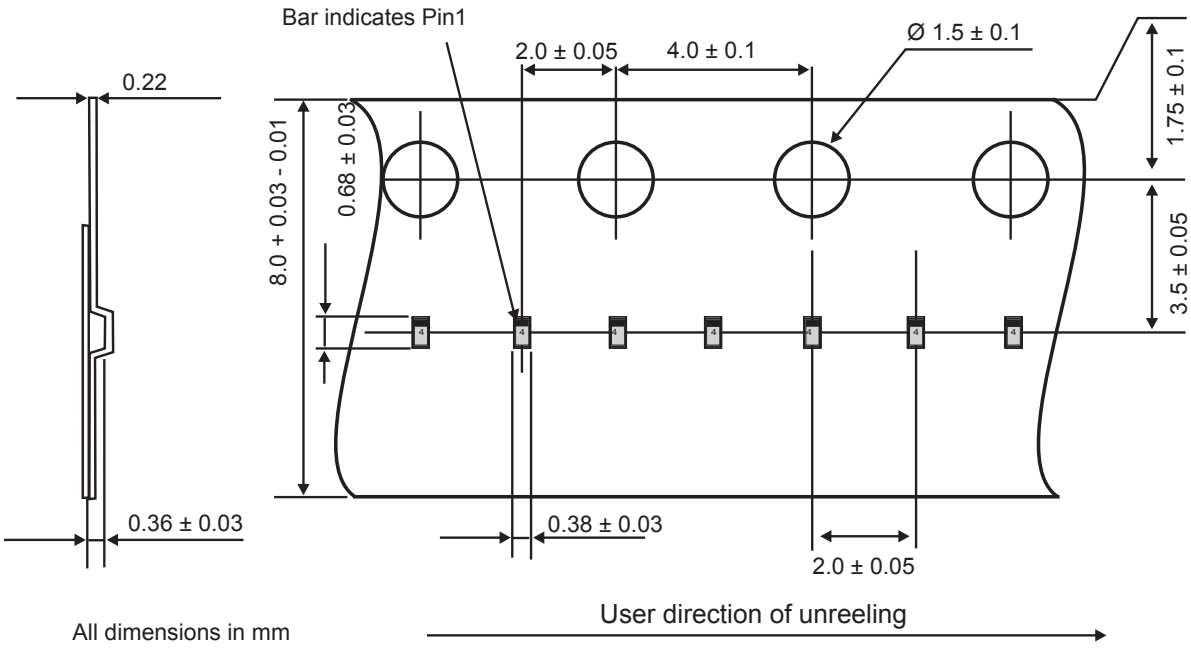


Figure 8. **Marking**



Note: The marking codes can be rotated by 90° or 180° to differentiate assembly location. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 9. **Tape and reel specification**

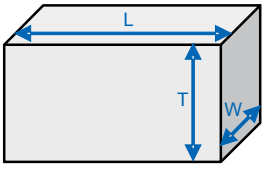


3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).

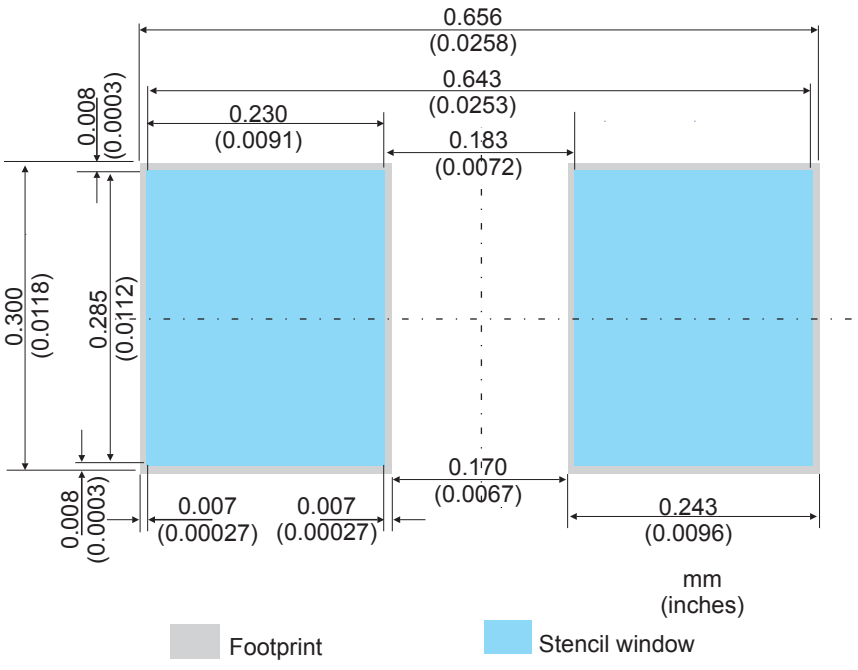
Figure 10. Stencil opening recommendation



   b. General design rule
      - Stencil thickness (T) = 75 ~ 125 µm
      - $\frac{W}{T} \geq 1.5$
      - $\frac{L \times W}{2T(L+W)} \geq 0.66$

1. Reference design
   a. Stencil opening thickness: 80 µm
   b. Other dimensions: see below figure.

Figure 11. Recommended stencil window position, stencil opening thickness: 80 µm



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component displacement during PCB movement.
4. Use solder paste with fine particles: Type 4 (powder particle size 20-48 µm per IPC J STD-005).

3.3 Placement

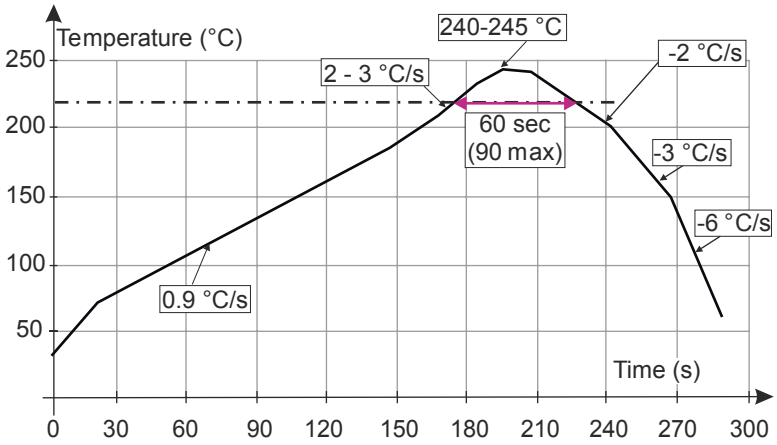
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.5 Reflow profile

Figure 12. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Table 6. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
BAT30F4	4[1]	Flat CSPS	0.116 mg	15000	Tape and reel

1. *The marking codes can be rotated by 90° or 180° to differentiate assembly location*

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
13-May-2014	1	First issue
24-Nov-2014	2	Updated Table 2.
13-Apr-2015	3	Updated Features and Description.
11-Feb-2016	4	Updated Table 3 and Figure 4.
26-Feb-2016	5	Updated Table 2. Added Table 3, Table 5 and Figure 7.
05-Jun-2018	6	Updated Table 3. Static electrical characteristics, Table 5. 0201 package mechanical data and Table 6. Ordering information.
24-Sep-2018	7	Updated Table 3. Static electrical characteristics.

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