1100 2.5-Inch and M.2 SATA NAND Flash SSD

MTFDDAK256TBN, MTFDDAK512TBN, MTFDDAK1T0TBN, MTFDDAK2T0TBN, MTFDDAV256TBN, MTFDDAV512TBN, MTFDDAV1T0TBN

Features

- Micron® 3D TLC NAND Flash
- RoHS-compliant package
- SATA 6 Gb/s interface
- TCG/Opal 2.0-compliant self-encrypting drive (SED)
- Compatible with Microsoft eDrive®
- Hardware-based AES-256 encryption engine
- ATA modes supported
  - PIO mode 3, 4
  - Multiword DMA mode 0, 1, 2
  - Ultra DMA mode 0, 1, 2, 3, 4, 5, 6
- Industry-standard, 512-byte sector size support
- Hot-plug/hot-remove capable (2.5")
- Device sleep (DEVSLP), extreme low-power mode
- Native command queuing support with 32-command slot support
- ATA-8 ACS3 command set compliant
- ATA security feature command set and password login support
- Secure erase (data page) command set: fast and secure erase
- Sanitize device feature set support
- Self-monitoring, analysis, and reporting technology (SMART) command set
- Dynamic write acceleration
- Adaptive thermal monitoring
- Power loss protection for data-at-rest
- Performance[1, 2]
  - PCMark® Vantage (HDD test suite score): Up to 84,000
  - Sequential 128KB READ: Up to 530 MB/s
  - Sequential 128KB WRITE: Up to 500 MB/s
  - Random 4KB READ: Up to 55,000 IOPS
  - Random 4KB WRITE: Up to 83,000 IOPS
  - READ/WRITE latency: 85µs/40µs (TYP)
- Reliability
  - MTTF: 1.5 million device hours[3]
  - Static and dynamic wear leveling
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{15} bits read
- Low power consumption
  - Device Sleep numbers: <4mW
  - DIPM numbers: 110mW TYP[4]
- Endurance: Total bytes written (TBW)
  - 120TB
- Capacity (unformatted): 128GB
- 2.5-inch × 7mm form factor
- Secure firmware update with digitally signed firmware image
- Operating temperature
  - Commercial (0°C to +70°C)[5]

Notes:
1. Typical I/O performance numbers as measured fresh-out-of-the-box (FOB) using Iometer with a queue depth of 32 and write cache enabled.
2. 4 KB transfers used for READ/WRITE latency values.
3. The product achieves a mean time to failure (MTTF) based on population statistics not relevant to individual units.
4. Active average power measured during execution of MobileMark® with DIPM (device-initiated power management) enabled.
5. Temperature measured by SMART attribute 194.

Warranty: Contact your Micron sales representative for further information regarding the product, including product warranties.

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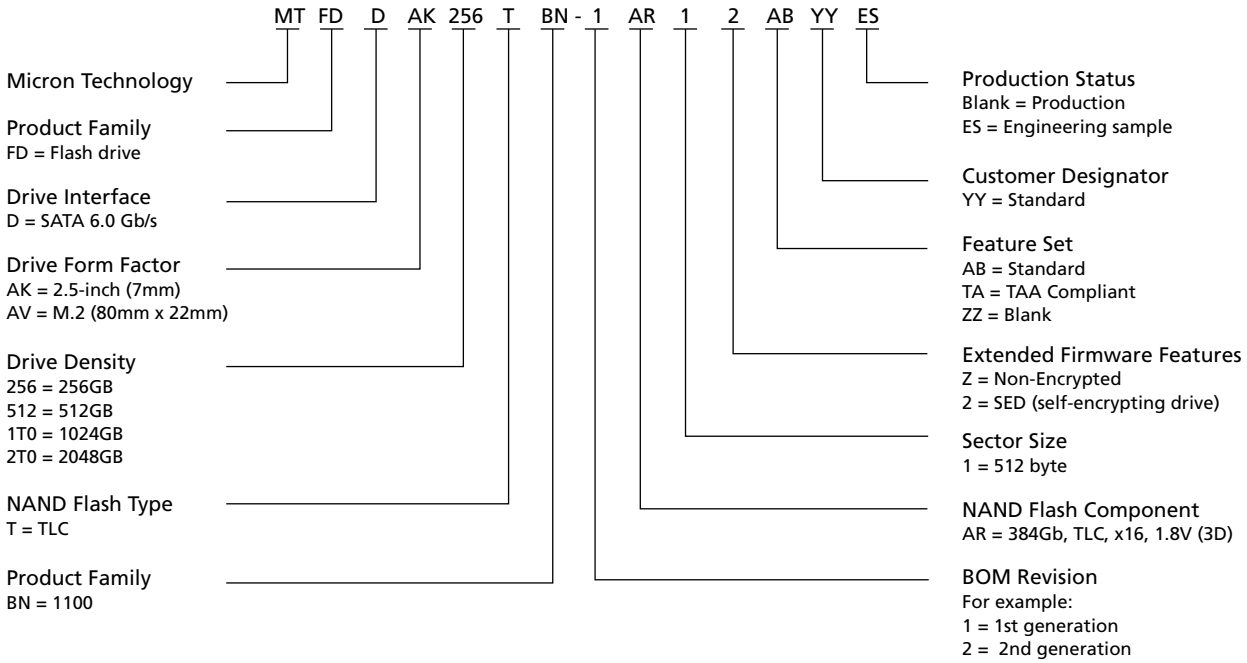
Part Numbering Information

Micron's 1100 SSD is available in different configurations and densities. The chart below is a comprehensive list of options for the 1100 series devices; not all options listed can be combined to define an offered product. Visit www.micron.com for a list of valid part numbers.

Figure 1: Part Number Chart



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General Description

Micron's solid state drive (SSD) uses a single-chip controller with a SATA interface on the system side and up to four channels of Micron NAND Flash internally. Available in both M.2 and 2.5-inch form factors, the SSD integrates easily in existing storage infrastructures.

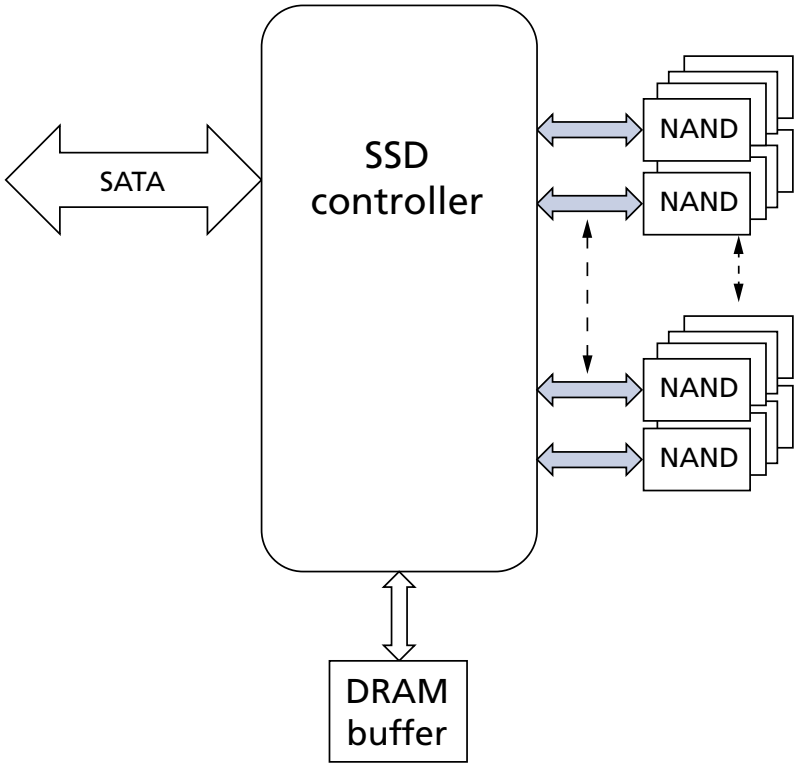
The SSD is designed to use the SATA interface efficiently during both READs and WRITEs while delivering bandwidth-focused performance. SSD technology enables enhanced boot times, faster application load times, reduced power consumption and extended reliability.

The self-encrypting drive (SED) features a FIPS-compliant, AES-256 encryption engine, providing hardware-based, secure data encryption, with no loss of SSD performance. This SED follows the TCG/Opal specification for trusted peripherals.

When TCG/Opal features are not enabled, the device can perform alternate data encryption by invoking the ATA security command set encryption features, to provide full-disk encryption (FDE) managed in the host system BIOS. TCG/Opal and ATA security feature sets cannot be enabled simultaneously.

The data encryption is always running; however, encryption keys are not managed and the data is not secure until either TCG/Opal or ATA security feature sets are enabled.

Figure 2: Functional Block Diagram



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Performance

Measured performance can vary for a number of reasons. The major factors affecting drive performance are the capacity of the drive and the interface of the host. Additionally, overall system performance can affect the measured drive performance. When comparing drives, it is recommended that all system variables are the same, and only the drive being tested varies.

Performance numbers will vary depending on the host system configuration.

For SSDs designed for the client computing market, Micron specifies performance in fresh-out-of-box (FOB) state. Data throughput measured in steady state may be lower than FOB state, depending on the nature of the data workload.

For a description of these performance states and of Micron's best practices for performance measurement, refer to Micron's technical marketing brief, Best Practices for SSD Performance Measurement.

Table 1: Drive Performance

Capacity	256GB	512GB	1024GB	2048GB	
Interface Speed	**6 Gb/s**				**Unit**
PCMark vantage	84,000	84,000	84,000	84,000	HDD score
Sequential read (128KB transfer)	530	530	530	530	MB/s
Sequential write (128KB transfer)	500	500	500	500	MB/s
Random read (4KB transfer)	55,000	92,000	92,000	92,000	IOPS
Random write (4KB transfer)	83,000	83,000	83,000	83,000	IOPS
READ latency (TYP)	85	85	85	85	µs
WRITE latency (TYP)	40	40	40	40	µs

Notes:
1. Performance numbers are maximum values, except as noted.
2. Typical I/O performance numbers as measured using Iometer with a queue depth of 32 and write cache enabled. Fresh-out-of-box (FOB) state is assumed. For performance measurement purposes, the SSD may be restored to FOB state using the SECURE ERASE command.
3. Iometer measurements are performed on an 20GB span of logical block addresses (LBAs).
4. 4KB transfers with a queue depth of 1 are used to measure READ/WRITE latency values with write cache enabled.
5. System variations will affect measured results. For comparison, PCMark scores are measured with the SSD as a secondary drive in a two-drive system. When measured as an OS drive, system overhead can cause lower scores.

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Logical Block Address Configuration

The drive is set to report the number of logical block addresses (LBA) that will ensure sufficient storage space for the specified capacity. Standard LBA settings, based on the IDEMA standard (LBA1-03), are shown below.

Table 2: Standard LBA Settings

	Total LBA		Max LBA		User Available Bytes
Capacity	Decimal	Hexadecimal	Decimal	Hexadecimal	(Unformatted)
256GB	500,118,192	1DCF32B0	500,118,191	1DCF32AF	256,060,514,304
512GB	1,000,215,216	3B9E12B0	1,000,215,215	3B9E12AF	512,110,190,592
1024GB	2,000,409,264	773BD2B0	2,000,409,263	773BD2AF	1,024,209,543,168
2048GB	4,000,797,360	EE7752B0	4,000,797,359	EE7752AF	2,048,408,248,320

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Reliability

Micron's SSDs incorporate advanced technology for defect and error management. They use various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 3: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
<1 sector per 10^{15} bits read	READ

Mean Time To Failure

Mean time to failure (MTTF) for the SSD can be predicted based on the component reliability data using the methods referenced in the Telcordia SR-332 reliability prediction procedures for electronic equipment.

Table 4: MTTF

Capacity	MTTF (Operating Hours)[1]
256GB	1.5 million
512GB	
1024GB	
2048GB	

Note: 1. The product achieves a mean time to failure (MTTF) of 1.5 million hours, based on population statistics not relevant to individual units.

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Endurance

Endurance for the SSD can be predicted based on the usage conditions applied to the device, the internal NAND component cycles, the write amplification factor, and the wear-leveling efficiency of the drive. The table below shows the drive lifetime for each SSD capacity by client computing and sequential input and based on predefined usage conditions.

Table 5: Drive Lifetime – Client Computing

Capacity	Drive Lifetime (Total Bytes Written)
256GB	120TB
512GB	240TB
1024GB	400TB
2048GB	

Notes:
1. Total bytes written validated with the drive 90% full.
2. SSD volatile write cache is enabled.
3. Access patterns used during reliability testing are 25% sequential and 75% random and consist of the following: 1% are 512B; 44% are 4 KiB; 35% are 64 KiB; and 20% are 128 KiB.
4. Host workload parameters, including write cache settings, I/O alignment, transfer sizes, randomness, and percent full, that are substantially different than the described notes may result in varied endurance results.
5. GB/day can be calculated by dividing the total bytes written value by the number of days in the interval of interest (365 days × number of years). For example: 100 TB/3 years/365 days = 91 GB/day for 3 years.

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Electrical Characteristics

Environmental conditions beyond those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: SATA Power Consumption

Capacity	Device Sleep Typical	Idle Average	Active Average	Active Maximum (128KB transfer)	Unit
256GB	2	55	70	3000	mW
512GB				4000	
1024GB	4	65	75	5000	mW
2048GB	25	110	150	6000	

Notes:
1. Data taken at 25°C using a 6 Gb/s SATA interface.
2. Active average power measured while running MobileMark productivity suite.
3. Device-initiated power management (DIPM) enabled. DIPM slumber and DEVSLP enabled.
4. Active maximum power is an average power measurement performed using Iometer with 128KB sequential write transfers.

Table 7: Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Voltage input, 2.5-inch	V5	4.5	5.5	V	–
Voltage input, M.2	3V3	3.14	3.46	V	–
Operating temperature	T_C	0	70	°C	1
Non-operating temperature	–	–40	85	°C	–
Rate of temperature change	–	–	20	°C/hour	–
Relative humidity (non-condensing)	–	5	95	%	–

Note:
1. Operating temperature is best measured by reading the SSD's on-board temperature sensor, which is recorded in SMART attribute 194 (0xC2).

Table 8: Shock and Vibration

Parameter/Condition	Specification
Non-operating shock	1500G/0.5ms
Non-operating vibration	5–800Hz @ 3.10G

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Dynamic Write Acceleration

Dynamic write acceleration optimizes SSD performance for typical client-computing environments, where WRITE operations tend to occur in bursts of commands with idle time between these bursts.

Capacity for accelerated performance is derived from the adaptive usage of the SSD's native NAND array, without sacrificing user-addressable storage. Recent advances in Micron NAND technology enable the SSD firmware to achieve acceleration through on-the-fly mode switching between SLC and TLC modes to create a high-speed SLC pool that changes in size and location with usage conditions.

During periods of idle time between write bursts, the drive may free additional capacity for accelerated write performance. The amount of accelerated capacity recovered during idle time depends on the portion of logical addresses that contain user data and other runtime parameters. In applications that do not provide sufficient idle time, the device may need to perform SLC-to-TLC data migration during host activity.

Under accelerated operation, write performance may be significantly higher than non-accelerated operations. Power consumption per-byte written is lower during accelerated operation, which may reduce overall power consumption and heat production.

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Adaptive Thermal Monitoring

The device features adaptive thermal monitoring. While most host computers exhibit operating environments that keep an SSD running in the range of 40°C to 45°C, adaptive thermal monitoring enables the SSD to operate in a wide variety of environments by helping to prevent the host computer from running at excessive temperatures.

Adaptive thermal monitoring reduces total SSD power consumption by the device controller, as well as the NAND media, by injecting time-based delays between internal processing of media commands when the device temperature reaches 75°C. The delay times used are bound to the microsecond range and are based on a proportional and differential control equation of the general form shown here:

$$u(t) = Kp \times T_p(t) + Kd \times \frac{dT_d}{dt}$$

The delay-control equation is tuned for a steady-state temperature target, which has been designed as an optimum balance of hardware temperature tolerances and drive performance. Steady-state temperature targets are hardware-configuration dependent and may range around 80°C. Temperatures below the intended steady-state target will not produce a proportional component delay, but may produce a differential component based on the current rate of temperature change according to the control equation. When the feature is active, DRAM refresh rates are also adjusted to improve data integrity and stability while operating outside of temperature specifications.

When the device temperature falls below 73°C, normal operation will continue without induced delays. If the temperature continues to rise above the temperature target and exceeds a hardware-dependent critical threshold, the device will abort host commands to prevent component damage. The critical threshold values have a 5°C margin on top of the target threshold of 85°C.

Device temperature values used by the adaptive thermal monitoring feature are based on an internal temperature sensor located on the device PCB and may differ from case or package temperatures as measured by a thermocouple. Device temperature is accessible through SMART attribute 194, though usage of the SMART feature is not necessary for adaptive thermal monitoring functionality.

Adaptive thermal monitoring does not change the current negotiated speed of the SATA bus, nor require or cause any new commands to be issued on the SATA bus. Rated throughput performance is not guaranteed at any point above the maximum specified operating temperature.

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TCG/Opal Support

Table 9: TCG/Opal Support Parameters

Property	Supported?	Comments
TCG Storage Specifications		
OPAL: TCG Storage Security SubSystem Class	Specification 2.00	Revision 1.00, Feb 24, 2012
TCG Core Specification	Specification 2.00	Revision 2.00, Nov 4, 2011
TCG Storage Interface Interactions Specification	TCG Reference Specification	Specification Version 1.02 Revision 1.00 30 December, 2011
OPAL SSC 1.00 (backward compatibility)	Not supported	–
OPAL SSC Additional Feature Set Specification		
Additional DataStore Table	Supported	Specification 1.00 Revision 1.00, Feb 24, 2012
Single User Mode	Supported	Specification 1.00 Revision 1.00, Feb 24, 2012
TCG Storage Protection Mechanisms for Secrets	Supported	Specification Version 1.00 Revision 1.07 17 August, 2011
PSID – Physical Presence SID	Supported	Specification Version 1.00 Committee Draft Revision 1.05 February 9, 2011
GUDID (Globally Unique Serial Number)	Supported	Mandatory GUDID Proposal 11/03/2011 (Microsoft)
SID Authority Disable	Supported	SID Authority Disable Proposal 9/26/2011 (Microsoft)
Modifiable CommonName Columns	Supported	Modifiable CommonName Columns Proposal 7/22/2010 (Microsoft)
OPAL SSC Feature Set – Specific List		
ALL OPAL Mandatory Features	Supported	–
Close Session (optional)	Supported	Allows TPer to notify the host it has aborted a session
Restricted Command & Table (optional)	Not Supported	The interface control template enables TPer control over selected interface commands; the benefit is the reduction of undesired side effects
Type Table (not required)	Not Supported	–
Activate Method	Supported	–
Revert Method	Supported	–
Revert SP Method	Supported	–
Activate Method Within Transactions	Not Supported	As per OPAL, this behavior is out of the scope
Revert Method within Transactions	Not Supported	As per OPAL, this behavior is out of the scope
Revert SP Method within Transactions	Not Supported	As per OPAL, this behavior is out of the scope
Creation/Deletion of Tables/Rows after Manufacturing	Not Supported	As per OPAL, this behavior is out of the scope
TPer Feature		
COM ID Management Support	Not Supported	Dynamic COM ID allocation & management not supported
Buffer Management Support	Not Supported	Flow control

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Table 9: TCG/Opal Support Parameters (Continued)

Property	Supported?	Comments
ACK/NACK Support	Not Supported	Session reliability
Async Support	Not Supported	Asynchronous protocol support with multiple commands per session
Geometry Reporting Feature		
ALIGN	Supported	Alignment is not required
Logical Block Size	512 bytes	Logical block size = 512 bytes
Alignment Granularity	512 bytes	Logical block size = 512 bytes
Lowest Aligned LBA	0	–
OPAL SSC V2.00 Feature Descriptor		
Base COM ID	0x1000	0x1000-0xFFFF defined for COM ID management
Number of COM IDs	1	–
Range Crossing Behavior	0	If drive receives a READ or WRITE command that spans multiple LBA ranges and the LBA ranges are not locked, then: 1. Process the data transfer, if Range Crossing = 0 2. Terminate the command with "Other Invalid Command Parameter" if Range Crossing = 1
Number of Locking SP Admin Authorities Supported	4	As per OPAL 2.0, drive should support at least 4 admin
Number of Locking SP User Authorities Supported	16	As per OPAL 2.0, drive should support at least 8 users
Initial C_PIN_SID PIN Indicator	0x00	0x00 = The initial C_PIN_SID PIN value is equal to the C_PIN_MSID PIN value 0xFF = The initial C_PIN_SID PIN value is VU, and MAY not be equal to the C_PIN_MSID PIN value OPAL 2.0 (only) Customer-specific SID – Configurable
Behavior of C_PIN_SID PIN upon Ter Revert	0x00	0x00 = The C_PIN_SID PIN value becomes the value of the C_PIN_MSID PIN column after successful invocation of revert on the admin SP's object in the SP table 0xFF = The C_PIN_SID PIN value changes to a VU value after successful invocation of revert on the admin SP's object in the SP table and MAY not be equal to the C_PIN_MSID PIN value OPAL 2.0 (only)
DataStore Table Feature		
Maximum number of DataStore Tables	16	The maximum number of the DataStore tables that the TPer supports, including the DataStore table defined in OPAL SSC 2.0
Maximum total size of DataStore Tables	12MB	Specifies the maximum total size in bytes of all of the DataStore tables that TPer supports, including the DataStore table defined in OPAL SSC 2.0
MBR Table	128MB	–

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Table 9: TCG/Opal Support Parameters (Continued)

Property	Supported?	Comments
Byte Table Access Granularity		
Mandatory Write Granularity	1	TPer enforces when the host invokes the set method on byte tables; it should be less than or equal to 8192; it should be less than or equal to Recommended Access Granularity, OPAL 2.0 (only)
Recommended Access Granularity	8192	TPer recommends when the host invokes the set or get method on byte tables; it should be less than or equal to 8192
Cryptographic Features		
AES Key Size	256 Bits	AES key is generated by using CTR DRBG algorithm (FIPS Compliant)
AES Mode	XTS	IV swapped
Number of Ranges/Band Supported	16	Unique AES key per range/band; range crossing is allowed if the range is unlocked
Re-Encryption	Not Supported	–
Key Management		Cryptographic
Crypto Erase Completion Time <1s	Yes	–
Cryptographic Algorithms are Certified by FIPS-197	No	Designed to meet, no plans for certification
AES 256-Bit CBC/ECB Mode	Supported	ECB mode used only for generating the random key by CTR DRBG
CTR DRBG	Supported	–
SHA 256	Supported	–
RSA 2048 Signature Verification	Supported	–
TPer Communication Properties		
Max ComPacket Size	131072	256 sectors (128K)
Max Response ComPacket Size	131072	256 sectors (128K)
Max Packet Size	128512	–
Max Individual Token Size	123904	–
Max Packets	1	–
Max SubPackets	1	–
Max Sessions	1	Each session requires a set of buffers and variables
Max Transaction Limit	1	Transaction are inside sessions
Max Methods	1	Methods are contained in a transaction
Max Authentications	21	21 = 16 users + 4 admins + 1 anybody
Def Session Timeout	Yes	The session timeout length (in milliseconds) used by the TPer by default
IEEE1667		
Probe Silo	Supported	–
TCG Storage Silo	Supported	–

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Table 9: TCG/Opal Support Parameters (Continued)

Property	Supported?	Comments
Other than Probe and TCG Storage Silo	Not Supported	–
IEEE1667 Major Version	2	–
IEEE1667 Minor Version	0	–
Maximum P_OUT Transfer Size	131072	256 sectors (128K)
Others		
FDE (ATA Security with Key Management)	Yes	–
Secure Firmware Download	Supported	Firmware image is validated by using SHA256 and RSA2048 algorithm

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Device ID

Table 10: Identify Device

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
0				General configuration bit-significant information
	15	F	0b	0 = ATA device
	14–8	X	0000100b	Retired
	7	F	0b	Obsolete
	6	F	1b	Obsolete
	5–3	X	000b	Retired
	2	V	0b	Response incomplete
	1	X	0b	Retired
	0	F	0b	Reserved
1			3FFFh	Obsolete
2		F	C837h	Specific configuration
3		F	0010h	Obsolete
4		F	0000h 0000h	Retired
6		F	003Fh	Obsolete
7		(O)V	0000h 0000h	Reserved for assignment by the CompactFlash™ Association
9		X	0000h	Retired
10		(M)F	varies	Serial number (20 ASCII characters)
20		X	0000h 0000h 0000h	Retired/Obsolete
23		(M)F	varies	Firmware revision (8 ASCII characters)
27		(M)F	varies	Model number (40 ASCII characters)
47	15–8	F	80h	80h
	7–0	F	10h	00h = Reserved 01h-FFh = Maximum number of logical sectors that shall be transferred per DRQ data block on READ/WRITE MULTIPLE commands.
48				Trusted Computing feature set options
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–1	F	0000000000000b	Reserved for the Trusted Computing Group
	0	F	varies	1 = Trusted Computing feature set is supported This bit will be 1 for TCG drives, otherwise 0

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
49				Capabilities
	15–14	F	00b	Reserved for the IDENTIFY PACKET DEVICE command
	13	F	1b	1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device
	12	F	0b	Reserved for the IDENTIFY PACKET DEVICE command
	11	F	1b	1 = IORDY supported 0 = IORDY may be supported
	10	F	1b	1 = IORDY may be disabled.
	9	F	1b	1 = LBA supported
	8	F	1b	1 = DMA supported
	7–2	F	000000b	Retired
	1–0	F	00b	Long physical sector alignment error reporting
50				Capabilities
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–2	F	000000000000b	Reserved
	1	X	0b	Obsolete
	0	F	1b	Shall be set to one to indicate a vendor specific standby timer value minimum
51		X	0000h 0000h	Obsolete
53	15–8	F	00000000b	Free-fall control sensitivity
	7–3	F	00000b	Reserved
	2	F	1b	1 = The fields reported in word 88 are valid. 0 = The fields reported in word 88 are not valid.
	1	F	1b	1 = The fields reported in words (70:64) are valid. 0 = The fields reported in words (70:64) are not valid.
	0	X	1b	Obsolete
54		X	3FFFh 0010h 003Fh FC10h 00FBh	Obsolete

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
59	15	F	1b	1 = The BLOCK ERASE EXT command is supported.
	14	F	0b	1 = The OVERWRITE EXT command is supported.
	13	F	varies	1 = The CRYPTO SCRAMBLE EXT command is supported. This bit will be 1 for TCG drives, otherwise 0
	12	F	1b	1 = The Sanitize feature set is supported.
	11	F	0b	Commands allowed during a sanitize operation are as specified by ACS-2
	10	F	0b	SANITIZE ANTIFREEZE LOCK EXT command is supported
	9	F	0b	Reserved
	8	V	1b	1 = Multiple sector setting is valid.
	7–0	V	00010000b	xxh = Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE MULTIPLE commands
60–61		M(F)	Varies by capacity	Total number of user addressable logical sectors
62		X	0000h	Obsolete
63	15–11	F	00000b	Reserved
	10	V	0b	1 = Multiword DMA mode 2 is selected. 0 = Multiword DMA mode 2 is not selected.
	9	V	0b	1 = Multiword DMA mode 1 is selected. 0 = Multiword DMA mode 1 is not selected.
	8	V	0b	1 = Multiword DMA mode 0 is selected. 0 = Multiword DMA mode 0 is not selected.
	7–3	F	0000b	Reserved
	2	F	1b	1 = Multiword DMA mode 2 and below are supported.
	1	F	1b	1 = Multiword DMA mode 1 and below are supported.
	0	F	1b	1 = Multiword DMA mode 0 is supported.
64	15–2	F	00000000000000b	Reserved
	1–0	F	11b	PIO modes supported
65		F	0078h	Minimum Multiword DMA transfer cycle time per word Cycle time in nanoseconds
66		F	0078h	Manufacturer's recommended Multiword DMA transfer cycle time Cycle time in nanoseconds
67		F	0078h	Minimum PIO transfer cycle time without flow control Cycle time in nanoseconds
68		F	0078h	Minimum PIO transfer cycle time with IORDY flow control Cycle time in nanoseconds

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
69				Additional Supported
	15	F	0b	1 = CFast Specification Support
	14	F	1b	1 = Deterministic read after Trim is supported.
	13	F	0b	1 = Long Physical Sector Alignment Error Reporting Control is supported.
	12	F	0b	Obsolete
	11	F	1b	1 = READ BUFFER DMA is supported.
	10	F	1b	1 = WRITE BUFFER DMA is supported.
	9	F	0b	Obsolete
	8	F	1b	1 = DOWNLOAD MICROCODE DMA is supported.
	7	F	varies	1 = IEEE-1667 supported
	6	F	0b	1 = Optional ATA device 28-bit commands supported
	5	F	1b	1 = Read zero after Trim is supported
	4	F	Varies	1 = Device encrypts all user data
	3	F	1b	1 = Extended number of user addressable sectors is supported.
	2	F	0b	1 = All write cache is nonvolatile
	1–0	F	00b	Reserved
70		F	0000h	Reserved
71		F	0000h 0000h 0000h 0000h	Reserved for the IDENTIFY PACKET DEVICE command
75				Queue depth
	15–5	F	00000000000b	Reserved
	4–0	F	11111b	Maximum queue depth - 1

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
76				Serial ATA capabilities
	15	F	1b	1 = Supports READ LOG DMA EXT as equivalent to READ LOG EXT
	14	F	0b	1 = Supports device automatic partial to slumber transitions
	13	F	0b	1 = Supports host automatic partial to slumber transitions
	12	F	1b	Supports Native Command Queuing priority information
	11	F	0b	Supports Unload while NCQ commands outstanding
	10	F	1b	Supports Phy event counters
	9	F	0b	Supports receipt of host initiated interface power management requests
	8	F	1b	Supports Native Command Queueing
	7–4	F	0000b	Reserved for Serial ATA
	3	F	1b	1 = Supports Serial ATA Gen-3 speed (6.0 Gb/s)
	2	F	1b	1 = Supports Serial ATA Gen-2 speed (3.0 Gb/s)
	1	F	1b	1 = Supports Serial ATA Gen-1 speed (1.5 Gb/s)
	0	F	0b	Reserved (set to 0)
77				Serial ATA additional capabilities
	15–8	F	00000000b	Reserved for future Serial ATA definition
	7	F	1b	1 = Supports DEVSLP_to_ReducedPwrState
	6	F	1b	Supports RECEIVE FPDMA QUEUED and SEND FPDMA QUEUED commands
	5	F	0b	Supports NCQ Queue Management Command
	4	F	0b	Supports NCQ Streaming
	3–1	V	Varies	Coded value indicating current negotiated Serial ATA signal speed
	0	F	0b	Shall be cleared to zero

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
78				Serial ATA features supported
	15–12	F	0000b	Reserved
	11	F	0b	1 = Supports Rebuild Assist
	10	F	0b	1 = Supports Device Initiated Interface Power Management Software Settings Preservation
	9	F	0b	1 = Supports Hybrid Information
	8	F	1b	1 = Device sleep supported
	7	F	0b	1 = Supports NCQ Autosense
	6	F	1b	1 = Supports software settings preservation
	5	F	0b	1 = HARDWARE FEATURE CONTROL SUPPORTED bit
	4	F	0b	1 = Supports in-order data delivery
	3	F	1b	1 = Supports device initiate interface power management
	2	F	1b	1 = Supports DMA Setup Auto-Activate optimization
	1	F	0b	1 = Supports non-zero buffer offsets in DMA Setup FIS
	0	F	0b	Reserved (set to 0)
79				Serial ATA features enabled
	15–12	V	0000b	Reserved
	11	V	0b	1 = Rebuild Assist enabled
	10	V	0b	Reserved
	9	V	0b	1 = Hybrid Information feature is enabled
	8	V	0b	1 = Device sleep enabled
	7	V	0b	1 = Device automatic partial to slumber transitions enabled
	6	V	1b	1 = Software settings preservation enabled
	5	V	0b	1 = Hardware feature control is enabled
	4	V	0b	1 = In-order data delivery enabled
	3	V	0b	1 = Device initiating interface power management enabled
	2	V	0b	1 = DMA Setup Auto-Activate optimization enabled
	1	V	0b	1 = Non-zero buffer offsets in DMA Setup FIS enabled
	0	V	0b	Reserved (set to 0)

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
80				Major revision number
	15–11	F	00000b	Reserved
	10	F	1b	1 = Supports ACS-3
	9	F	1b	1 = Supports ATA8-ACS2
	8	F	1b	1 = Supports ATA8-ACS
	7	F	1b	1 = Supports ATA/ATAPI-7
	6	F	1b	1 = Supports ATA/ATAPI-6
	5	F	1b	1 = Supports ATA/ATAPI-5
	4	F	1b	Obsolete
	3	F	1b	Obsolete
	2	S	0b	Obsolete
	1	S	0b	Obsolete
	0	F	0b	Reserved
81		F	006Dh	Minor revision number
				006Dh = ACS-3 version 5
82				Command set supported
	15	X	0b	Obsolete
	14	F	1b	1 = NOP command supported
	13	F	1b	1 = READ BUFFER command supported
	12	F	1b	1 = WRITE BUFFER command supported
	11	X	0b	Obsolete
	10	X	0b	Obsolete
	9	F	0b	1 = DEVICE RESET command supported
	8	F	0b	Obsolete
	7	F	0b	Obsolete
	6	F	1b	1 = Read look-ahead supported
	5	F	1b	1 = Write cache supported
	4	F	0b	Shall be cleared to zero to indicate that the PACKET feature set is not supported.
	3	F	1b	1 = Mandatory Power Management feature set supported
	2	F	0b	Obsolete
	1	F	1b	1 = Security feature set supported
	0	F	1b	1 = SMART feature set supported

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
83				Command set supported
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	1b	1 = FLUSH CACHE EXT command supported
	12	F	1b	1 = Mandatory FLUSH CACHE command supported
	11	X	0b	Obsolete
	10	F	1b	1 = 48-bit address feature set supported
	9	F	0b	Obsolete
	8	X	0b	Obsolete
	7	F	0b	Obsolete
	6	F	0b	1 = SET FEATURES subcommand required to spin-up after power-up
	5	F	0b	1 = Power-Up In Standby feature set supported
	4	F	0b	Obsolete
	3	F	varies	1 = Advanced Power Management feature set supported
	2	F	0b	1 = CFA feature set supported
	1	F	0b	Obsolete
	0	F	1b	1 = DOWNLOAD MICROCODE command supported
84				Command set/feature supported extension
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	1b	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
	12	F	0b	Obsolete
	11	F	0b	Obsolete
	10–9	F	00b	Obsolete
	8	F	1b	1 = 64-bit word wide name supported
	7	F	0b	Obsolete
	6	F	1b	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported
	5	F	1b	1 = General Purpose Logging feature set supported
	4	F	0b	1 = Streaming feature set supported
	3	F	0b	Obsolete
	2	F	0b	Reserved
	1	F	1b	1 = SMART self-test supported
	0	F	1b	1 = SMART error logging supported

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
85				Command set/feature enabled.
	15	X	0b	Obsolete
	14	F	1b	1 = NOP command supported
	13	F	1b	1 = READ BUFFER command supported
	12	F	1b	1 = WRITE BUFFER command supported
	11	X	0b	Obsolete
	10	X	0b	Obsolete
	9	F	0b	1 = DEVICE RESET command supported
	8	V	0b	Obsolete
	7	V	0b	Obsolete
	6	V	1b	1 = Read look-ahead enabled
	5	V	1b	1 = Write cache enabled
	4	F	0b	Shall be cleared to zero to indicate that the PACKET feature set is not supported.
	3	F	1b	Power Management feature set is supported
	2	F	0b	Obsolete
	1	V	0b	1 = Security Mode feature set enabled
	0	V	1b	1 = SMART feature set enabled
86				Command set/feature enabled.
	15	F	1b	1 = Words 120-119 are valid
	14	F	0b	1 = Reserved
	13	F	1b	1 = FLUSH CACHE EXT command supported
	12	F	1b	1 = FLUSH CACHE command supported
	11	X	0b	Obsolete
	10	F	1b	1 = 48-bit Address features set supported
	9	V	0b	Obsolete
	8	F	0b	Obsolete
	7	F	0b	Obsolete
	6	F	0b	1 = SET FEATURES subcommand required to spin-up after power-up
	5	V	0b	1 = Power-Up In Standby feature set enabled
	4	V	0b	Obsolete
	3	V	1b	1 = Advanced Power Management feature set enabled
	2	F	0b	1 = CFA feature set supported
	1	F	0b	Obsolete
	0	F	1b	1 = DOWNLOAD MICROCODE command supported

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
87				Command set/feature enabled/supported
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	1b	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported
	12	V	0b	Obsolete
	11	V	0b	Obsolete
	10–9	F	00b	Obsolete
	8	F	1b	1 = 64-bit word wide name supported
	7	F	0b	Obsolete
	6	F	1b	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported
	5	F	1b	1 = General Purpose Logging feature set supported
	4	V	0b	Obsolete
	3	V	0b	Obsolete
	2	V	0b	1 = Media serial number is valid
	1	F	1b	1 = SMART self-test supported
	0	F	1b	1 = SMART error logging supported

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
88				Ultra DMA modes
	15		0b	Reserved
	14		0b	1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected
	13		0b	1 = Ultra DMA mode 5 is selected 0 = Ultra DMA mode 5 is not selected
	12		0b	1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected
	11		0b	1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected
	10		0b	1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected
	9		0b	1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected
	8		0b	1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected
	7		0b	Reserved
	6		1b	1 = Ultra DMA mode 6 and below are supported
	5		1b	1 = Ultra DMA mode 5 and below are supported
	4		1b	1 = Ultra DMA mode 4 and below are supported
	3		1b	1 = Ultra DMA mode 3 and below are supported
	2		1b	1 = Ultra DMA mode 2 and below are supported
	1		1b	1 = Ultra DMA mode 1 and below are supported
	0		1b	1 = Ultra DMA mode 0 IS supported
89		(O)F	0001h	Time required for security erase unit completion
90		(O)F	0001h	Time required for enhanced security erase completion
91		(O)V	00FEh	Current advanced power management value
92		(O)V	FFFEh	Master Password Identifier
93		F	0000h	Shall be 0000h for SATA devices
94		F	0000h	Obsolete
95		(O)V	0000h	Stream Minimum Request Size
96		(O)V	0000h	Streaming Transfer Time – DMA
97		(O)V	0000h	Streaming Access Latency – DMA and PIO
98		(O)F	0000h 0000h	Streaming Performance Granularity (98-99)
100		V	Varies by capacity	Maximum user LBA for 48-bit Address feature set
104		(O)V	0000h	Streaming Transfer Time – PIO
105		F	0008h	Maximum number of 512-byte blocks of LBA Range Entries per DATA SET MANAGEMENT command

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
106				Physical sector size/logical sector size
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13	F	0b	1 = Device has multiple logical sectors per physical sector
	12	F	0b	1 = Device logical sector longer than 256 words
	11–4	F	00000000b	Reserved
	3–0	F	0000b	2^x logical sectors per physical sector
107		(O)F	0000h	Inter-seek delay for ISO-7779 acoustic testing in microseconds
108	15–12	F	0101b	NAA (3-0)
	11–0		000000001010b	IEEE OUI (23-12)
109	15–4	F	000001110101b	IEEE OUI (11-0)
	3–0		Varies	Unique ID (35-32)
110		(M)F	Varies	5-0 Unique ID (31-16)
111		(M)F	Varies	Unique ID (15-0)
112		(O)F	0000h 0000h 0000h 0000h	Reserved for 12- bit word-wide name extension to 128 bits
116		(O)	0000h	Obsolete
117		(O)F	0000h 0000h	Words per Logical Sector
119				Commands and feature sets supported (continued from words 84–82)
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–10	F	0000b	Reserved
	9	F	0b	1 = DSN feature set is supported
	8	F	1b	1 = Accessible Max address configuration feature set is supported
	7	F	0b	1 = Extended Power Conditions feature set is supported
	6	F	0b	1 = Sense Data Reporting feature set is supported
	5	F	0b	1 = Free-fall control feature set is supported
	4	F	1b	1 = The DOWNLOAD MICROCODE command with mode 3 is supported
	3	F	1b	1 = READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported
	2	F	1b	1 = The WRITE UNCORRECTABLE EXT command is supported
	1	F	1b	1 = The Write-Read-Verify feature set is supported
	0	F	0b	Obsolete

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
120				Commands and feature sets supported or enabled (continued from words 87–85)
	15		0b	Shall be cleared to zero
	14		1b	Shall be set to one
	13–10		0000b	Reserved
	9		0b	1 = DSN feature set is enabled
	8		0b	Reserved
	7		0b	1 = EPC feature set is enabled
	6		0b	1 = Sense Data Reporting feature set is enabled
	5		0b	1 = Free-fall control feature set is enabled
	4		1b	1 = The DOWNLOAD MICROCODE command with mode 3 is supported
	3		1b	1 = The READ LOG DMA EXT and WRITE LOG DMA EXT commands are supported
	2		1b	1 = The WRITE UNCORRECTABLE EXT command is supported
	1		0b	1 = The Write-Read-Verify feature set is enabled
	0		0b	Obsolete
121		F	0000h 0000h 0000h 0000h 0000h 0000h	Reserved for expanded supported and enabled settings
127		(O)	0000h	Obsolete
128				Security status
	15–9	F	0000000b	Reserved
	8	V	0b	Security level 0 = High, 1 = Maximum
	7–6	F	00b	Reserved
	5	F	1b	1 = Enhanced security erase supported
	4	V	0b	1 = Security count expired
	3	V	0b	1 = Security frozen
	2	V	0b	1 = Security locked
	1	V	0b	1 = Security enabled
	0	F	1b	1 = Security supported
129–159		X	Vendor specific data	Vendor specific
160		X	0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h	Reserved for assignment by the CompactFlash Association
168	15–4	F	000h	Reserved
	3-0	F	Varies	Device Nominal Form Factor

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
169				DATA SET MANAGEMENT command support
	15–1	F	000000000000000b	Reserved
	0	F	1b	1 = The Trim bit in the DATA SET MANAGEMENT command is supported
170		F	0000h 0000h 0000h 0000h	Additional product identifier
174		F	0000h 0000h	Reserved
176		(O)V	Varies	Current media serial number (60 ASCII characters)
206				SCT Command Transport
	15–12	X	0000b	Vendor-specific
	11–6	F	000000b	Reserved
	5	F	1b	SCT Command Transport Data Tables supported
	4	F	1b	SCT Command Transport Features Control supported
	3	F	0b	SCT Command Transport Error Recovery Control supported
	2	F	1b	SCT Command Transport Write Same supported
	1	F	0b	Obsolete
	0	F	1b	SCT Command Transport supported
207		F	0000h 0000h	Reserved for CE-ATA
209		(O)		Alignment of logical blocks within a larger physical block
	15	F	0b	Shall be cleared to zero
	14	F	1b	Shall be set to one
	13–0	F	00000000000000b	Logical sector offset within the first physical sector where the first logical sector is placed
210		(O)V	0000h 0000h	Write-Read-Verify Sector Count Mode 3 Only
212		(O)F	0000h 0001h	Verify Sector Count Mode 2 Only
214		(O)	0000h	Obsolete
215		(O)V	0000h	Obsolete
216		(O)V	0000h	Obsolete
217		(M)F	0001h	Nominal media rotation rate (ATA8-ACS 1699-D Revision 6)
218		(O)V	0000h	Reserved
219				Obsolete
220	15–8	F	00h	Reserved
	7–0	V	00h	Write-Read-Verify feature set current mode
221			0000h	Reserved

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
222				Transport Major revision number. 0000h or FFFFh = device does not report version
	15–12		0001b	Transport Type - 0 = Parallel, 1 = Serial, 2-15 = Reserved Parallel (Type = 0) Serial (Type = 1)
	11–8		0000b	Reserved
	7		1b	Supports SATA Rev 3.2
	6		1b	Supports SATA Rev 3.1
	5		1b	Supports SATA Rev 3.0
	4		1b	Supports SATA Rev 2.6
	3		1b	Supports SATA Rev 2.5
	2		1b	Supports SATA II: Extensions
	1		1b	Supports SATA 1.0a
	0		1b	Supports ATA8-APT ATA8-AST
223		(M)F	0000h	Transport Minor revision number
224		F	0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h	Reserved for CE-ATA
230-233			Varies	Extended number of user addressable sectors
234		(O)F	0001h	Minimum number of 512 byte units per DOWNLOAD MICRO-CODE command for mode 3
235			00FFh	Maximum number of 512 byte units per DOWNLOAD MICRO-CODE command for mode 3
236			0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h	Reserved
243	15		0b	Reserved
	14		varies	Bit 14 = 1 Supports FDE security features
	13-0		00000000000000b	Reserved
244			0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h 0000h	Reserved

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Table 10: Identify Device (Continued)

See Note 1 for setting definitions

Word	Bit(s)	Setting	Default Value	Description
255		(M)F		Integrity word
	15–8		Varies	Checksum
	7–0		A5h	Signature

Note: 1. F = The content of the word is fixed and does not change.
V = The content of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = The content of the word may be fixed or variable.
R = The content of the word is reserved and will be zero.
M = Support of the word is mandatory.
O = Support of the word is optional.

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Commands

Table 11: Supported ATA Command Set

See ACS-3 standard for command details

Command Name	Command Code (hex)
AMAC-GET NATIVE MAX ADDRESS EXT	78h/0000h
AMAC-SET ACCESSIBLE MAX ADDRESS EXT	78h/0001h
AMAC-FREEZE ACCESSIBLE MAX ADDRESS EXT	78h/0002h
CHECK POWER MODE	98h or E5h
DATA SET MANAGEMENT – TRIM	06h/0001h
DOWNLOAD MICROCODE	92h
DOWNLOAD MICROCODE DMA	93h
EXECUTE DEVICE DIAGNOSTIC	90h
FLUSH CACHE	E7h
FLUSH CACHE EXT	EAh
IDENTIFY DEVICE	ECh
IDLE	E3h or 97h
IDLE IMMEDIATE	E1h or 95h
INITIALIZE DEVICE PARAMETERS	91h
READ BUFFER	E4h
READ DMA (with retry)	C8h
READ DMA (without retry)	C9h
READ DMA EXT	25h
READ FPDMA QUEUED	60h
READ LOG EXT	2Fh
READ MULTIPLE	C4h
READ MULTIPLE EXT	29h
READ SECTOR(S) EXT	24h
READ SECTOR(S) (with retry)	20h
READ SECTOR(S) (without retry)	21h
READ VERIFY SECTOR(S) EXT	42h
READ VERIFY SECTOR(S) (with retry)	40h
READ VERIFY SECTOR(S) (without retry)	41h
RECEIVE FPDMA QUEUED	65h
SANITIZE DEVICE	B4h
SCT WRITE SAME	02h/0001h 02h/0002h 02h/0101h 02h/0102h
SCT SET FEATURE CONTROL	04h/01h
SCT RETURN FEATURE CONTROL	04h/02h
SCT RETURN FEATURE OPTION FLAG	04h/03h

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Table 11: Supported ATA Command Set (Continued)

See ACS-3 standard for command details

Command Name	Command Code (hex)
SCT RETURN SCT DATA TABLE	05h/01h
SECURITY DISABLE PASSWORD	F6h
SECURITY ERASE PREPARE	F3h
SECURITY ERASE UNIT	F4h
SECURITY FREEZE LOCK	F5h
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SEND FPDMA QUEUED	64h
SET FEATURES	EFh
SET MULTIPLE MODE	C6h
SLEEP	E6h or 99h
SMART DISABLE OPERATIONS	B0h/D9h
SMART ENABLE OPERATIONS	B0h/D8h
SMART ENABLE/DISABLE AUTOSAVE	B0h/D2h
SMART EXECUTE OFF-LINE IMMEDIATE	B0h/D4h
SMART READ DATA	B0h/D0h
SMART READ LOG	B0h/D5h
SMART RETURN STATUS	B0h/DAh
SMART WRITE LOG	B0h/D6h
STANDBY	E2h or 96h
STANDBY IMMEDIATE	E0h or 94h
TRUSTED NON-DATA	5Bh
TRUSTED RECEIVE	5Ch
TRUSTED RECEIVE DMA	5Dh
TRUSTED SEND	5Eh
TRUSTED SEND DMA	5Fh
WRITE BUFFER	E8h
WRITE DMA (with retry)	CAh
WRITE DMA (without retry)	CBh
WRITE DMA EXT	35h
WRITE DMA FUA EXT	3Dh
WRITE FPDMA QUEUED	61h
WRITE LOG EXT	3Fh
WRITE MULTIPLE	C5h
WRITE MULTIPLE EXT	39h
WRITE MULTIPLE FUA EXT	CEh
WRITE SECTOR(S) (with retry)	30h

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Table 11: Supported ATA Command Set (Continued)

See ACS-3 standard for command details

Command Name	Command Code (hex)
WRITE SECTOR(S) EXT	34h
WRITE UNCORRECTABLE EXT	45h

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Interface Connectors

2.5" 7 mm

Figure 3: 2.5" 7 mm SSD Interface Connections

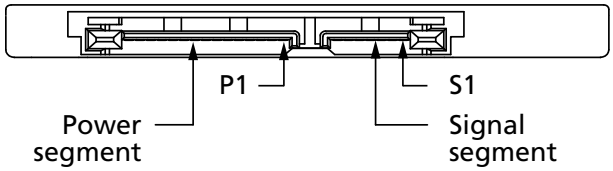

Table 12: SATA Signal Segment Pin Assignments

Signal Name	Type	Description
S1	GND	Ground
S2	A	Differential signal pair A and A#
S3	A#	
S4	GND	Ground
S5	B#	Differential signal pair B and B#
S6	B	
S7	GND	Ground

Table 13: 2.5-Inch SATA Power Segment Pin Assignments

Pin#	Signal Name	Description
P1	RETIRED	No connect
P2	RETIRED	No connect
P3	DEVSLP	Device sleep
P4	GND	Ground
P5	GND	Ground
P6	GND	Ground
P7	V5	5V power, precharge
P8	V5	5V power
P9	V5	5V power
P10	GND	Ground
P11	DAS	Device activity signal
P12	GND	Ground
P13	V12	No connect
P14	V12	No connect
P15	V12	No connect

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M.2 2280

Figure 4: M.2 2280 SSD Interface Connections

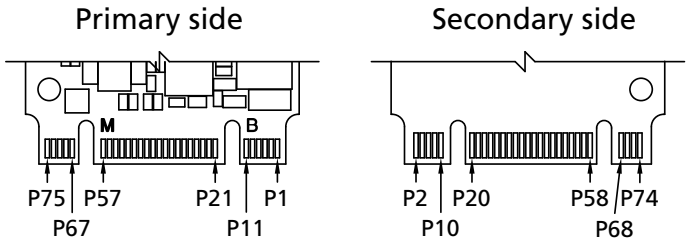

Table 14: M.2 2280 Signal Assignments

Primary Side			Secondary Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
1	CONFIG_3	Ground	2	3V3	3.3V
3	GND	Ground	4	3V3	3.3V
5	NC	No connect	6	NC	No connect
7	NC	No connect	8	NC	No connect
9	NC	No connect	10	DAS/DSS	Drive activity (host LED)
11	NC	No connect	Key		
Key			20	NC	No connect
21	CONFIG_0	Ground	22	NC	No connect
23	NC	No connect	24	NC	No connect
25	NC	No connect	26	NC	No connect
27	GND	Ground	28	NC	No connect
29	NC	No connect	30	NC	No connect
31	NC	No connect	32	NC	No connect
33	GND	Ground	34	NC	No connect
35	NC	No connect	36	NC	No connect
37	NC	No connect	38	DEVSLP	Device sleep
39	GND	Ground	40	NC	No connect
41	SATA +B	SATA B differential pair	42	NC	No connect
43	SATA -B		44	NC	No connect
45	GND	Ground	46	NC	No connect
47	SATA -A	SATA A differential pair	48	NC	No connect
49	SATA +A		50	NC	No connect
51	GND	Ground	52	NC	No connect
53	NC	No connect	54	NC	No connect
55	NC	No connect	56	Reserved	Vendor use
57	GND	Ground	58	Reserved	Vendor use
Key			Key		

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Table 14: M.2 2280 Signal Assignments (Continued)

Primary Side			Secondary Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
67	NC	No connect	68	Reserved	No connect
69	CONFIG_1	Ground	70	3V3	3.3V
71	GND	Ground	72	3V3	3.3V
73	GND	Ground	74	3V3	3.3V
75	CONFIG_2	Ground			

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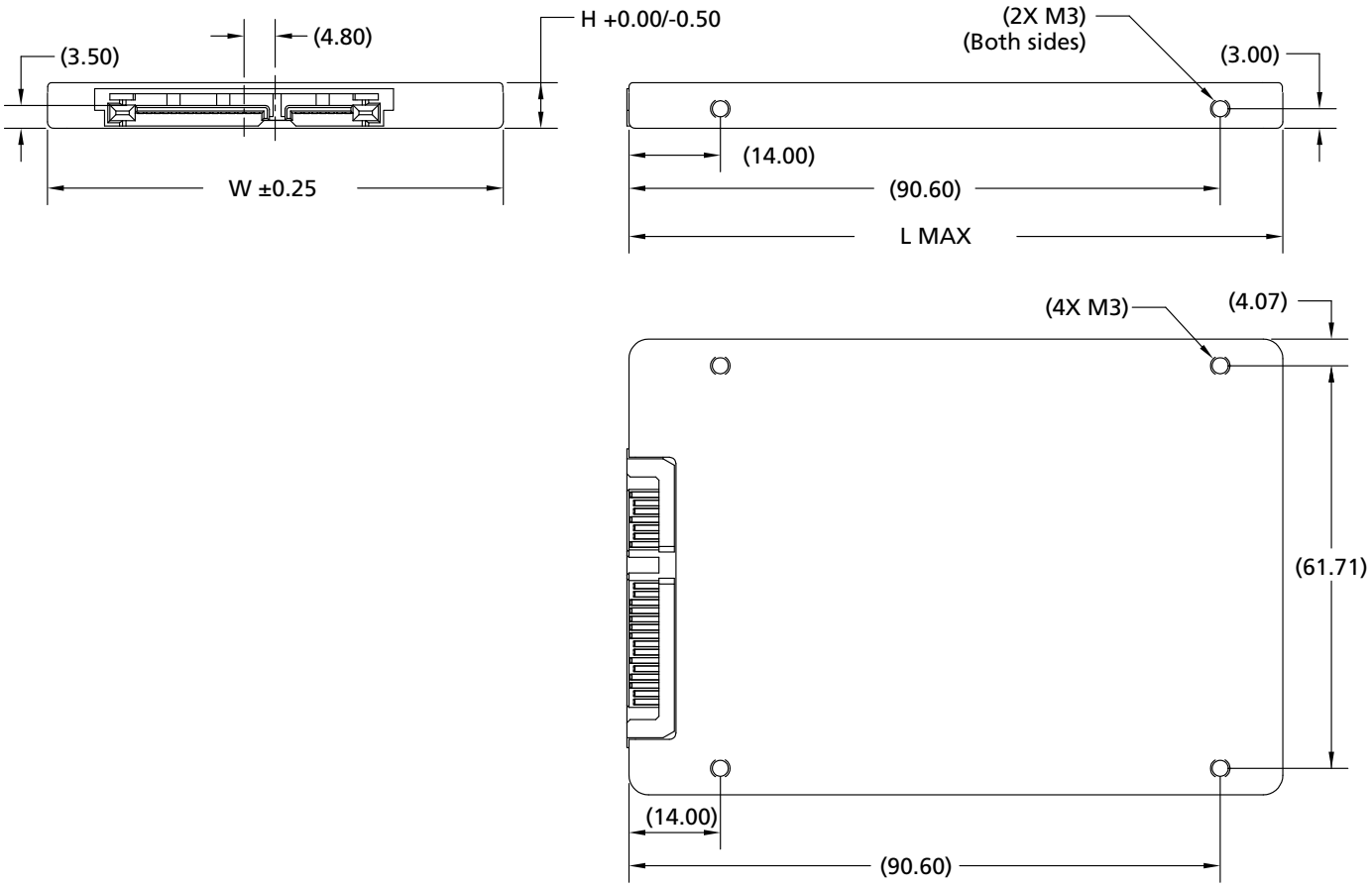
Physical Configuration

2.5" 7 mm

Product mass: 56 grams MAX

Physical dimensions conform to the applicable form factor specifications as listed in the figure below.

Figure 5: 2.5-Inch Package – 7mm



Note: 1. All dimensions are in millimeters.

Table 15: 2.5-Inch Package Dimensions

Density (GB)	W	L	H	Unit
256	69.85	100.45	7.00	mm
512				
1024				
2048				

Note: 1. Dimension values in millimeter per SFF 8201 Rev. 2.7.

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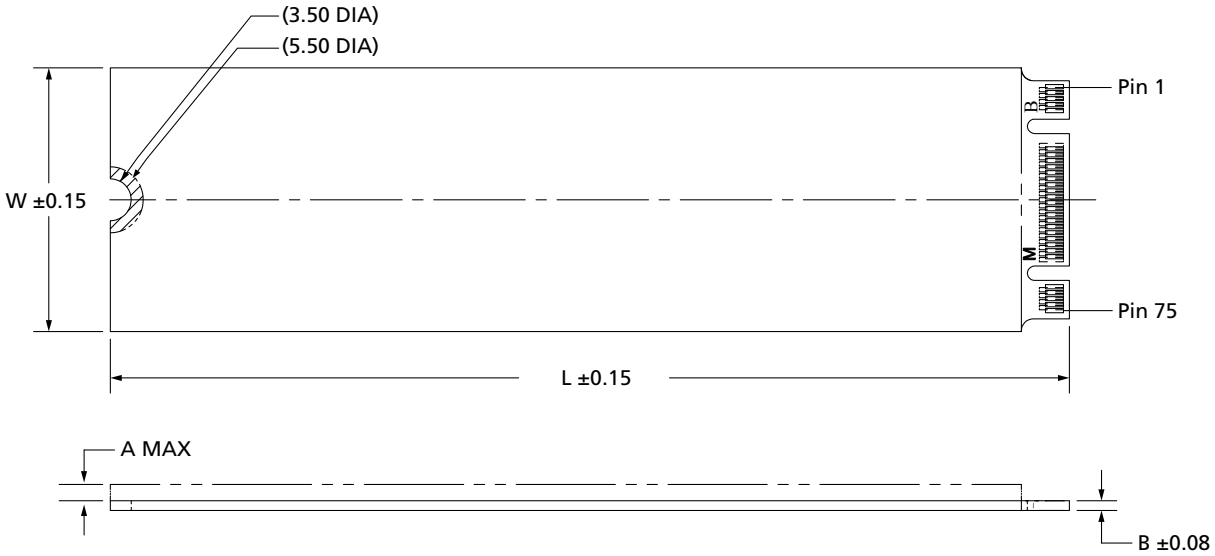
M.2 2280

Product mass: 10 grams MAX

Physical dimensions conform to the applicable form factor specifications as listed in the figure below.

Figure 6: M.2 Type 2280 Package



Note: 1. All dimensions are in millimeters.

Table 16: M.2 Type 2280 Package Dimensions

Density (GB)	Specification	W	L	A	B	Unit
256	S2	22.00	80.00	1.35	0.80	mm
512						
1024	S3			1.50		

Note: 1. M.2 2280 dimension values in millimeter per PCI Express M.2 Specification Rev. 1.0.

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Compliance

Micron SSDs comply with the following:

- Micron Green Standard
- Built with sulfur resistant resistors
- CE (Europe): EN 55032 Class B, RoHS
- FCC: CFR Title 47, Part 15 Class B
- UL/cUL: approval to UL-60950-1, 2nd Edition, IEC 60950-1:2005 (2nd Edition); EN 60950-1 (2006) + A11:2009+ A1:2010 + A12:2011 + A2:2013
- BSMI (Taiwan): approval to CNS 13438 Class B and CNS 15663
- RCM (Australia, New Zealand): AS/NZS CISPR32 Class B
- KC RRL (Korea): approval to KN32 Class B, KN 35 Class B

  B 급 기기 (가정용 정보통신기기) 이 기기는 가정용으로 전자파적합등록을한 기기로서 주거 지역에서는 물론 모든지역에서 사용할 수 있습니다.

- W.E.E.E.: compliance with EU WEEE directive 2012/19/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced.
- TUV (Germany): approval to IEC60950/EN60950
- VCCI (Japan): 2015-04 Class B

  この装置は、クラス B 情報技術装置です。この装置は、家庭環境で使用することを目的としていますが、この装置がラジオやテレビジョン受信機に近接して使用されると、受信障害を引き起こすことがあります。
  取扱説明書に従って正しい取り扱いをして下さい。
  VCCI－B

- IC (Canada): ICES-003 Class B
  - This Class B digital apparatus complies with Canadian ICES-003.
  - Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.

FCC Rules

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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References

- Serial ATA: High-speed serialized AT attachment, Serial ATA working group, available at www.sata-io.org
- SATA 3.2 GOLD
- ATA-8 ACS3 (T13/2161-D, Revision 5)
- TCG Storage Security Subsystem Class Opal; Specification 2.00 Revision 1.00, Feb 24, 2012
- TCG Core Specification; Specification 2.00 Revision 2.00, Nov 4, 2011
- TCG Storage Interface Interactions: Specification Version 1.02 Revision 1.00 30 December, 2011
- IEEE-1667: "Standard Protocol for Authentication in Host Attachments of Transient Storage Devices"
- SFF 8201 Rev 2.7: For form factor
- PCI Express M.2 Specification rev 1.0: For form factor
- Trade Agreements Act of 1979 (19 U.S.C. 2501)

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Revision History

Rev. D – 10/17

- Updated the certifications list
- Updated Table 10, Word 83 to reflect both APM ON & OFF available options

Rev. C – 12/16

- Added TAA Compliant option
- Updated pin names for M.2 in Table 14

Rev. B – 5/16

- Updated random 4KB read IOPS
- Updated Adaptive Thermal Monitoring, TCG/Opal Support and Device ID sections
- Updated doc ID number
- Misc. documentation edits

Rev. A – 12/15

- Initial release

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