ASL1507SHN; ASL2507SHN

Single-phase and two-phase boost converter with limp-home mode

Rev. 1 — 26 April 2018 Product data sheet

1 Introduction

The ASL1507SHN is a highly integrated and flexible one-phase DC-to-DC boost converter IC. The IC has one integrated gate driver which can drive one external power metal-oxide-semiconductor field-effect transistor (MOSFET) and two integrated proportional-integral (PI) controllers which can regulate the output voltage. It has a serial peripheral interface (SPI) allowing control and diagnostic communication with an external microcontroller.

The ASL2507SHN is a highly integrated and flexible two-phase DC-to-DC boost converter IC. The IC has two integrated gate drivers which can drive two external power metal-oxide-semiconductor field-effect transistors (MOSFETs) and two integrated proportional-integral (PI) controllers which can regulate the output voltage on both channels. It has a serial peripheral interface (SPI) allowing control and diagnostic communication with an external microcontroller.

The ASL1507SHN; ASL2507SHN is designed primarily for use in automotive LED lighting applications and provides an optimized supply voltage for ASLx416/17SHN multichannel LED buck driver.

For simplicity, the data sheet states always 'gate drivers' and 'output voltages'. The ASL1507SHN has only one gate driver and can only drive one output.

2 General description

The ASL1507SHN; ASL2507SHN has a fixed frequency peak current mode control with parabolic/non-linear slope compensation. It can operate with input voltages from 5.5 V to 40 V. It can be configured in boost topology via SPI for output voltages of up to 80 V, to power the LED buck driver IC.

The ASL1507SHN is a single-phase boost converter with one output voltage. The ASL2507SHN is a two-phase boost converter, which can have two independent outputs. The ASL2507SHN is configurable via the SPI interface, as a single output converter with either one phase or two phases, or two independent output voltages. In case the SPI communication is lost in an abnormal situation, it switches to limp-home mode operation ensuring system safety.

The ASL1507SHN; ASL2507SHN boost converter can drive up to two external low-side N channel MOSFETs from an internally regulated adjustable supply. It can drive either logic or standard level MOSFETs.

The integrated SPI interface also allows for programming the supply under/overvoltage range, output voltage range, frequency spread spectrum, and DC-to-DC switching frequency. It enables the optimization of external components and flexibility for electromagnetic compatibility (EMC) design. This interface can be used also to provide diagnostic information such as the device temperature, battery voltage, VGG voltage, output voltage etc.

The ASL1507SHN; ASL2507SHN integrates a non-volatile memory (NVM) to save the default configuration internally. The configuration includes boost ramp-up, boost voltage, frequency setting, error detection and etc. The default configuration is used in limp-home mode (SPI fail) and autonomous mode (no MCU). Additional features include input undervoltage lockout and thermal shutdown when the junction temperature of the ASL1507SHN; ASL2507SHN exceeds $T_{sd(otp)}$.

The device is housed in a very small HVQFN32 package with an exposed thermal pad. It is designed to meet the stringent requirements of automotive applications. It is fully AEC-Q100 grade 1 qualified. It operates over the −40 °C to +125 °C ambient automotive temperature range.

3 Features and benefits

- AEC-Q100 grade 1 qualified
- Limp-home mode ensuring system safety
- Up to two flexible output voltages with 3 % accuracy programmable via SPI
- Single phase on each output or double phase on one output
- Fixed frequency operation via built-in oscillator from 125 kHz to 700 kHz
- Slope compensation to track the frequency and output voltage
- Programmable control loop compensation
- Programmable spread spectrum functionality
- Gate switching is halted when overvoltage on output is detected
- Programmable gate voltage
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI)
- Output voltage monitoring
- Supply voltage measurement
- Control signal to enable the device low quiescent current < 5 µA when EN = 0
- Read-back programmed voltage and frequency range via SPI
- Junction temperature monitoring via SPI
- Small package outline HVQFN32
- Wide operating input voltage range from +5.5 V to +40 V
- Operating ambient temperature range of −40 °C to +125 °C

4 Applications

- Automotive LED lighting
  - Daytime running lights
  - Position or park light
  - Low beam
  - High beam
  - Turn indicator
  - Fog light
  - Cornering light

5 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
ASL1507SHN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-12
ASL2507SHN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-12

6 Block diagram

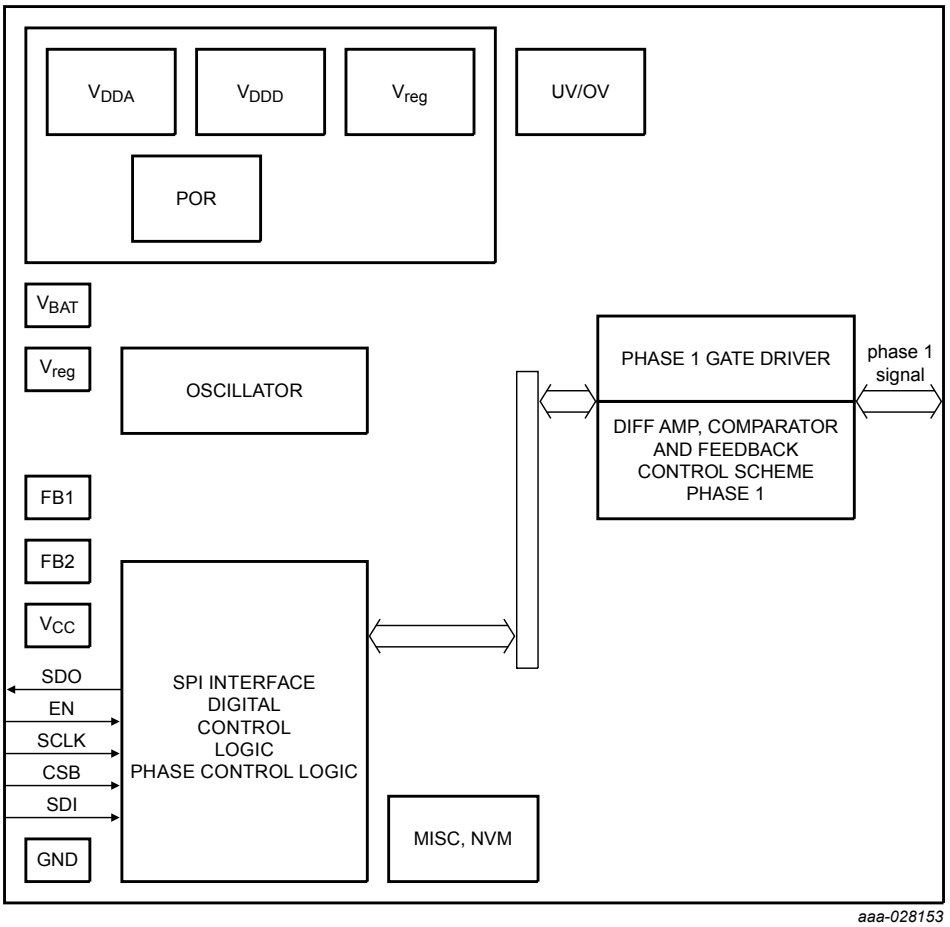


Figure 1. Block diagram for ASL1507SHN

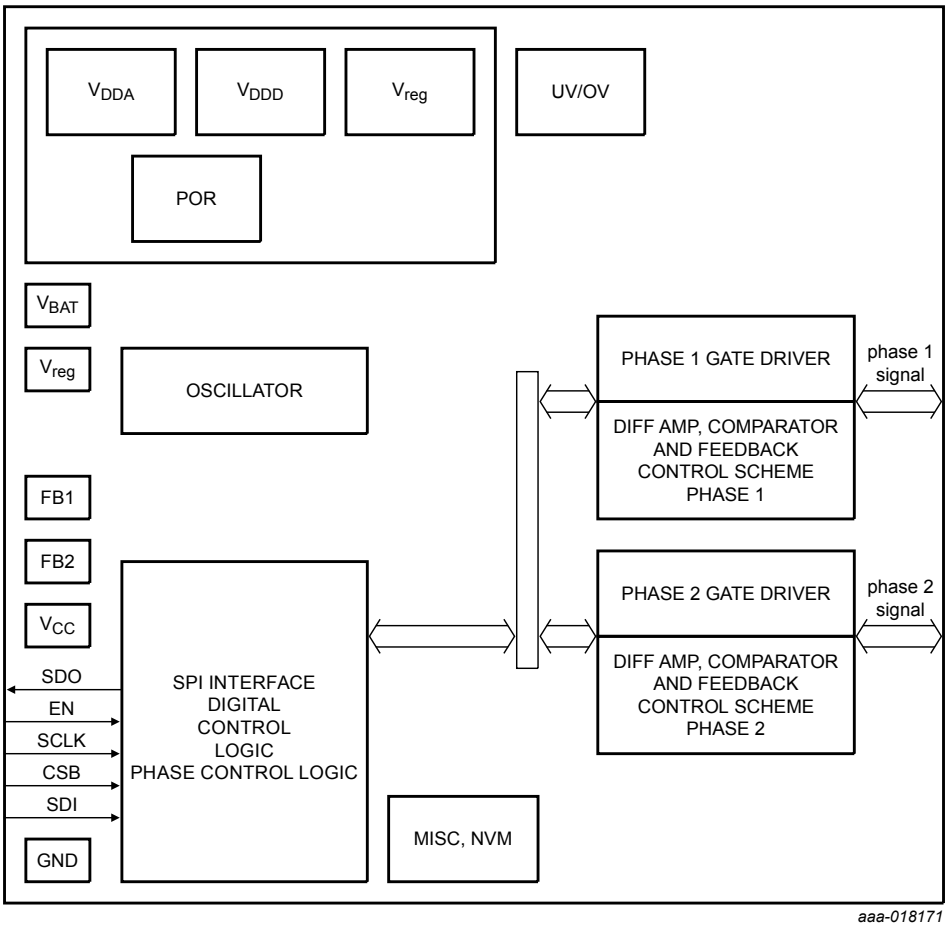
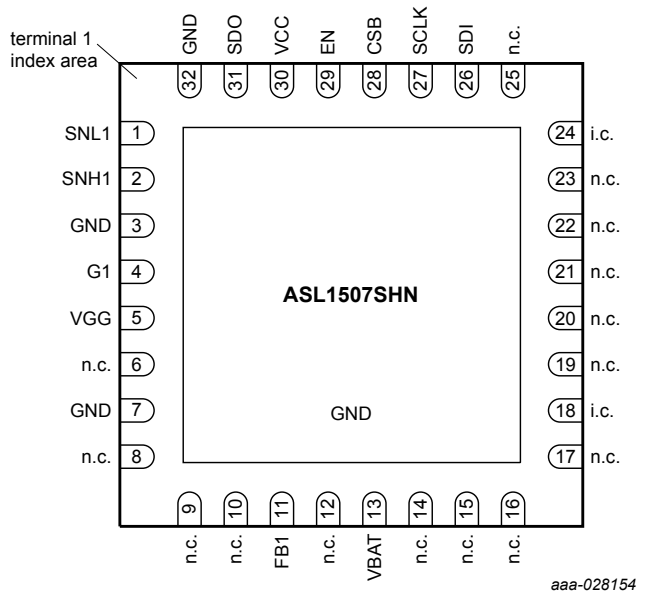


Figure 2. Block diagram for ASL2507SHN

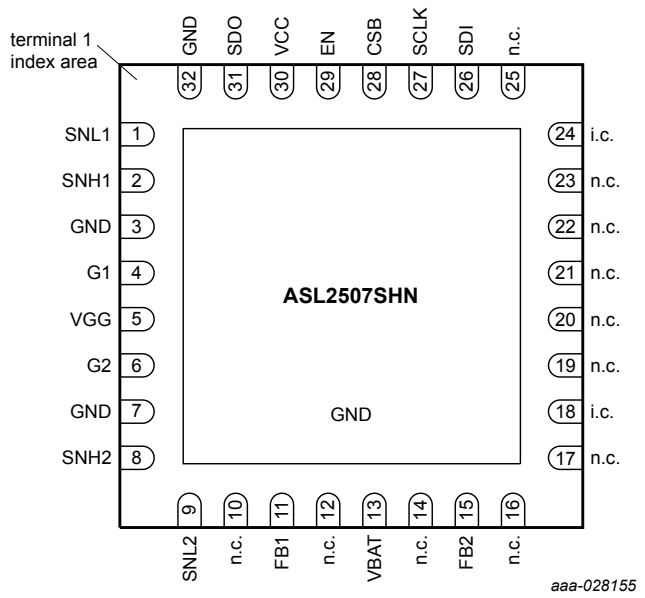
7 Pinning information

7.1 Pinning



Transparent top view

Figure 3. Pin configuration for ASL1507SHN



Transparent top view

Figure 4. Pin configuration for ASL2507SHN

7.2 Pin description

Table 2. Pin description

Symbol		Pin	Description
ASL1507SHN	ASL2507SHN		
SNL1	SNL1	1	phase 1 sense low
SNH1	SNH1	2	phase 1 sense high
GND	GND	3	ground
G1	G1	4	phase 1 gate driver
VGG	VGG	5	gate driver supply
n.c.[1]	-	6	not connected
-	G2	6	phase 2 gate driver
GND	GND	7	ground
n.c.[1]	-	8	not connected
-	SNH2	8	phase 2 sense high
n.c.[1]	-	9	not connected
-	SNL2	9	phase 2 sense low
n.c.[1]	n.c.[1]	10	not connected
FB1[2]	FB1[2]	11	feedback, output 1
n.c.[1]	n.c.[1]	12	not connected
VBAT	VBAT	13	battery supply
n.c.[1]	n.c.[1]	14	not connected
n.c.[1]	-	15	not connected
-	FB2[2]	15	feedback, output 2
n.c.[1]	n.c.[1]	16	not connected
n.c.[1]	n.c.[1]	17	not connected
i.c.[3]	i.c.[3]	18	internally connected
n.c.[1]	n.c.[1]	19	not connected
n.c.[1]	n.c.[1]	20	not connected
n.c.[1]	n.c.[1]	21	not connected
n.c.[1]	n.c.[1]	22	not connected
n.c.[1]	n.c.[1]	23	not connected
i.c.[3]	i.c.[3]	24	internally connected
n.c.[1]	n.c.[1]	25	not connected
SDI	SDI	26	SPI data input
SCLK	SCLK	27	SPI clock
CSB	CSB	28	SPI chip select
EN	EN	29	enable signal

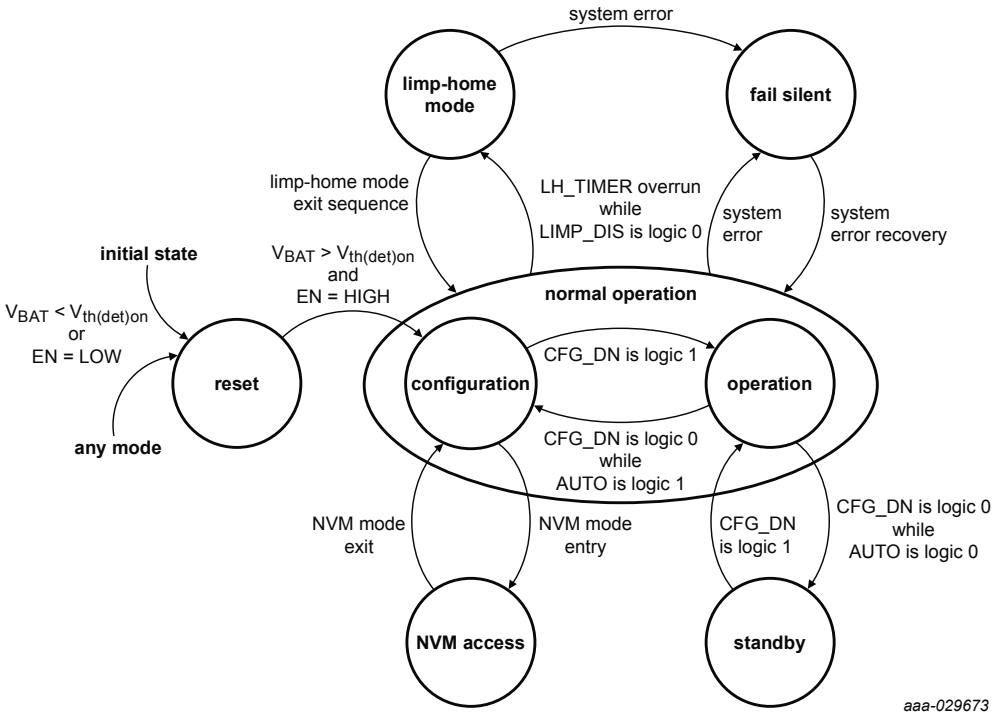
Symbol		Pin	Description
ASL1507SHN	ASL2507SHN		
VCC	VCC	30	external 5 V supply
SDO	SDO	31	SPI data output
GND	GND	32	chip ground

[1] Not connected pins are internally not connected and can be left floating or can be connected to any voltage level.
[2] See Figure 6 and Figure 19 for recommend connections for pin FB1 and FB2.
[3] Internally connected pins should be connected to GND.

For enhanced thermal and electrical performance, the exposed center pad of the package should be soldered to board ground (and not to any other voltage level).

8 Functional description

8.1 Operating modes



Remark: All outputs should be turned off at least 200 ns before the transition from operation to off mode is executed.

Figure 5. State diagram

Table 3. Operating modes

Mode	Control registers	Configuration registers	Diagnostic IC registers	VGG	V_{O1} V_{O2}	Remark
Reset	n.a.	n.a.	n.a.	off	off	device is off, no communication possible
Configuration	read/write	read/write	read	off	off	VGG is off if the output was not previously enabled
				according to register	off	VGG stays on as soon as the output has been enabled
Operation	read/write	read	read	locked	according to register	configuration register is locked
Fail silent	read/write	read[1]	read	off	off	communication possible, but the output is off; restart via EN possible
Standby	read/write	read/write	read	according to register	off	
Limp-home mode	read	read	read	according to NVM settings	according to NVM settings	operating per NVM settings
NVM access	read/write	read/write	read	off	off	NVM read/write possible

[1] Setting the bit CFG_DN to logic 0 also grants write access to the configuration registers.

Table 4. Operation mode register (address 56h)

Bit	Symbol	Description	Value	Function
7 to 3	STATE[4:0]	operation mode of the device	0 0100	configuration mode
			1 0101	operation mode
			1 0111	standby mode
			1 1011	NVM access mode
			1 1100 1 1101 1 1110 0 1011	fail silent mode
			others	internal states used during state transitions
2 to 0	internal	internally used	-	-

8.1.1 Reset mode

The ASL1507SHN; ASL2507SHN switches to reset mode, if the input voltage drops below the power-on detection threshold voltage $V_{th(det)pon}$ or the pin EN is LOW.

The SPI interface and output are turned off when the ASL1507SHN; ASL2507SHN is in the reset mode.

8.1.2 Configuration mode

The ASL1507SHN; ASL2507SHN switches from reset mode to configuration mode, as soon as the input voltage is above the power-on detection threshold voltage $V_{th(det)pon}$ and pin EN is HIGH.

The configuration registers can be set when the ASL1507SHN; ASL2507SHN is in the configuration mode.

8.1.3 Standby mode

The ASL1507SHN; ASL2507SHN switches from operation to standby mode when bit CFG_DN is set to logic 0 while bit AUTO is set to logic 0 as well. In standby mode V_{O1} and V_{O2} are turned off while VGG remains on.

8.1.4 Operation mode

The ASL1507SHN; ASL2507SHN switches from configuration mode to operation mode, as soon as the configuration done bit is set. Once the bit is set to logic 1, the configuration registers are locked and cannot be changed.

In operation mode, the output is available as configured via the SPI interface. Setting the bit VO1EN or VO2EN, starts up VGG. Once VGG is in regulation (signaled by bit VGG_OK), the output voltages V_{O1} and V_{O2} are turned on accordingly. When the converters are on, the battery monitoring functionality is available.

8.1.5 Fail silent mode

The ASL1507SHN; ASL2507SHN switches from operation, configuration, standby, or limp-home mode to fail silent mode, when the junction temperature exceeds the overtemperature shutdown threshold or a VGG error is detected. It also switches modes when the input voltage is below the undervoltage detection threshold or above the overvoltage detection threshold.

In fail silent mode, all outputs are turned off and only the SPI interface remains operational.

8.1.6 Limp-home mode

The ASL1507SHN; ASL2507SHN limp-home mode is activated by detecting loss of SPI communication. In limp-home mode, the outputs are operating according to predefined conditions in an NVM; see Section 8.12 for more information.

During limp-home mode operation, the SPI interface remains functional but only the limp-home mode control register can be written. The other registers offer only read access.

8.1.7 NVM access mode

The ASL1507SHN; ASL2507SHN switches from configuration mode to NVM access mode when the NVM access mode entry command is given. In NVM access mode, the NVM settings can be defined and read back.

8.2 Boost converter configuration

The ASL1507SHN; ASL2507SHN is an automatic boost converter IC delivering constant DC-to-DC voltage to a load. It has a fixed frequency current-mode control for an enhanced stable operation.

The ASL2507SHN offers two phases. Each phase consists of a coil, a resistor, a MOSFET and a diode as shown in Figure 6.

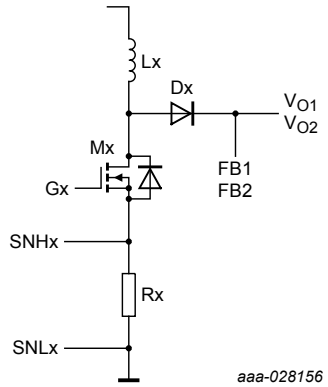


Figure 6. Phase of the boost converter with IC and application connections

To allow a flexible use of the ASL1507SHN; ASL2507SHN, the configuration is based on virtual phases, which are then mapped to a real. That is, physical phase according to the physical connections and conditions of the circuitry around the ASL1507SHN; ASL2507SHN as shown in Figure 7.

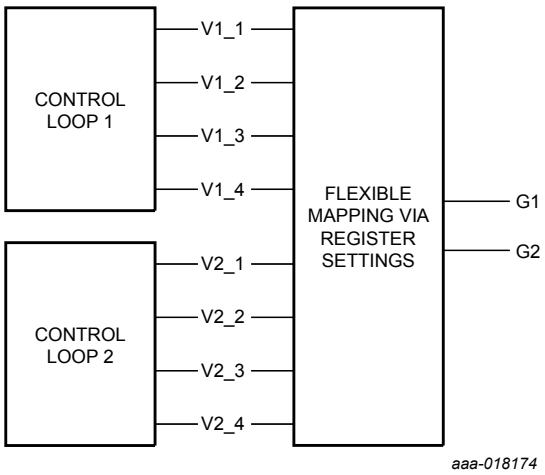


Figure 7. Mapping of virtual phases (V1_1 to V2_4) to physical phases (G1 and G2)

8.2.1 Configuration of the virtual phases

The ASL2507SHN can generate up to two internal phases for up to two virtual outputs. With the internal phase control enable registers, it can be selected, how many virtual phases are generated for the individual virtual outputs.

Table 5. SS scenario logic 1 (address 0Bh)

Bit	Symbol	Description	Value	Function
7	SS_WIDTH1[1:0]	spread spectrum width for logic 1	-	refer to Section 8.4
6				
5	SS_SCEN1[1:0]	SS scenario for logic 1	-	refer to Section 8.4
4				
3	EN_P4_1	phase 4 enabled	0	phase 4 is off
			1	phase 4 is enabled
2	EN_P3_1	phase 3 enabled	0	phase 3 is off
			1	phase 3 is enabled
1	EN_P2_1	phase 2 enabled	0	phase 2 is off
			1	phase 2 is enabled
0	EN_P1_1	phase 1 enabled	0	phase 1 is off
			1	phase 1 is enabled

Table 6. SS scenario logic 2 (address 0Ch)

Bit	Symbol	Description	Value	Function
7	SS_WIDTH2[1:0]	spread spectrum width for logic 2	-	refer to Section 8.4
6				
5	SS_SCEN2[1:0]	SS scenario for logic 2	-	refer to Section 8.4
4				
3	EN_P4_2	phase 4 enabled	0	phase 4 is off
			1	phase 4 is enabled
2	EN_P3_2	phase 3 enabled	0	phase 3 is off
			1	phase 3 is enabled
1	EN_P2_2	phase 2 enabled	0	phase 2 is off
			1	phase 2 is enabled
0	EN_P1_2	phase 1 enabled	0	phase 1 is off
			1	phase 1 is enabled

8.2.2 Association of gate drivers to the output voltages

Each phase that the ASL2507SHN offers must be associated to one of the outputs. Multiple combinations are possible. For example, all phases to one of the outputs, or one phase to one output and one phase to another one.

Table 7. Gate driver output (address 02h)

Bit	Symbol	Description	Value	Function
7 to 2	reserved	reserved	000000	reserved; should remain clear for future use
1	O_G2	association gate driver 2	0	gate driver 2 is connected to V_{O1}
			1	gate driver 2 is connected to V_{O2}
0	O_G1	association gate driver 1	0	gate driver 1 is connected to V_{O1}
			1	gate driver 1 is connected to V_{O2}

8.2.3 Association of gate drivers to the internal phase generation

The gate drivers that the ASL1507SHN; ASL2507SHN offer must be associated to one of the internal virtual logics. It is established with the gate driver phase and phase select configuration registers. Internal logic 1 and logic 2 include four phases, which are used connecting to physical gate driver.

Table 8. Gate driver phase (address 0Fh)

Bit	Symbol	Description	Value	Function
7 to 2	reserved	reserved	000000	reserved; should remain clear for future use
1	O_GP2	association gate driver 2	0	gate driver 2 is connected to logic 1
			1	gate driver 2 is connected to logic 2
0	O_GP1	association gate driver 1	0	gate driver 1 is connected to logic 1
			1	gate driver 1 is connected to logic 2

Table 9. Phase select configuration (address 10h)

Bit	Symbol	Description	Value	Function
7 to 4	reserved	reserved	0000	reserved; should remain clear for future use
3 and 2	PHSEL2[1:0]	phase select gate driver 2	00	routing from phase 1
			01	routing from phase 2
			10	routing from phase 3
			11	routing from phase 4
1 and 0	PHSEL1[1:0]	phase select gate driver 1	00	routing from phase 1
			01	routing from phase 2
			10	routing from phase 3
			11	routing from phase 4

8.2.4 Enabling of connected phases

The gate driver enable register is used to configure which of the phases is active.

Table 10. Gate driver enable (address 01h)

Bit	Symbol	Description	Value	Function
7 to 2	reserved	reserved	000000	reserved; should remain clear for future use
1[1]	EN_G2	phase 2 enabled	0	phase 2 is off
			1	phase 2 is enabled
0	EN_G1	phase 1 enabled	0	phase 1 is off
			1	phase 1 is enabled

[1] For the ASL1507SHN, this bit is reserved.

8.2.5 Configuration of the boost converter frequencies

The operation frequency of the boost converters is set via several SPI registers. To ensure a stable phase delay between the different phases, all timings are derived from the same oscillator. An integer number downscales the internal oscillator frequency for each regulation loop. The slower clock controls the off-time of a phase and the delay from one phase of the regulation loop to the next internal phase. The number of phases determinates finally when the phase is turned on again and so defines the operation frequency of the boost converter.

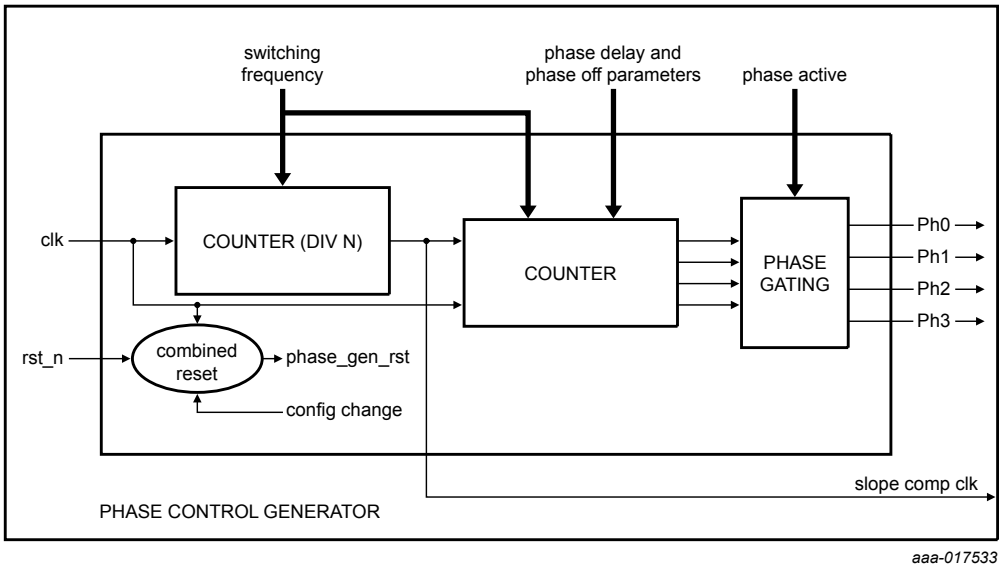


Figure 8. Phase control generator

Table 11. Clock divider for V_{O1} (address 09h)

Bit	Symbol	Description	Value	Function
7 to 0	CLKDIV1[7:0]	clock divider for output voltage 1	00h	clock is not divided
			...	clock is divided by CLKDIV1[7:0] + 1
			FFh	clock is divided by 256

Table 12. Clock divider for V_{O2} (address 0Ah)

Bit	Symbol	Description	Value	Function
7 to 0	CLKDIV2[7:0]	clock divider for output voltage 2	00h	clock is not divided
			...	clock is divided by CLKDIV2[7:0] + 1
			FFh	clock is divided by 256

Table 13. Phase-off time and phase delay of output 1 (address 0Dh)

Bit	Symbol	Description	Value	Function
7 to 3	PHDEL1[4:0]	delay to next phase of output 1	00h	phase delay is one clock period of the divided clock
			...	phase delay is PHDEL1[4:0] + one clock period of the divided clock
			1Fh	phase delay is 32 clock periods of the divided clock
2 to 0	PHOFF1[2:0]	phase-off time of output 1	00h	phase-off time is one clock period of the divided clock
			...	phase-off time is PHOFF1[2:0] of the divided clock
			07h	phase-off time is seven clock periods of the divided clock

Table 14. Phase-off time and phase delay of output 2 (address 0Eh)

Bit	Symbol	Description	Value	Function
7 to 3	PHDEL2[4:0]	delay to next phase of output 2	00h	phase delay is one clock period of the divided clock
			...	phase delay is PHDEL2[4:0] + one clock period of the divided clock
			1Fh	phase delay is 32 clock periods of the divided clock
2 to 0	PHOFF2[2:0]	phase-off time of output 2	00h	phase-off time is one clock period of the divided clock
			...	phase-off time is PHOFF2[2:0] of the divided clock
			07h	phase-off time is seven clock periods of the divided clock

Remark: *To obtain the best performance of the internal slope compensation, keep the possible settings of the delay between the phases close to 32.*

8.2.6 Control loop parameter setting

The ASL1507SHN; ASL2507SHN is able to operate with a wide range of external components and offers wide range of operating frequencies. To achieve the maximum performance for each set of operation conditions, set the control loop parameters according to the external components and the operating frequency.

Table 15. Loop filter proportional configuration (address 11h)

Bit	Symbol	Description	Value	Function
7 to 4	PROP2[3:0]	proportional factor output 2	0h	proportional factor output 2 is 0.05
			...	proportional factor output 2 is PROP2[3:0] × 0.05 + 0.05
			Fh	proportional factor output 2 is 0.8
3 to 0	PROP1[3:0]	proportional factor output 1	0h	proportional factor output 1 is 0.05
			...	proportional factor output 1 is PROP1[3:0] × 0.05 + 0.05
			Fh	proportional factor output 1 is 0.8

Table 16. Loop filter integral configuration (address 12h)

Bit	Symbol	Description	Value	Function
7 to 4	INTEG2[3:0]	integral factor output 2	0h	integral factor output 2 is 0.005
			...	integral factor output 2 is INTEG2[3:0] × 0.005 + 0.005
			Fh	integral factor output 2 is 0.08
3 to 0	INTEG1[3:0]	integral factor output 1	0h	integral factor output 1 is 0.005
			...	integral factor output 1 is INTEG1[3:0] × 0.005 + 0.005
			Fh	integral factor output 1 is 0.08

Table 17. Slope compensation configuration (address 13h)

Bit	Symbol	Description	Value	Function
7 to 4	SLPCMP2[3:0]	slope compensation factor output 2	0h	slope compensation factor output 2 = 112 kΩ
			1h	slope compensation factor output 2 = 84 kΩ
			2h	slope compensation factor output 2 = 70 kΩ
			4h	slope compensation factor output 2 = 56 kΩ
			8h	slope compensation factor output 2 = 28 kΩ
3 to 0	SLPCMP1[3:0]	slope compensation factor output 1	0h	slope compensation factor output 1 = 112 kΩ
			1h	slope compensation factor output 1 = 84 kΩ
			2h	slope compensation factor output 1 = 70 kΩ
			4h	slope compensation factor output 1 = 56 kΩ
			8h	slope compensation factor output 1 = 28 kΩ

Table 18. Current sense slope resistor configuration (address 14h)

Bit	Symbol	Description	Value	Function
7 to 4	reserved	reserved	-	
3 and 2	SLPR2[1:0]	slope resistor configuration for gate driver 2	0h	250 Ω
			1h	500 Ω
			2h	1000 Ω
			3h	1500 Ω
1 and 0	SLPR1[1:0]	slope resistor configuration for gate driver 1	0h	250 Ω
			1h	500 Ω
			2h	1000 Ω
			3h	1500 Ω

8.3 Output voltage programmability

The ASL1507SHN; ASL2507SHN provides the possibility to program the output voltage and output overvoltage protection of the output via the SPI interface.

8.3.1 Output voltage target programming

The target output voltage can be programmed via the output voltage registers. As the ASL1507SHN; ASL2507SHN is a boost converter, the output voltage cannot be lower than the supply voltage minus the drop of the converter diode (Dx in Figure 6).

Table 19. Output voltage 1 register (address 03h)

Bit	Symbol	Description	Value	Function
7 to 0	V_VO1[7:0]	target voltage output 1	00h	output 1 is turned off
			...	target voltage output 1 = 0.3606 V × V_VO1[7:0]
			FFh	maximum target output voltage = 90 V

Table 20. Output voltage 2 register (address 04h)

Bit	Symbol	Description	Value	Function
7 to 0	V_VO2[7:0]	target voltage output 2	00h	output 2 is turned off
			...	target voltage output 2 = 0.3606 V × V_VO2[7:0]
			FFh	maximum target output voltage = 90 V

8.3.2 Output overvoltage protection programming

Due to fast changes in the supply or the output, disruption is possible in the output voltage. To avoid high voltages damaging the attached components, the ASL1507SHN; ASL2507SHN offers a programmable overvoltage protection threshold. Once the output voltage is above this threshold, the gate pin of the output stops toggling. It results in a halt of the energy delivery to the output.

Once the output voltage recovers and is below the threshold again, the gate pin starts toggling again. The regulation loop regulates the output back to the target value.

For stable operation of the device, the limit voltage output register should be programmed higher than the corresponding output voltage registers. The limit voltage output setting should be chosen to allow the regulation loop to operate continuously in case of overshoots due to load changes.

Table 21. Limit voltage output 1 register (address 05h)

Bit	Symbol	Description	Value	Function
7 to 0	VMAX_VO1[7:0]	limit output 1	00h	output 1 is turned off
			...	output overvoltage protection output 1 = 0.3606 V × VMAX_VO1[7:0]
			FFh	maximum output overvoltage protection output 1 = 90 V

Table 22. Limit voltage output 2 register (address 06h)

Bit	Symbol	Description	Value	Function
7 to 0	VMAX_VO2[7:0]	limit output 2	00h	output 2 is turned off
			...	output overvoltage protection output 2 = 0.3606 V × VMAX_VO2[7:0]
			FFh	maximum output overvoltage protection output 2 = 90 V

8.3.3 Output voltage ramp up

Output voltage ramp up is a feature which ramps up the target voltage. Timing and step size can be programmed.

Table 23. Ramp up output 1 (address 1Fh)

Bit	Symbol	Description	Value	Function
7 and 6	reserved	reserved	-	
5	RAMP1	ramp up select	0	ramp up enabled
			1	ramp up disabled
4 to 2	STEP_T1[2:0]	step time for V_{O1}	000	40 µs
			001	80 µs
			010	160 µs
			011	320 µs
			100	520 µs
			101	1040 µs
			110	2040 µs
			111	4040 µs
1 and 0	STEP_V1[1:0]	step size for V_{O1}	00	0.7 V
			01	1.4 V
			10	2.8 V
			11	5.6 V

Table 24. Ramp up output 2 (address 20h)

Bit	Symbol	Description	Value	Function
7 and 6	reserved	reserved	-	
5	RAMP2	ramp up select	0	ramp up enabled
			1	ramp up disabled
4 to 2	STEP_T2[2:0]	step time for V_{O2}	000	40 µs
			001	80 µs
			010	160 µs
			011	320 µs
			100	520 µs
			101	1040 µs
			110	2040 µs
			111	4040 µs
1 and 0	STEP_V2[1:0]	step size for V_{O2}	00	0.7 V
			01	1.4 V
			10	2.8 V
			11	5.6 V

8.3.4 Dead-band setting

The regulation loop of the output voltage of the ASL1507SHN; ASL2507SHN uses a selectable dead-band. A higher dead-band setting results into higher noise level on the output, but fewer regulation adjustments thus a more smooth regulation. This setting is part of the internal register 5 (address 30h). The content of this register can only be changed in configuration mode.

Table 25. Internal register 5 (address 30h)

Bit	Symbol	Description	Value	Function
7 and 6	reserved	reserved	-	
5 and 4	DEAD_BAND[1:0]	dead-band setting	00	180 mV
			01	350 mV
			10	700 mV
			11	1.4 V
3 to 0	internal	internally used	9h	no modification allowed

8.4 Frequency spread spectrum

The frequency spread spectrum achieves clock dithering, on-chip technique for EMI reduction. Slope clock division factor is changed dynamically based on spread spectrum ramp profiles (triangular ramp) or using a PRBS (random) generator. The frequencies used by the system during spread spectrum operation can be calculated with the following formula.

$$f_{sw(used)} = \frac{f_{osc(int)}}{\frac{f_{osc(int)}}{f_{sw(set)}} + x} \quad (1)$$

$f_{sw(used)}$ is the used switching frequency of the system without spread spectrum enabled.

$f_{sw(set)}$ is the set switching frequency.

$f_{osc(int)}$ is the internal oscillator frequency.

x is according to Table 29 and Table 30.

Table 26. Spread spectrum enable register (address 1Ch)

Bit	Symbol	Description	Value	Function
7	reserved	reserved	-	
6	internal	internally used	0	internally used; must remain logic 0
5	RESTART_TEMP	restart after TEMP error	1	restart after power down due to TEMP error condition, once TEMP error gets cleared
			0	no restart in case of TEMP error
4	RESTART_VBAT	restart after VBAT error	1	restart after power down due to VBAT UV/OV error condition, once VBAT UV/OV error gets cleared
			0	no restart in case of VBAT UV/OV error
3	EN_PRBS_CH2_SPREAD_SPECTRUM	enable the spread spectrum scenario	0	disable; ramp profile active
			1	enable; random profile active
2	EN_CH2_SPREAD_SPECTRUM		0	disable
			1	enable
1	EN_PRBS_CH1_SPREAD_SPECTRUM		0	disable; ramp profile active
			1	enable; random profile active
0	EN_CH1_SPREAD_SPECTRUM		0	disable
			1	enable

Table 27. SS scenario logic 1 register (address 0Bh)

Bit	Symbol	Description	Value	Function
7 and 6	SS_WIDTH1[1:0]	spread spectrum width for logic 1	-	see Table 29 and Table 30
5 and 4	SS_SCEN1[1:0]	SS scenario for logic 1	-	see Table 29 and Table 30
3	EN_P4_1	phase 4 enabled	-	see Table 5
2	EN_P3_1	phase 3 enabled	-	see Table 5
1	EN_P2_1	phase 2 enabled	-	see Table 5
0	EN_P1_1	phase 1 enabled	-	see Table 5

Table 28. SS scenario logic 2 register (address 0Ch)

Bit	Symbol	Description	Value	Function
7 and 6	SS_WIDTH2[1:0]	spread spectrum width for logic 2	-	see Table 29 and Table 30
5 and 4	SS_SCEN2[1:0]	SS scenario for logic 2	-	see Table 29 and Table 30
3	EN_P4_2	phase 4 enabled	-	see Table 6
2	EN_P3_2	phase 3 enabled	-	see Table 6
1	EN_P2_2	phase 2 enabled	-	see Table 6
0	EN_P1_2	phase 1 enabled	-	see Table 6

Table 29. Ramp profile

SS_SCENx[1:0]	SS_WIDTHx[1:0]			
	00	01	10	11
00 01	0 to 255 and 255 to 0	0 to 127 and 127 to 0	0 to 63 and 63 to 0	0 to 31 and 31 to 0
10	−256 to 0 and 0 to −256	−128 to 0 and 0 to −128	−64 to 0 and 0 to −64	−32 to 0 and 0 to −32
11	−128 to +127 and +127 to −128	−64 to +63 and +63 to −64	−32 to +31 and +31 to −32	−16 to +15 and +15 to −16

Table 30. Random profile

SS_SCENx[1:0]	SS_WIDTHx[1:0]			
	00	01	10	11
00 01	0 to 255	0 to 127	0 to 63	0 to 31
10	−128 to −1	−64 to −1	−32 to −1	−16 to −1
11	−128 to +127	−64 to +63	−32 to +31	−16 to +15

8.5 Coil peak current limitation

The ASL1507SHN; ASL2507SHN offers a function to limit peak current inside the coil and therefore to limit the input current for the system. Furthermore, this functionality can be used to avoid magnetic saturation of the coils. It also allows some soft start feature to be realized with this function.

With the maximum phase current V_{Ox} register, the maximum peak current for the phase can be configured. Once the voltage between pins SNLx and SNHx achieves maximum level, the gate will be turned off until the next switching cycle. To avoid subharmonic oscillations when the coil peak current limitation is becoming active, the slope compensation remains active. It reduces the coil peak current toward the end of the switching cycle to ensure stable operation of the system.

In order to avoid that this function interferes with the normal regulation, the limit should be placed well above the maximum expected current.

Table 31. Maximum coil current V_{O1} register (address 07h)

Bit	Symbol	Description	Value	Function
7 to 0	IMAX1[7:0]	coil current limitation assigned to V_{O1}	00h	no current allowed
			...	maximum peak current = (IMAX1[7:0] × 1.8 V / 256 − 0.24 V) / R_{sense}
			80h	maximum allowed setting = (128 / 255 × 1.8 V − 0.24 V) / R_{sense}
			...	not allowed
			FFh	not allowed

Table 32. Maximum coil current V_{O2} register (address 08h)

Bit	Symbol	Description	Value	Function
7 to 0	IMAX2[7:0]	coil current limitation assigned to V_{O2}	00h	no current allowed
			...	maximum peak current = (IMAX2[7:0] × 1.8 V / 256 − 0.24 V) / R_{sense}
			80h	maximum allowed setting = (128 / 255 × 1.8 V − 0.24 V) / R_{sense}
			...	not allowed
			FFh	not allowed

8.6 Enabling the output voltage

The ASL1507SHN; ASL2507SHN provides two independent output voltages. In operation mode, the output voltages are turned on with the bit VO1EN and VO2EN.

As soon as one of the outputs is turned on, the VGG voltage regulator is turned on. After $t_{startup}$ the gate drivers start switching, provided the bit VGG_OK is set.

Table 33. Function control register (address 00h)

Bit	Symbol	Description	Value	Function
7	reserved	reserved	n.a.	reserved; should remain cleared for future use
6	EN_VBAT_MEASUREMENT	enable VBAT measurement	0	disabled
			1	VBAT measurement is available before starting the converter
5 and 4	internal	internally used	00	internally used; must remain 00
3	CNT_CSB	count chip select time	0	chip select low count feature is disabled
			1	chip select low count feature is enabled
2	VO2EN	enable output 2	0	output 2 is turned off
			1	output 2 is turned on when the device is in operation mode
1	VO1EN	enable output 1	0	output 1 is turned off
			1	output 1 is turned on when the device is in operation mode
0	CFG_DN	configuration done bit	0	device is in configuration mode; no configuration lock
			1	device is in operation mode; configuration lock is active

8.7 Gate voltage supply

The ASL1507SHN; ASL2507SHN has an integrated linear regulator to generate the supply voltage of the gate drivers. The integrated linear regulator is internally connected to the pin VGG. The voltage generated by the linear regulator can be set via the VGG control register.

Table 34. VGG control register (address 15h); bit 4 in NVM address 00h register is set to logic 0

Bit	Symbol	Description	Value	Function
7 to 0	VGG[7:0]	supply voltage for gate drivers	00h	not allowed
			...	not allowed
			80h	maximum output voltage = 7.98 V
			...	16.07 − 0.0632 × VGG[7:0]
			B7h	minimum output voltage = 4.50 V
			...	not allowed
			FFh	not allowed

Table 35. VGG control register (address 15h); bit 4 in NVM address 00h register is set to logic 1

Bit	Symbol	Description	Value	Function
7 to 0	VGG[7:0]	supply voltage for gate drivers	00h	not allowed
			...	not allowed
			5Dh	maximum output voltage = 10.19 V
			...	16.07 − 0.0632 × VGG[7:0]
			B7h	minimum output voltage = 4.50 V
			...	not allowed
			FFh	not allowed

If a setting between FFh and B7h is used, the device may not start up VGG. If the device operates, parameters of VGG are not guaranteed.

8.7.1 Gate voltage supply diagnostics

The diagnostic options for the gate voltage supply are:

- VGG available; details can be found in Section 8.10
- VGG protection active; details can be found in Section 8.10

8.8 Supply voltage monitoring

The ASL1507SHN; ASL2507SHN continuously measures the voltage at pin VBAT. It allows the system to monitor the supply voltage without additional external components. It also offers the option to put an automatic undervoltage/overvoltage protection in place.

8.8.1 Battery voltage measurement

The ASL1507SHN; ASL2507SHN continuously measures the voltage at pin VBAT. The measurement result is available in the battery voltage register when the output is enabled or when bit 6 in SPI register 00h is set to logic 1.

Table 36. Battery voltage register (address 45h)

Bit	Symbol	Description	Value	Function
7 to 0	V_VBAT[7:0]	battery voltage	00h	battery voltage = 0 V
			...	battery voltage = 0.3606 V × V_VBAT[7:0]
			FFh	maximum measurable battery voltage = 90 V

8.8.2 Undervoltage detection

The ASL1507SHN; ASL2507SHN offers a variable undervoltage detection threshold. When the supply voltage drops below this threshold, the undervoltage detect bit is set and the gate pin stops toggling and no more power is delivered to the output.

Table 37. Undervoltage threshold register (address 1Bh)

Bit	Symbol	Description	Value	Function
7 to 0	V_VBAT_UV[7:0]	undervoltage detection threshold	00h	undervoltage detection threshold = 0 V
			...	undervoltage detection threshold = 0.3606 V × V_VBAT_UV[7:0]
			FFh	maximum undervoltage detection threshold = 90 V

8.8.3 Overvoltage detection

The ASL1507SHN; ASL2507SHN offers a variable overvoltage detection threshold. When the supply voltage rises above this threshold, the overvoltage detect bit is set and fail silent mode is entered. The gate pin stops toggling and no power is delivered to the output.

Table 38. Overvoltage threshold register (address 1Ah)

Bit	Symbol	Description	Value	Function
7 to 0	V_VBAT_OV[7:0]	overvoltage detection threshold	00h	overvoltage detection threshold = 0 V
			...	overvoltage detection threshold = 0.3606 V × V_VBAT_OV[7:0]
			FFh	maximum overvoltage detection threshold = 90 V

8.9 Junction temperature information

The ASL1507SHN; ASL2507SHN provides a measurement of the IC junction temperature. The measurement information is available in the junction temperature register.

Table 39. Junction temperature register (address 46h)

Bit	Symbol	Description	Value	Function
7 to 0	T_JUNCTION[7:0]	junction temperature	00h to 17h	device junction temperature below −40 °C
			18h	device junction temperature = −40 °C
			...	device junction temperature = T_JUNCTION[7:0] × (215 / 106) °C − 88 °C
			82h	device junction temperature = 175 °C
			83h to FFh	device junction temperature above 175 °C

8.10 Diagnostic information

The diagnostic register contains useful information for diagnostic purposes. Details for each bit can be found in the following subsections.

Table 40. Diagnostic register (address 5Fh)

Bit	Symbol	Description	Value	Function
7	VO1_OK	V_{O1} regulated	0	V_{O1} is deviating from the target value
			1	V_{O1} is regulated to the target value
6	VO2_OK	V_{O2} regulated	0	V_{O2} is deviating from the target value
			1	V_{O2} is regulated to the target value
5	VGG_OK	VGG regulation OK	0	VGG is not available
			1	VGG is available
4	TJ_ERR	device temperature is too high	0	device temperature below $T_{sd(otp)}$
			1	device temperature above $T_{sd(otp)}$
3	VBAT_UV	VBAT undervoltage	0	no undervoltage at VBAT detected
			1	undervoltage at VBAT detected
2	VBAT_OV	VBAT overvoltage	0	no overvoltage at VBAT detected
			1	overvoltage at VBAT detected
1	SPI_ERR	SPI error	0	last SPI command was executed correctly
			1	last SPI command was erroneous and has been discarded
0	VGG_ERR	VGG error	0	VGG protection not active
			1	VGG protection has turned on and VGG is deactivated

8.10.1 Bit VBAT_OV

The bit VBAT_OV depends on the battery monitoring functionality as described in Section 8.8.3. It indicates that the device has detected an overvoltage condition and enables an option to select the auto recover or fail silent mode.

A write access to the diagnostic register or entering off mode, clears the bit. Independent of the clearing of the bit, the device stays in fail silent mode.

8.10.2 Bit VBAT_UV

The bit VBAT_UV depends on the battery monitoring functionality as described in Section 8.8.2. It indicates that the device has detected an undervoltage condition.

A write access to the diagnostic register or entering off mode, clears the bit. Independent of the clearing of the bit, the device stays in fail silent mode.

8.10.3 Bit SPI_ERR

The device evaluates all SPI accesses to the device for the correctness of the commands. When the command is not allowed, the SPI_ERR bit is set.

A write access to the diagnostic register or entering off mode, clears the bit.

8.10.4 Bit TJ_ERR

The bit TJ_ERR indicates that the junction temperature has exceeded the maximum allowable temperature and the device has entered fail silent mode.

A write access to the diagnostic register or entering off mode, clears the bit. Independent of the clearing of the bit, the device stays in fail silent mode.

8.10.5 Bit VGG_ERR

The bit VGG_ERR is set when the gate voltage did not reach the VGG_OK window (when $V_{drv(G)VGG\_OK}$ is within the range) within $t_{startup}$. Once bit VGG_ERR is set, it indicates that an error on the gate voltage regulator has been detected and the device has entered fail silent mode. A write access to the diagnostic register clears the VGG_ERR bit. The device stays in fail silent mode irrespective of the clearing of the bit.

8.10.6 Bit VGG_OK

The bit VGG_OK indicates that the gate driver voltage is regulated to the target voltage and allows the gate drivers to drive the gate driver pins.

If the gate driver voltage is outside the VGG_OK window ($V_{reg(VGG\_OK)}$) after $t_{startup}$, the device clears the VGG_OK bit and the device enters fail silent mode.

8.10.7 Bits VO1_OK and VO2_OK

The bits VO1_OK and VO2_OK indicate whether the output voltage is regulated to the target value. The bits are set as soon as the corresponding output voltage is $V_{O(VO\_OK)}$ for more than $t_{fltr(Vo)}$. The bits are cleared when the corresponding output is not equal to $V_{O(VO\_OK)}$ for more than $t_{fltr(Vo)}$.

8.11 Restart on error

In case the ASL1507SHN; ASL2507SHN enters fail silent mode, it switches off the outputs.

In default mode, the EN pin must be cycled and the ASL1507SHN; ASL2507SHN should be reconfigured to start operation. In another mode of operation, ASL1507SHN; ASL2507SHN can be configured which does not require the EN pin cycling. In this mode, when the error condition is resolved, the state machine automatically exits the fail silent mode. The operation restarts as configured prior to entering the fail silent mode. This auto restart mode can be controlled through NVM by programming the bits.

Restart can be independently done for TJ_ERR, VBAT_UV and VBAT_OV conditions; refer to Section 8.4.

8.12 Limp-home mode

In case of detection of a loss of SPI communication, the ASL1507SHN; ASL2507SHN enters limp-home mode. In limp-home mode, ASL1507SHN; ASL2507SHN operates according to predefined conditions stored in an NVM.

The settings with which the device operates in limp-home settings can be configured in NVM use mode. In NVM use mode, the outputs are disabled. After configuration, the limp-home settings will be permanently stored if not changed. Once the ASL1507SHN; ASL2507SHN detects a loss of SPI communication in normal operation, the device populates these settings into the registers and operates according to them.

In case the system recovers from the error, limp-home mode can be left via the exit limp-home mode sequence. With the completion of the exit sequence, the device operates according to the SPI register.

Limp-home offer the same operational features as normal operation.

Bit 3 in register 54h indicates the limp-home mode status of the device.

Table 41. Limp-home mode indication (address 54h)

Bit	Symbol	Description	Value	Function
7 to 4	internal	internally used	-	-
3	LHM	limp-home mode indication	1	device is in limp-home mode
			0	device is not in limp-home mode
2 to 0	internal	internally used	-	-

8.12.1 Limp-home mode activation

The limp-home mode can be enabled and disabled in end-user application with the LIMP_DIS bit (bit 2 of the multi-content NVM data field). Once enabled the ASL1507SHN; ASL2507SHN is expecting a write command to the limp-home mode control register (address 3Ch) with the bits LIMP_EXIT[2:0] all set to logic 1. The write command refreshes the LH_TIMER. In case the LH_TIMER it not refreshed before it expires, the device enters into limp-home mode.

Refer to Section 8.13.1 for more information on starting the NVM write sequence.

8.12.2 Limp-home mode operation

Once the system enters to limp-home mode, the ASL1507SHN; ASL2507SHN switches to the configuration as defined in the NVM memory for limp-home mode. The ASL1507SHN; ASL2507SHN modifies the control registers accordingly.

During limp-home mode operation, the SPI interface remains functional, but only the limp-home mode control register can be written. The other registers offer only read access.

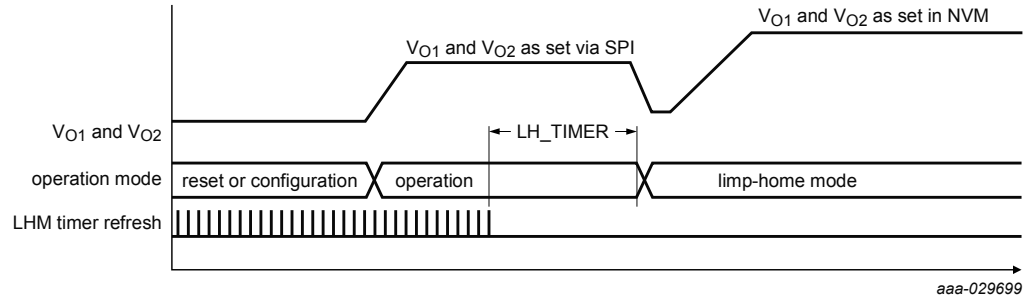


Figure 9. Limp-home mode startup

8.12.3 Limp-home mode deactivation

To deactivate limp-home mode, a dedicated limp-home mode deactivation sequence must be written to the limp-home mode control register (address 3Ch).

Table 42. Limp-home mode deactivation sequence

Deactivation step	Data to LIMP_EXIT[2:0]
Step 1	001
Step 2	010
Step 3	100
Limp-home refresh	111

Once the deactivation sequence is completed, the ASL1507SHN; ASL2507SHN immediately starts to react on SPI communication. The registers remain as set for the limp-home mode. Once the system is back to operation mode, all registers are accessible as defined for operation mode again.

8.12.4 Limp-home mode control register

The limp-home mode control register allows control of the limp-home mode.

Table 43. Limp-home mode control register (address 3Ch)

Bit	Symbol	Description	Value	Function
7	reserved			n.a.
6 to 4	LIMP_EXIT[2:0]	limp-home mode deactivation sequence		limp-home mode deactivation and refresh pattern; see Table 42
3 to 1	LH_TIMER[2:0]	limp-home timeout	000	5.4096 ms
			001	10.8192 ms
			010	21.6396 ms
			011	43.2792 ms
			100	86.5584 ms
			101	173.1168 ms
			110	346.2336 ms
			111	692.4792 ms
0	reserved			n.a.

8.13 NVM memory

The ASL1507SHN; ASL2507SHN features an internal error correction module to ensure reliable operation of the NVM memory. All required ECC codes can be internally generated and in case of errors the corrections are done automatically.

Table 44. ECC code register (address 39h)

Bit	Symbol	Description	Value	Function
7	EEB	disables ECC block for write operation	0	must be kept logic 0
6	ECB	disables ECC block for read operation	0	must be kept logic 0
5 to 0	NVM_WRITE_ECC[5:0]	-	00000	error correction code for NVM write data; not used when bit EEB is logic 0

Table 45. NVM control register (address 3Ah)

Bit	Symbol	Description	Value	Function
7 to 4	internal	internally used	-	-
3 and 2	NVM_MODE[1:0]	enter and exit NVM program mode	01	enter NVM access mode
			10	exit NVM access mode
			others	invalid; no action
1 and 0	NVM_ACCESS[1:0]	initiate NVM read/write commands	00 changes to 01	initiate NVM read[1]
			00 changes to 10	initiate NVM write[1]
			others	invalid; no action

[1] NVM accesss is only executed when NVM_DONE is set to logic 1.

Table 46. NVM status register (address 55h)

Bit	Symbol	Description	Value	Function
7 to 5	internal	internally used	-	-
4	NVM_ACCESS	customer NVM access possible	0	not possible
			1	possible when in NVM access mode
3	ILLEGAL_NVM	illegal NVM access	0	not happened
			1	at least one illegal NVM access happened
2 and 1	internal	internally used	-	-
0	NVM_DONE	NVM action complete	0	NVM action in progress
			1	NVM action completed

8.13.1 NVM write sequence

To write an NVM register, the device must be in NVM access mode. The following sequence should be used.

1. Check that the ASL1507SHN; ASL2507SHN is in configuration mode (register 56h shows binary 0010 0XXXb) and limp-home mode is not active (register 54h shows binary XXXX X0XXb).
2. Enter NVM access mode by setting register 3Ah to 04h.
3. Confirm that the ASL1507SHN; ASL2507SHN is in NVM access mode (register 56h shows binary 1101 1XXXb).
4. Write target NVM address to NVM address register (register 36h is target register).
5. Write target NVM_DATA[15:8] into data register 37h.
6. Write target NVM_DATA[7:0] into data register 38h.
7. Ensure that the ECC is calculated internally (register 39h = 00h).
8. Ensure that the NVM is ready (register 55h shows binary XXXX XXX1b).
9. Initiate NVM write:
   - Write register 3Ah with XXXX 0100b.
   - Write register 3Ah with XXXX 0110b.
10. Wait until NVM access is completed (register 55h shows binary XXXX XXX1b).
11. If further NVM access is required, start at step four of the read or write sequence.
12. Exit NVM access mode by setting register 3Ah to 08h.
13. NVM access complete; for reset set pin EN = LOW.

Note:

The IC is only considering the NVM content programmed as valid when bit 1 and bit 0 in the NVM register 00h indicate 10b. The IC is allowing 200 write cycles to the NVM. The number for write counts can be stored in the NVM write counter in NVM address 01h. This counter should be increased after each update.

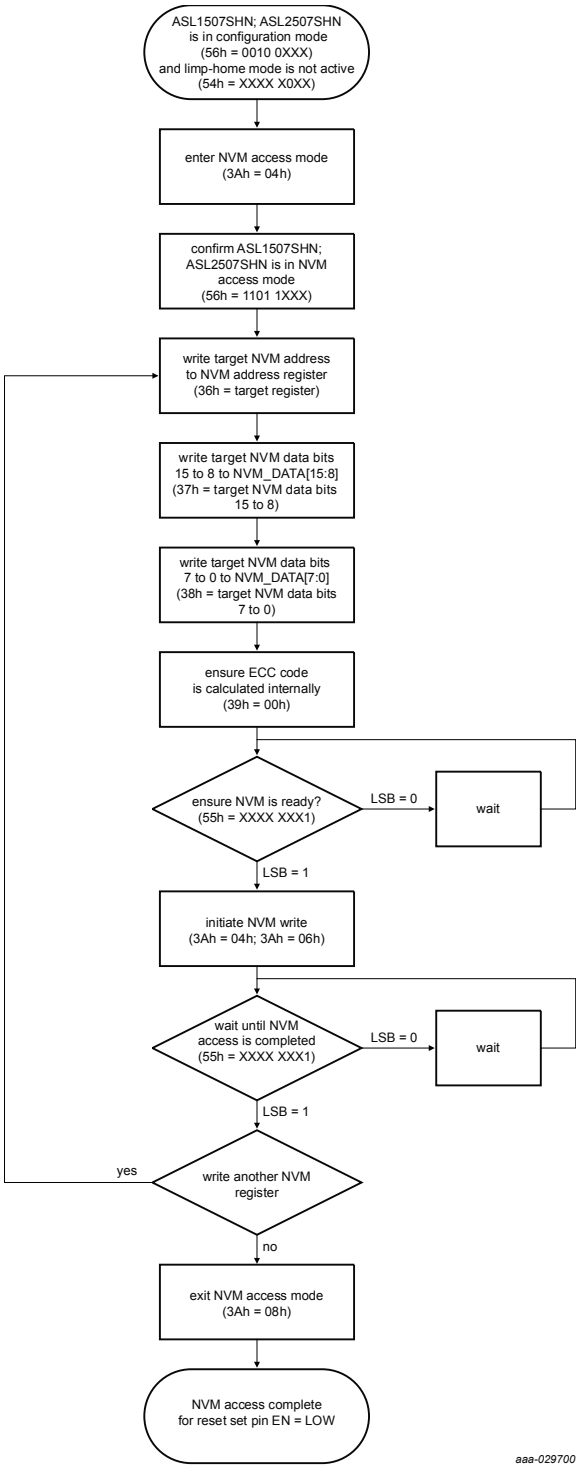


Figure 10. Sequence to write into NVM registers

8.13.2 NVM read sequence

To read an NVM register, the device must be in NVM access mode. The following sequence should be used.

1. Check that the ASL1507SHN; ASL2507SHN is in configuration mode (register 56h shows binary 0010 0XXXb) and limp-home mode is not active (register 54h shows binary XXXX X0XXb).
2. Enter NVM access mode by setting register 3Ah to 04h.
3. Confirm that the ASL1507SHN; ASL2507SHN is in NVM access mode (register 56h shows binary 1101 1XXXb).
4. Write target NVM address to NVM address register (register 36h is target register).
5. Ensure that the NVM is ready (register 55h shows binary XXXX XXX1b).
6. Initiate NVM read:
   - Write register 3Ah with XXXX 0100b.
   - Write register 3Ah with XXXX 0101b.
7. Wait until NVM access is completed (register 55h shows binary XXXX XXX1b).
8. Data from the NVM is now available in NVM data read register 59h for NVM_DATA[15:8] and register 5Ah for NVM_DATA[7:0].
9. If further NVM access is required, start at step four of the read or write sequence.
10. Exit NVM access mode by setting register 3Ah to 08h.
11. NVM access complete; for reset set pin EN = LOW.

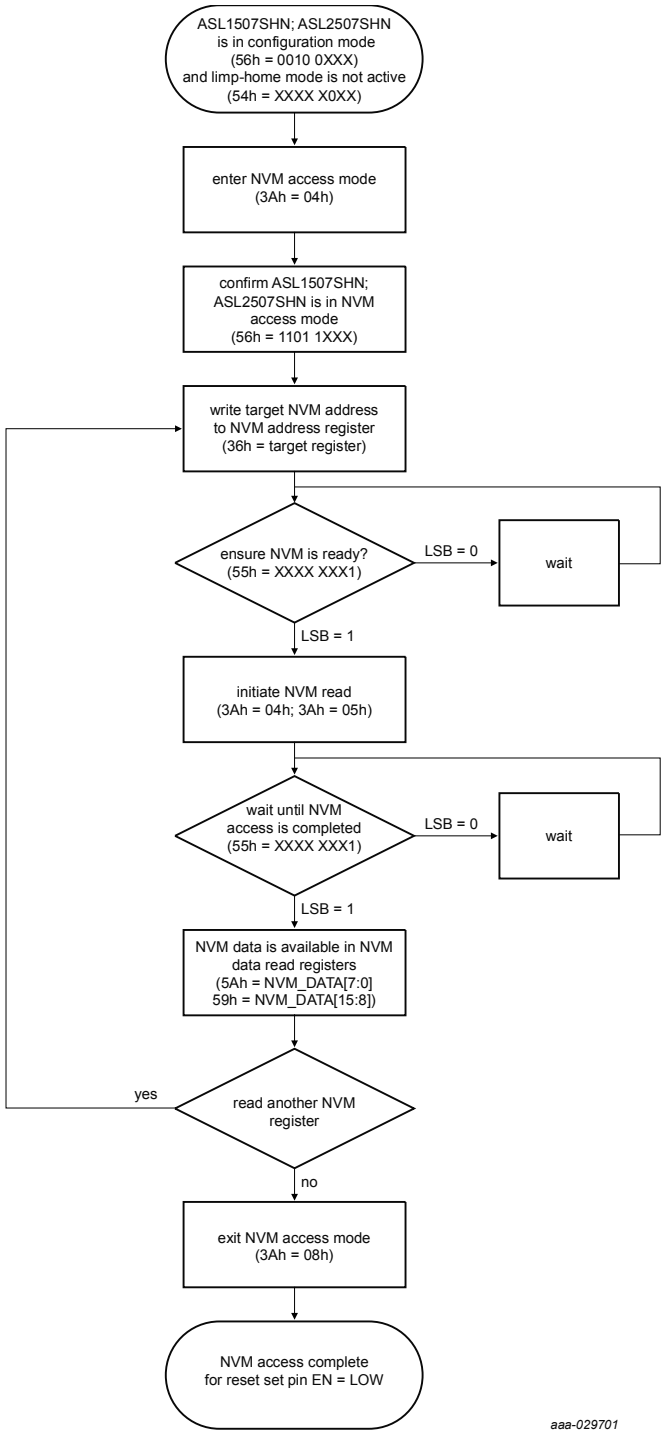


Figure 11. Sequence to read from NVM registers

8.13.3 NVM register map

The ASL1507SHN; ASL2507SHN allows limp-home values during NVM access. Table 47 shows the linking of the NVM addresses to the register addresses.

Table 47. Mapping of NVM registers to control registers

NVM address linked to SPI register 36h[4:0]	NVM_DATA[15:8] linked to SPI register 37h and 59h	NVM_DATA[7:0] linked to SPI register 38h and 5Ah
00h	n.a.	multi-content NVM data fields
01h	NVM write count bit 15 to bit 8	NVM write count bit 7 to bit 0
02h	n.a.	function control
03h	n.a.	gate driver enable
04h	gate driver output	output voltage 1
05h	output voltage 2	limit voltage output 1
06h	limit voltage output 2	maximum coil current V_{O1}
07h	maximum coil current V_{O2}	clock divider for V_{O1}
08h	clock divider for V_{O2}	SS scenario logic 1
09h	SS scenario logic 2	phase-off time and phase delay of output 1
0Ah	phase-off time and phase delay of output 2	gate driver phase
0Bh	phase select configuration	loop filter proportional configuration
0Ch	loop filter integral configuration	slope compensation configuration
0Dh	current sense slope resistor configuration	VGG control
0Eh	internal 1	overvoltage threshold
0Fh	undervoltage threshold	spread spectrum enable
10h	internal 2	internal 3
11h	internal 4	internal 5
12h	ramp up output 1	ramp up output 2

The NVM data fields that contain more than just one register are shown in Table 48.

Table 48. Overview of multi-content NVM data field

NVM address	Name	7	6	5	4	3	2	1	0
00h					enable VGG voltage range to 16 V	AUTO	LIMP_DIS	customer write pattern to indicate that NVM is programmed: 00 is not programmed (internal defaults are used) 01 is programmed 10 is programmed 11 is not programmed (internal defaults are used)	

8.14 Autonomous mode

Autonomous mode enables the chip to load the configuration from NVM and start conversion as soon as EN is HIGH without waiting for SPI configuration from MCU or detection of SPI communication timeout.

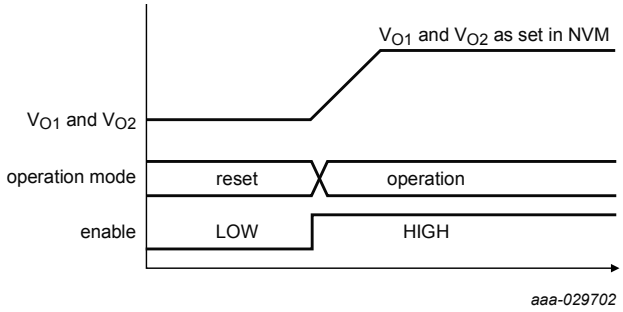


Figure 12. Autonomous mode operation

Table 49. Comparison of limp-home mode and autonomous mode

Mode	Condition	IC operation	SPI	Exit
Limp-home	the watchdog timer detects an SPI communication error	the state machine goes through power-down sequence and then copies the NVM configuration to the SPI registers to resume the operation but with the NVM setting	only access to the limp-home mode control register	microcontroller has to write the unlock pattern to the register
Autonomous	if bit AUTO is set to logic 1 in NVM	the state machine copies the required settings from NVM into the SPI registers along with the CFG_DN bit to start the converter	microcontroller less operation, default no SPI communication needed, if auto and limp-home are enabled at the same time, startup in autonomous mode	power down, reset the bit AUTO

8.14.1 Limp-home mode/autonomous mode NVM

Table 50 summarizes the NVM programming options for both limp-home and autonomous modes.

Table 50. NVM programming options

NVM address 00h	Feature
LIMP_DIS = 1; AUTO = 0	no limp-home and no autonomous
LIMP_DIS = 0; AUTO = 0	limp-home mode enabled (in case of limp-home timeout, the system applies settings from NVM)
LIMP_DIS = 1; AUTO = 1	autonomous mode enabled
LIMP_DIS = 0; AUTO = 1	startup immediately with autonomous mode; limp-home mode enabled

8.15 SPI

The ASL1507SHN; ASL2507SHN uses an SPI interface to communicate with an external microcontroller. The SPI interface can be used for setting the output voltage, reading and writing the control register.

8.15.1 SPI introduction

The SPI provides the communication link with the microcontroller, supporting multi-slave operations. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing the application to read back the registers without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- CSB - SPI chip select: active LOW
- SCLK - SPI clock: default level is LOW due to low-power concept
- SDI - SPI data input
- SDO - SPI data output: floating when pin CSB is HIGH

Bit sampling is performed on the falling clock edge and data is shifted on the rising clock edge as illustrated in Figure 13.

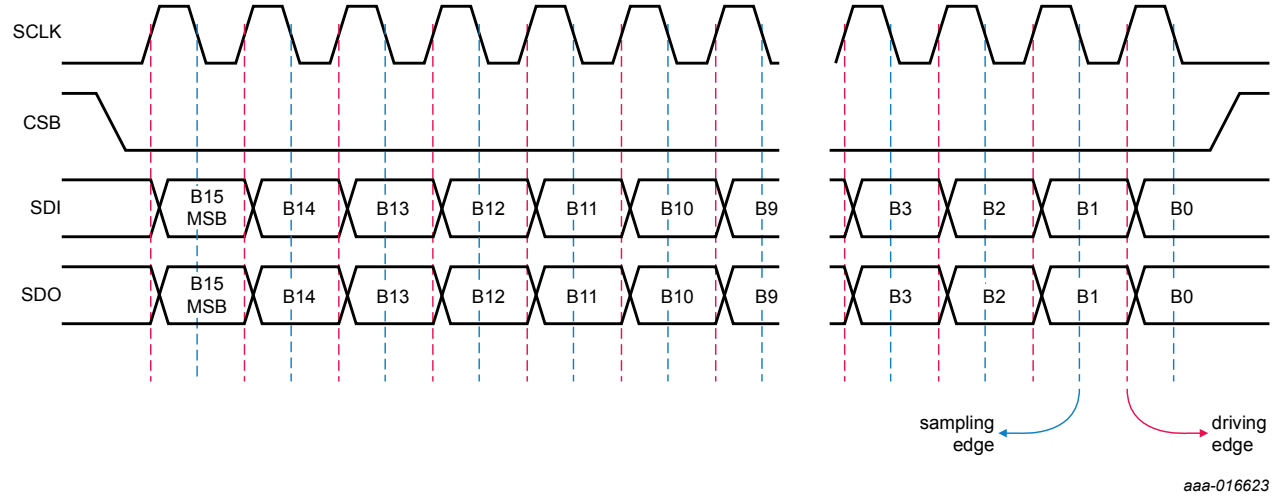


Figure 13. SPI timing protocol

The data bits of the ASL1507SHN; ASL2507SHN are arranged in registers of 1 byte length. Each register is assigned to a 7-bit address. For writing into a register, 2 bytes must be sent to the LED driver.

The first byte is an identifier byte that consists of the 7-bit address and one read-only bit. For writing, the read-only bit must be set to logic 0. The second byte is the data that is written into the register. So an SPI access consists of at least 16 bit.

Figure 14 together with Table 51 and Table 52 demonstrates the SPI frame format.

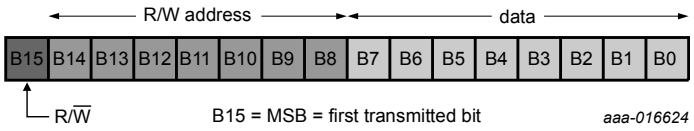


Figure 14. SPI frame format

Table 51. SPI frame format for a transition to the device

Bit	Symbol	Description	Value	Function
15	B15	R/$\overline{W}$ bit	0	write access
			1	read access
14 to 8	B[14:8]	address bits	XXX XXXX	selected address
7 to 0	B[7:0]	data bits	XXXX XXXX	transmitted data

Table 52. SPI frame format for a transition from the device[1]

Bit	Symbol	Description	Value	Function
15 to 8	B[15:8]	diagnostic register 1	XXXX XXXX	content of diagnostic register 1
7 to 0	B[7:0]	data bits	XXXX XXXX	when previous command was a valid read command, content of the register that is supposed to be read
			XXXX XXXX	when previous command was a valid write command, new content of the register that was supposed to be written

[1] The first SPI command after leaving the off mode returns 00h.

The master initiates the command sequence. The sequence begins with CSB pin pulled LOW and lasts until it is asserted HIGH.

The ASL1507SHN; ASL2507SHN also tolerates SPI accesses with a multiple of 16 bits. It allows a daisy chain configuration of the SPI.

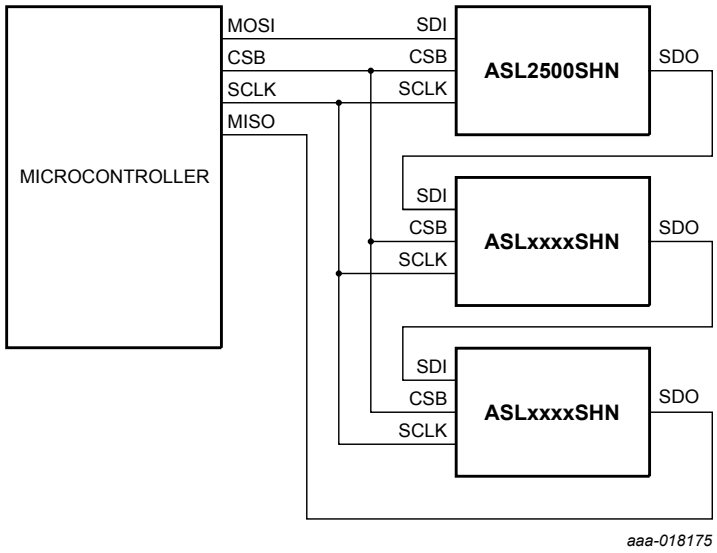


Figure 15. Daisy chain configuration

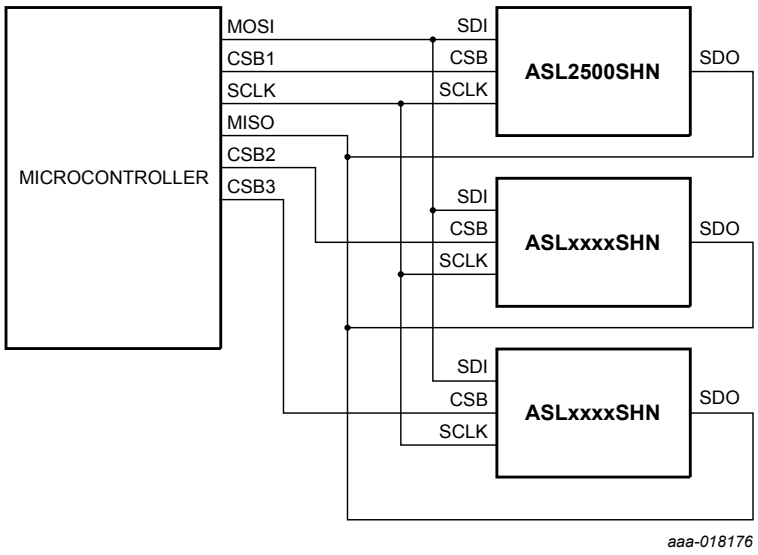


Figure 16. Physical parallel slave connection

During the SPI data transfer, the identifier byte and the actual content of the addressed registers is returned via the SDO pin. The same happens for pure read accesses. Here the read-only bit must be set to logic 1. The content of the data bytes that are transmitted to the ASL1507SHN; ASL2507SHN is ignored.

The ASL1507SHN; ASL2507SHN monitors the number of data bits that are transmitted. If the number is not 16, or a multiple of 16, then a write access is ignored and the SPI error indication bit is set.

8.15.2 Typical use case illustration (write/read)

Consider a daisy chain scheme with one master connected to four slaves in daisy chain fashion. The following commands are performed during one sequence (first sequence).

- Write data FFh to register 1Ah of slave 1
- Read from register 2h of slave 2
- Write data AFh to register 2Fh of slave 3
- Read from register 44h of slave 4

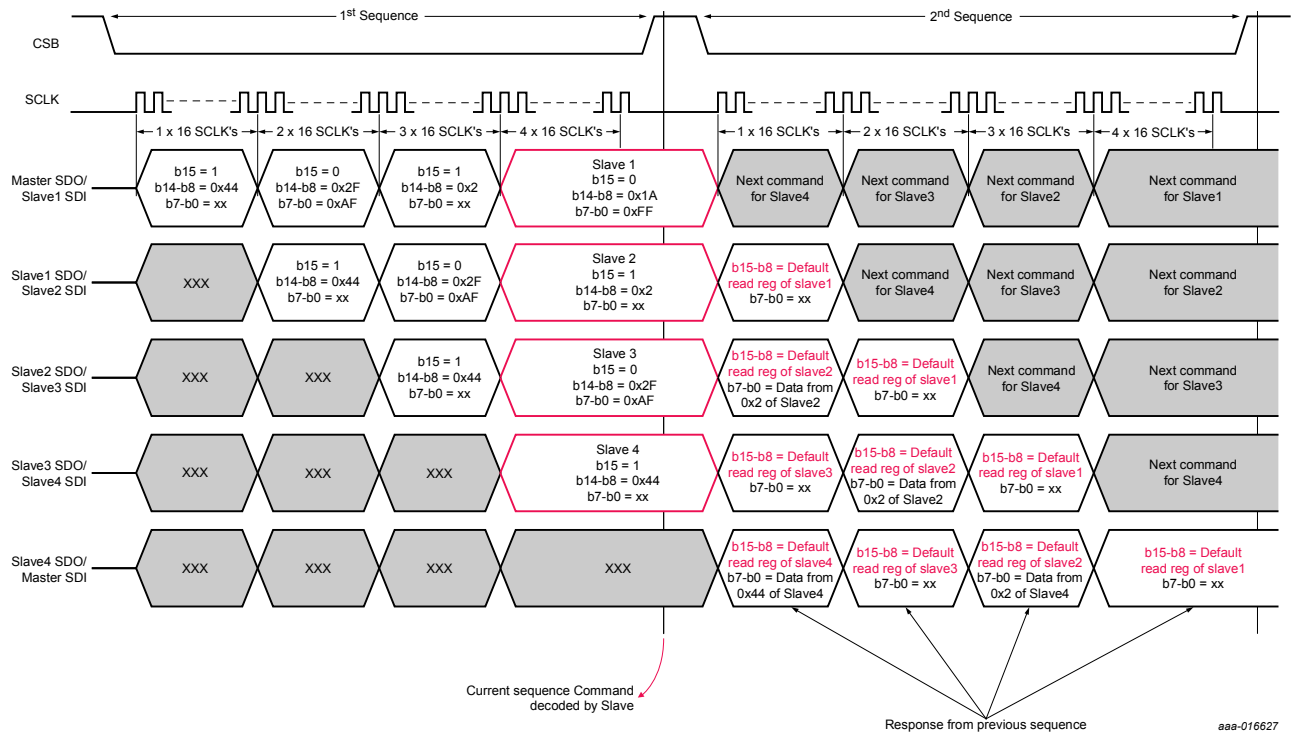


Figure 17. SPI frame format

8.15.3 Diagnostics for the SPI interface

The device is evaluating all SPI access to the device for the correctness of the commands. When the command is not allowed, the SPI_ERR bit is set. The conditions that are considered as erratic accesses are:

- SPI write is attempted to a read-only location or reserved location
- SPI write is attempted during operation to a configuration register
- SPI read is attempted from a reserved location
- SPI command does not consist of a multiple of 16 clock counts

If an SPI access is considered to be erratic, no modifications to an SPI register are made. The access after the erratic SPI command returns for bit 15 to bit 8 the content of the diagnostic register, and for bit 7 to bit 0 as 00h.

For details about the SPI_ERR bit, see Section 8.10.3.

8.15.4 Register map

8.15.4.1 Control registers

Table 53 provides an overview of the control registers and their reset value.

Table 53. Control register group overview

Address	Name	Reset value	7	6	5	4	3	2	1	0
00h	function control	00h	reserved	EN_VBAT_MEASUREMENT	-	-	CNT_CSB	VO2EN[1]	VO1EN[1]	CFG_DN
01h	gate driver enable	00h	reserved						EN_G2[2]	EN_G1[2]
03h	output voltage 1	00h	V_VO1[7:0]							
04h	output voltage 2	00h	V_VO2[7:0]							
05h	limit voltage output 1	00h	VMAX_VO1[7:0]							
06h	limit voltage output 2	00h	VMAX_VO2[7:0]							
07h	maximum coil current V_{O1}	46h	IMAX1[7:0]							
08h	maximum coil current V_{O2}	46h	IMAX2[7:0]							
1Ch	spread spectrum enable	09h	refer to Section 8.4							
1Fh	ramp up output 1	00h	reserved		RAMP1	STEP_T1[2:0]			STEP_V1[1:0]	
20h	ramp up output 2	00h	reserved		RAMP2	STEP_T2[2:0]			STEP_V2[1:0]	
3Ch	limp-home mode control		reserved	LIMP_EXIT[2:0]			LH_TIMER[2:0]			reserved

[1] Bit is locked with bit CFG_DN = 1. When bit CFG_DN = 0, bits can be changed. Read is always possible.

[2] With the gate driver enable bits, the individual gate drivers that were enabled when CFG_DN and VGG_OK were set to logic 1, can be turned on and off during operation of the system. The gate drivers that are disabled, when the CFG_DN and VGG_OK are set to logic 1, are off, even when the bits are set to logic 1 later.

8.15.4.2 Configuration registers

Table 54 provides an overview of the configuration registers. The configuration registers inside the control block can only be written in configuration mode. In the other modes, this register can only be read.

Table 54. Configuration register group overview

Address	Name	Reset value	7	6	5	4	3	2	1	0
02h	gate driver output	00h	reserved						O_G2	O_G1
09h	clock divider for V_{O1}	0Fh	CLKDIV1[7:0]							
0Ah	clock divider for V_{O2}	0Fh	CLKDIV2[7:0]							
0Bh	SS scenario logic 1	0Fh	SS_ WIDTH1[1:0]		SS_ SCEN1[1:0]		EN_P4_1	EN_P3_1	EN_P2_1	EN_P1_1
0Ch	SS scenario logic 2	0Fh	SS_ WIDTH2[1:0]		SS_ SCEN2[1:0]		EN_P4_2	EN_P3_2	EN_P2_2	EN_P1_2
0Dh	phase-off time and phase delay of output 1	39h	PHDEL1[4:0]					PHOFF1[2:0]		
0Eh	phase-off time and phase delay of output 2	39h	PHDEL2[4:0]					PHOFF2[2:0]		
0Fh	gate driver phase	00h	reserved						O_GP2	O_GP1
10h	phase selection configuration	E4h	reserved				PHSEL2[1:0]		PHSEL1[1:0]	
11h	loop filter proportional configuration	00h	PROP2[3:0]				PROP1[3:0]			
12h	loop filter integral configuration	00h	INTEG2[3:0]				INTEG1[3:0]			
13h	slope compensation configuration	88h	SLPCMP2[3:0]				SLPCMP1[3:0]			
14h	current sense slope resistor configuration	00h	reserved				SLPR2[1:0]		SLPR1[1:0]	
15h	VGG control	FFh	VGG[7:0]							
1Ah	overvoltage threshold	FFh	V_VBAT_OV[7:0]							
1Bh	undervoltage threshold	00h	V_VBAT_UV[7:0]							
36h	NVM address	00h	reserved		address for NVM data to be written or read[5:0]					
37h	NVM data MSB	00h	NVM write data MSB byte							
38h	NVM data LSB	00h	NVM write data LSB byte							
39h	ECC code	00h	EEB[7]	ECB[7]	NVM_WRITE_ECC[5:0]					
3Ah	NVM control	00h	internal				NVM_MODE[1:0]		NVM_ACCESS[1:0]	

8.15.4.3 Internal registers

The ASL1507SHN; ASL2507SHN uses the SPI registers to control some internal functions. In order to avoid any unintended behavior of the device, do not modify these registers but leave them all at their default value.

Table 55. Internal register overview

Address	Name	Reset value	7	6	5	4	3	2	1	0
19h	internal 1	82h	-	-	-	-	-	-	-	-
25h	internal 2	27h	-	-	-	-	-	-	-	-
26h	internal 3	3Bh	-	-	-	-	-	-	-	-
2Fh	internal 4	E8h	-	-	-	-	-	-	-	-
30h	internal 5	09h	-	-	-	-	-	-	-	-

8.15.4.4 Diagnostic registers

Table 56. Diagnostic register group overview

Address	Name	7	6	5	4	3	2	1	0
41h	CSB count LOW	CSB_CNT[7:0]							
42h	CSB count HIGH	CSB_CNT[15:8]							
45h	battery voltage	V_VBAT[7:0]							
46h	junction temperature	T_JUNCTION[7:0]							
54h	limp-home mode indication	internal				LHM	internal		
55h	NVM status register	internal			NVM_ ACCESS	ILLEGAL_ NVM	internal		NVM_ DONE
56h	operation mode register	STATE[4:0]					internal		
59h	NVM data MSB	NVM read data MSB byte							
5Ah	NVM data LSB	NVM read data LSB byte							
5Fh	diagnostic register	VO1_OK	VO2_OK	VGG_OK	TJ_ERR	VBAT_ UV	VBAT_ OV	SPI_ERR	VGG_ ERR

9 Limiting values

Table 57. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	EN = LOW	−0.3	+60	V
		EN = HIGH	−0.3	+40	V
V_{VCC}	voltage on pin VCC		−0.3	+5.5	V
V_{GND}	ground supply voltage	voltage between ground pins	−0.6	+0.6	V
V_{fbck}	feedback voltage	pins FB1 and FB2	−0.3	+80	V
V_O	output voltage	in accordance with register 03h and 04h	10	80	V
V_{IO}	input/output voltage	pins SDO, SDI, CSB, SCLK and EN	−0.3	+5.5	V
V_{VGG}	voltage on pin VGG		−0.3	+20	V
V_{sense}	sense voltage	pins SNL1 and SNL2	−0.3	+0.3	V
		pins SNH1 and SNH2	−0.3	+1.8	V
V_G	gate voltage	pins G1 and G2	−0.3	+10	V
V_x	voltage on pin x	internally connected pins	−0.3	+1.8	V
T_j	junction temperature		−40	+175	°C
		during programming of NVM	0	80	°C
T_{stg}	storage temperature		−55	+175	°C
V_{ESD}	electrostatic discharge voltage	HBM [1]	−2	+2	kV
		CDM [2]	−500	+500	V

[1] Human Body Model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ).
[2] Charged Device Model (CDM): according to AEC-Q100-011 (field induced charge; 4 pF).

10 Thermal characteristics

Table 58. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	HVQFN32 package JEDEC [1]	37	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer.

11 Static characteristics

Table 59. Static characteristics

Minimum and maximum values are specified for the following conditions: V_{VBAT} = 4.5 V to 40 V, V_{EN} = 4.5 V to 5.5 V, V_{VCC} = 4.5 V to 5.5 V and T_j = −40 °C to +175 °C. All voltages are defined regarding ground, positive currents flow into the IC. Typical values are given at V_{VBAT} = 40 V, V_{EN} = 5 V, V_{VCC} = 5 V and T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply pin VBAT						
I_{BAT}	battery supply current	operating; no load on VGG; gate pins LOW; one phase; one output	5	13	-	mA
		operating; no load on VGG; gate pins LOW	-	20	-	mA
I_{off}	off-state current	EN = LOW	-	-	5	µA
$V_{th(det)pon}$	power-on detection threshold voltage		-	-	4.5	V
Supply pin VCC						
I_{VCC}	supply current on pin VCC	operating	-	-	250	µA
Pin EN						
I_{EN}	current on pin EN	operating	-	-	225	µA
Output voltage						
$V_{O(acc)}$	output voltage accuracy	deviation from target set value for V_{O1}	−0.03 × V_{O1} − 0.721	-	+0.03 × V_{O1} + 0.721	V
		deviation from target set value for V_{O2}	−0.03 × V_{O2} − 0.721	-	+0.03 × V_{O2} + 0.721	V
$V_{reg(VO)VO\_OK}$	VO_OK output voltage regulator voltage	bits VO1_OK and VO2_OK are set when V_{O1} and V_{O2} are within the range regarding the target value	−5.4	-	+2.4	V
VGG output characteristics						
V_{reg}	regulator voltage	$V_{BAT} \geq V_{reg} + V_{do(reg)}$	4.46	-	10.04	V
$V_{do(reg)}$	regulator dropout voltage	$I_{reg} \leq 50$ mA; regulator in saturation	-	0.5	1.0	V
		$I_{reg} \leq 160$ mA; regulator in saturation	-	1.6	3.2	V
$V_{reg(acc)}$	regulator voltage accuracy	25 °C to $T_{j(max)}$	−5	-	+5	%
		−40 °C to +25 °C	−7	-	+5	%
$V_{reg(VGG\_OK)}$	VGG_OK regulator voltage	bit VGG_OK is set when VGG is within the range regarding the target value	-	2.4	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Serial peripheral interface inputs; pins SDI, SCLK, and CSB						
$V_{th(sw)}$	switching threshold voltage		0.3 × V_{VCC}	-	0.7 × V_{VCC}	V
$R_{pd(int)}$	internal pull-down resistance	on pin SCLK	40	-	80	kΩ
		on pin CSB	40	-	80	kΩ
		on pin SDI	40	-	80	kΩ
Serial peripheral interface data output; pin SDO						
V_{OH}	HIGH-level output voltage	I_{OH} = −4 mA; V_{VCC} = 4.5 V to 5.5 V	V_{VCC} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA; V_{VCC} = 4.5 V to 5.5 V	-	-	0.4	V
I_{LOZ}	OFF-state output leakage current	V_{CSB} = V_{VCC}; V_O = 0 V to V_{VCC}	−5	-	+5	µA
Temperature protection						
$T_{sd(otp)}$	overtemperature protection shutdown temperature		150	175	200	°C
ΔT_j	junction temperature variation	T_j = 130 °C	−20	-	+20	°C
VBAT monitoring						
$V_{BAT(acc)}$	battery supply voltage accuracy		−0.035 × V_{BAT} − 0.3606	-	+0.035 × V_{BAT} + 0.3606	V

12 Dynamic characteristics

Table 60. Dynamic characteristics

Minimum and maximum values are specified for the following conditions: V_{VBAT} = 4.5 V to 40 V, V_{EN} = 4.5 V to 5.5 V, V_{VCC} = 4.5 V to 5.5 V and T_j = −40 °C to +175 °C. All voltages are defined regarding ground, positive currents flow into the IC. Typical values are given at V_{VBAT} = 40 V, V_{EN} = 5 V, V_{VCC} = 5 V and T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{DCDC}	DC-to-DC converter frequency		125	-	700	kHz
$f_{DCDC(acc)}$	DC-to-DC converter frequency accuracy	operating; trimmed	−5	-	+5	%
$t_{startup}$	start-up time	for SPI read and write	-	-	150	µs
$f_{osc(int)}$	internal oscillator frequency		-	180	-	MHz
Serial peripheral interface timing; pins CSB, SCLK, SDI, and SDO						
$t_{cy(clk)}$	clock cycle time		250	-	-	ns
$t_{SPILEAD}$	SPI enable lead time		50	-	-	ns
t_{SPILAG}	SPI enable lag time		50	-	-	ns
$t_{clk(H)}$	clock HIGH time		125	-	-	ns
$t_{clk(L)}$	clock LOW time		125	-	-	ns
$t_{su(D)}$	data input set-up time		50	-	-	ns
$t_{h(D)}$	data input hold time		50	-	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(Q)}$	data output valid time	pin SDO; C_L = 20 pF	-	-	130	ns
$t_{WH(S)}$	chip select pulse width HIGH		250	-	-	ns
Gate driver characteristics for pin G1 and pin G2						
$t_{ch(G)}$	gate charge time	20 % to 80 %; V_{VGG} = 7.5 V; C_L = 2000 pF	-	-	30	ns
$t_{dch(G)}$	gate discharge time	80 % to 20 %; V_{VGG} = 7.5 V; C_L = 2000 pF	-	-	14	ns
Regulated voltages						
$t_{err(startup)}$	start-up error time	VGG	-	2.5	-	ms
$t_{det(err)}$	error detection time	VGG after start-up	-	31.5	-	µs
$t_{fltr(Vo)}$	output voltage filter time	VO1_OK and VO2_OK	-	31.5	-	µs

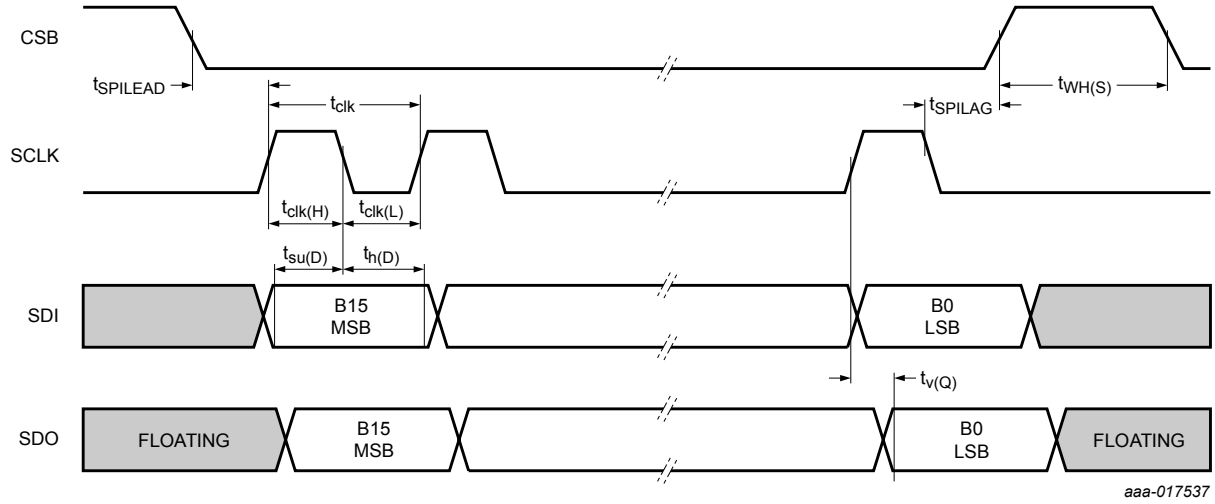


Figure 18. SPI timing diagram

13 Application information

Figure 19 provides an application example for the ASL2507SHN in a typical two-phase boost converter IC with one output voltage.

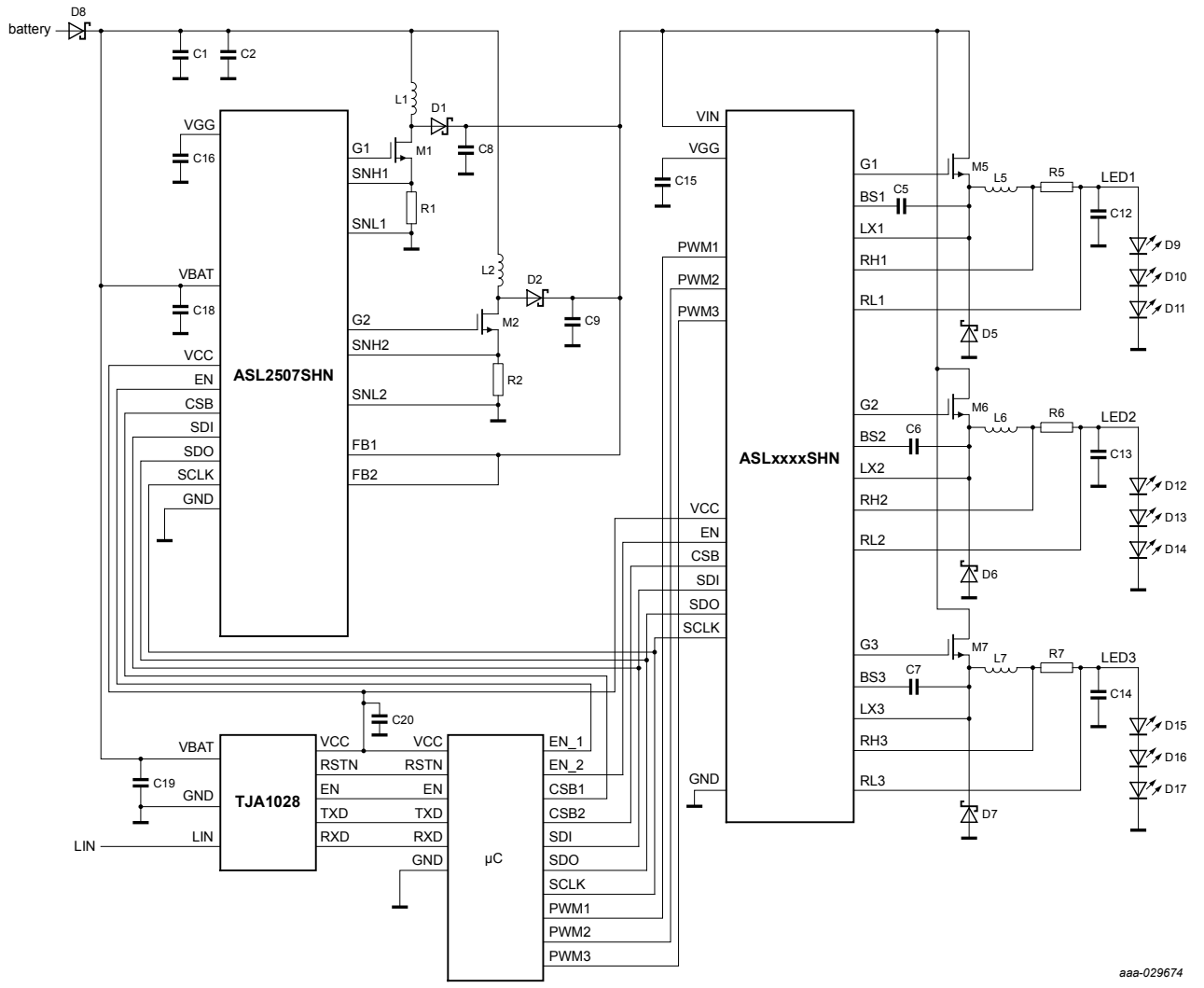


Figure 19. ASL2507SHN, configured as two-phase, single output boost converter

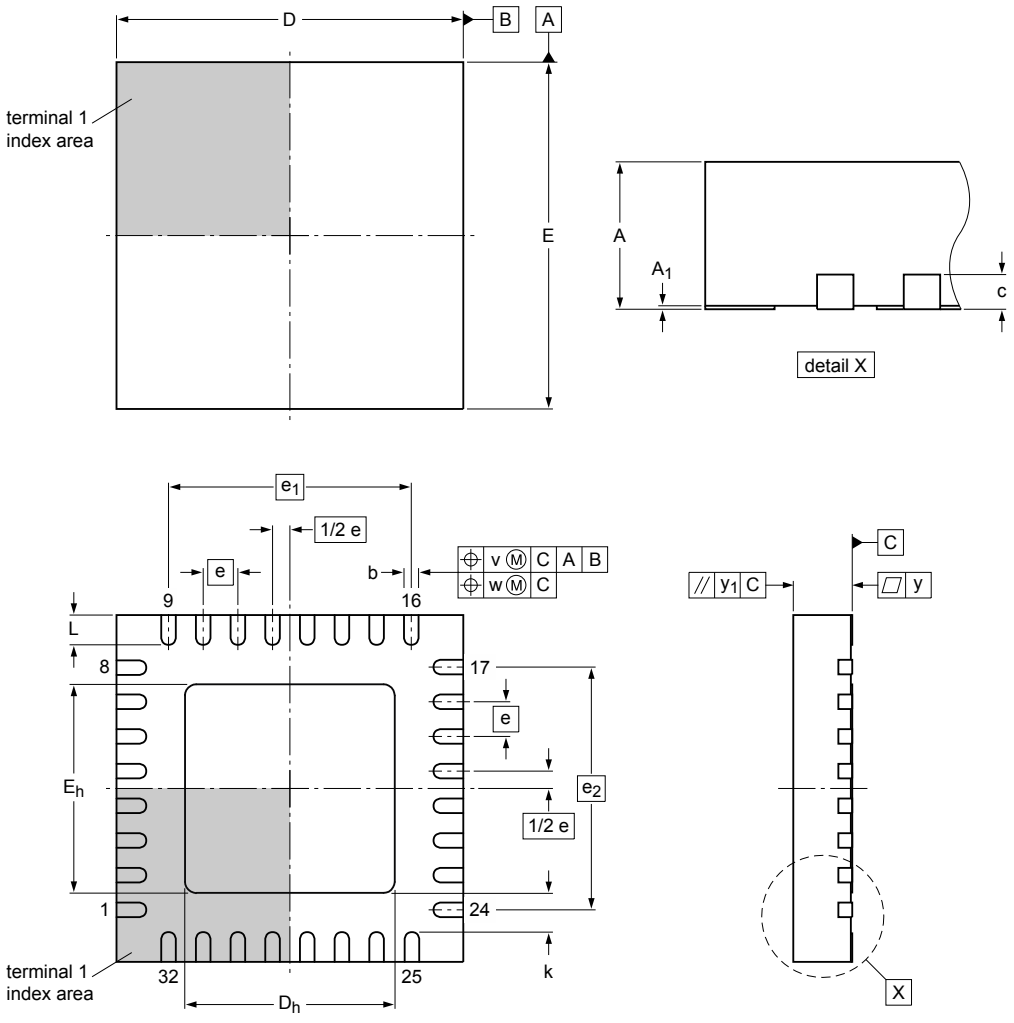
14 Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q100 - *Failure mechanism-based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15 Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-12**



Dimensions (mm are the original dimensions)

Unit	A	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	k	L	v	w	y	y_1
max	1.00	0.05	0.30		5.1	3.1	5.1	3.1					0.50				
mm nom	0.85	0.02	0.21	0.2	5.0	3.0	5.0	3.0	0.5	3.5	3.5		0.44	0.1	0.05	0.05	0.1
min	0.80	0.00	0.18		4.9	2.9	4.9	2.9				0.5	0.30				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot617-12_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT617-12		MO-220				~~13-10-14~~ 13-11-05

Figure 20. Package outline SOT617-12 (HVQFN32)

16 Revision history

Table 61. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ASL1507_ASL2507 v.1	20180426	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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