LMH0395 3G HD/SD SDI Dual Output Low Power Extended Reach Adaptive Cable Equalizer

Check for Samples: LMH0395

FEATURES

- **SMPTE 424M, SMPTE 292M, SMPTE 344M, SMPTE 259M, and DVB-ASI compliant**
- **Equalized cable lengths (Belden 1694A): 200m at 2.97 Gbps, 220m at 1.485 Gbps, and 400m at 270 Mbps**
- **Ultra low power consumption: 140 mW (dual outputs), 115 mW (single output)**
- **Dual differential outputs; second output can be independently powered down**
- **Power save mode with auto sleep control (17 mW typical power consumption in power save mode)**
- **Designed for crosstalk immunity**
- **Output de-emphasis to compensate for FR4 board trace losses**
- **Digital and analog programmable $MUTE_{REF}$ threshold**
- **Optional SPI register access**
- **Input data rates: 125 Mbps to 2.97 Gbps**
- **Internally terminated 100Ω LVDS outputs with programmable output common mode voltage and swing**
- **Programmable launch amplitude optimization**
- **Cable length indicator**
- **Single 2.5V supply operation**
- **24-pin LLP package**
- **Industrial temperature range: −40°C to +85°C**

APPLICATIONS

- **SMPTE 424M, SMPTE 292M, SMPTE 344M, and SMPTE 259M serial digital interfaces**
- **Broadcast Video routers, switchers, and distribution amplifiers**

DESCRIPTION

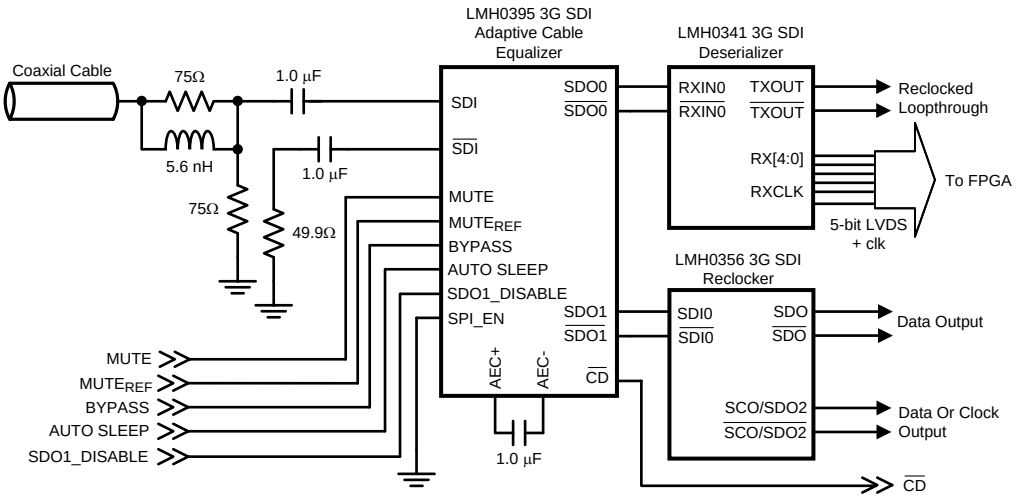
The LMH0395 3 Gbps HD/SD SDI Dual Output Low Power Extended Reach Adaptive Cable Equalizer is designed to equalize data transmitted over cable (or any media with similar dispersive loss characteristics). The equalizer operates over a wide range of data rates from 125 Mbps to 2.97 Gbps and supports SMPTE 424M, SMPTE 292M, SMPTE 344M, SMPTE 259M, and DVB-ASI standards.

The LMH0395 provides extended cable reach with improved immunity to crosstalk and ultra low power consumption. The equalizer includes active sensing circuitry that ensures robust performance and enhanced immunity to variations in the input signal launch amplitude. The LMH0395 offers power management to further reduce power consumption when no input signal is present.

The LMH0395 has two differential serial data outputs, increasing flexibility and eliminating the need for a fanout buffer on the output in many applications. The outputs may be independently enabled and controlled. The output drivers offer programmable de-emphasis for up to 40” of FR4 trace losses.

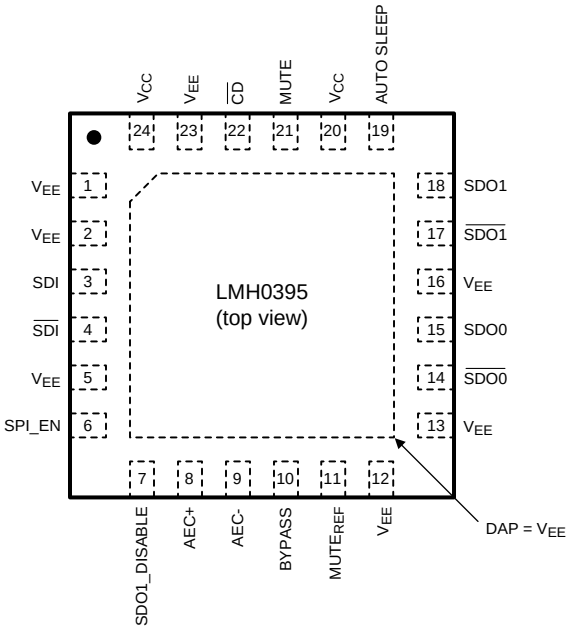
The LMH0395 supports two modes of operation. In pin mode, the LMH0395 operates with control pins to set its operating state. In SPI mode, an optional SPI serial interface can be used to access and configure multiple LMH0395 devices in a daisy-chain configuration. This allows programming the output common mode voltage and swing, output de-emphasis level, input launch amplitude, and power management settings, as well as access to a cable length indicator and all pin mode features.

Typical Application (Pin Mode)

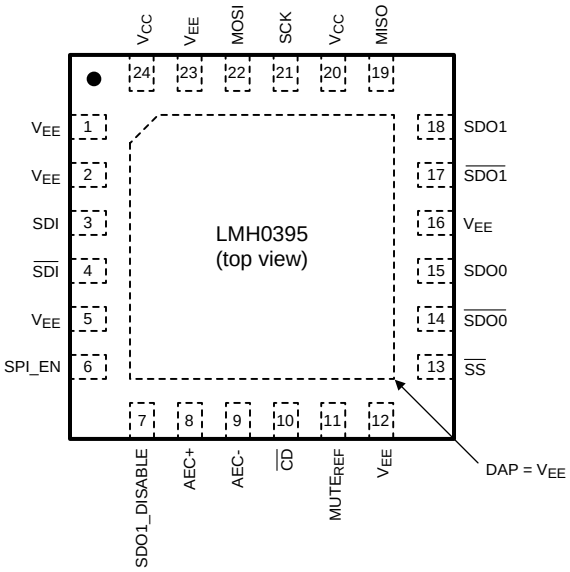


Connection Diagram

Figure 1. Pin Mode (non-SPI) / SPI_EN = GND



SPI Mode / SPI_EN = V_{CC}



The exposed die attach pad is a negative electrical terminal for this device. It should be connected to the negative power supply voltage.

Figure 2. 24-Pin LLP

Table 1. Pin Descriptions – Pin Mode (non-SPI) / SPI_EN = GND

Pin	Name	I/O, Type	Description
1	V_{EE}	Ground	Negative power supply (ground).
2	V_{EE}	Ground	Negative power supply (ground).
3	SDI	I, SDI	Serial data true input.
4	$\overline{SDI}$	I, SDI	Serial data complement input.
5	V_{EE}	Ground	Negative power supply (ground)
6	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
7	SDO1_DISABLE	I, LVCMOS	Output driver 1 (SDO1, $\overline{SDO1}$) disable. This pin has an internal pullup. H (or no connection) = Output driver 1 is in a high impedance state. L = Output driver 1 is enabled.
8	AEC+	I/O, Analog	AEC loop filter external capacitor (1µF) positive connection (capacitor is optional).
9	AEC-	I/O, Analog	AEC loop filter external capacitor (1µF) negative connection (capacitor is optional).
10	BYPASS	I, LVCMOS	Equalization bypass. This pin has an internal pulldown. H = Equalization is bypassed (no equalization occurs). L = Normal operation.
11	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
12	V_{EE}	Ground	Negative power supply (ground).
13	V_{EE}	Ground	Negative power supply (ground).
14	$\overline{SDO0}$	O, LVDS	Serial data output 0 complement.
15	SDO0	O, LVDS	Serial data output 0 true.
16	V_{EE}	Ground	Negative power supply (ground).
17	$\overline{SDO1}$	O, LVDS	Serial data output 1 complement.
18	SDO1	O, LVDS	Serial data output 1 true

Table 1. Pin Descriptions – Pin Mode (non-SPI) / SPI_EN = GND (continued)

Pin	Name	I/O, Type	Description
19	AUTO SLEEP	I, LVCMOS	Auto Sleep. AUTO SLEEP has precedence over MUTE and BYPASS. This pin has an internal pullup. H = When no input signal is detected, the device will power down and the outputs will be in a high impedance state. L = Device will not enter auto power down.
20	V_{CC}	Power	Positive power supply (+2.5V).
21	MUTE	I, LVCMOS	Output mute. $\overline{CD}$ may be tied to this pin to inhibit the output when no input signal is present. MUTE has precedence over BYPASS. This pin has an internal pulldown. H = Outputs are forced to a constant logic high state. L = Outputs are enabled.
22	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
23	V_{EE}	Ground	Negative power supply (ground).
24	V_{CC}	Power	Positive power supply (+2.5V).
DAP	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground).

Table 2. Pin Descriptions – SPI Mode / SPI_EN = V_{CC}

Pin	Name	I/O, Type	Description
1	V_{EE}	Ground	Negative power supply (ground).
2	V_{EE}	Ground	Negative power supply (ground).
3	SDI	I, SDI	Serial data true input.
4	$\overline{SDI}$	I, SDI	Serial data complement input.
5	V_{EE}	Ground	Negative power supply (ground).
6	SPI_EN	I, LVCMOS	SPI register access enable. This pin has an internal pulldown. H = SPI register access mode. L = Pin mode.
7	SDO1_DISABLE	I, LVCMOS	Output driver 1 (SDO1, $\overline{SDO1}$) disable. This pin has an internal pullup. H (or no connection) = Output driver 1 is in a high impedance state. L = Output driver 1 is enabled.
8	AEC+	I/O, Analog	AEC loop filter external capacitor (1µF) positive connection (capacitor is optional).
9	AEC-	I/O, Analog	AEC loop filter external capacitor (1µF) negative connection (capacitor is optional).
10	$\overline{CD}$	O, LVCMOS	Carrier detect. H = No input signal detected. L = Input signal detected.
11	$MUTE_{REF}$	I, Analog	Mute reference input. Sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the maximum cable to be equalized before muting. $MUTE_{REF}$ may be either unconnected or connected to ground for normal $\overline{CD}$ operation.
12	V_{EE}	Ground	Negative power supply (ground).
13	$\overline{SS}$ (SPI)	I, LVCMOS	SPI slave select. This pin has an internal pullup.
14	$\overline{SDO0}$	O, LVDS	Serial data output 0 complement.
15	SDO0	O, LVDS	Serial data output 0 true.
16	V_{EE}	Ground	Negative power supply (ground).
17	$\overline{SDO1}$	O, LVDS	Serial data output 1 complement.
18	SDO1	O, LVDS	Serial data output 1 true.
19	MISO (SPI)	O, LVCMOS	SPI Master Input / Slave Output. LMH0395 control data transmit.
20	V_{CC}	Power	Positive power supply (+2.5V).
21	SCK (SPI)	I, LVCMOS	SPI serial clock input.
22	MOSI (SPI)	I, LVCMOS	SPI Master Output / Slave Input. LMH0395 control data receive. This pin has an internal pulldown.
23	V_{EE}	Ground	Negative power supply (ground).
24	V_{CC}	Power	Positive power supply (+2.5V).
DAP	V_{EE}	Ground	Connect exposed DAP to negative power supply (ground).

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage	3.1V
Input Voltage (all inputs)	−0.3V to V_{CC}+0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	+125°C
Package Thermal Resistance θ_{JA} 24-pin LLP θ_{JC} 24-pin LLP	 +40°C/W +6°C/W
ESD Rating (HBM)	≥±6 kV
ESD Rating (MM)	≥±300V
ESD Rating (CDM)	≥±2 kV

(1) "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Recommended Operating Conditions

Supply Voltage (V_{CC} – V_{EE})	2.5V ±5%
Input Coupling Capacitance	1.0 µF
Operating Free Air Temperature (T_A)	−40°C to +85°C

DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1) (2).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{IH}	Input Voltage High Level		Logic Inputs	1.7		V_{CC}	V
V_{IL}	Input Voltage Low Level			V_{EE}		0.7	V
V_{SDI}	Input Voltage Swing	0m cable length, (3)	SDI, $\overline{SDI}$	720	800	880	mV_{P-P}
V_{CMIN}	Input Common Mode Voltage				1.65		V
V_{SSP-P}	Differential Output Voltage, P-P	100Ω load, default register settings (4),Figure 3	SDO0, $\overline{SDO0}$ SDO1, $\overline{SDO1}$	500	700	900	mV_{P-P}
V_{OD}	Differential Output Voltage			250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complimentary Output States					50	mV
V_{OS}	Offset Voltage			1.1	1.2	1.35	V
ΔV_{OS}	Change in Magnitude of V_{OS} for Complimentary Output States					50	mV
I_{OS}	Output Short Circuit Current					30	mA
	$MUTE_{REF}$ DC Voltage (floating)		$MUTE_{REF}$		1.3		V
	$MUTE_{REF}$ Range				0.8		V
V_{OH}	Output Voltage High Level	I_{OH} = -2 mA	$\overline{CD}$, MISO	2.0			V
V_{OL}	Output Voltage Low Level	I_{OL} = +2 mA				0.2	V
I_{CC}	Supply Current	Normal operation, dual outputs (5)			55	78	mA
		Normal operation, single output (5)			45	65	mA
		Power save mode			7	10	mA

(1) Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to V_{EE} = 0 Volts.
(2) Typical values are stated for V_{CC} = +2.5V and T_A = +25°C.
(3) The LMH0395 can be optimized for different launch amplitudes via the SPI.
(4) The differential output voltage and offset voltage are adjustable via the SPI.
(5) Typical I_{CC} is measured with a 2.97 Gbps input signal.

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{MIN}	Minimum Input Data Rate		SDI, $\overline{SDI}$		125		Mbps
BR_{MAX}	Maximum Input Data Rate					2970	Mbps
	Jitter for Various Cable Lengths	2.97 Gbps, Belden 1694A, 0-100 meters (2)				0.2	UI
		2.97 Gbps, Belden 1694A, 100-140 meters (2)				0.3	UI
		2.97 Gbps, Belden 1694A, 140-180 meters (2)				0.5	UI
		2.97 Gbps, Belden 1694A, 180-200 meters			0.55		UI
		1.485 Gbps, Belden 1694A, 0-200 meters (2)				0.2	UI
		1.485 Gbps, Belden 1694A, 200-220 meters			0.3		UI
		270 Mbps, Belden 1694A, 0-400 meters (2)				0.3	UI
t_r, t_f	Output Rise Time, Fall Time	20% – 80%, 100Ω load, (3), Figure 3	SDO0, $\overline{SDO0}$ SDO1, $\overline{SDO1}$		90	130	ps
	Mismatch in Rise/Fall Time	(3)			2	15	ps
t_{OS}	Output Overshoot	(3)			1	5	%
RL_{IN}	Input Return Loss	5 MHz - 1.5 GHz, (4)	SDI, $\overline{SDI}$	15			dB
		1.5 GHz - 3.0 GHz, (4)		10			dB
R_{IN}	Input Resistance	single-ended			1.5		kΩ
C_{IN}	Input Capacitance	single-ended			0.7		pF

(1) Typical values are stated for V_{CC} = +2.5V and T_A = +25°C.
(2) Based on design and characterization data over the full range of recommended operating conditions of the device. Jitter is measured in accordance with SMPTE RP 184, SMPTE RP 192, and the applicable serial data transmission standard: SMPTE 424M, SMPTE 292M, or SMPTE 259M.
(3) Specification is guaranteed by characterization.
(4) Input return loss is dependent on board design. The LMH0395 exceeds this specification on the SD395 evaluation board with a return loss network consisting of a 5.6 nH inductor in parallel with a 75Ω series resistor on the input.

SPI Interface AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (1).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
Recommended Input Timing Requirements							
f_{SCK}	SCK Frequency		SCK			20	MHz
t_{PH}	SCK Pulse Width High	Figure 4, Figure 5		40			% SCK period
t_{PL}	SCK Pulse Width Low			40			% SCK period
t_{SU}	MOSI Setup Time	Figure 4, Figure 5	MOSI	4			ns
t_H	MOSI Hold Time			4			ns
t_{SSSU}	$\overline{SS}$ Setup Time	Figure 4, Figure 5	$\overline{SS}$	14			ns
t_{SSH}	$\overline{SS}$ Hold Time			4			ns
t_{SSOF}	$\overline{SS}$ Off Time			1			SCK period
Switching Characteristics							
t_{ODZ}	MISO Driven-to-Tristate Time	Figure 5	MISO			20	ns
t_{OZD}	MISO Tristate-to-Driven Time					10	ns
t_{OD}	MISO Output Delay Time					15	ns

(1) Typical values are stated for V_{CC} = +2.5V and T_A = +25°C.

Timing Diagrams

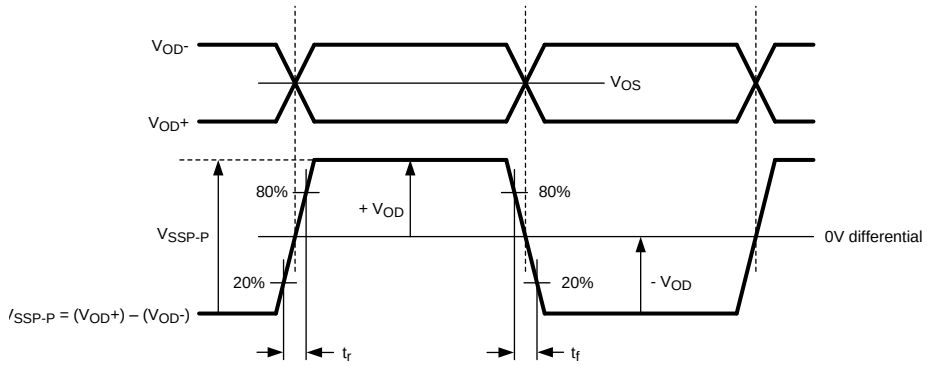


Figure 3. LVDS Output Voltage, Offset, and Timing Parameters

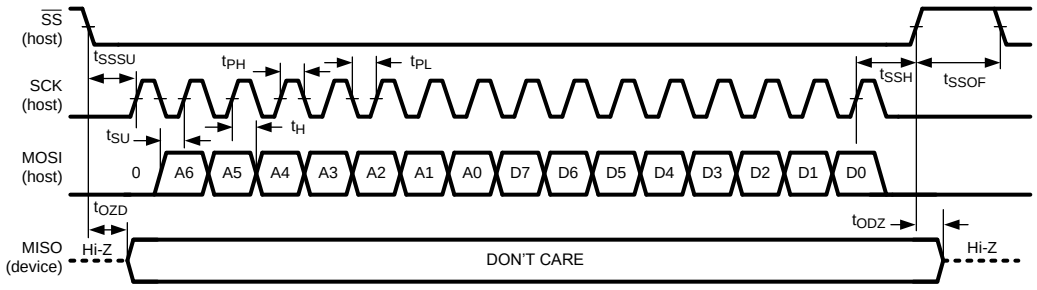


Figure 4. SPI Write

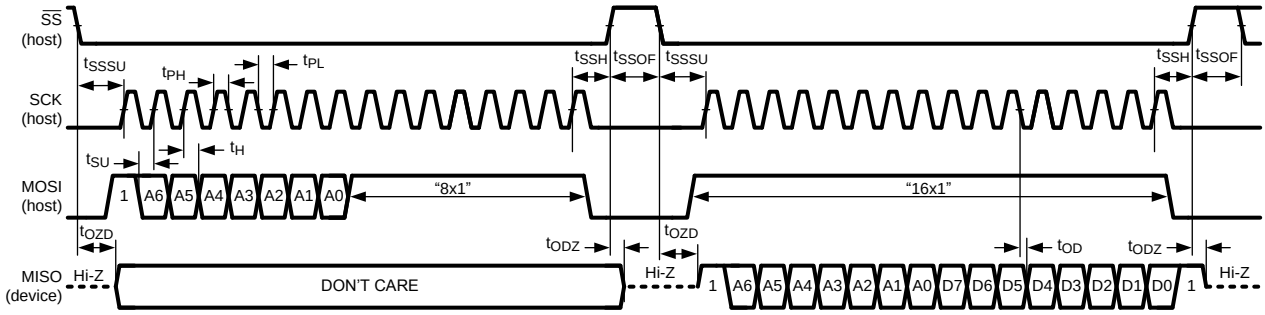
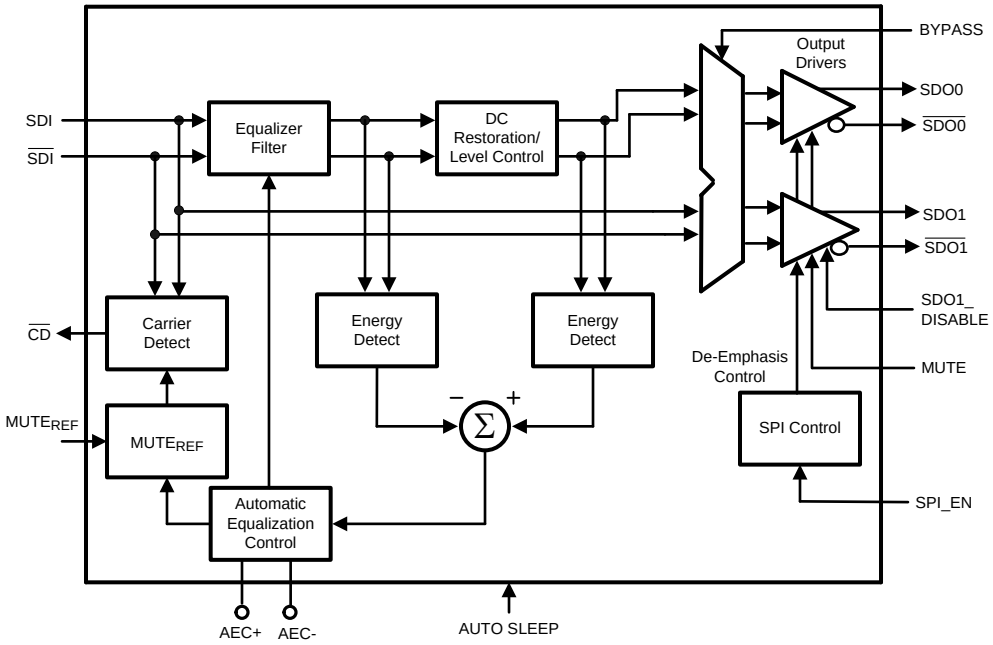


Figure 5. SPI Read

Block Diagram(Pin Mode)



Device Operation

BLOCK DESCRIPTION

The **Equalizer Filter** block is a multi-stage adaptive filter. If Bypass is high, the equalizer filter is disabled.

The **DC Restoration / Level Control** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restoration circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The signals before and after the DC Restoration / Level Control block are used to generate the **Automatic Equalization Control (AEC)** signal. This control signal sets the gain and bandwidth of the equalizer filter.

The **Carrier Detect** block generates the carrier detect signal based on the SDI input and an adjustment from the **Mute Reference** block.

The **SPI Control** block uses the MOSI, MISO, SCK, and $\overline{SS}$ signals in SPI mode to control the SPI registers. SPI_EN selects between SPI mode and pin mode. In pin mode, SPI_EN is driven logic low.

The **Output Drivers** produce SDO0, $\overline{SDO0}$, SDO1, and $\overline{SDO1}$.

MUTE REFERENCE (MUTE$_{REF}$)

The mute reference sets the threshold for $\overline{CD}$ and (with $\overline{CD}$ tied to MUTE) determines the amount of cable to equalize before automatically muting the outputs. This is set by applying a voltage inversely proportional to the length of cable to equalize. The applied voltage must be greater than the MUTE$_{REF}$ floating voltage (typically 1.3V) in order to change the $\overline{CD}$ threshold. As the applied MUTE$_{REF}$ voltage is increased, the amount of cable that can be equalized before carrier detect is de-asserted and the outputs are muted is decreased. MUTE$_{REF}$ may be left unconnected or connected to ground for normal $\overline{CD}$ operation. Optionally, the LMH0395 allows the mute reference to be set digitally via SPI register 03h.

Figure 6 shows the minimum MUTE$_{REF}$ input voltage required to force carrier detect to inactive vs. Belden 1694A cable length. The results shown are valid for Belden 1694A cable lengths of 0-200m at 2.97 Gbps, 0-220m at 1.485 Gbps, and 0-400m at 270 Mbps.

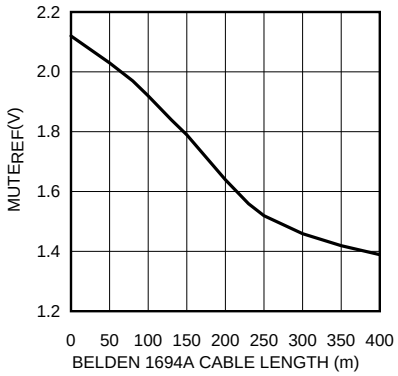


Figure 6. MUTE$_{REF}$ vs. Belden 1694A Cable Length

CARRIER DETECT ($\overline{CD}$) AND MUTE

Carrier detect $\overline{CD}$ indicates if a valid signal is present at the LMH0395 input. This signal is logical OR operation of internal energy detector and MUTE$_{REF}$ setting (if used). Internal energy detector detects energy across different data rates. If MUTE$_{REF}$ is used, the carrier detect threshold will be altered accordingly. $\overline{CD}$ provides a high voltage when no signal is present at the LMH0395 input. $\overline{CD}$ is low when a valid input signal is detected.

MUTE can be used to manually mute or enable the output drivers. Applying a high input to MUTE will mute the LMH0395 outputs by forcing the output to a logic 1. Applying a low input will force the outputs to be active.

In pin mode, $\overline{CD}$ and MUTE may be tied together to automatically mute the output when no input signal is present.

AUTO SLEEP

The auto sleep mode allows the LMH0395 to power down when no input signal is detected. If the AUTO SLEEP pin is set high, the LMH0395 goes into a deep power save mode when no signal is detected. The device powers on again once an input signal is detected. If the AUTO SLEEP pin is set low, the LMH0395 will always be on and will not enter power save mode. The auto sleep functionality can be turned off by setting AUTO SLEEP low or tying this pin to ground. An additional auto sleep setting available in SPI mode can be used to force the equalizer to power down regardless of whether there is an input signal or not. Auto sleep has precedence over mute and bypass modes.

In auto sleep mode, the time to power down the equalizer when the input signal is removed is less than 200 µs and should not have any impact on the system timing requirements. The device will wake up automatically once an input signal is detected, and the delay between signal detection and full functionality of the equalizer is negligible (about 5 ms). The overall system will be limited only by the settling time constant of the equalizer adaptation loop.

INPUT INTERFACING

The LMH0395 accepts either differential or single-ended input. The input must be AC coupled. The Typical Application (Pin Mode) diagram shows the typical configuration for a single-ended input. The unused input must be properly terminated as shown.

The LMH0395 can be optimized for different launch amplitudes via the SPI (see LAUNCH AMPLITUDE OPTIMIZATION in the SPI Register Access section).

The LMH0395 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

OUTPUT INTERFACING

The LMH0395 dual output differential pairs, SDO0, $\overline{\text{SDO0}}$, SDO1, and $\overline{\text{SDO1}}$ are internally terminated 100Ω LVDS outputs. These outputs can be DC coupled to most common differential receivers.

The default output common mode voltage (V_{OS}) is 1.2V. The output common mode voltage may be adjusted via the SPI in 200 mV increments, from 0.8V to 1.2V (see OUTPUT DRIVER ADJUSTMENTS AND DE-EMPHASIS SETTING in the SPI Register Access section). When the output common mode is supply referenced, the common mode voltage is about 1.35V (for 700 mV_{P-P} differential swing). This adjustable output common mode voltage offers flexibility for interfacing to many types of receivers.

The default differential output swing (V_{SSP-P}) is 700 mV_{P-P}. The differential output swing may be adjusted via the SPI. Valid options are 400, 600, 700, or 800 mV_{P-P} (see OUTPUT DRIVER ADJUSTMENTS AND DE-EMPHASIS SETTING in the SPI Register Access section).

The LMH0395 output should be DC coupled to the input of the receiving device where possible. 100Ω differential transmission lines should be used to connect between the LMH0395 outputs and the input of the receiving device.

The LMH0395 output should not be DC coupled to CML inputs. If there are strong pullup resistors (i.e. 50Ω) at the receiving device, AC coupling should be used. The value of these AC-coupling capacitors should be large enough (typically 4.7 µF) to accommodate for the SD pathological video pattern.

Figure 7 shows an example of a DC-coupled interface between the LMH0395 and LMH0346 SDI reclocker. The differential transmission line should be terminated with a 100Ω resistor at the receiving device as shown. The resistor should be placed as close as possible to the LMH0346 input. If desired, this network may be terminated with two 50Ω resistors and a center-tap capacitor to ground in place of the single 100Ω resistor.

Figure 8 shows an example of a DC-coupled interface between the LMH0395 and LMH0356 SDI reclocker. The LMH0356 inputs have internal 50Ω terminations (100Ω differential) to terminate the transmission line, so no additional components are required.

The LMH0395 output drivers are equipped with programmable output de-emphasis to minimize inter-symbol interference caused by the loss dispersion from driving signals across PCB traces (see OUTPUT DRIVER ADJUSTMENTS AND DE-EMPHASIS SETTING in the SPI Register Access section). De-emphasis works with all combinations of output common mode voltage and output voltage swing settings to support DC coupling to the receiving device.

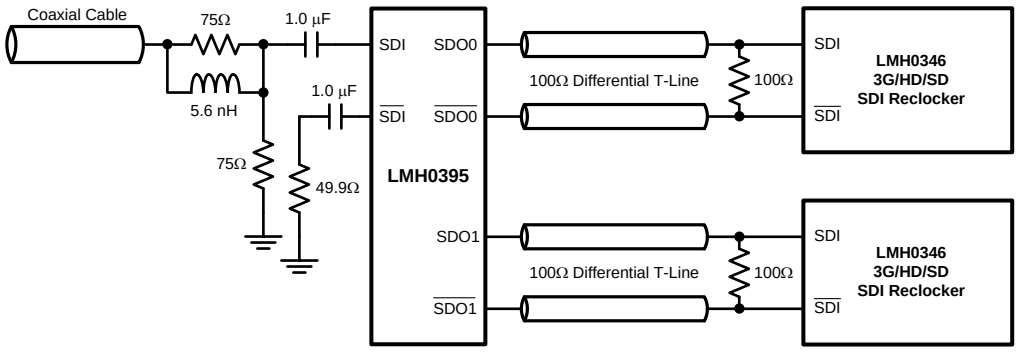


Figure 7. DC Output Interface to LMH0346 Reclocker

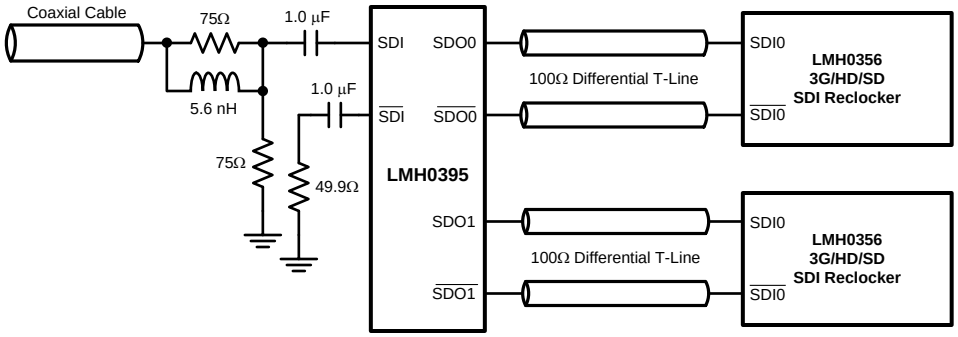


Figure 8. DC Output Interface to LMH0356 Reclocker

SPI Register Access

Setting SPI_EN high enables the optional SPI register access mode. In SPI mode, the LMH0395 provides register access to all of its features along with a cable length indicator, programmable output de-emphasis, programmable output common mode voltage and swing, digital $MUTE_{REF}$, and launch amplitude optimization. There are eight supported 8-bit registers in the device (see Table 3). The LMH0395 supports SPI daisy-chaining among an unlimited number of LMH0395 devices.

SPI Transaction Overview

Each SPI transaction to a single device is 16-bits long. The transaction is initiated by driving $\overline{SS}$ low, and completed by returning $\overline{SS}$ high. The 16-bit MOSI payload consists of the read/write command ("1" for reads and "0" for writes), the seven address bits of the device register (MSB first), and the eight data bits (MSB first). The LMH0395 MOSI input data is latched on the rising edge of SCK, and the MISO output data is sourced on the falling edge of SCK.

In order to facilitate daisy-chaining, the prior SPI command, address, and data are shifted out on the MISO output as the current command, address, and data are shifted in on the MOSI input. For SPI writes, the MISO output is typically ignored as "Don't Care" data. For SPI reads, the MISO output provides the requested read data (after 16 periods of SCK). The MISO output is active when $\overline{SS}$ low, and tri-stated when $\overline{SS}$ is high.

SPI Write

The SPI write is shown in Figure 4. The SPI write is 16 bits long. The 16-bit MOSI payload consists of a "0" (write command), seven address bits, and eight data bits. The $\overline{SS}$ signal is driven low, and the 16 bits are sent to the LMH0395's MOSI input. After the SPI write, $\overline{SS}$ must return high. The prior SPI command, address, and data shifted out on the MISO output during the SPI write is shown as "Don't Care" on the MISO output in Figure 4.

SPI Read

The SPI read is shown in Figure 5. The SPI read is 32 bits long, consisting of a 16-bit read transaction followed by a 16-bit dummy read transaction to shift out the read data on the MISO output. The first 16-bit MOSI payload consists of a "1" (read command), seven address bits, and eight "1"s which are ignored. The second 16-bit MOSI payload consists of 16 "1"s which are ignored but necessary in order to shift out the requested read data on the MISO output. The $\overline{SS}$ signal is driven low, and the first 16 bits are sent to the LMH0395's MOSI input. The prior SPI command, address, and data are shifted out on the MISO output during the first 16-bit transaction, and are typically ignored (this is shown as "Don't Care" on the MISO output in Figure 5. $\overline{SS}$ must return high and then is driven low again before the second 16 bits (all "1"s) are sent to the LMH0395's MOSI input. Once again, the prior SPI command, address, and data are shifted out on the MISO output, but this data now includes the requested read data. The read data is available on the MISO output during the second 8 bits of the 16-bit dummy read transaction, as shown by D7-D0 in Figure 5.

SPI Daisy-Chain Operation

The LMH0395 SPI controller supports daisy-chaining the serial data between an unlimited number of LMH0395 devices. Each LMH0395 device is directly connected to the SCK and $\overline{SS}$ pins on the host. However, only the first LMH0395 device in the chain is connected to the host's MOSI pin, and only the last device in the chain is connected to the host's MISO pin. The MISO pin of each intermediate LMH0395 device in the chain is connected to the MOSI pin of the next LMH0395 device, creating a serial shift register. This daisy-chain architecture is shown in Figure 9.

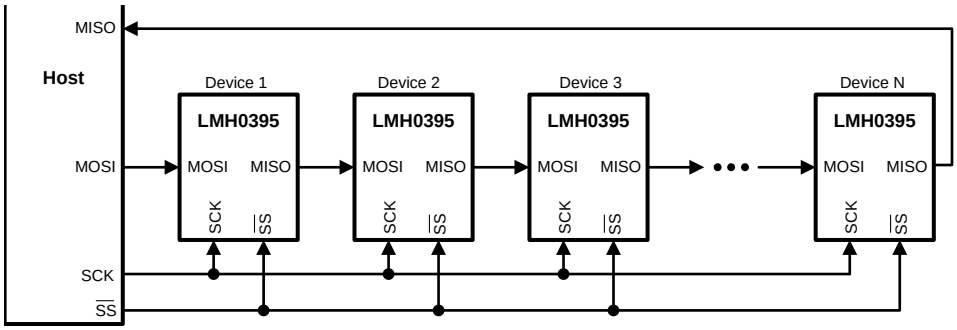


Figure 9. SPI Daisy Chain System Architecture

In a daisy-chain configuration of N LMH0395 devices, the host conceptually sees a shift register of length 16xN. Therefore the length of SPI transactions (as previously described) is 16xN bits, and $\overline{SS}$ must be asserted for 16xN clock cycles for each SPI transaction.

SPI Daisy-Chain Write

Figure 10 shows the SPI daisy-chain write for a daisy-chain of N devices. The $\overline{SS}$ signal is driven low and SCK is toggled for 16xN clocks. The 16xN bit MOSI payload (sent to Device 1 in the daisy-chain) consists of the 16-bit SPI write data for Device N (the last device in the chain), followed by the write data for Device N-1, Device N-2, etc., ending with the write data for Device 1 (the first device in the chain). The 16-bit SPI write data for each device consists of a "0" (write command), seven address bits, and eight data bits. After the SPI daisy-chain write, $\overline{SS}$ must return high and then the write occurs for all devices in the daisy-chain.

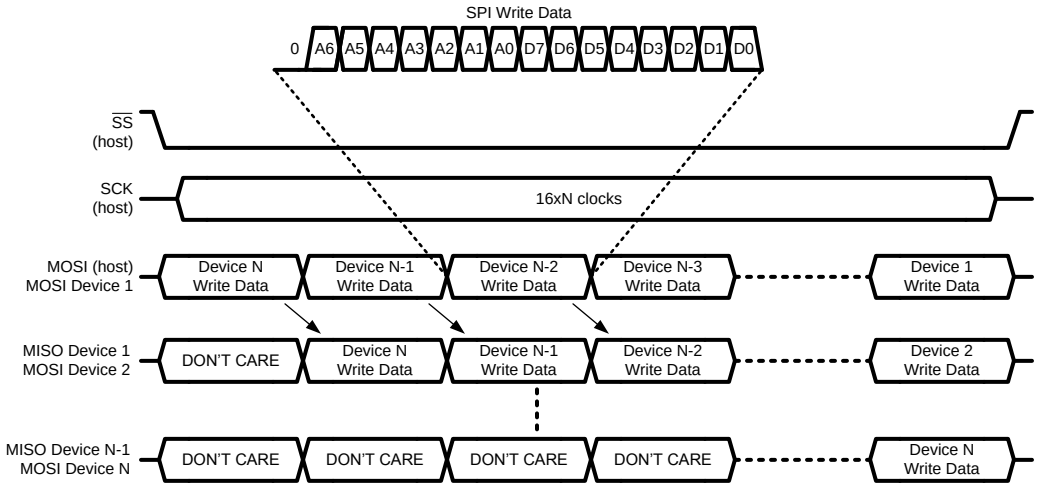


Figure 10. SPI Daisy-Chain Write

SPI Daisy-Chain Read

Figure 11 shows the SPI daisy-chain read for a daisy-chain of N devices. The SPI daisy-chain read is 32xN bits long, consisting of 16xN bits for the read transaction followed by 16xN bits for the dummy read transaction (all "1"s) to shift out the read data on the MISO output. The $\overline{SS}$ signal is driven low and SCK is toggled for 16xN clocks. The first 16xN bit MOSI payload (sent to Device 1 in the daisy-chain) consists of the 16-bit SPI read data for Device N (the last device in the chain), followed by the read data for Device N-1, Device N-2, etc., ending with

the read data for Device 1 (the first device in the chain). The 16-bit SPI read data for each device consists of a "1" (read command), seven address bits, and eight "1"s (which are ignored). After the first 16xN bit transaction, $\overline{SS}$ must return high (to latch the data) and then is driven low again before the second 16xN bit transaction of all "1"s is sent to the MOSI input. The requested read data is shifted out on MISO starting with the data for Device N and ending with the data for Device 1. After this transaction, $\overline{SS}$ must return high.

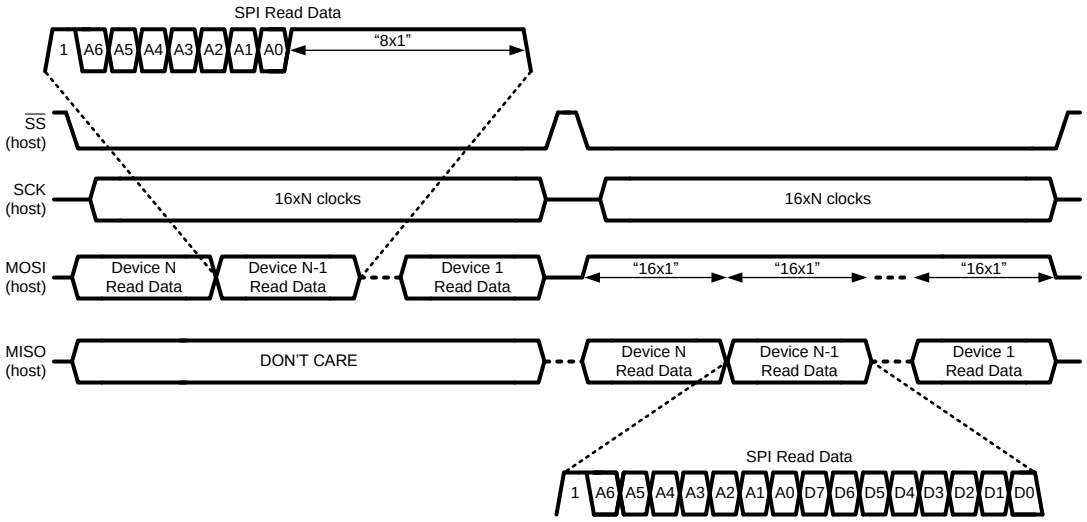


Figure 11. SPI Daisy-Chain Read

SPI Daisy-Chain Read and Write Example

The following example further clarifies LMH0395 SPI daisy-chain operation. Assume a daisy-chain of three LMH0395 devices (Device 1, Device 2, and Device 3), with Device 1 as the first device in the chain and Device 3 as the last device in the chain, as shown by the first three devices in Figure 9. Since there are three devices in the daisy-chain, each SPI transaction is 48-bits long.

This example shows an SPI operation combining SPI reads and writes in order to accomplish the following three tasks:

1. Write 0x22 to register 0x01 of Device 1 in order to set the output swing of output driver 0 to 400 mV_{P-P}.
2. Read the contents of register 0x00 of Device 2.
3. Write 0x10 to register 0x00 of Device 3 in order to force the sleep mode.

Figure 12 shows the two 48-bit SPI transactions required to complete these tasks (the bits are shifted in left to right).

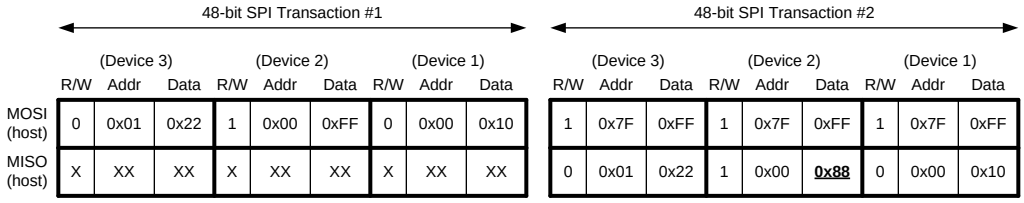


Figure 12. SPI Daisy-Chain Read and Write Example

The following occurs at the end of the first transaction:

1. Write 0x22 to register 0x01 of Device 1.
2. Latch the data from register 0x00 of Device 2.
3. Write 0x10 to register 0x00 of Device 3.

In the second transaction, three dummy reads (each consisting of 16 "1"s) are shifted in, and the read data from Device 2 (with value 0x88) appears on MISO in the 25th through 32nd clock cycles.

SPI Daisy-Chain Length Detection

A useful operation for the host may be to detect the length of the daisy-chain. This is a simple matter of shifting in a series of dummy reads with a known data value (such as 0x5A). For an SPI daisy-chain of N LMH0395 devices, the known data value will appear on the host's MISO pin after N+1 writes. Assuming a daisy-chain of three LMH0395 devices, the result of this operation is shown in Figure 13.

	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data
MOSI (host)	1	0x7F	0x5A	1	0x7F	0x5A	1	0x7F	0x5A	1	0x7F	0x5A
MISO (host)	X	XX	XX	X	XX	XX	X	XX	XX	**1**	**0x7F**	**0x5A**

Figure 13. SPI Daisy-Chain Length Detection

OUTPUT DRIVER ADJUSTMENTS AND DE-EMPHASIS SETTING

The output driver swing (amplitude), offset voltage (common mode voltage), and de-emphasis level are adjustable via SPI register 01h. The output driver to control with SPI register 01h (either output driver 0 or output driver 1) can be selected via bit 2 of SPI register 00h.

The output swing is adjustable via bits [7:6] of SPI register 01h. The default value for these register bits is “10” for a peak to peak differential output voltage of 700 mV_{P-P}. The output swing can be set for 400 mV_{P-P}, 600 mV_{P-P} , 700 mV_{P-P}, or 800 mV_{P-P}.

The offset voltage is adjustable via bits [5:4] of SPI register 01h. The default value for these register bits is “10” for an output offset of 1.2V. The output common mode voltage may be adjusted in 200 mV increments, from 0.8V to 1.2V. It can be set to “11” for the maximum offset voltage. At this maximum offset voltage setting, the outputs are referenced to the positive supply and the offset voltage is around 1.35V.

The output de-emphasis is turned on or off by bit 3 of SPI register 01h, and the de-emphasis level is set by bits [2:1] of SPI register 01h. The output de-emphasis level may be set for 0 dB (for driving up to 10” FR4), 3 dB (for driving 10-20” FR4), 5 dB (for driving 20-30” FR4), or 7 dB (for driving 30-40” FR4).

LAUNCH AMPLITUDE OPTIMIZATION

The LMH0395 can compensate for attenuation of the input signal prior to the equalizer. This compensation is useful for applications with a passive splitter at the equalizer input or a non-ideal input termination network, and is controlled by SPI register 02h.

Bit 7 of SPI register 02h is used for the launch amplitude setting. At the default setting of “0”, the LMH0395 operates normally and expects a launch amplitude of 800 mV_{P-P}. Bit 7 may be set to “1” to optimize the LMH0395 for input signals with 6 dB of attenuation (400 mV_{P-P}).

CABLE LENGTH INDICATOR (CLI)

The cable length indicator (CLI) provides an indication of the length of the cable attached to input. CLI is accessible via bits [7:0] of SPI register 06h. The 8-bit setting ranges in decimal value from 0 to 247 (“00000000” to “11110111” binary), corresponding to 0 to 400m of Belden 1694A cable. For 3G and HD input, CLI is 1.25m per step. For SD input, CLI is 1.25m per step, less 20m, from 0 to 191 decimal, and 3.5m per step from 192 to 247 decimal.

To calculate the Belden 1694A cable length (in meters) from the CLI decimal value for 3G or HD input:

$$\text{Cable Length} = \text{CLI} \times 1.25 \quad (1)$$

To calculate the Belden 1694A cable length (in meters) from the CLI decimal value for SD input:

$$For\ CLI \le 191,$$
$$Cable\ Length = (CLI \times 1.25) - 20$$
$$For\ CLI > 191,$$
$$Cable\ Length = ((191 \times 1.25) - 20) + ((CLI - 191) \times 3.5) \quad (2)$$

Figure 14 shows typical CLI values vs. Belden 1694A cable length. CLI is valid for Belden 1694A cable lengths of 0-200m at 2.97 Gbps, 0-220m at 1.485 Gbps, and 0-400m at 270 Mbps. Note: Given the continuous adaptive nature of the equalizer, this setting changes by some steps constantly.

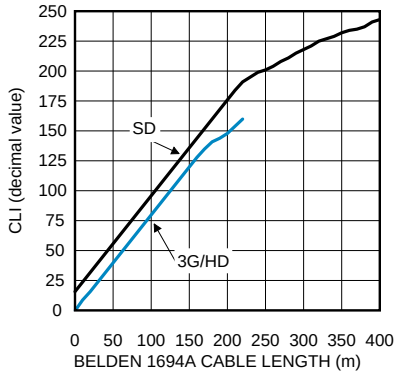


Figure 14. CLI vs. Belden 1694A Cable Length

Application Information

APPLICATION CIRCUIT (SPI MODE)

Figure 15 shows the application circuit for the LMH0395 in SPI mode. (Note: The application circuit shows an external capacitor connected between the AEC+ and AEC- pins as commonly configured in legacy equalizers. This capacitor is optional and not necessary for the LMH0395; the AEC+ and AEC- pins may be left unconnected with no change in performance.)

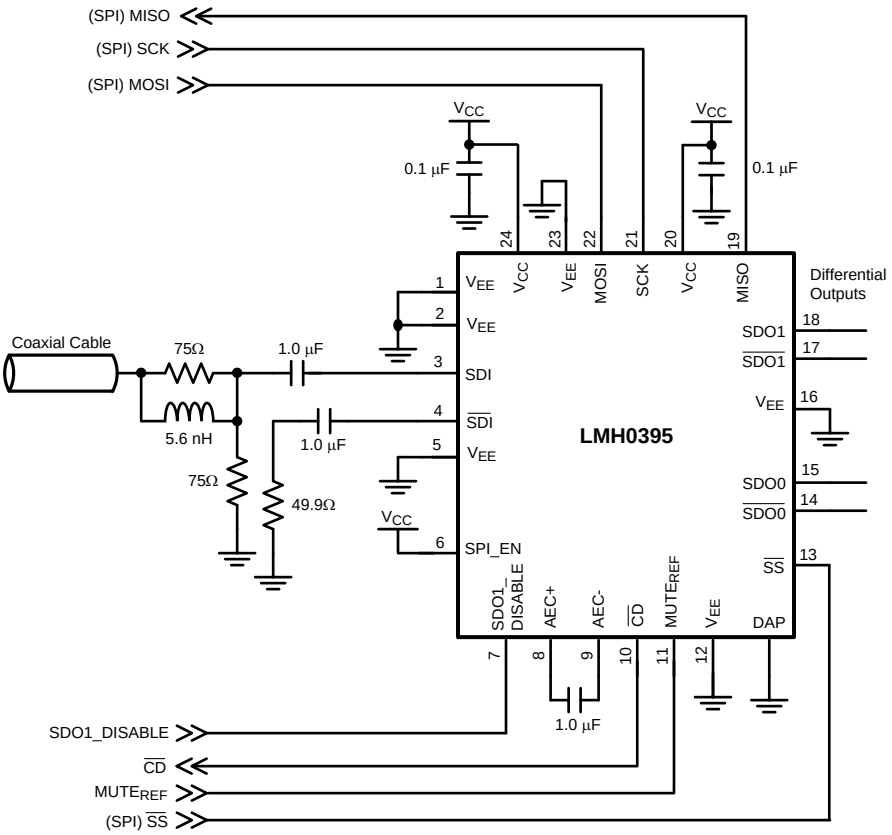


Figure 15. Application Circuit (SPI Mode)

INTERFACING TO 3.3V SPI

The LMH0395 may be controlled via optional SPI register access. The LMH0395 SPI pins support 2.5V LVCMOS logic levels and are compliant with JEDEC JESD8-5 (see DC Electrical Characteristics). Care must be taken when interfacing the SPI pins to other voltage levels.

The 2.5V LMH0395 SPI pins may be interfaced to a 3.3V compliant SPI host by using a voltage divider or level translator. One implementation is a simple resistive voltage divider as shown in Figure 16.

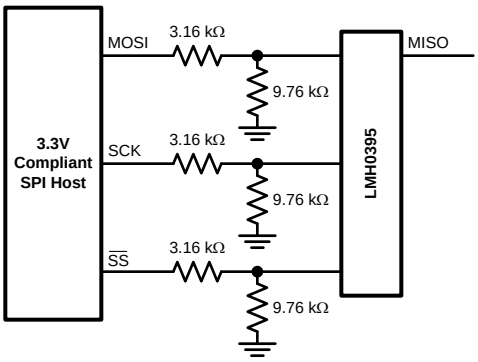


Figure 16. 3.3V SPI Interfacing

CROSSTALK IMMUNITY

Single-ended SDI signals are susceptible to crosstalk and good design practices should be employed to minimize its effects. Most crosstalk originates through capacitive coupling from adjacent signals routed closely together via traces and connectors. To reduce capacitive coupling, SDI signals should be appropriately spaced apart or insulated from one another. This can be accomplished by physically isolating signal traces in the layout and by providing additional ground pins between signal traces in connectors as necessary. These techniques help to reduce crosstalk but do not eliminate it.

The LMH0395 was designed specifically with crosstalk in mind and incorporates advanced circuit design techniques that help to isolate and minimize the effects of cross-coupling in high-density system designs. Lab evaluations and customer testimonials have shown other adaptive cable equalizers are much more susceptible to crosstalk, resulting in significant cable reach degradation. The LMH0395's enhanced design results in minimal degradation in cable reach in the presence of crosstalk and overall superior immunity against cross-coupling from neighboring channels.

PCB LAYOUT RECOMMENDATIONS

For information on layout and soldering of the LLP package, pease refer to the following application note: **AN-1187, "Leadless Leadframe Package (LLP)."**

The SMPTE 424M, 292M, and 259M standards have stringent requirements for the input return loss of receivers, which essentially specify how closely the input must resemble a 75Ω network. Any non-idealities in the network between the BNC and the equalizer will degrade the input return loss. Care must be taken to minimize impedance discontinuities between the BNC and the equalizer to ensure that the characteristic impedance of this trace is 75Ω. Please consider the following PCB recommendations:

- Use surface mount components, and use the smallest components available. In addition, use the smallest size component pads.
- Select trace widths that minimize the impedance mismatch between the BNC and the equalizer.
- Select a board stack up that supports both 75Ω single-ended traces and 100Ω loosely-coupled differential traces.
- Place return loss components closest to the equalizer input pins.
- Maintain symmetry on the complimentary signals.
- Route 100Ω traces uniformly (keep trace widths and trace spacing uniform along the trace).
- Avoid sharp bends in the signal path; use 45° or radial bends.
- Place bypass capacitors close to each power pin, and use the shortest path to connect equalizer power and ground pins to the respective power or ground planes.
- Remove ground plane under input/output components to minimize parasitic capacitance.

SPI Registers

Table 3. SPI Registers

Address	R/W	Name	Bits	Field	Default	Description
00h	R/W	General Control	7	Carrier Detect		Read only. 0: No carrier detected. 1: Carrier detected.
			6	Mute	0	Mute has precedence over Bypass. 0: Normal operation. 1: Outputs muted.
			5	Bypass	0	0: Normal operation. 1: Equalizer bypassed.
			4:3	Sleep Mode	01	Sleep mode control. Sleep has precedence over Mute and Bypass. 00: Disable sleep mode (force equalizer to stay enabled). 01: Sleep mode active when no input signal detected. 10: Force equalizer into sleep mode (powered down) regardless of whether there is an input signal or not. 11: Reserved.
			2	Driver Select	0	Select output driver for control/status. 0: Register 01h bits [7:1] control output driver 0 (SDO0, $\overline{SDO0}$) 1: Register 01h bits [7:1] control output driver 1 (SDO1, $\overline{SDO1}$)
			1	Master Reset	0	Reset registers and state machine. (This bit is self-clearing.) 0: Normal operation. 1: Reset registers and state machine.
			0	Acquisition Reset	0	Reset state machine. (This bit is self-clearing.) 0: Normal operation. 1: Reset state machine.
01h	R/W	Output Driver	7:6	Output Swing	10	Output driver swing (V_{SSP-P}). 00: V_{SSP-P} = 400 mV_{P-P}. 01: V_{SSP-P} = 600 mV_{P-P}. 10: V_{SSP-P} = 700 mV_{P-P}. 11: V_{SSP-P} = 800 mV_{P-P}.
			5:4	Offset Voltage	10	Output driver offset voltage (common mode voltage). 00: V_{OS} = 0.8V. 01: V_{OS} = 1.0V. 10: V_{OS} = 1.2V. 11: V_{OS} referenced to positive supply.
			3	De-Emphasis	0	Output driver de-emphasis control. 0: De-emphasis disabled. 1: De-emphasis enabled.
			2:1	De-Emphasis Amplitude Level	01	Output driver de-emphasis level. 00: 0 dB (no de-emphasis). 01: 3 dB de-emphasis. 10: 5 dB de-emphasis. 11: 7 dB de-emphasis.
			0	Reserved	0	Reserved (read only).

Table 3. SPI Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
02h	R/W	Launch Amplitude Control	7	Launch Amplitude Control	0	Launch amplitude optimization setting. 0: Normal optimization with no external attenuation (800 mV_{P-P} launch amplitude). 1: Optimized for 6 dB external attenuation (400 mV_{P-P} launch amplitude).
			6:0	Reserved	1101000	Reserved as 1101000. Always write 1101000 to these bits.
03h	R/W	$MUTE_{REF}$	7	Driver 1 Disable	0	SDO1_DISABLE pin has precedence over this register setting; must set SDO1_DISABLE pin low first to allow control of Driver 1 Disable via this register bit. 0: Output driver 1 (SDO1, $\overline{SDO1}$) enabled. 1: Output driver 1 (SDO1, $\overline{SDO1}$) disabled.
			6	Driver 0 Disable	0	0: Output driver 0 (SDO0, $\overline{SDO0}$) enabled. 1: Output driver 0 (SDO0, $\overline{SDO0}$) disabled.
			5	$MUTE_{REF}$ Mode	0	0: Use $MUTE_{REF}$ pin. 1: Use digital $MUTE_{REF}$.
			4:0	Digital $MUTE_{REF}$ Setting	11111	Digital $MUTE_{REF}$ (10m per step). 00000: Mute when cable (EQ boost) ≥ 10m. ..... 01111: Mute when cable (EQ boost) ≥ 160m. ..... 11111: Never mute.
04h	R	Device ID	7:6	Reserved	00	Reserved.
			5:4	EQ ID	10	00: LMH0384 device. 01: LMH0394 device. 10: LMH0395 device. 11: Reserved.
			3:0	Die Revision	0011	Die revision.
05h	R	Rate Indicator	7:6	Reserved	00	Reserved.
			5	Rate Indicator		0: SD. 1: 3G/HD.
			4:0	Reserved	11000	Reserved.
06h	R	Cable Length Indicator	7:0	Cable Length Indicator		Cable Length Indicator (CLI), with 10% accuracy. 00000000: Short cable. ..... 11110111: Maximum cable. 11111000: Reserved. ..... 11111111: Reserved.

Table 3. SPI Registers (continued)

Address	R/W	Name	Bits	Field	Default	Description
07h	R	Launch Amplitude Indication	7:2	Launch Amplitude Indication		Indication of launch amplitude: 1% or 0.08 dB per step with 5% accuracy. 000000: Nominal -32%. ..... 011111: Nominal -1%. 100000: Nominal. 100001: Nominal +1%. ..... 111111: Nominal +31%.
			1:0	Reserved		Reserved.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LMH0395SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L0395	Samples
LMH0395SQE/NOPB	ACTIVE	WQFN	RTW	24	250	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L0395	Samples
LMH0395SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	L0395	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

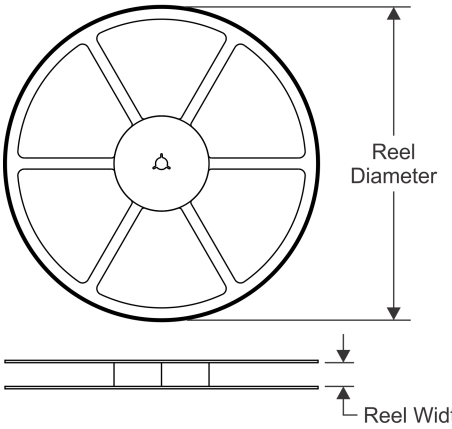
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

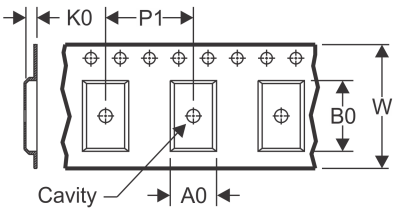
(4) Only one of markings shown within the brackets will appear on the physical device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

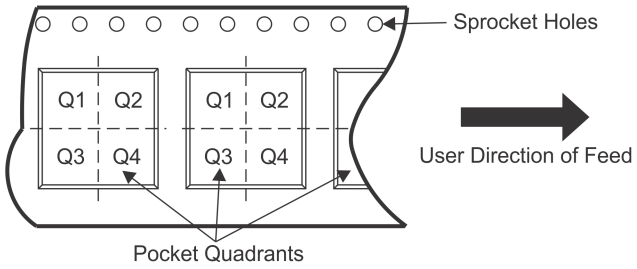


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

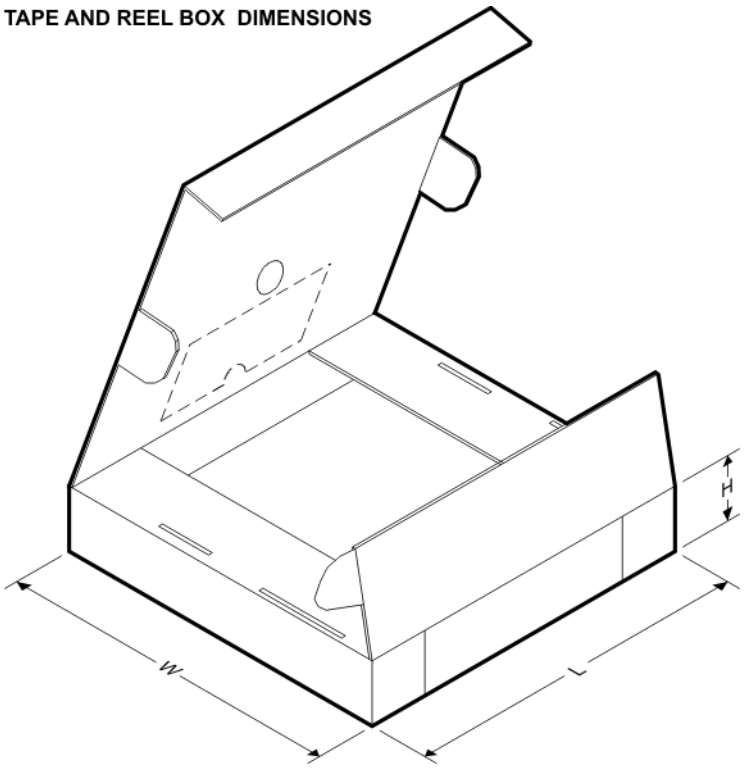
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0395SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0395SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH0395SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

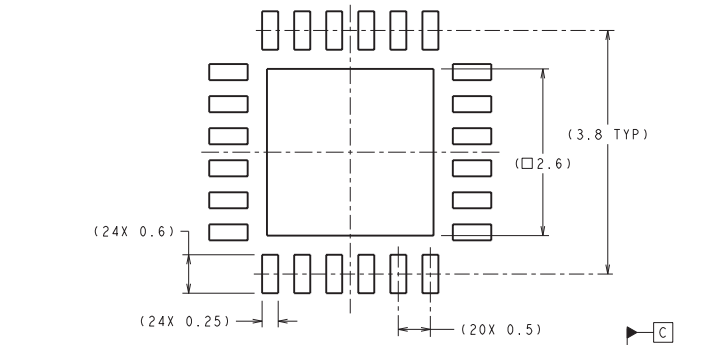
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

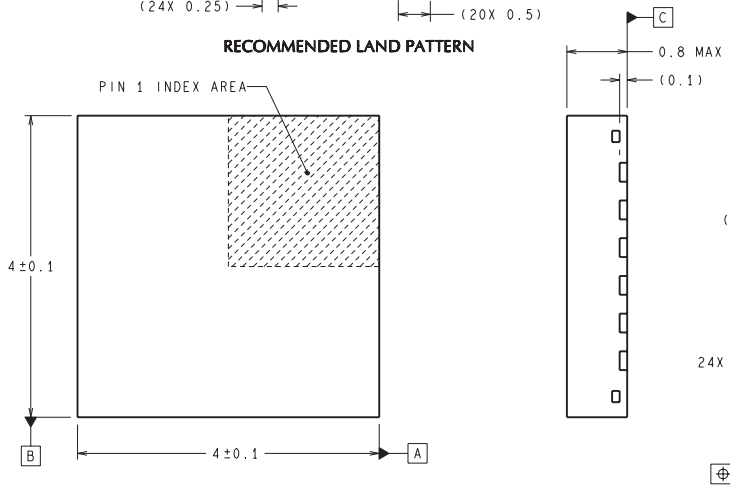
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0395SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LMH0395SQE/NOPB	WQFN	RTW	24	250	210.0	185.0	35.0
LMH0395SQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

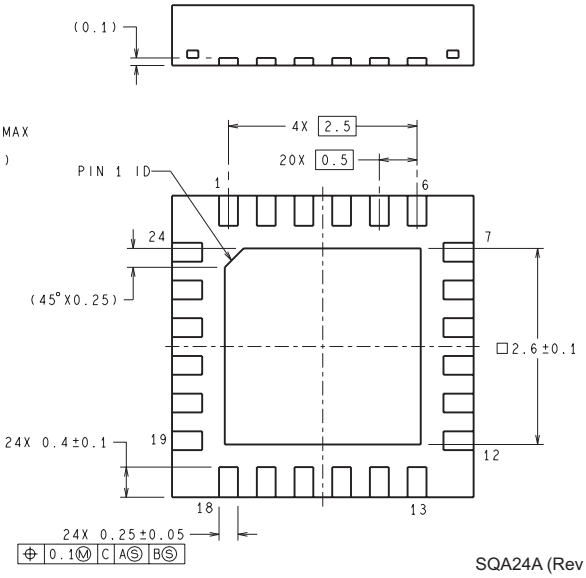
RTW0024A



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SQA24A (Rev B)

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