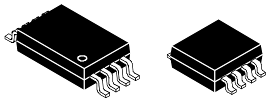


VOLTAGE PROTECTION FOR 2-, 3-, OR 4-CELL Lion BATTERIES (2^{nd} PROTECTION)

FEATURES

- **2-, 3-, or 4-Cell Secondary Protection**
- **Low Power Consumption $I_{CC} < 2\ \mu A$ [$VCELL_{(ALL)} < V_{(PROTECT)}$]**
- **High Accuracy Over Sense Voltage:**
  - **bq29400: 4.35 V ±25 mV**
  - **bq29400A: 4.40 V ±25 mV**
  - **bq29401: 4.45 V ±25 mV**
  - **bq29405: 4.65 V ±25 mV**
- **Prefixed Protection Threshold Voltage**
- **Programmable Delay Time**
- **High Power Supply Ripple Rejection**
- **Stable During Pulse Charge Operation**

APPLICATIONS

- **2^{nd} Level Protection in Lion Battery Packs in**
  - **Notebook PCs**
  - **Portable Instrumentation**
  - **Medical and Test Equipment**

DESCRIPTION

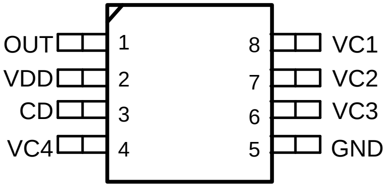
The bq29400, bq29400A, bq29401, and bq29405 are BiCMOS secondary protection ICs for 2-, 3-, or 4-cell Lithium-Ion battery packs that incorporate a high-accuracy precision over voltage detection circuit. They include a programmable delay circuit for over voltage detection time.

FUNCTION

Each cell in a multiple cell pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq2940x device starts charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes from a low level to a high level.

**PW PACKAGE
(TOP VIEW)**

**DCT PACKAGE
(TOP VIEW)**



ORDERING INFORMATION

T_A	$V_{(PROTECT)}$	PACKAGE			
		MSSOP (DCT3)	SYMBOL	TSSOP (PW)(1)	SYMBOL
–25°C to 85°C	4.35 V	bq29400DCT3	CIQ	bq29400PW	2400
	4.40 V	bq29400ADCT3	CIT	Not Available	-
	4.45 V	bq29401DCT3	CIR	bq29401PW	2401
	4.65 V	bq29405DCT3	CIS	Not Available	-

(1) The bq29400, bq29400A, bq29401, and bq29405 are available taped and reeled. Add an R suffix to the device type (e.g., bq29400PWR) to order tape and reel version.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)(2)

		UNIT
Supply voltage range	(VDD)	–0.3 V to 28 V
Input voltage range	(VC1, VC2, VC3, VC4)	–0.3 V to 28 V
Output voltage range	(OUT)	–0.3 V to 28 V
	(CD)	–0.3 V to 28 V
Continuous total power dissipation		See Dissipation Rating Table
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature (soldering, 10 sec)		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground of this device except the differential voltage of VC1-VC2, VC2-VC3, VC3-VC4 and VC4-GND.

PACKAGE DISSIPATION RATINGS

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DCT	412 mW	3.3 mW/°C	264 mW	214 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Supply Voltage		4.0		25	V
V_I	Input voltage range	VC1, VC2, VC3, VC4	0		V_{DD}+0.3	V
$t_{d(CD)}$	Delay time capacitance			0.22		μF
R_{IN}	Voltage-monitor filter resistance		100	1k		Ω
C_{IN}	Voltage-monitor filter capacitance		0.01	0.1		μF
R_{VD}	Supply-voltage filter resistance		0		1	kΩ
C_{VD}	Supply-voltage filter capacitance			0.1		μF
T_A	Operating ambient temperature range		–25		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C (unless otherwise noted)[1]

PARAMETER			TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{(OA)}$	Over voltage detection accuracy				25	35	mV
			T_A = –20°C to 85°C		25	50	
$V_{(PROTECT)}$	Over voltage detection voltage[1]	bq29400			4.35		V
		bq2940A			4.40		
		bq29401			4.45		
		bq29405			4.65		
V_{hys}	Over voltage detection hysteresis[1]				300		mV
I_I	Input current		V2, V3 , VC4 input = VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V			0.3	μA
t_{D1}	Over voltage detection delay time		CD = 0.22 μF	1.0	1.5	2.0	S
$I_{(CD\_dis)}$	CD GND clamp current		CD = 1 V	5	12		μA
I_{CC}	Supply current		VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V (see Figure 1)		2.0	3.0	μA
			VC1 = VC2 = VC3 = VC4 = VC3–VC4 = VC4–GND = 2.3 V (see Figure 1)		1.5	2.5	
$V_{(OUT)}$	OUT pin drive voltage		VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = $V_{(PROTECT)}$MAX, VDD = VC1, IOH = 0 mA		7		V
			VC1=VC2=VC3=VC4=$V_{(PROTECT)}$MAX, VDD=4.3V, T_A= 0°C to 70°C, IOH = – 40μA	1.5	2.0	2.5	V
I_{OH}	High-level output current		OUT = 3V, VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 4.7 V	–1			mA
I_{OL}	Low-level output current		OUT = 0.1 V VC1–VC2 = VC2–VC3 = VC3–VC4 = VC4–GND = 3.5 V	5			μA

(1) Levels of the over-voltage detection and the hysteresis can be adjusted. For assistance contact Texas Instruments sales representative.

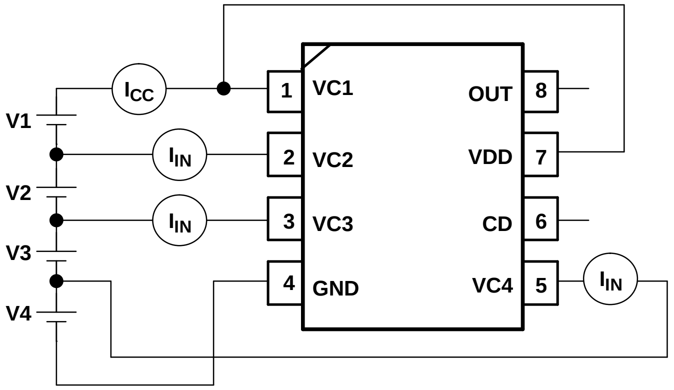


Figure 1. I_{CC}, I_{IN} Measurement (TSSOP Package)

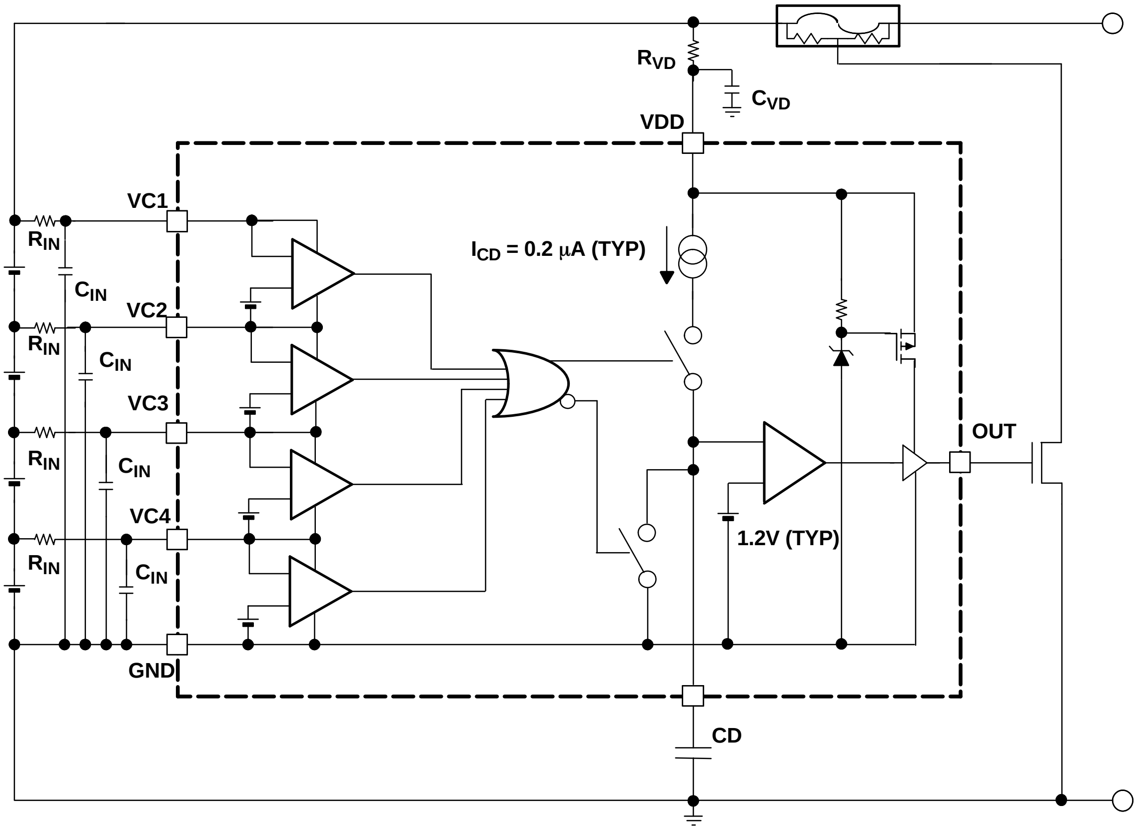
Terminal Functions

TERMINAL			DESCRIPTION
MSOP (DTC)	TSSOP (PW)	NAME	
8	1	VC1	Sense voltage input for most positive cell
7	2	VC2	Sense voltage input for second most positive cell
6	3	VC3	Sense voltage input for third most positive cell
5	4	GND	Ground pin
4	5	VC4	Sense voltage input for least positive cell

Terminal Functions (continued)

TERMINAL			DESCRIPTION
MSOP (DTC)	TSSOP (PW)	NAME	
3	6	CD	An external capacitor is connected to determine the programmable delay time
2	7	VDD	Power supply
1	8	OUT	Output

FUNCTIONAL BLOCK DIAGRAM



OVERVOLTAGE PROTECTION

When one of the cell voltages exceeds $V_{(PROTECT)}$, an internal current source begins to charge the capacitor, $C_{(DELAY)}$, connected to the CD pin. If the voltage at the CD pin, $V_{CD,}$ reaches 1.2 V, the OUT pin is activated and transitions high. An externally connected NCH FET is activiated and blows the external fuse in the positive battery rail, see Figure 1.

If all cell voltages fall below $V_{(PROTECT)}$ before the voltage at pin CD reaches 1.2 V, the delay time does not run out. An internal switch clamps the CD pin to GND and discharges the capacitor, $C_{(DELAY)}$, and secures the full delay time for the next occurring overvoltage event.

Once the pin OUT is activated, it transitions back from high to low after all battery cells reach $V_{(PROTECT)}$ - $V_{hys.}$

DELAY TIME CALCULATION

The delay time is calculated as follows:

$$t_d = \frac{\left[1.2\text{ V} \times C_{(DELAY)}\right]}{I_{CD}}$$

$$C_{(DELAY)} = \frac{\left[t_d \times I_{CD}\right]}{1.2\text{ V}}$$

Where $I_{(CD)}$ = CD current source = 0.2 µA

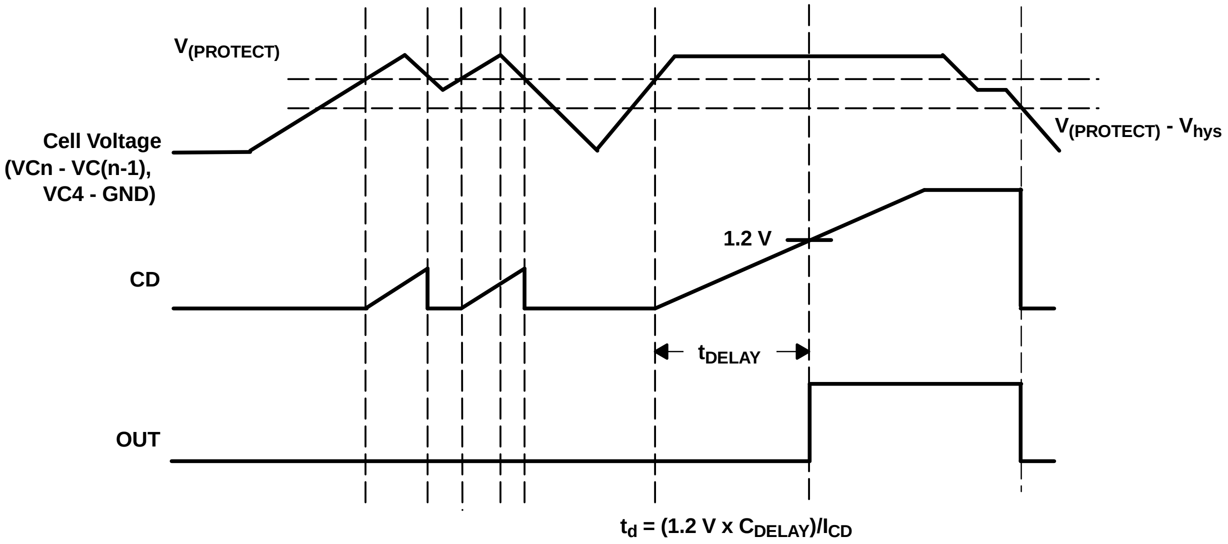


Figure 2. Timing for Overvoltage Sensing

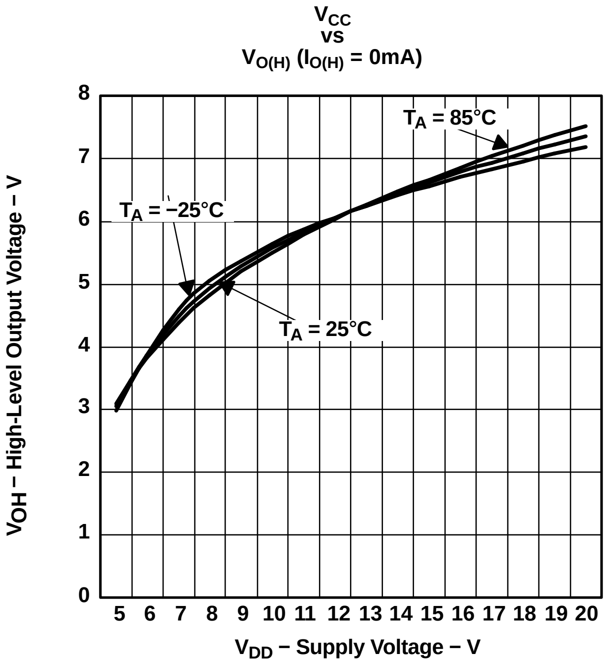


Figure 3.

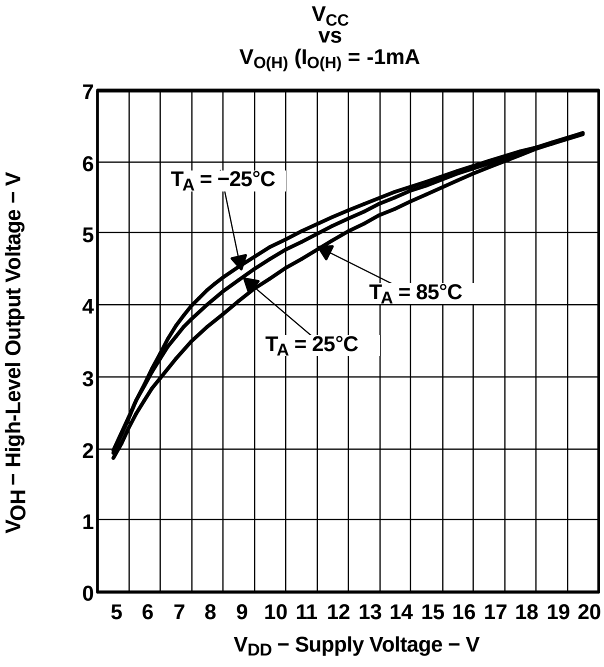


Figure 4.

APPLICATION INFORMATION

BATTERY CONNECTIONS

The following diagrams show the TSSOP package device in different cell configurations.

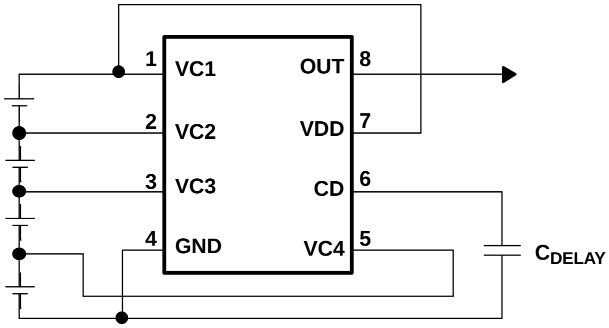


Figure 5. 4-Series Cell Configuration

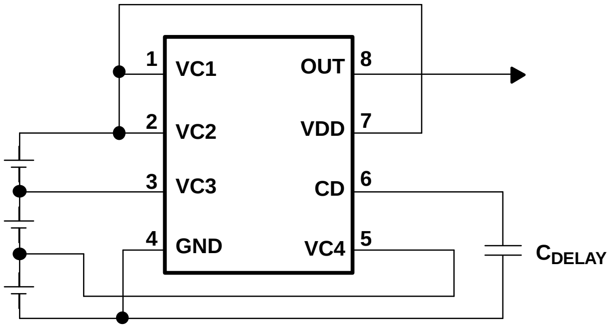


Figure 6. 3-Series Cell Configuration (Connect together VC1 and VC2)

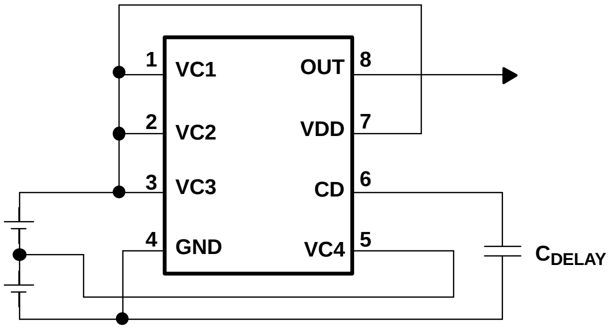


Figure 7. 2-Series Cell Configuration

CELL CONNECTIONS

To prevent incorrect output activation the following connection sequences must be used.

4-Series Cell Configuration

- VC1(=VDD) → VC2 → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC2 → VC1(=VDD)

3-Series Cell Configuration

- VC1(=VC2=VDD) → VC3 → VC4 → GND or
- GND → VC4 → VC3 → VC1(=VC2=VDD)

2-Series Cell Configuration

- VC1(=VC2=VC3=VDD) → VC4 → GND or
- GND → VC4 → VC1(=VC2=VC3=VDD)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ29400ADCT3	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-25 to 85	CIT W	Samples
BQ29400ADCT3E6	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-25 to 85	CIT W	Samples
BQ29400ADCT3R	OBSOLETE	SM8	DCT	8		TBD	Call TI	Call TI	-25 to 85		
BQ29400DCT3	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM		CIQ	Samples
BQ29400DCT3E6	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM		CIQ	Samples
BQ29400PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	29400	Samples
BQ29400PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	29400	Samples
BQ29401DCT	NRND	SM8	DCT	8		TBD	Call TI	Call TI	-20 to 85		
BQ29401DCT3	OBSOLETE	SM8	DCT	8		TBD	Call TI	Call TI		CIR	
BQ29401DCT3E6	ACTIVE	SM8	DCT	8		TBD	Call TI	Call TI			Samples
BQ29401PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	29401	Samples
BQ29401PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	29401	Samples
BQ29405DCT3	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-25 to 85	CIS W	Samples
BQ29405DCT3E6	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU SNBI	Level-1-260C-UNLIM	-25 to 85	CIS W	Samples
BQ29405DCT3R	NRND	SM8	DCT	8		TBD	Call TI	Call TI	-25 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

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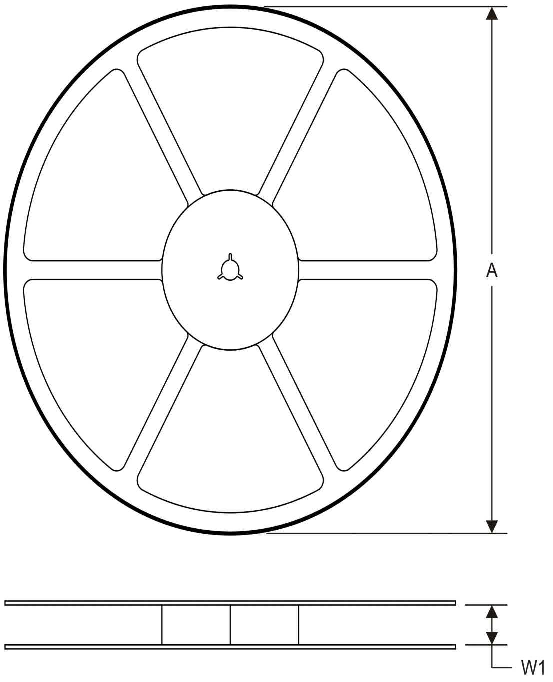
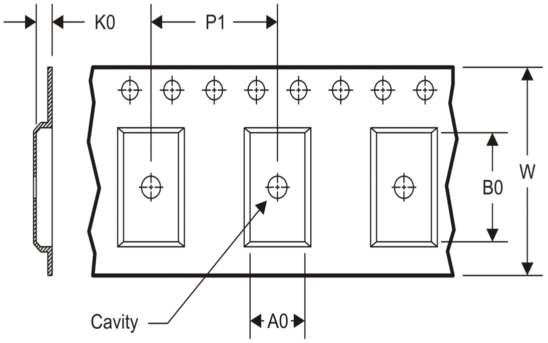
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



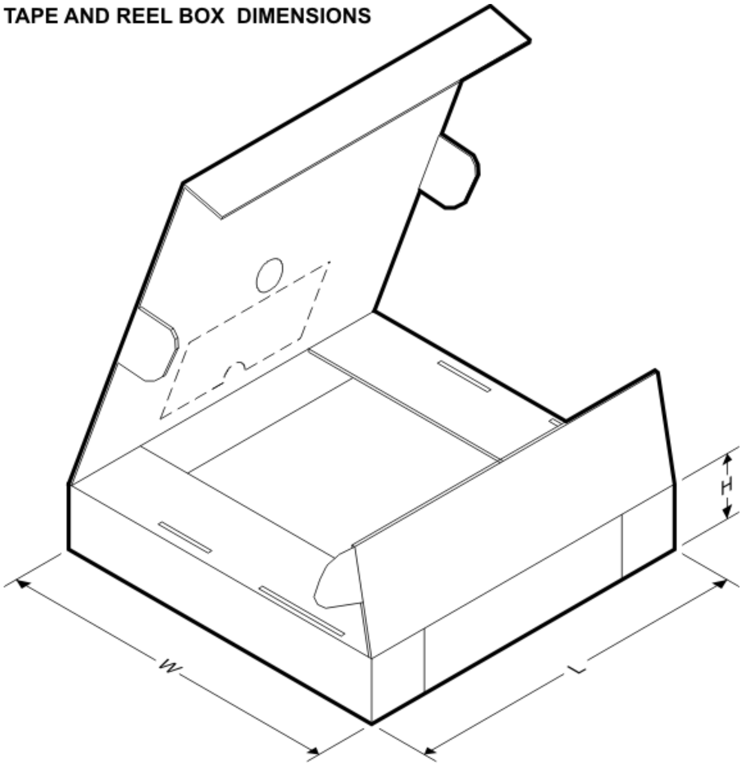
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ29400PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

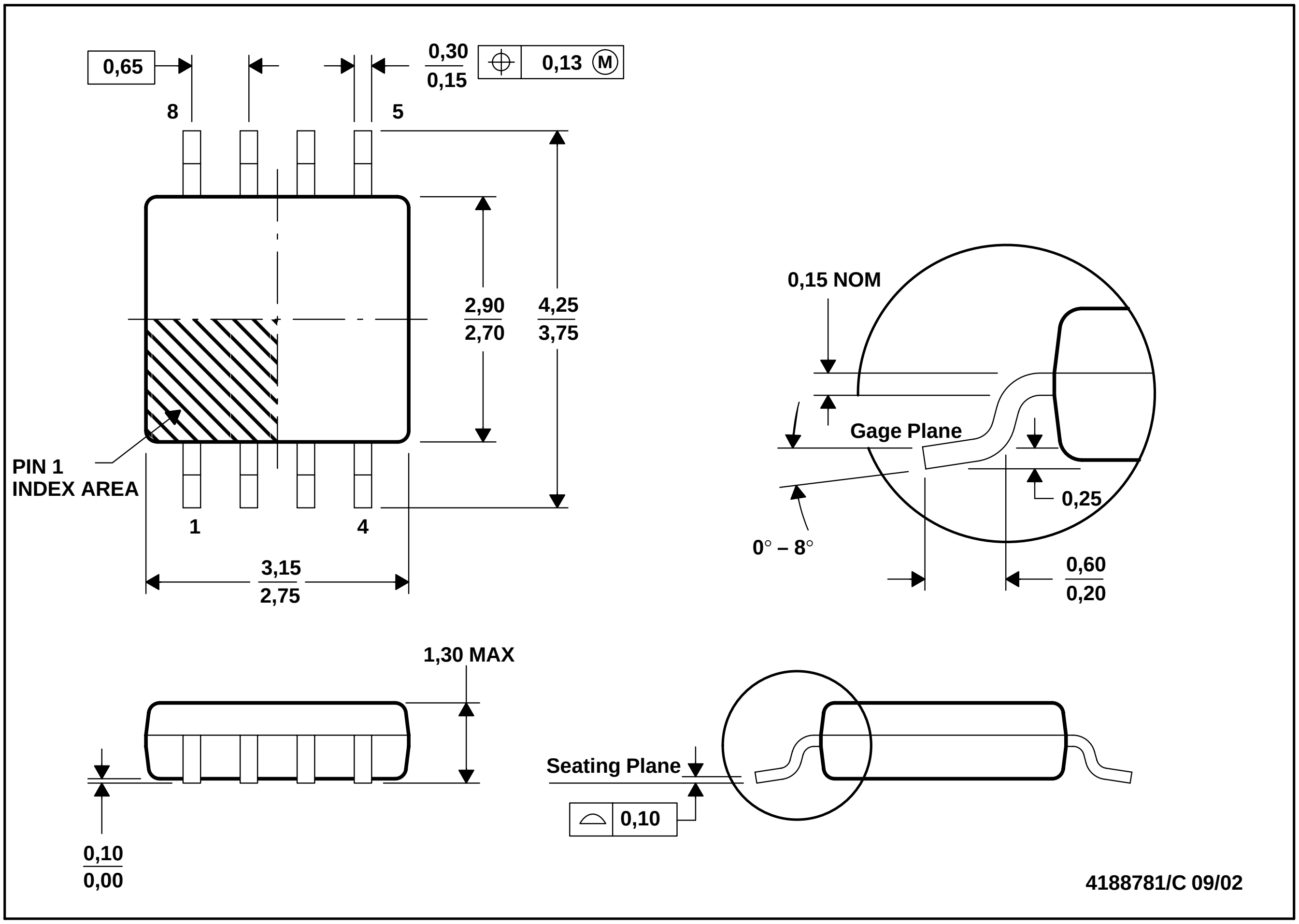
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

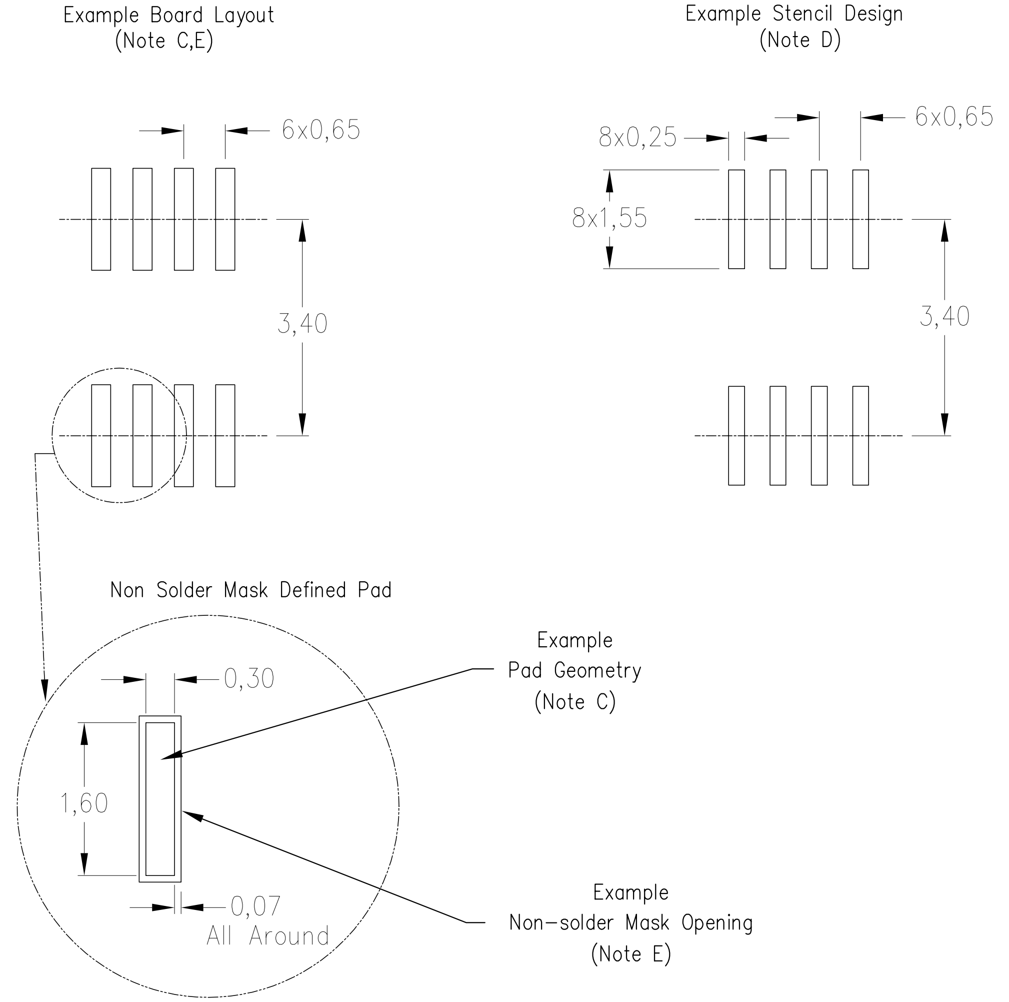
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ29400PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

DCT (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. Falls within JEDEC MO-187 variation DA.

DCT (R–PDSO–G8) PLASTIC SMALL OUTLINE



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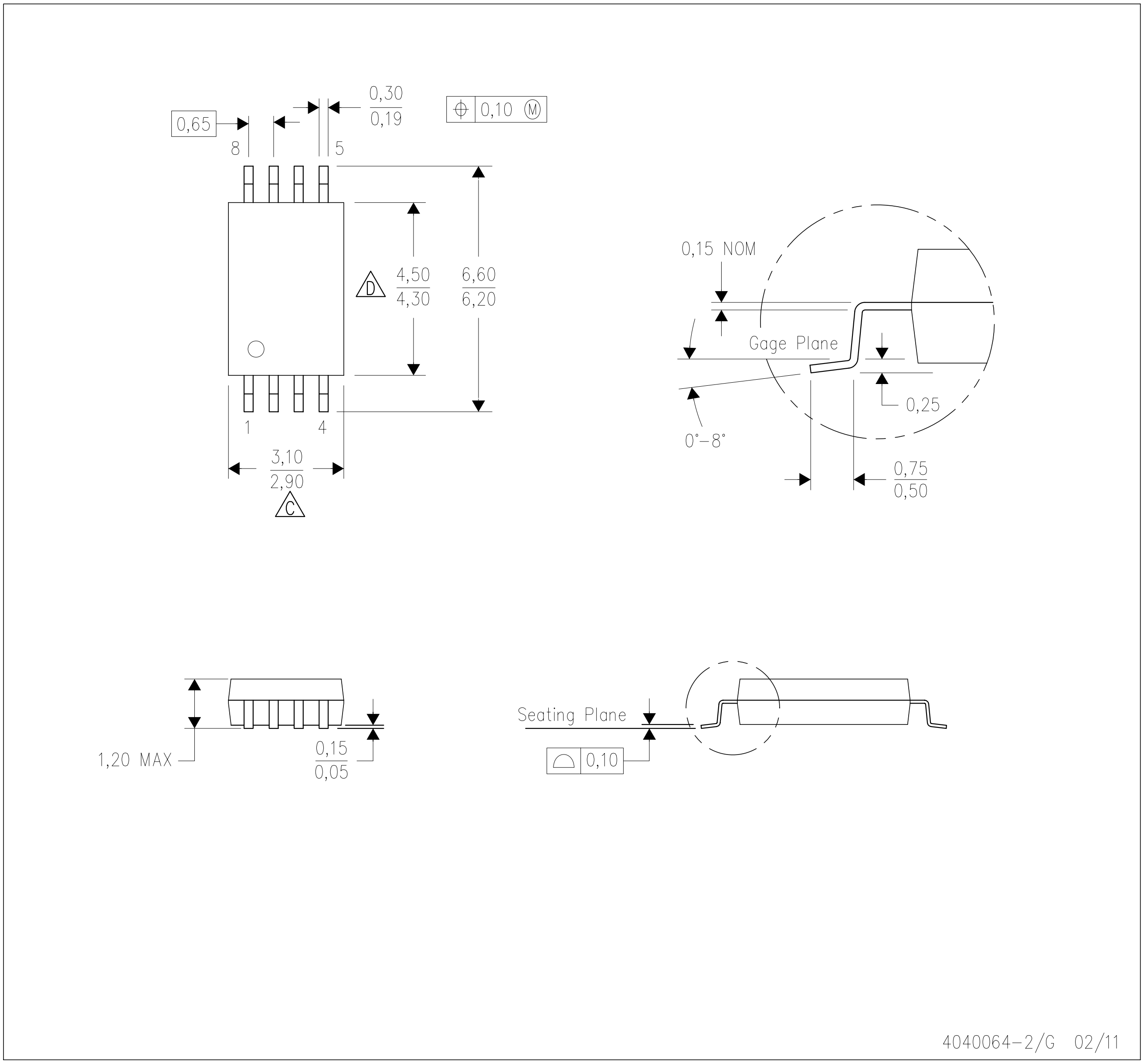
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

E. Falls within JEDEC MO–153

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