
# PSMN4R1-60YL

## N-channel 60 V, 4.1 mΩ logic level MOSFET in LFPAK56

20 October 2016 Product data sheet

## 1. General description

Logic level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

## 2. Features and benefits

- Advanced TrenchMOS provides low $R_{DSon}$ and low gate charge
- Logic level gate operation
- Avalanche rated, 100% tested
- LFPAK provides maximum power density in a Power SO8 package

## 3. Applications

- Synchronous rectifier in LLC topology
- Chargers & adaptors with $V_{out}$ < 10 V
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

## 4. Quick reference data

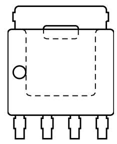
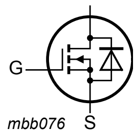
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | - | 60 | V |
| $I_D$ | drain current | $V_{GS}$ = 5 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | - | 100 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 238 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | - | 3.3 | 4.8 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $I_D$ = 25 A; $V_{DS}$ = 48 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | - | 18.1 | - | nC |

[1] Continuous current is limited by package.

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | S | source |   **LFPAK56; Power-SO8 (SOT669)** |   |
| 2 | S | source | | |
| 3 | S | source | | |
| 4 | G | gate | | |
| mb | D | mounting base; connected to drain | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PSMN4R1-60YL | LFPAK56; Power-SO8 | Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads | SOT669 |

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | 25 °C ≤ $T_j$ ≤ 175 °C | | - | 60 | V |
| $V_{DGR}$ | drain-gate voltage | $R_{GS}$ = 20 kΩ | | - | 60 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 238 | W |
| $I_D$ | drain current | $V_{GS}$ = 5 V; $T_{mb}$ = 25 °C; Fig. 2 | [1] | - | 100 | A |
| | | $V_{GS}$ = 5 V; $T_{mb}$ = 100 °C; Fig. 2 | [1] | - | 100 | A |
| $I_{DM}$ | peak drain current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C; Fig. 3 | | - | 593 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [1] | - | 100 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p$ ≤ 10 µs; $T_{mb}$ = 25 °C | | - | 593 | A |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 100 A; $V_{sup} \leq$ 60 V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4 | [2][3] | - | 199 | mJ |

[1] Continuous current is limited by package.
[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[3] Refer to application note AN10273 for further information.

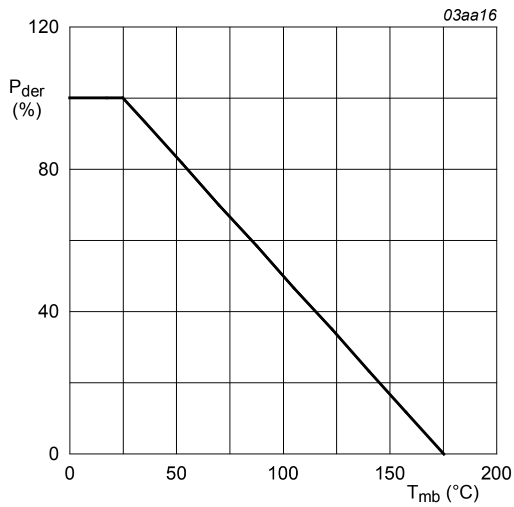
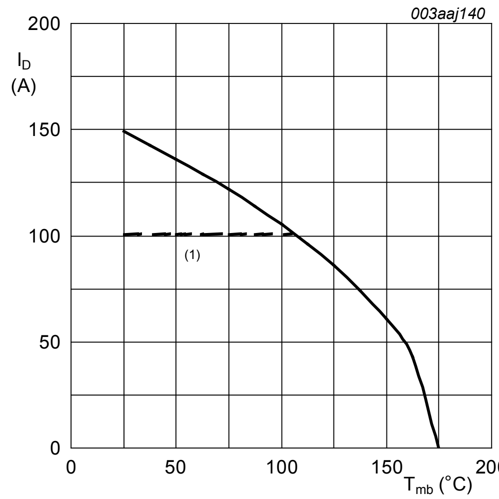



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$




(1) Capped at 100A due to package

**Fig. 2. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 5V$$

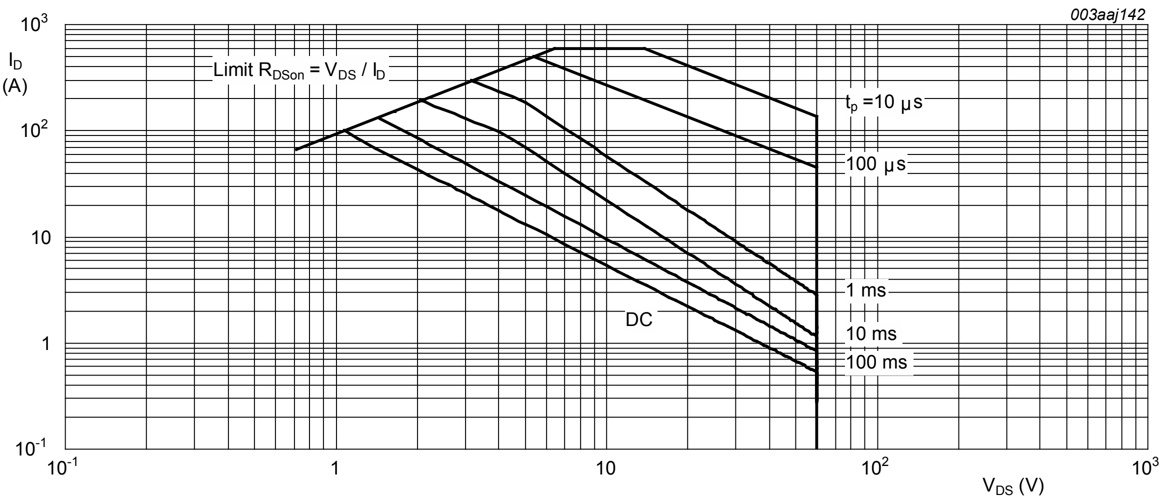



**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$$T_{mb} = 25°C; \; I_{DM} \; is \; a \; single \; pulse$$

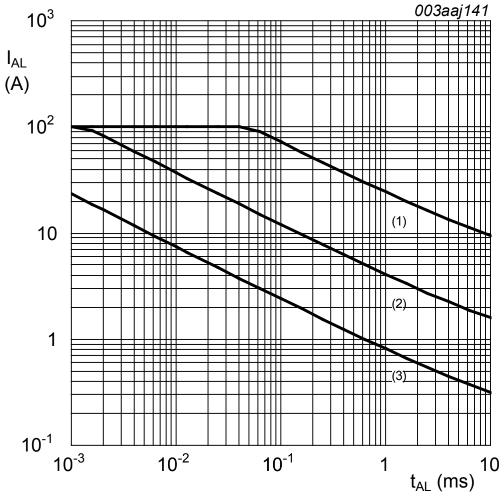



**Fig. 4. Avalanche rating; avalanche current as a function of avalanche time**

(1) $T_{j(init)} = 25°C$; (2) $T_{j(init)} = 150°C$; (3) Repetitive Avalanche

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | - | 0.63 | K/W |

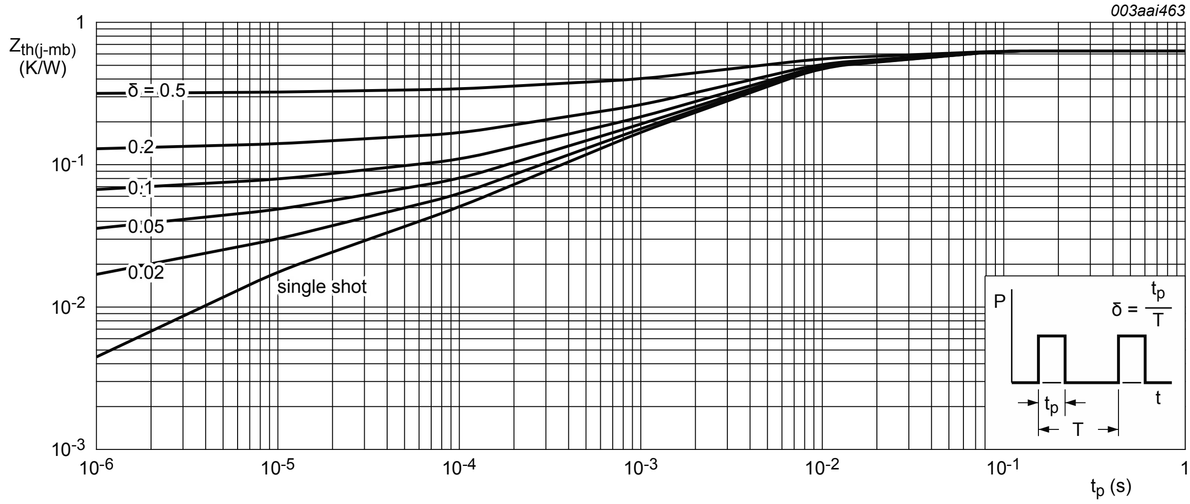


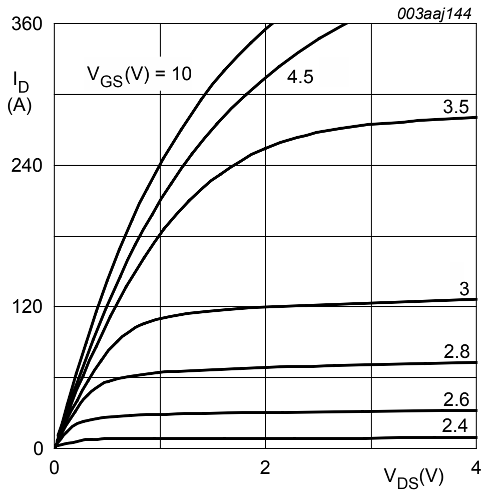

**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 60 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 54 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 25 °C; Fig. 9; Fig. 10 | | 1.4 | 1.7 | 2.1 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = -55 °C; Fig. 9 | | - | - | 2.45 | V |
| | | $I_D$ = 1 mA; $V_{DS}$=$V_{GS}$; $T_j$ = 175 °C; Fig. 9 | | 0.5 | - | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 60 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | | - | - | 500 | µA |
| | | $V_{DS}$ = 60 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.12 | 10 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -16 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | - | 3.3 | 4.8 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 25 A; $T_j$ = 25 °C; Fig. 11 | | - | 2.9 | 4.1 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 25 A; $T_j$ = 175 °C; Fig. 11; Fig. 12 | | - | - | 10.8 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 25 A; $V_{DS}$ = 48 V; $V_{GS}$ = 10 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | - | 103 | - | nC |
| | | $I_D$ = 25 A; $V_{DS}$ = 48 V; $V_{GS}$ = 5 V; $T_j$ = 25 °C; Fig. 13; Fig. 14 | | - | 54.8 | - | nC |
| $Q_{GS}$ | gate-source charge | | | - | 13.6 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 18.1 | - | nC |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 25 V; $V_{GS}$ = 0 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 15 | | - | 5890 | 7853 | pF |
| $C_{oss}$ | output capacitance | | | - | 506 | 607 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 276 | 378 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 45 V; $R_L$ = 1.8 Ω; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 5 Ω; $T_j$ = 25 °C | | - | 28 | - | ns |
| $t_r$ | rise time | | | - | 53 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 80 | - | ns |
| $t_f$ | fall time | | | - | 47 | - | ns |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 25 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.78 | 1.2 | V |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{rr}$ | reverse recovery time | $I_S$ = 20 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; $T_j$ = 25 °C | | - | 29 | - | ns |
| $Q_r$ | recovered charge | | | - | 28 | - | nC |




$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**

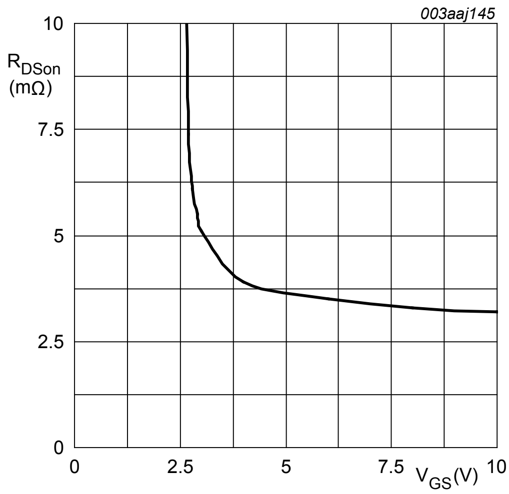



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25°C$; $I_D = 25A$

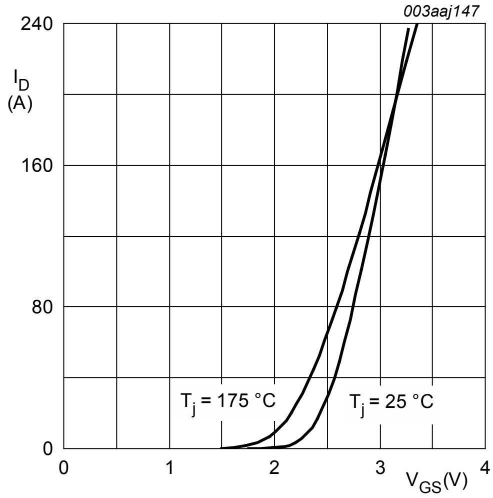



**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$

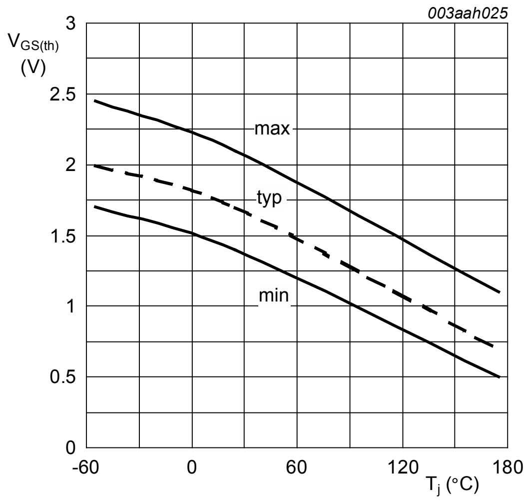



**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1$ mA; $V_{DS} = V_{GS}$

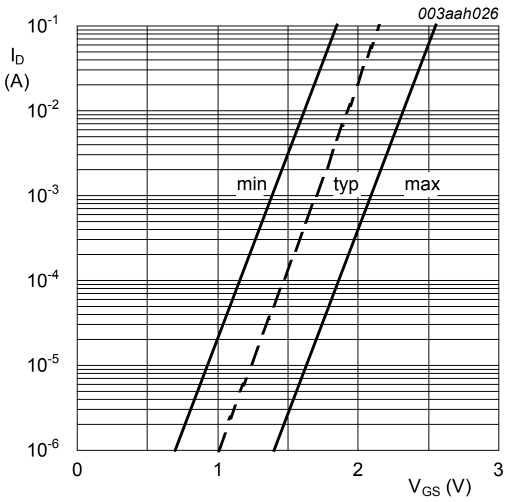
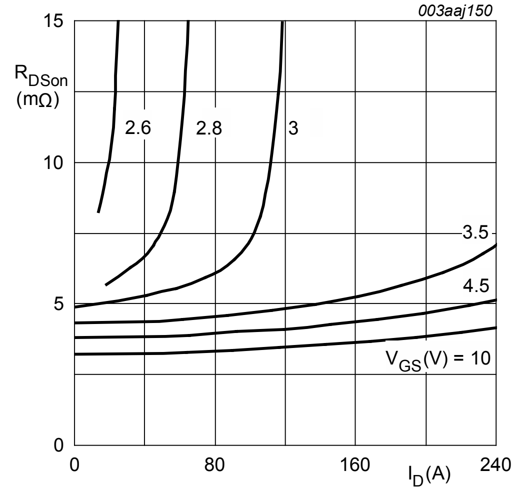



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25°C;\ V_{DS} = 5V$




$T_j$ = 25 °C; $t_p$ = 300 μs

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

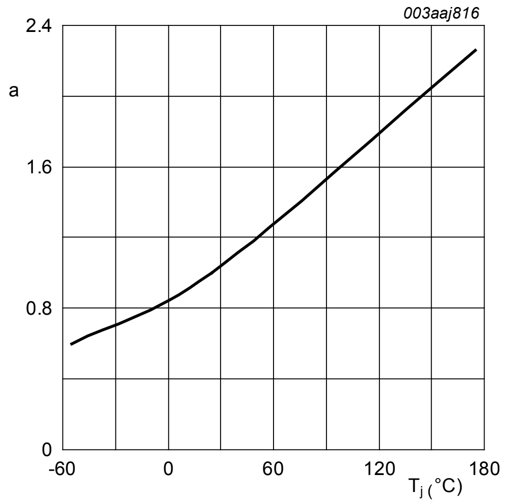



**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

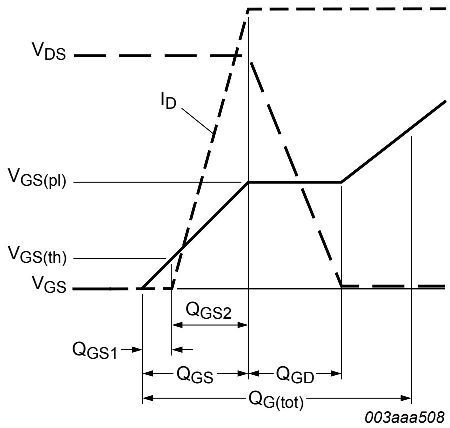



**Fig. 13. Gate charge waveform definitions**

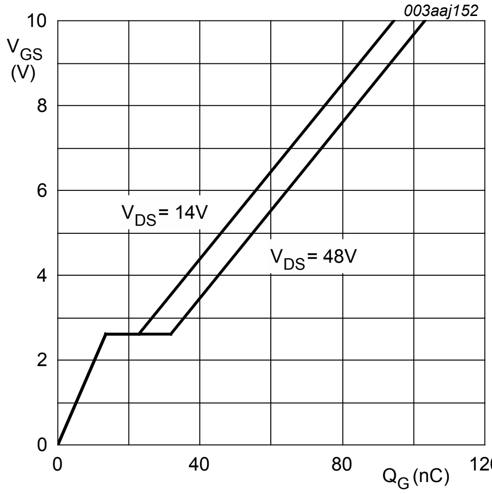



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

$T_j = 25°C;\ I_D = 25A$

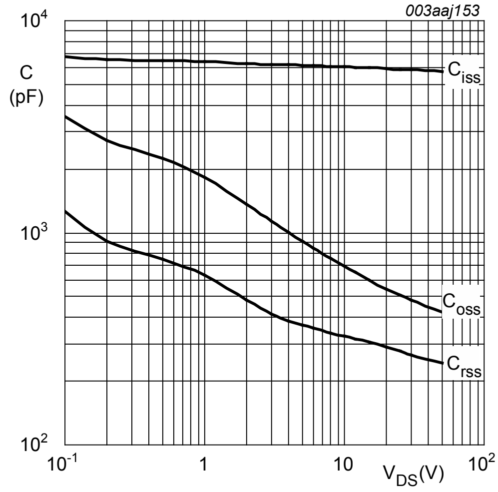



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$T_j = 25°C;\ I_D = 25A$

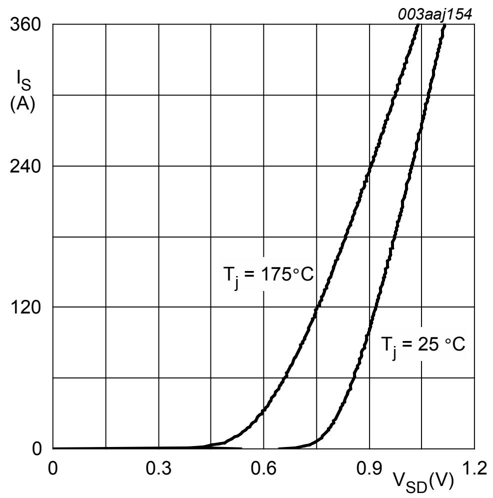
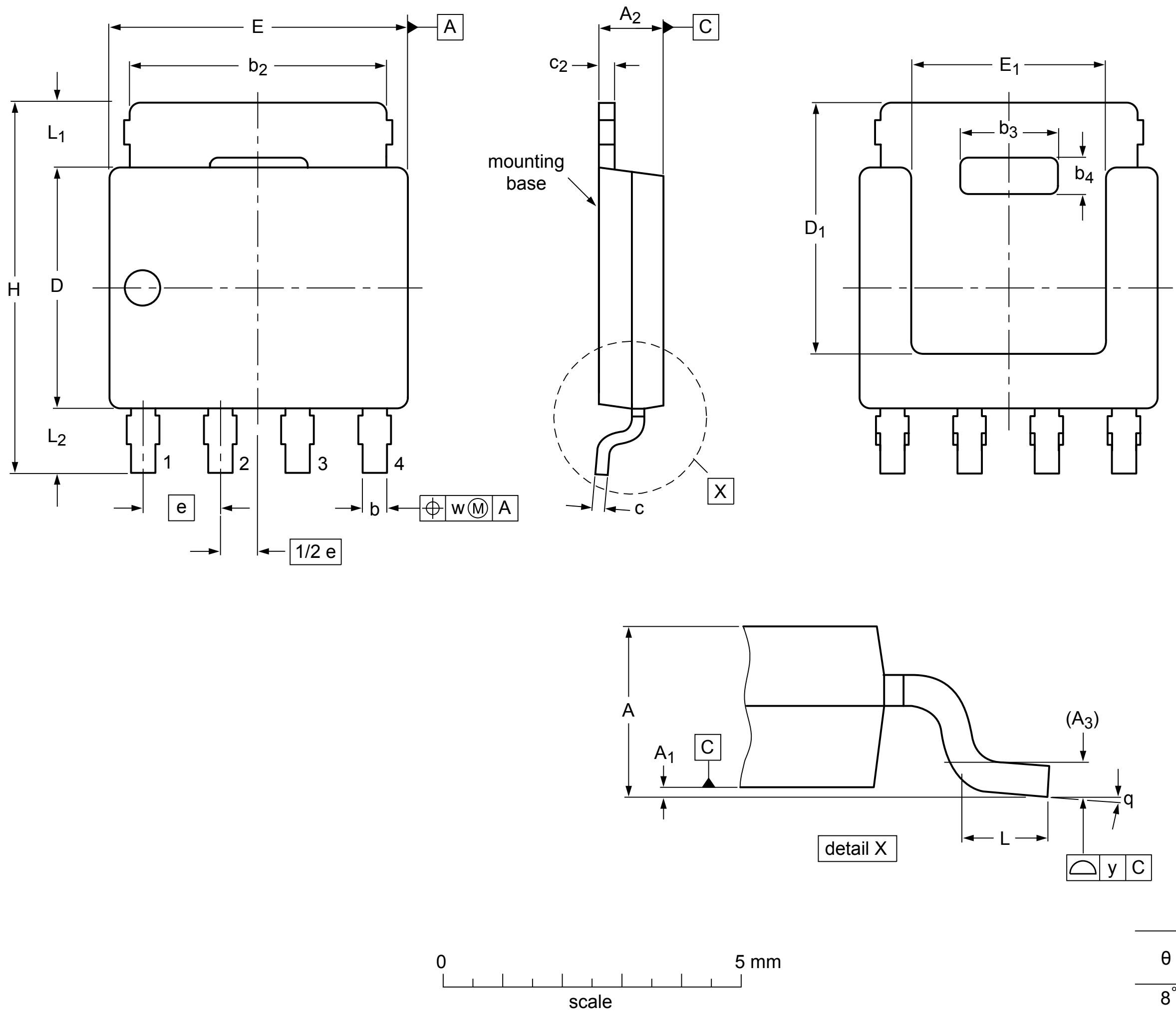



**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$V_{GS} = 0V$

## 10. Package outline

**Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads** **SOT669**




Dimensions (mm are the original dimensions)

| Unit(1) | | A | $A_1$ | $A_2$ | $A_3$ | b | $b_2$ | $b_3$ | $b_4$ | c | $c_2$ | D(1) | $D_1$(1) | E(1) | $E_1$(1) | e | H | L | $L_1$ | $L_2$ | w | y | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1.20 | 0.15 | 1.10 | | 0.50 | 4.41 | 2.2 | 0.9 | 0.25 | 0.30 | 4.10 | 4.20 | 5.0 | 3.3 | | 6.2 | 0.85 | 1.3 | 1.3 | | | 8° |
| | nom | | | | 0.25 | | | | | | | | | | | 1.27 | | | | | 0.25 | 0.1 | |
| | min | 1.01 | 0.00 | 0.95 | | 0.35 | 3.62 | 2.0 | 0.7 | 0.19 | 0.24 | 3.80 | | 4.8 | 3.1 | | 5.8 | 0.40 | 0.8 | 0.8 | | | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

*sot669_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT669 | | MO-235 | | | | ~~11-03-25~~ 13-02-27 |

**Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)**

# 11. Legal information

## 11.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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## 12. Contents




**Date of release: 20 October 2016**