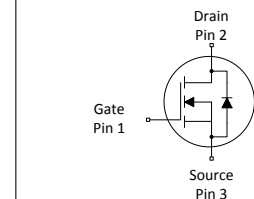


MOSFET

600V CoolMOS™ CFD7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. The latest CoolMOS™ CFD7 is the successor to the CoolMOS™ CFD2 series and is an optimized platform tailored to target soft switching applications such as phase-shift full-bridge (ZVS) and LLC. Resulting from reduced gate charge (Q_g), best-in-class reverse recovery charge (Q_{rr}) and improved turn off behavior CoolMOS™ CFD7 offers highest efficiency in resonant topologies. As part of Infineon's fast body diode portfolio, this new product series blends all advantages of a fast switching technology together with superior hard commutation robustness, without sacrificing easy implementation in the design-in process. The CoolMOS™ CFD7 technology meets highest efficiency and reliability standards and furthermore supports high power density solutions. Altogether, CoolMOS™ CFD7 makes resonant switching topologies more efficient, more reliable, lighter and cooler.



Features

- Ultra-fast body diode
- Low gate charge
- Best-in-class reverse recovery charge (Q_{rr})
- Improved MOSFET reverse diode dv/dt and di_F/dt ruggedness
- Lowest FOM $R_{DS(on)} \cdot Q_g$ and $R_{DS(on)} \cdot E_{oss}$
- Best-in-class $R_{DS(on)}$ in SMD and THD packages

Benefits

- Excellent hard commutation ruggedness
- Highest reliability for resonant topologies
- Highest efficiency with outstanding ease-of-use / performance tradeoff
- Enabling increased power density solutions

Potential applications

Suitable for Soft Switching topologies
Optimized for phase-shift full-bridge (ZVS), LLC Applications – Server, Telecom, EV Charging

Product Validation: Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	210	mΩ
$Q_{g,typ}$	23	nC
$I_{D,pulse}$	42	A
$E_{oss} @ 400V$	2.6	μJ
Body diode di_F/dt	1300	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPA60R210CFD7	PG-TO 220 FullPAK	60R210F7	see Appendix A

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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	7 5.0	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	42	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	49	mJ	$I_D=3.2\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.24	mJ	$I_D=3.2\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	3.2	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	25	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	7	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	42	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	70	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 7\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	1300	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 7\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_θ .

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	5.0	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	lead
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sld}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3.5	4	4.5	V	$V_{DS}=V_{GS}$, $I_D=0.24mA$
Zero gate voltage drain current ¹⁾	I_{DSS}	-	-	1	μA	$V_{DS}=600V$, $V_{GS}=0V$, $T_j=25^\circ C$ $V_{DS}=600V$, $V_{GS}=0V$, $T_j=125^\circ C$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.171	0.21	Ω	$V_{GS}=10V$, $I_D=4.9A$, $T_j=25^\circ C$ $V_{GS}=10V$, $I_D=4.9A$, $T_j=150^\circ C$
Gate resistance	R_G	-	11	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1015	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	18	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ²⁾	$C_{o(er)}$	-	33	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ³⁾	$C_{o(tr)}$	-	330	-	pF	$I_D=constant$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	22	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=6.0A$, $R_G=10.2\Omega$; see table 9
Rise time	t_r	-	16.5	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=6.0A$, $R_G=10.2\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	54	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=6.0A$, $R_G=10.2\Omega$; see table 9
Fall time	t_f	-	7.5	-	ns	$V_{DD}=400V$, $V_{GS}=10V$, $I_D=6.0A$, $R_G=10.2\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6	-	nC	$V_{DD}=400V$, $I_D=6.0A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	7	-	nC	$V_{DD}=400V$, $I_D=6.0A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	23	-	nC	$V_{DD}=400V$, $I_D=6.0A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.7	-	V	$V_{DD}=400V$, $I_D=6.0A$, $V_{GS}=0$ to $10V$

¹⁾ Maximum specification is defined by calculated six sigma upper confidence bound

²⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

³⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	1.0	-	V	$V_{GS}=0V$, $I_F=4.9A$, $T_J=25^{\circ}C$
Reverse recovery time	t_{rr}	-	92	184	ns	$V_R=400V$, $I_F=6.0A$, $di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	0.385	0.77	μC	$V_R=400V$, $I_F=6.0A$, $di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	7.5	-	A	$V_R=400V$, $I_F=6.0A$, $di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

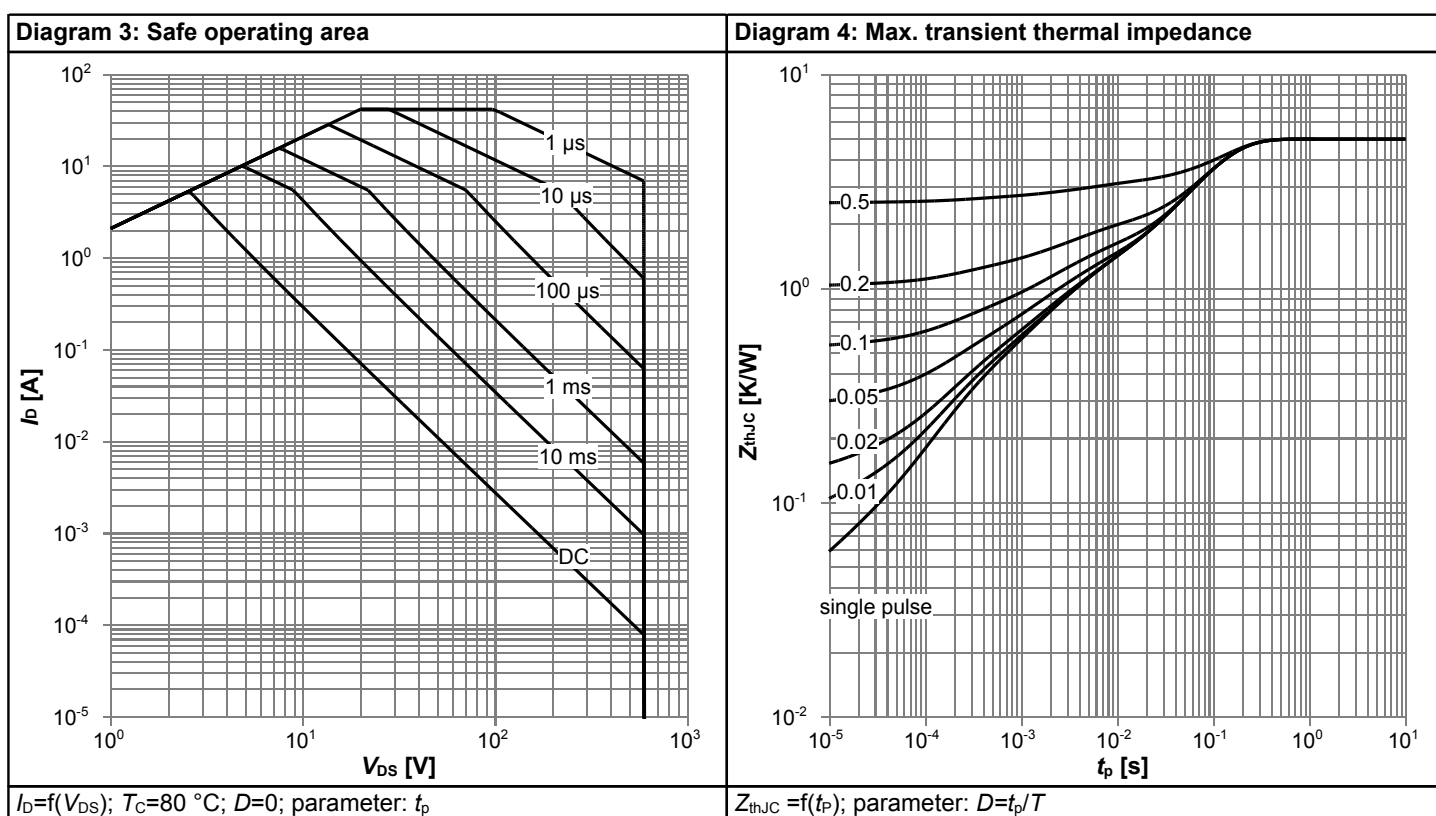
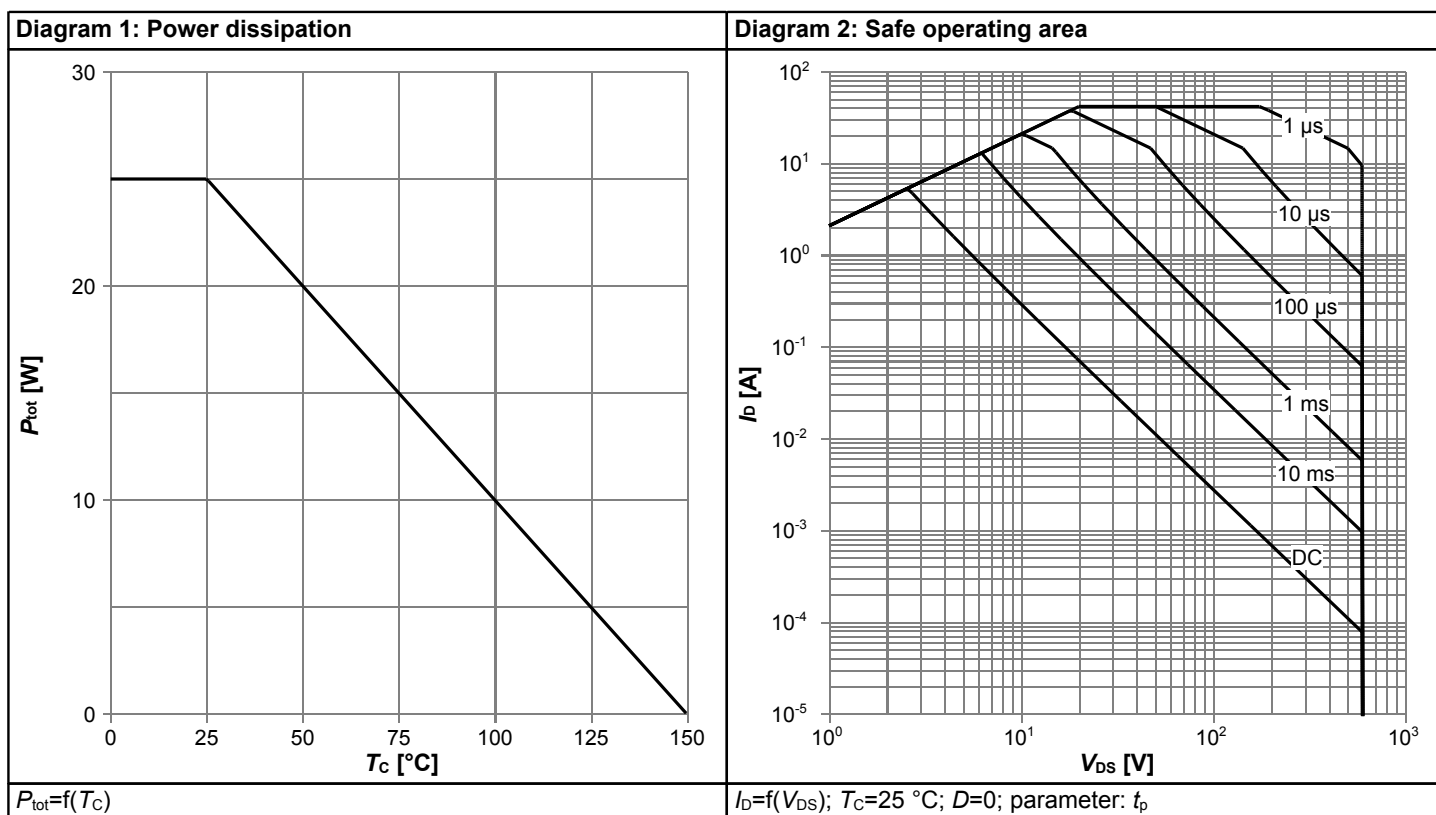
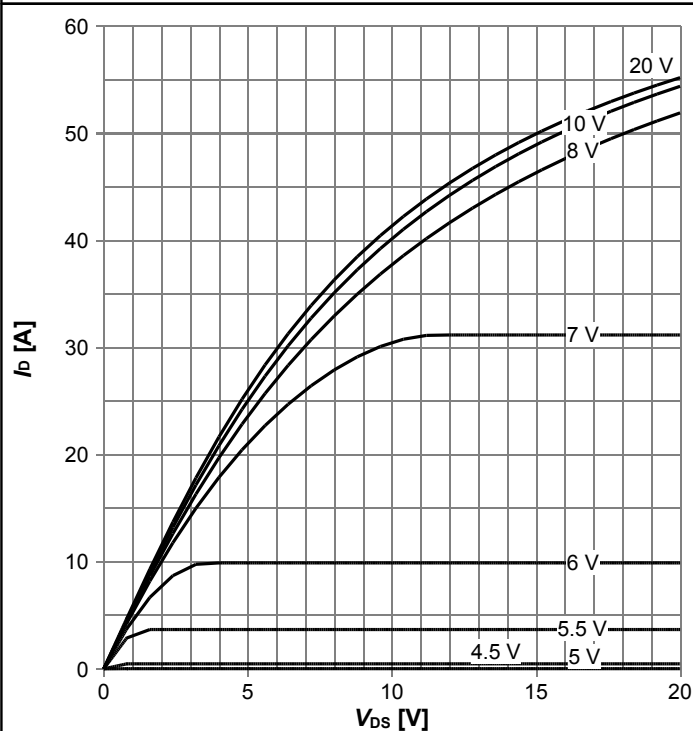
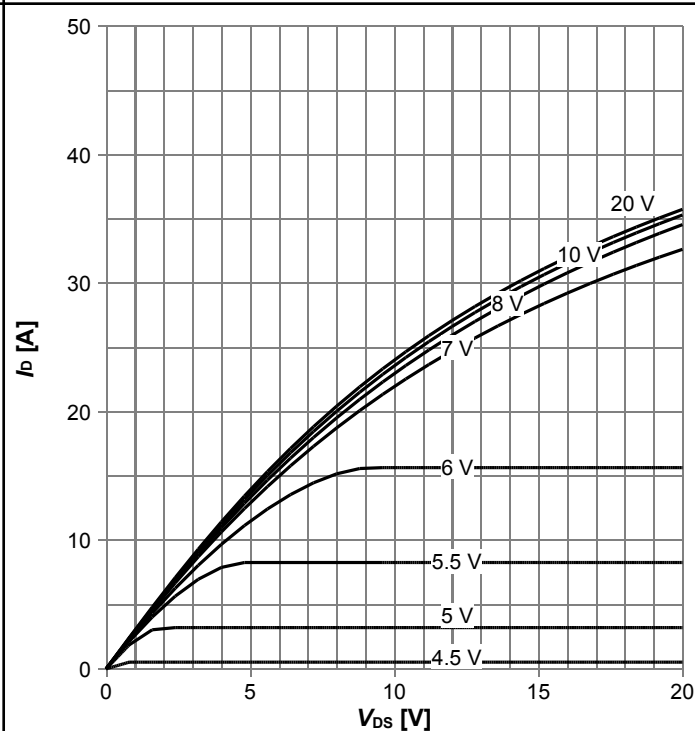


Diagram 5: Typ. output characteristics



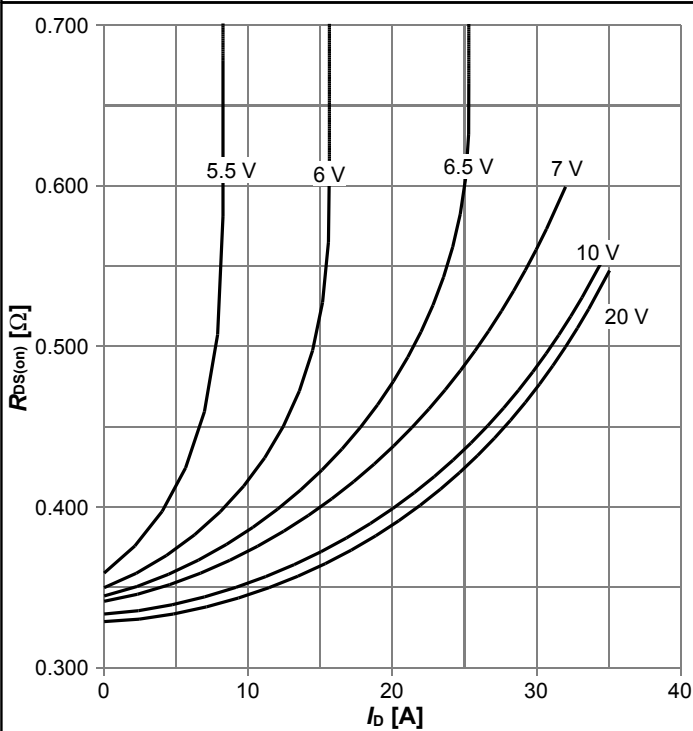
$I_D = f(V_{DS})$; $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



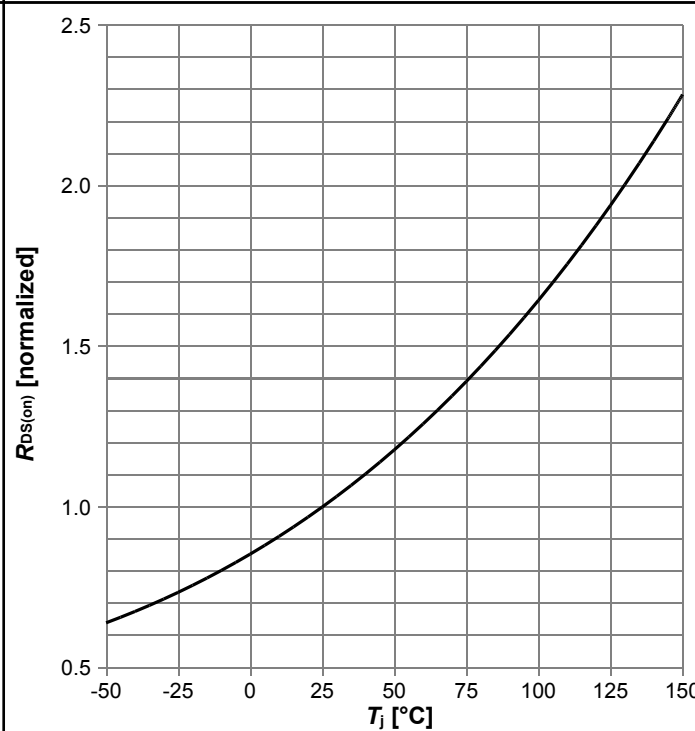
$I_D = f(V_{DS})$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



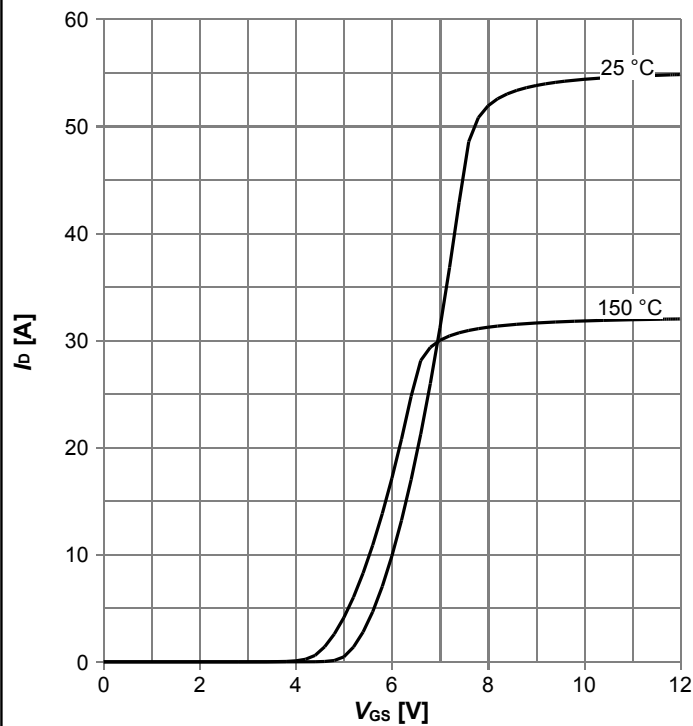
$R_{DS(on)} = f(I_D)$; $T_j = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



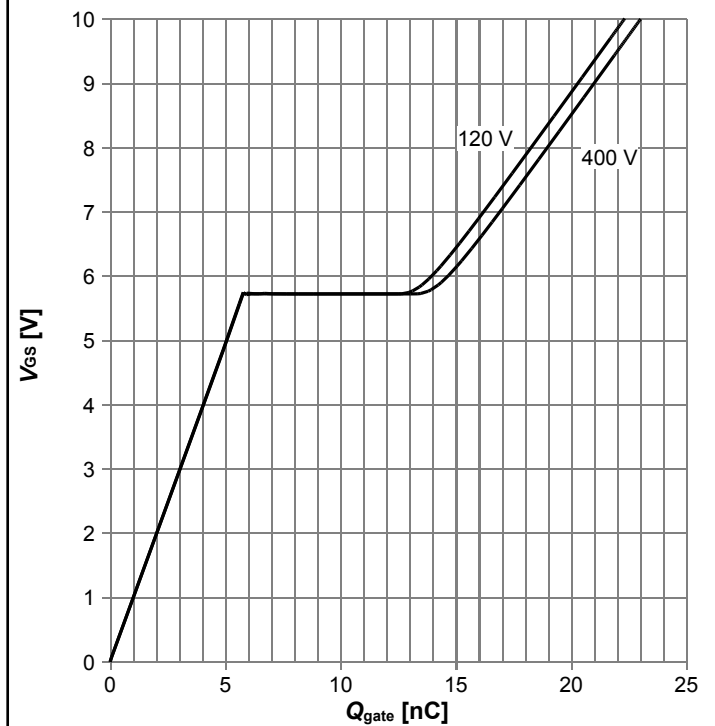
$R_{DS(on)} = f(T_j)$; $I_D = 4.9\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



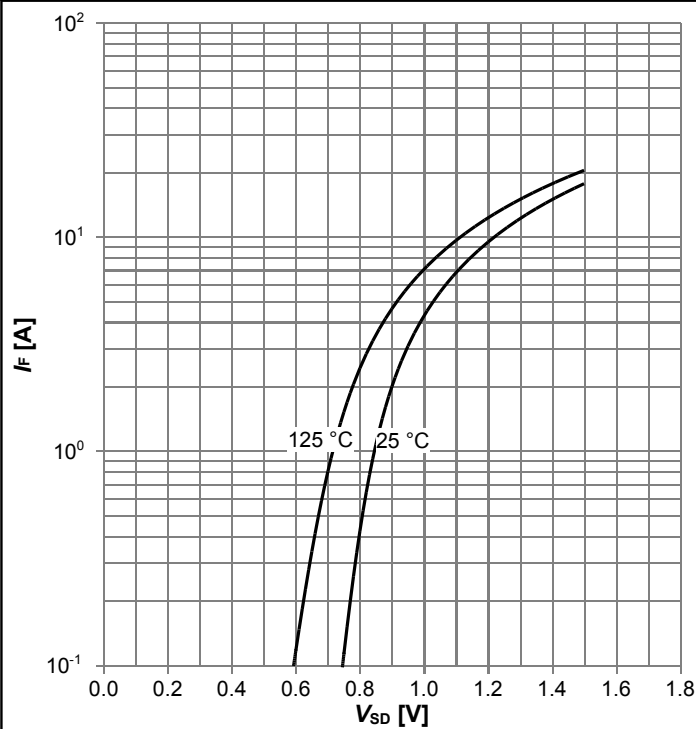
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



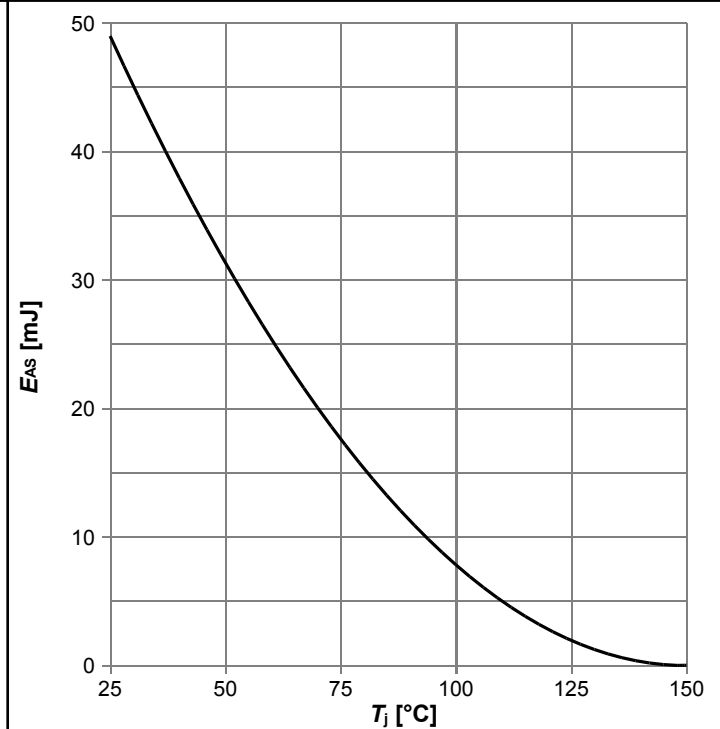
$V_{GS} = f(Q_{gate})$; $I_D = 6.0$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



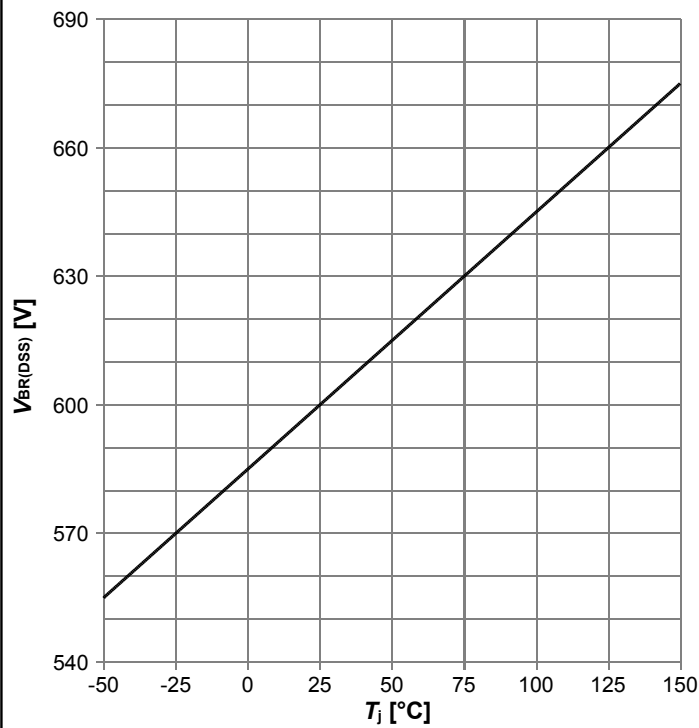
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



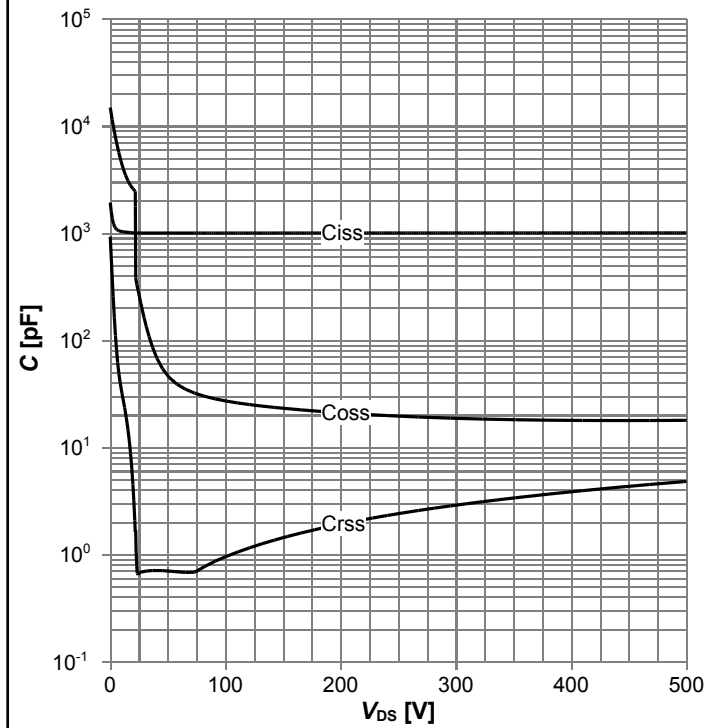
$E_{AS} = f(T_j)$; $I_D = 3.2$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



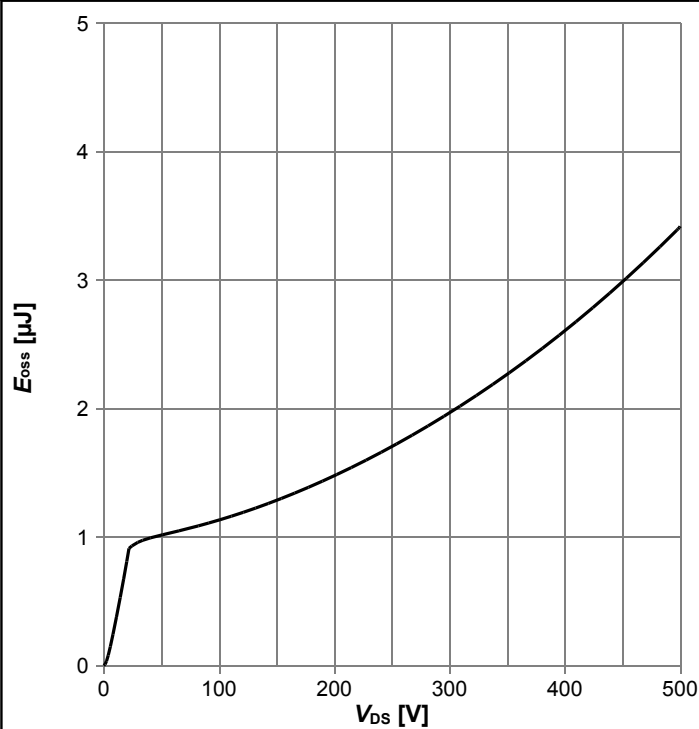
$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



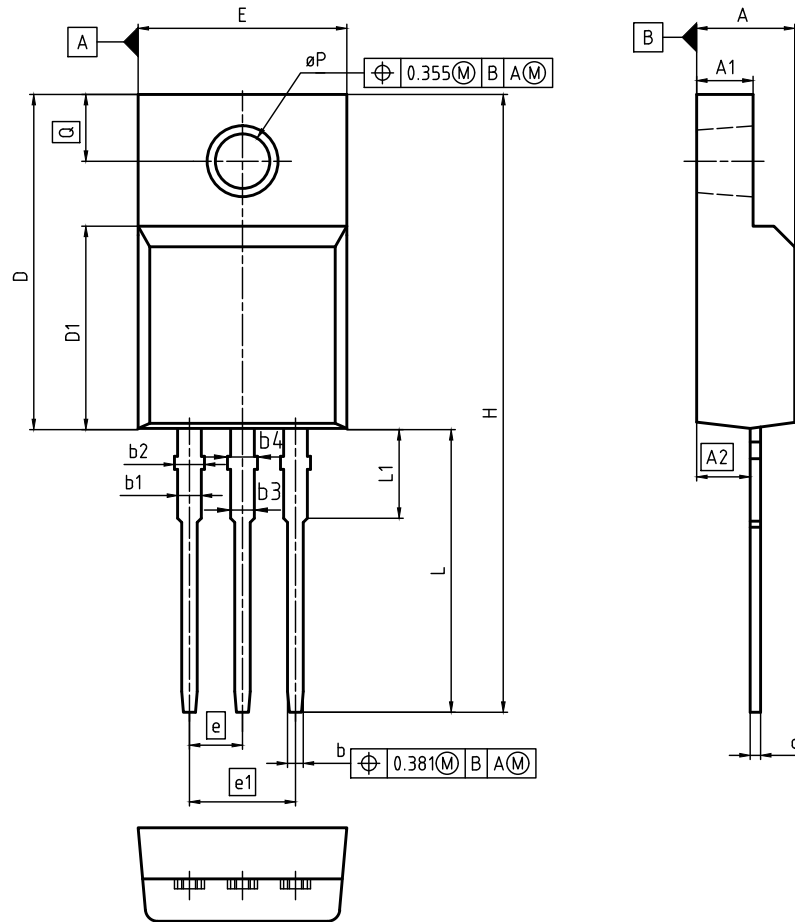
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss} = f(V_{DS})$

6 Package Outlines



DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.50	4.90	0.177	0.193
A1	2.34	2.85	0.092	0.112
A2	2.42	2.86	0.095	0.113
b	0.65	0.90	0.026	0.035
b1	0.95	1.38	0.037	0.054
b2	0.95	1.51	0.037	0.059
b3	0.65	1.38	0.026	0.054
b4	0.65	1.51	0.026	0.059
c	0.40	0.63	0.016	0.025
D	15.67	16.15	0.617	0.636
D1	8.97	9.83	0.353	0.387
E	10.00	10.65	0.394	0.419
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	3		3	
H	28.70	29.75	1.130	1.171
L	12.78	13.75	0.503	0.541
L1	2.83	3.45	0.111	0.136
øP	2.95	3.38	0.116	0.133
Q	3.15	3.50	0.124	0.138

DOCUMENT NO. Z8B00003319
SCALE 0 2.5 5mm
EUROPEAN PROJECTION
ISSUE DATE 24-10-2014
REVISION 05

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm/inches

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS CFD7 Webpage:** www.infineon.com
- **IFX CoolMOS CFD7 application note:** www.infineon.com
- **IFX CoolMOS CFD7 simulation model:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA60R210CFD7

Revision: 2018-04-20, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2018-04-20	Release of final version

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