

CoolMOS™ Power Transistor

Features

- Lowest figure-of-merit $R_{ON} \times Q_g$
- Ultra low gate charge
- Extreme dv/dt rated
- High peak current capability
- Qualified according to JEDEC¹⁾ for target applications
- Pb-free lead plating; RoHS compliant

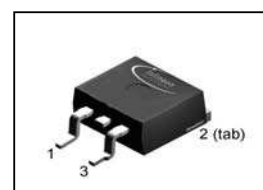
Product Summary

$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	0.125	Ω
$Q_{g,typ}$	53	nC

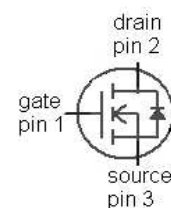
CoolMOS CP is specially designed for:

- Hard switching topologies, for Server and Telecom

PG-TO263



Type	Package	Ordering Code	Marking
IPB60R125CP	PG-TO263	SP000088488	6R125P



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}$	25	A
		$T_C=100\text{ °C}$	16	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	82	
Avalanche energy, single pulse	E_{AS}	$I_D=11\text{ A}$, $V_{DD}=50\text{ V}$	708	mJ
Avalanche energy, repetitive t_{AR} ^{2),3)}	E_{AR}	$I_D=11\text{ A}$, $V_{DD}=50\text{ V}$	1.2	
Avalanche current, repetitive t_{AR} ^{2),3)}	I_{AR}		11	A
MOSFET dv/dt ruggedness	dv/dt	$V_{DS}=0\ldots480\text{ V}$	50	V/ns
Gate source voltage	V_{GS}	static	± 20	V
		AC ($f>1\text{ Hz}$)	± 30	
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	208	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	°C

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous diode forward current	I_S	$T_C=25\text{ °C}$	16	A
Diode pulse current ²⁾	$I_{S,pulse}$		82	
Reverse diode dv/dt ⁴⁾	dv/dt		15	V/ns

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	R_{thJC}		-	-	0.6	K/W
Thermal resistance, junction - ambient	R_{thJA}	SMD version, device on PCB, minimal footprint	-	-	62	
		SMD version, device on PCB, 6 cm ² cooling area ⁵⁾	-	35	-	
Soldering temperature, wave- & reflowsoldering allowed	T_{solder}	reflow MSL1	-	-	260	°C

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$	600	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$, $I_D=1.1\text{ mA}$	2.5	3	3.5	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$	-	-	2	μA
		$V_{DS}=600\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$	-	20	-	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}$, $I_D=16\text{ A}$, $T_j=25\text{ °C}$	-	0.11	0.125	Ω
		$V_{GS}=10\text{ V}$, $I_D=16\text{ A}$, $T_j=150\text{ °C}$	-	0.30	-	
Gate resistance	R_G	$f=1\text{ MHz}$, open drain	-	2.1	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}$, $V_{DS}=100\text{ V}$, $f=1\text{ MHz}$	-	2500	-	pF
Output capacitance	C_{oss}		-	120	-	
Effective output capacitance, energy related ⁶⁾	$C_{o(er)}$	$V_{GS}=0\text{ V}$, $V_{DS}=0\text{ V}$ to 480 V	-	110	-	
Effective output capacitance, time related ⁷⁾	$C_{o(tr)}$		-	300	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=400\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=16\text{ A}$, $R_G=3.3\ \Omega$	-	15	-	ns
Rise time	t_r		-	5	-	
Turn-off delay time	$t_{d(off)}$		-	50	-	
Fall time	t_f		-	5	-	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD}=400\text{ V}$, $I_D=16\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$	-	12	-	nC
Gate to drain charge	Q_{gd}		-	18	-	
Gate charge total	Q_g		-	53	70	
Gate plateau voltage	$V_{plateau}$		-	5.0	-	V

Reverse Diode

Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}$, $I_F=16\text{ A}$, $T_j=25\text{ °C}$	-	0.9	1.2	V
Reverse recovery time	t_{rr}	$V_R=400\text{ V}$, $I_F=I_S$, $di_F/dt=100\text{ A}/\mu\text{s}$	-	430	-	ns
Reverse recovery charge	Q_{rr}		-	9	-	μC
Peak reverse recovery current	I_{rrm}		-	42	-	A

¹⁾ J-STD20 and JESD22

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Repetitive avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR} \cdot f$.

⁴⁾ $I_{SD}=I_D$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DCLink}=400\text{ V}$, $V_{peak} < V_{(BR)DSS}$, $T_j < T_{j,max}$, identical low side and high side switch.

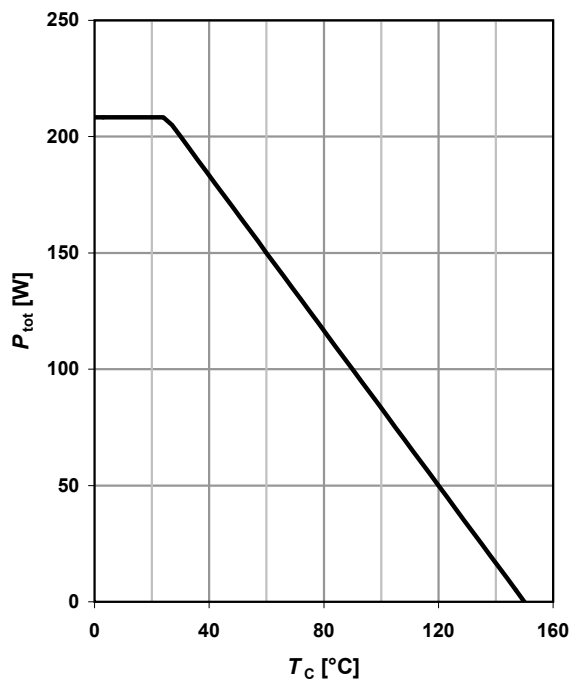
⁵⁾ Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical without blown air

⁶⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁷⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

1 Power dissipation

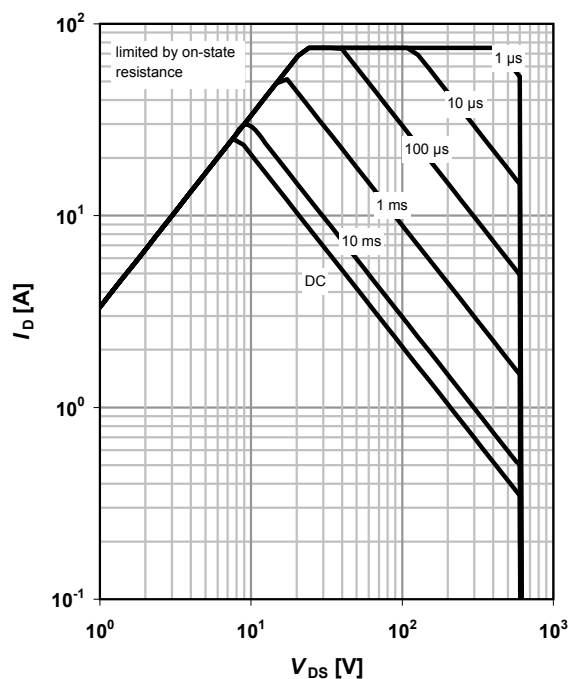
$$P_{\text{tot}} = f(T_C)$$



2 Safe operating area

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

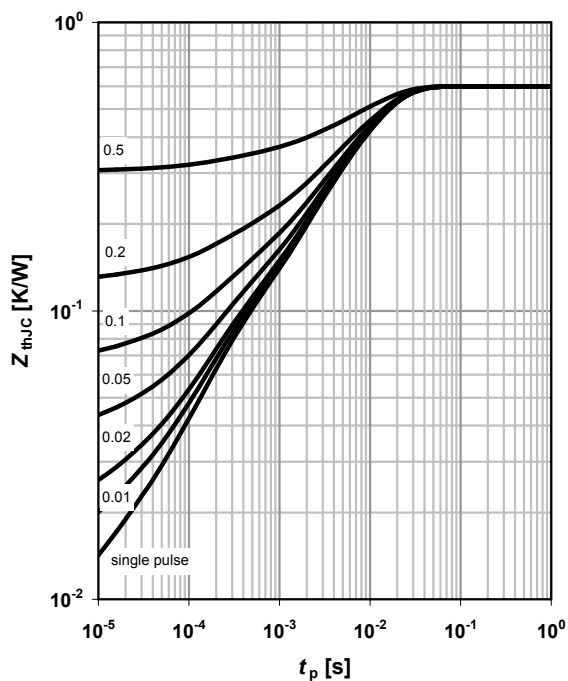
parameter: t_p



3 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

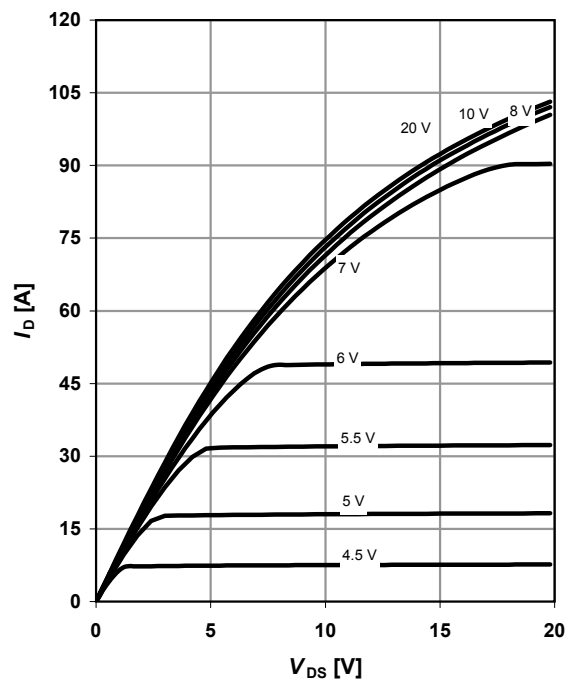
parameter: $D = t_p / T$



4 Typ. output characteristics

$$I_D = f(V_{DS}); T_J = 25^\circ\text{C}$$

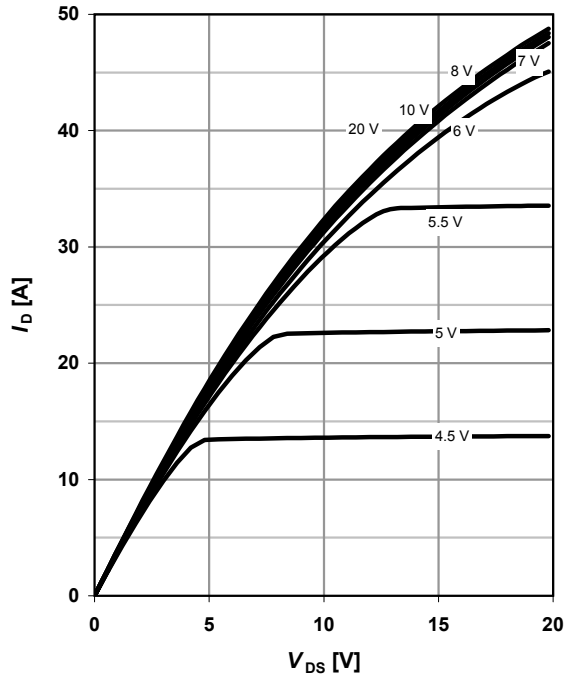
parameter: V_{GS}



5 Typ. output characteristics

$$I_D = f(V_{DS}); T_j = 150^\circ\text{C}$$

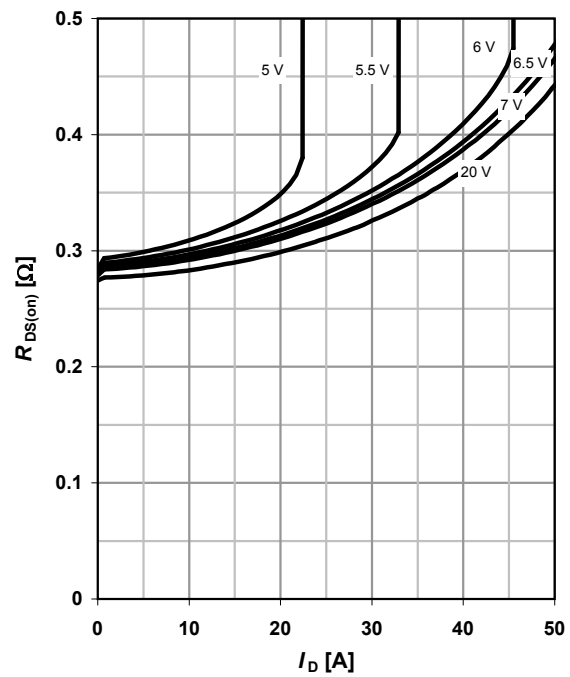
parameter: V_{GS}



6 Typ. drain-source on-state resistance

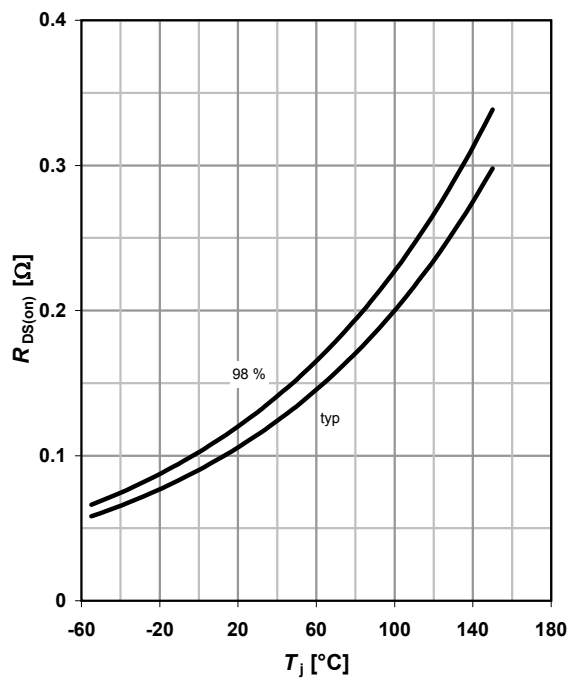
$$R_{DS(on)} = f(I_D); T_j = 150^\circ\text{C}$$

parameter: V_{GS}



7 Drain-source on-state resistance

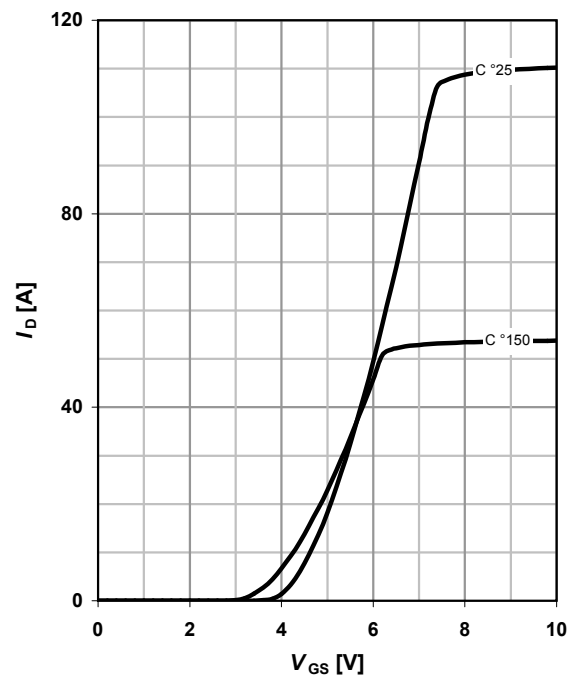
$$R_{DS(on)} = f(T_j); I_D = 16\text{ A}; V_{GS} = 10\text{ V}$$



8 Typ. transfer characteristics

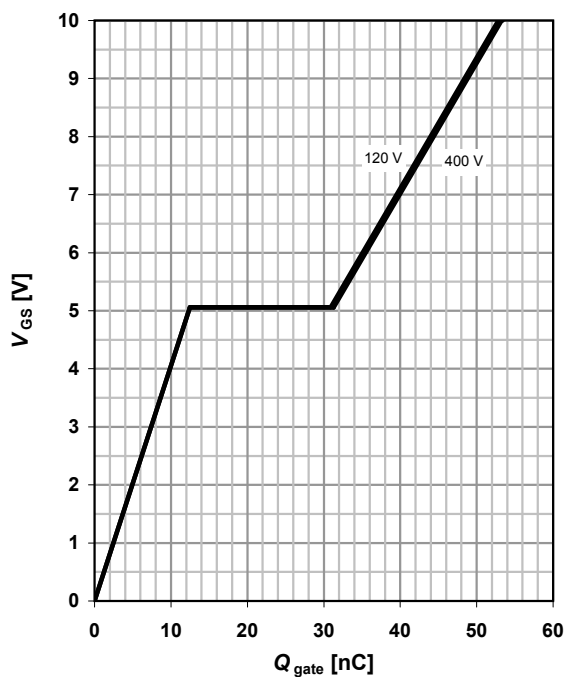
$$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|/R_{DS(on)\max}$$

parameter: T_j



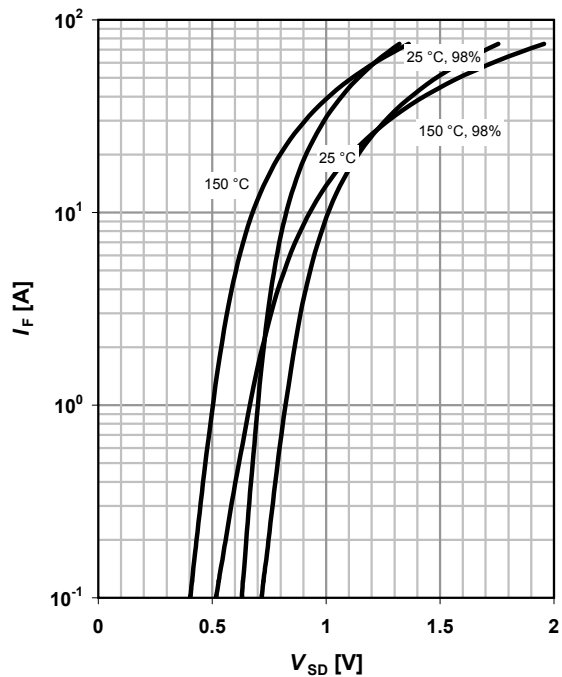
9 Typ. gate charge

 $V_{GS}=f(Q_{gate}); I_D=16\text{ A pulsed}$

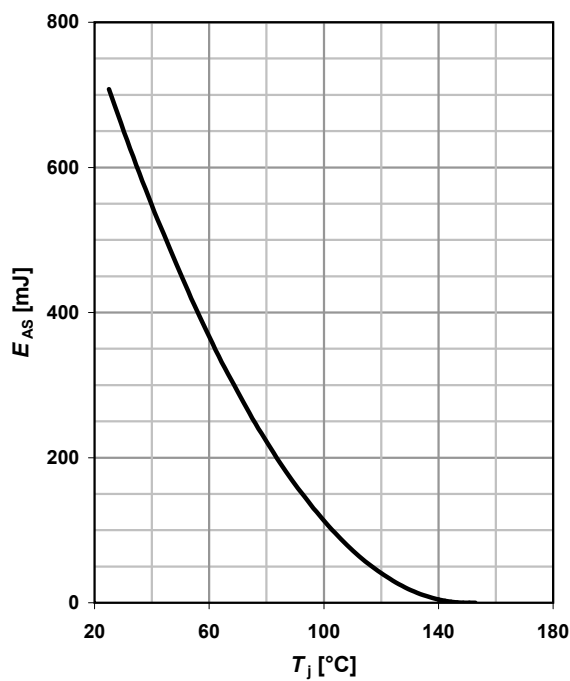
parameter: V_{DD}


10 Forward characteristics of reverse diode

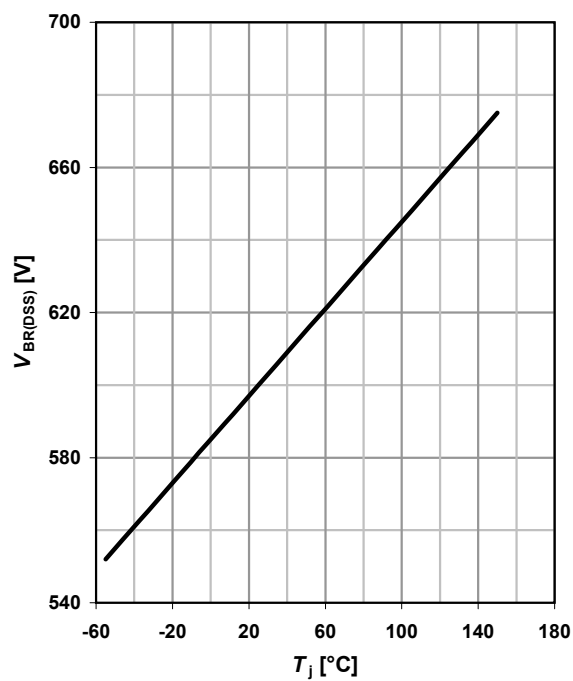
 $I_F=f(V_{SD})$

parameter: T_j


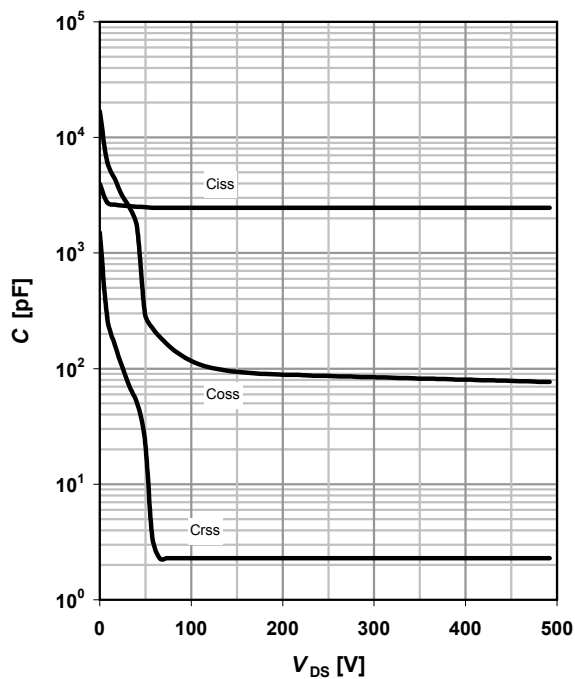
11 Avalanche energy

 $E_{AS}=f(T_j); I_D=11\text{ A}; V_{DD}=50\text{ V}$


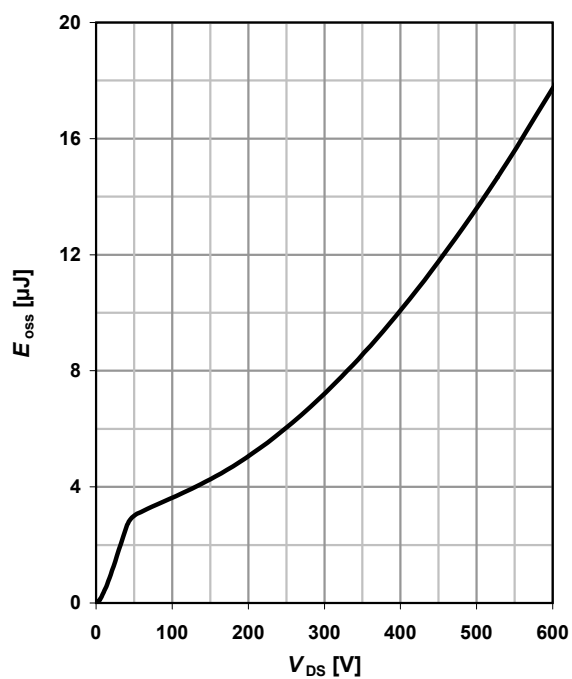
12 Drain-source breakdown voltage

 $V_{BR(DSS)}=f(T_j); I_D=0.25\text{ mA}$


13 Typ. capacitances

 $C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$


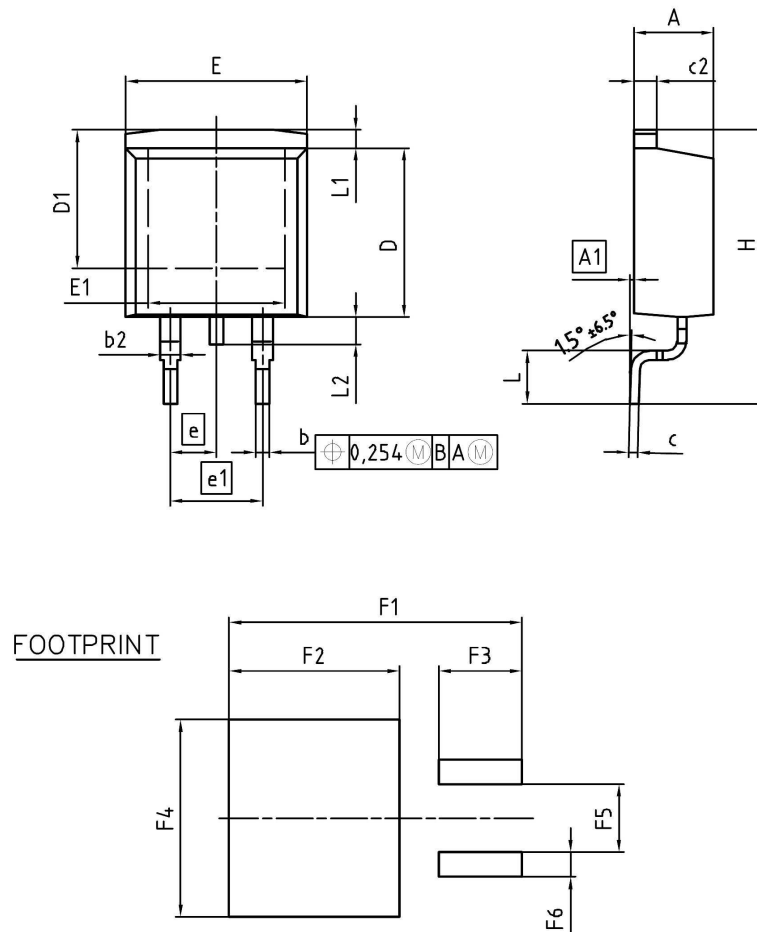
14 Typ. Coss stored energy

 $E_{oss} = f(V_{DS})$


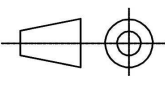
Definition of diode switching characteristics



Figure 1 Outline PG-TO 263, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	0.00	0.25	0.000	0.010
b	0.65	0.85	0.026	0.033
b2	0.95	1.15	0.037	0.045
c	0.33	0.65	0.013	0.026
c2	1.17	1.40	0.046	0.055
D	8.51	9.45	0.335	0.372
D1	7.10	7.90	0.280	0.311
E	9.80	10.31	0.386	0.406
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	2		2	
H	14.61	15.88	0.575	0.625
L	2.29	3.00	0.090	0.118
L1	0.70	1.60	0.028	0.063
L2	1.00	1.78	0.039	0.070
F1	16.05	16.25	0.632	0.640
F2	9.30	9.50	0.366	0.374
F3	4.50	4.70	0.177	0.185
F4	10.70	10.90	0.421	0.429
F5	3.65	3.85	0.144	0.152
F6	1.25	1.45	0.049	0.057

DOCUMENT NO. Z8B00003324
SCALE 0 5 5 7.5mm
EUROPEAN PROJECTION 
ISSUE DATE 30-08-2007
REVISION 01

Revision History

IPB60R125CP

Revision: 2018-04-04, Rev. 1.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.1	2018-04-04	Updated package outline

Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CoolGaN™, CoolMOS™, CoolSET™, CoolSiC™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, DrBlade™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, Infineon™, ISOFACE™, IsoPACK™, i-Wafer™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OPTIGA™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PROFET™, PRO-SiL™, RASIC™, REAL3™, ReverSave™, SatRIC™, SIEGET™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, SPOC™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

Trademarks updated August 2015

Other Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

erratum@infineon.com

Published by

Infineon Technologies AG

81726 München, Germany

© 2018 Infineon Technologies AG

All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.