Single-Supply, Low Power, Precision FET Input Quad Buffer

Data Sheet

AD8244

FEATURES

- **Low power**
  - **250 µA maximum supply current per amplifier**
- **FET input**
  - **2 pA maximum input bias current at 25°C**
  - **Extremely high input impedance**
- **Low noise**
  - **13 nV/√Hz voltage noise at 1 kHz**
  - **0.4 µV p-p voltage noise (0.1 Hz to 10 Hz)**
  - **0.8 fA/√Hz current noise at 1 kHz**
- **High dc precision**
  - **3 µV/°C maximum offset drift (B grade)**
- **3 MHz bandwidth**
- **Unique pinout**
  - **No leakage from inputs to supply pins**
  - **Provides guarding capability**
- **Rail-to-rail output**
- **Single-supply operation**
  - **Input range extends to ground**
- **Wide supply range**
  - **Single-supply: 3 V to 36 V**
  - **Dual-supply: ±1.5 V to ±18 V**
- **Available in a compact 10-lead MSOP**

APPLICATIONS

- **Biopotential electrodes**
- **Medical instrumentation**
- **High impedance sensor conditioning**
- **Filters**
- **Photodiode amplifiers**

PIN CONFIGURATION

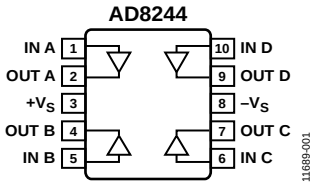

Figure 1. Pinout Isolates Inputs from Low-Impedance Leakage Sources

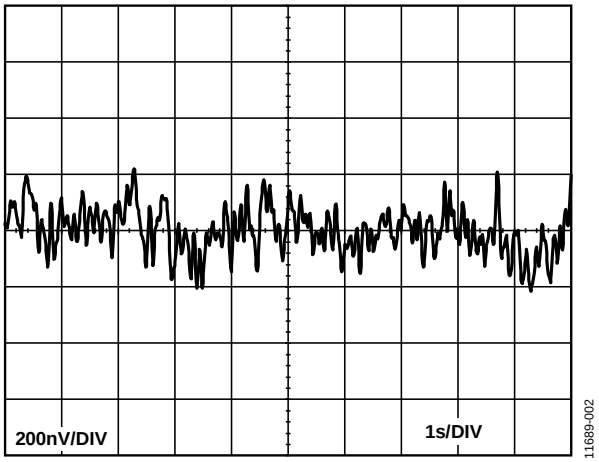

Figure 2. 0.1 Hz to 10 Hz Voltage Noise

GENERAL DESCRIPTION

The AD8244 is a precision, low power, FET input, quad unity-gain buffer that is designed to isolate very large source impedances from the rest of the signal chain. The 2 pA maximum bias current, near zero current noise, and 10 TΩ input impedance introduce almost no error, even with source impedance well into the megaohms.

Many traditional operational amplifier pinouts have a supply pin that is next to the noninverting input. A guard trace must be routed between these pins to avoid leakage currents much larger than the bias current of a FET input op amp. Guard traces can be routed between pins for large packages, such as DIP or even SOIC; however, the board area consumed by these packages is prohibitive for many modern applications. The AD8244 solves this problem with a unique pinout that physically separates the high impedance inputs from the low impedance supplies and outputs of the other buffers. This configuration simplifies guarding while reducing board space, allowing high performance and high density in the same design.

The AD8244 design is focused on solving problems specific to buffers. This includes close channel-to-channel matching which allows channels of the AD8244 to be used in differential signal chains with minimal error. With its low voltage noise, wide supply range, and high precision, the AD8244 is also flexible enough to provide high performance anywhere a unity-gain buffer is needed, even with low source resistance.

The AD8244 is specified over the industrial temperature range of −40°C to +85°C. It is available in a 10-lead MSOP package.

Rev. A Document Feedback

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REVISION HISTORY

12/14—Rev. 0 to Rev. A

Added Figure 1 Caption and Changes to Figure 2 ... 1
Changes to Low Output Impedance vs. Frequency Section ... 15
Changes to Electrocardiogram (ECG) Section, Filtering Section, Figure 42, and Figure 43 ... 16
Changes to Figure 44 ... 17
Changes to Ordering Guide ... 19

10/13—Revision 0: Initial Version

SPECIFICATIONS

$+V_S$ = 5 V, $-V_S$ = 0 V, T_A = 25°C, V_{IN} = 0.2 V, R_L = 10 kΩ to ground, unless otherwise noted.

Table 1.

		AD8244A			AD8244B			
Parameter	**Test Conditions/Comments**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
DC PERFORMANCE								
Offset Voltage			100	600		100	350	µV
Over Temperature	T_A = −40°C to +85°C			1.25			0.675	mV
Average Temperature Coefficient	T_A = −40°C to +85°C			10			5	µV/°C
Offset Voltage Matching	Channel to channel			800			500	µV
Input Bias Current			0.5	10		0.5	2	pA
Over Temperature	T_A = 85°C			150			50	pA
Input Bias Current Matching	Channel to channel		0.05			0.05	0.2	pA
Over Temperature	T_A = 85°C		2			2		pA
SYSTEM PERFORMANCE								
Nominal Gain			1			1		V/V
System Error[1]	V_{OUT} = 0.2 V to 3 V			0.08			0.05	%
Average Temperature Coefficient	T_A = −40°C to +85°C			2			1	ppm/°C
Gain Matching	Channel to channel			0.10			0.08	%
NOISE PERFORMANCE								
Voltage Noise								
Spectral Density	f = 1 kHz		13			13		nV/√Hz
Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.4			0.4	2	µV p-p
Current Noise								
Spectral Density	f = 1 kHz		0.8			0.8		fA/√Hz
Peak-to-Peak	f = 0.1 Hz to 10 Hz		8			8		fA p-p
DYNAMIC PERFORMANCE								
Small Signal Bandwidth	−3 dB		3			3		MHz
Slew Rate			0.8			0.8		V/µs
Settling Time to 0.01%	V_{OUT} = 0.2 V to 3 V		8			8		µs
INPUT CHARACTERISTICS								
Input Voltage Range[2]		0		4	0		4	V
Over Temperature	T_A = −40°C to +85°C	0		3.5	0		3.5	V
Input Impedance[3]			10||4			10||4		TΩ||pF
OUTPUT CHARACTERISTICS								
Output Swing	R_L = 10 kΩ to ground	0.025		4.9	0.025		4.9	V
Over Temperature	T_A = −40°C to +85°C	0.03		4.88	0.03		4.88	V
Output Swing	R_L = no load	0.025		4.97	0.025		4.97	V
Over Temperature	T_A = −40°C to +85°C	0.03		4.95	0.03		4.95	V
Short-Circuit Current			8			8		mA
Capacitive Load Drive			200			200		pF
POWER SUPPLY								
Operating Range	Single supply	3		36	3		36	V
	Dual supply	±1.5		±18	±1.5		±18	V
Power Supply Rejection	V_{IN} = 2.5 V, $+V_S$ = 4.5 V to 5.5 V		80			80		dB
Supply Current per Amplifier	I_{OUT} = 0 mA		180	250		180	250	µA
Over Temperature	T_A = −40°C to +85°C			300			300	µA
TEMPERATURE RANGE								
Specified Performance		−40		+85	−40		+85	°C

[1] Error as a percentage of the measurement. This includes the effects of open-loop gain and common-mode rejection ratio.
[2] The inputs of the AD8244 can go up to the positive supply; however, the input range is derated because error increases near the positive supply as the input transistors start to saturate. The inputs also maintain high impedance when driven slightly below ground.
[3] For more information on the input impedance, see Figure 24 and Figure 37.

V_S = ±5 V, T_A = 25°C, V_{IN} = 0 V, R_L = 10 kΩ, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	AD8244A Min	AD8244A Typ	AD8244A Max	AD8244B Min	AD8244B Typ	AD8244B Max	Unit
DC PERFORMANCE								
Offset Voltage			100	600		100	350	µV
Over Temperature	T_A = −40°C to +85°C			1.25			0.675	mV
Average Temperature Coefficient	T_A = −40°C to +85°C			10			5	µV/°C
Offset Voltage Matching	Channel to channel			800			500	µV
Input Bias Current			0.5	10		0.5	2	pA
Over Temperature	T_A = 85°C			150			50	pA
Input Bias Current Matching	Channel to channel		0.05			0.05	0.2	pA
Over Temperature	T_A = 85°C		2			2		pA
SYSTEM PERFORMANCE								
Nominal Gain			1			1		V/V
System Error[1]	V_{OUT} = −3 V to +3 V			0.05			0.03	%
Average Temperature Coefficient	T_A = −40°C to +85°C			2			1	ppm/°C
Gain Matching	Channel to channel			0.08			0.05	%
Nonlinearity	V_{OUT} = −3 V to +3 V		20			20		ppm
NOISE PERFORMANCE								
Voltage Noise								
Spectral Density	f = 1 kHz		13			13		nV/√Hz
Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.4			0.4	2	µV p-p
Current Noise								
Spectral Density	f = 1 kHz		0.8			0.8		fA/√Hz
Peak-to-Peak	f = 0.1 Hz to 10 Hz		8			8		fA p-p
DYNAMIC PERFORMANCE								
Small Signal Bandwidth	−3 dB		3.3			3.3		MHz
Slew Rate			0.8			0.8		V/µs
Settling Time to 0.01%	V_{OUT} = −3 V to +3 V		14			14		µs
INPUT CHARACTERISTICS								
Input Voltage Range[2]		−5		+4	−5		+4	V
Over Temperature	T_A = −40°C to +85°C	−5		+3.5	−5		+3.5	V
Input Impedance[3]			10‖4			10‖4		TΩ‖pF
OUTPUT CHARACTERISTICS								
Output Swing	R_L = 10 kΩ	−4.9		+4.9	−4.9		+4.9	V
Over Temperature	T_A = −40°C to +85°C	−4.88		+4.88	−4.88		+4.88	V
Output Swing	R_L = no load	−4.975		+4.97	−4.975		+4.97	V
Over Temperature	T_A = −40°C to +85°C	−4.95		+4.95	−4.95		+4.95	V
Short-Circuit Current			10			10		mA
Capacitive Load Drive			200			200		pF
POWER SUPPLY								
Operating Range	Single supply	3		36	3		36	V
	Dual supply	±1.5		±18	±1.5		±18	V
Power Supply Rejection	V_S = ±3 V to ±18 V		90		80	90		dB
Supply Current per Amplifier	I_{OUT} = 0 mA		180	250		180	250	µA
Over Temperature	T_A = −40°C to +85°C			300			300	µA
TEMPERATURE RANGE								
Specified Performance	T_A	−40		+85	−40		+85	°C

[1] Error as a percentage of the measurement. This includes the effects of open-loop gain and common-mode rejection ratio.
[2] The inputs of the AD8244 can go up to the positive supply; however, the input range is derated because error increases near the positive supply as the input transistors start to saturate.
[3] For more information on the input impedance, see Figure 24 and Figure 37.

V_S = ±15 V, T_A = 25°C, V_{IN} = 0 V, R_L = 10 kΩ, unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	AD8244A Min	AD8244A Typ	AD8244A Max	AD8244B Min	AD8244B Typ	AD8244B Max	Unit
DC PERFORMANCE								
Offset Voltage			100	600		100	350	µV
Over Temperature	T_A = −40°C to +85°C			1.25			0.545	mV
Average Temperature Coefficient	T_A = −40°C to +85°C			10			3	µV/°C
Offset Voltage Matching	Channel to channel			800			500	µV
Input Bias Current			0.9	10		0.9	3	pA
Over Temperature	T_A = 85°C			150			100	pA
Input Bias Current Matching	Channel to channel		0.05			0.05	0.2	pA
Over Temperature	T_A = 85°C		2			2		pA
SYSTEM PERFORMANCE								
Nominal Gain			1			1		V/V
System Error[1]	V_{OUT} = −10 V to +10 V			0.03			0.008	%
Average Temperature Coefficient	T_A = −40°C to +85°C			2			1	ppm/°C
Gain Matching	Channel to channel			0.05			0.01	%
Nonlinearity	V_{OUT} = −10 V to +10 V		5			5		ppm
NOISE PERFORMANCE								
Voltage Noise								
Spectral Density	f = 1 kHz		13			13		nV/√Hz
Peak-to-Peak	f = 0.1 Hz to 10 Hz		0.4			0.4		µV p-p
Current Noise								
Spectral Density	f = 1 kHz		0.8			0.8		fA/√Hz
Peak-to-Peak	f = 0.1 Hz to 10 Hz		8			8		fA p-p
DYNAMIC PERFORMANCE								
Small Signal Bandwidth	−3 dB		3.6			3.6		MHz
Slew Rate			0.8			0.8		V/µs
Settling Time to 0.01%	V_{OUT} = −10 V to +10 V		18			18		µs
INPUT CHARACTERISTICS								
Input Voltage Range[2]		−15		+14	−15		+14	V
Over Temperature	T_A = −40°C to +85°C	−15		+13.5	−15		+13.5	V
Input Impedance[3]			10‖4			10‖4		TΩ‖pF
OUTPUT CHARACTERISTICS								
Output Swing	R_L = 10 kΩ	−14.87		+14.87	−14.87		+14.87	V
Over Temperature	T_A = −40°C to +85°C	−14.84		+14.84	−14.84		+14.84	V
Output Swing	R_L = no load	−14.95		+14.95	−14.95		+14.95	V
Over Temperature	T_A = −40°C to +85°C	−14.93		+14.93	−14.93		+14.93	V
Short-Circuit Current			20			20		mA
Capacitive Load Drive			200			200		pF
POWER SUPPLY								
Operating Range	Single supply	3		36	3		36	V
	Dual supply	±1.5		±18	±1.5		±18	V
Power Supply Rejection	V_S = ±3 V to ±18 V		90		80	90		dB
Supply Current per Amplifier	I_{OUT} = 0 mA		180	250		180	250	µA
Over Temperature	T_A = −40°C to +85°C			300			300	µA
TEMPERATURE RANGE								
Specified Performance	T_A	−40		+85	−40		+85	°C

[1] Error as a percentage of the measurement. This includes the effects of open-loop gain and common-mode rejection ratio.
[2] The inputs of the AD8244 can go up to the positive supply; however, the input range is derated because error increases near the positive supply as the input transistors start to saturate.
[3] For more information on the input impedance, see Figure 24 and Figure 37.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	±18 V
Output Short-Circuit Current Duration	Indefinite
Maximum Voltage at IN x or OUT x[1]	$+V_S$ + 0.3 V
Minimum Voltage at IN x or OUT x[1]	$-V_S$ − 0.3 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to + 85°C
Maximum Junction Temperature	150°C
ESD	
Human Body Model (HBM)	3 kV
Charged Device Model (CDM)	1.25 kV
Machine Model (MM)	100 V

[1] For voltages beyond these limits, use input protection resistors. See the Input Protection section for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
10-Lead MSOP	152	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

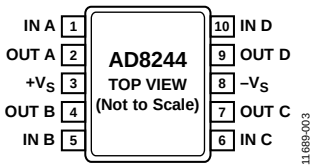

Figure 3. Pin Configuration

Table 6. Pin Function Description

Pin Number	Mnemonic	Description
1	IN A	Channel A Input
2	OUT A	Channel A Output
3	$+V_S$	Positive Supply Voltage
4	OUT B	Channel B Output
5	IN B	Channel B Input
6	IN C	Channel C Input
7	OUT C	Channel C Output
8	$-V_S$	Negative Supply Voltage
9	OUT D	Channel D Output
10	IN D	Channel D Input

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, T_A = 25°C, V_{IN} = 0 V, R_L = 10 kΩ, unless otherwise noted.

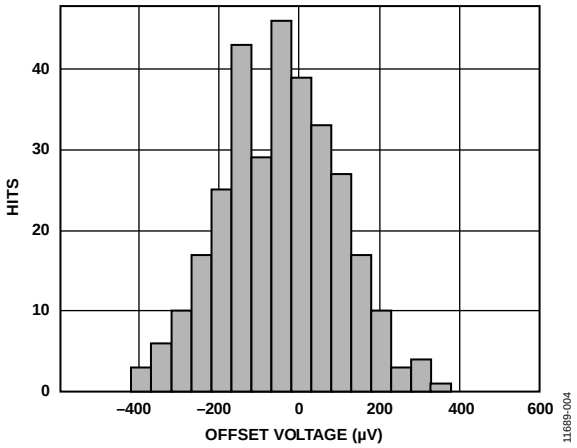

Figure 4. Typical Distribution of Offset Voltage

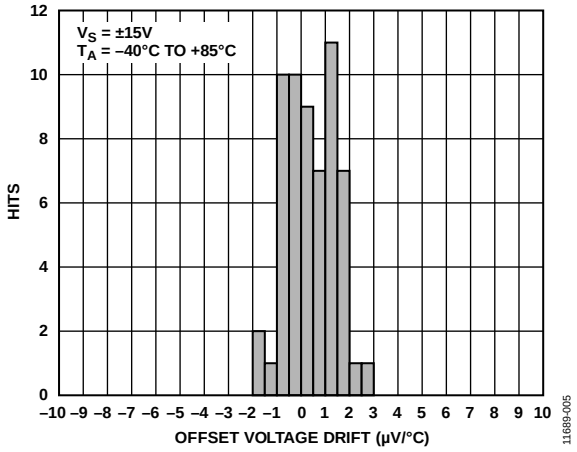

Figure 5. Typical Distribution of Offset Voltage Drift

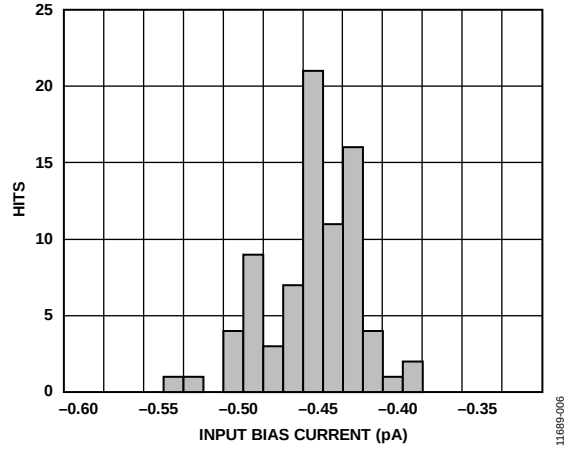

Figure 6. Typical Distribution of Input Bias Current

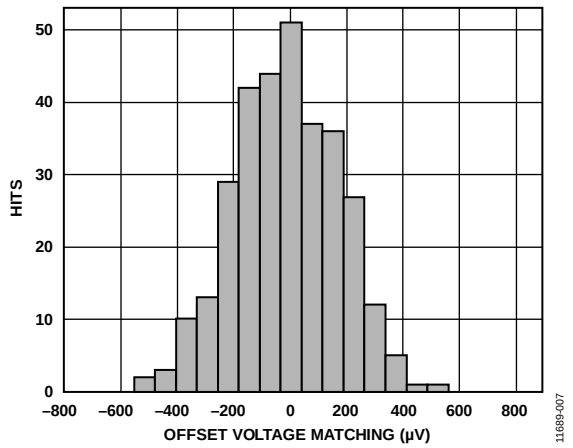

Figure 7. Typical Distribution of Offset Voltage Matching

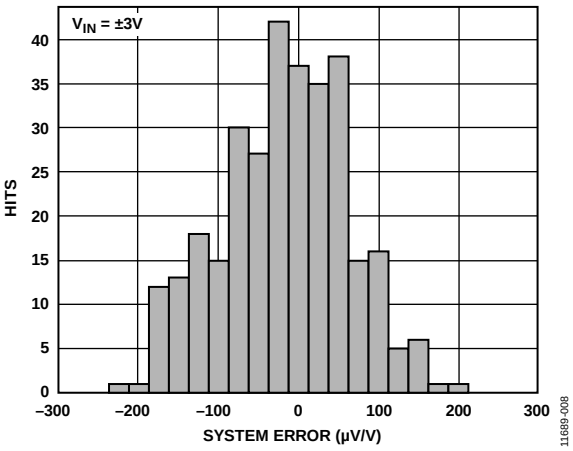

Figure 8. Typical Distribution of System Error

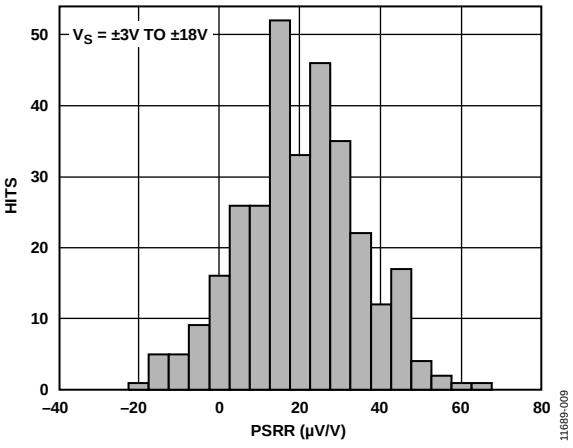

Figure 9. Typical Distribution of Power Supply Rejection Ratio (PSRR)

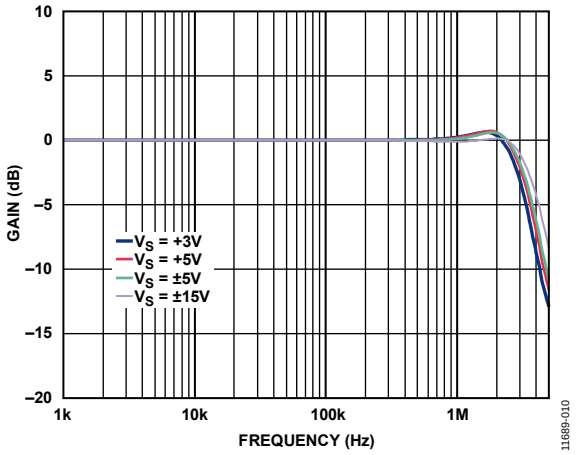

Figure 10. Gain vs. Frequency

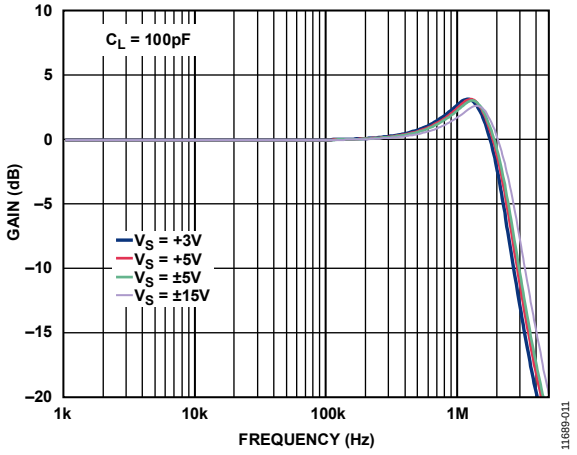

Figure 11. Gain vs. Frequency, C_L = 100 pF

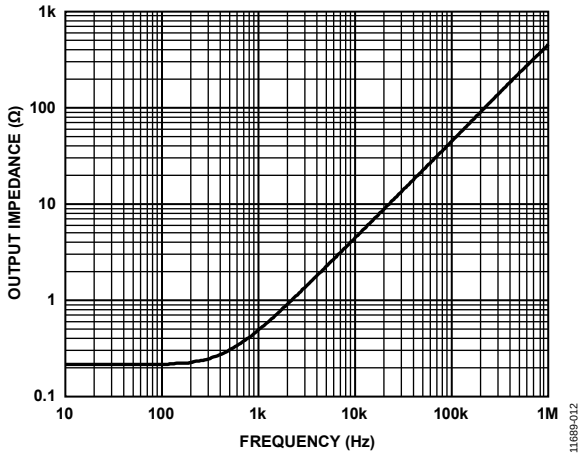

Figure 12. Output Impedance vs. Frequency

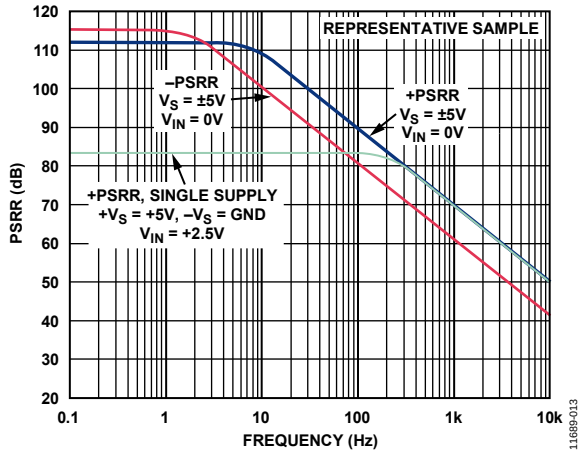

Figure 13. PSRR vs. Frequency

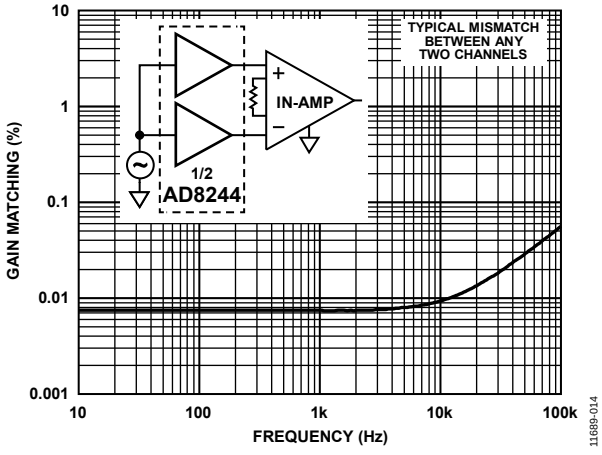

Figure 14. Gain Matching vs. Frequency

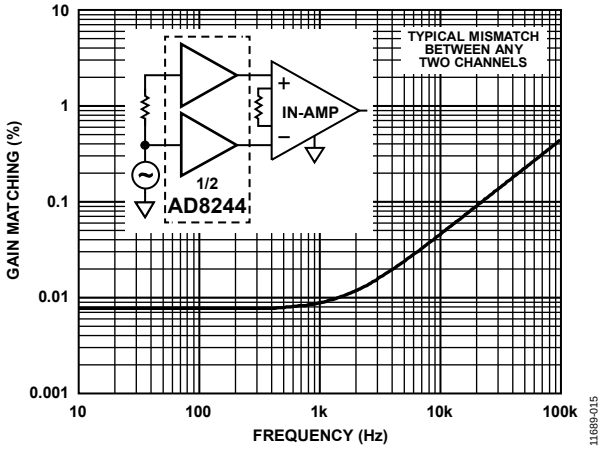

Figure 15. Gain Matching vs. Frequency, 1 kΩ Source Imbalance

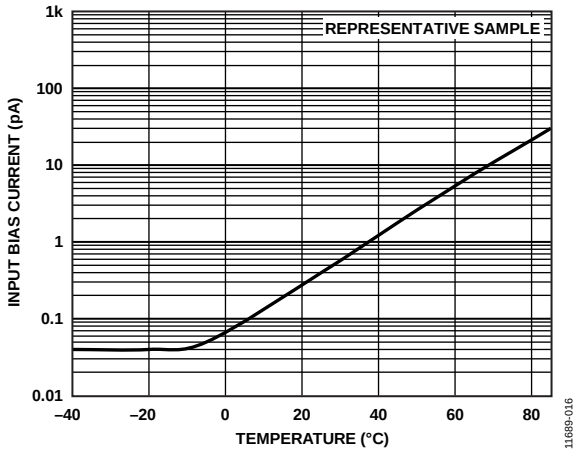

Figure 16. Input Bias Current vs. Temperature

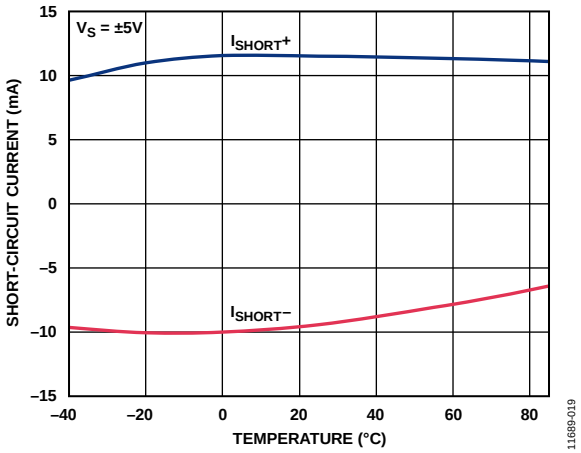

Figure 19. Short-Circuit Current vs. Temperature

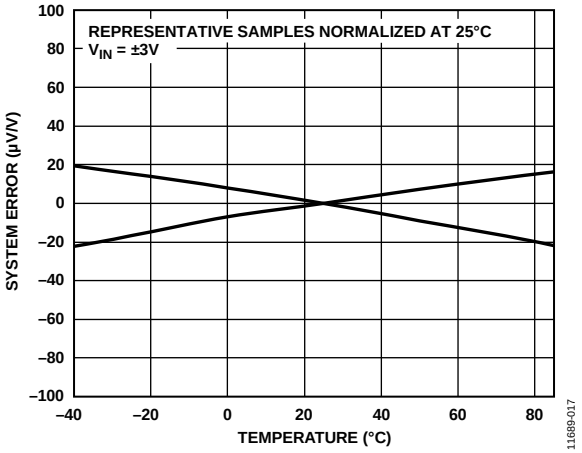

Figure 17. System Error vs. Temperature, Normalized at 25°C

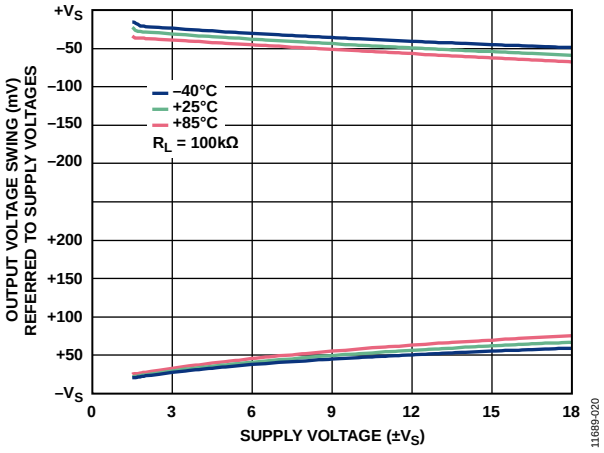

Figure 20. Output Voltage Swing vs. Supply Voltage, R_L = 100 kΩ

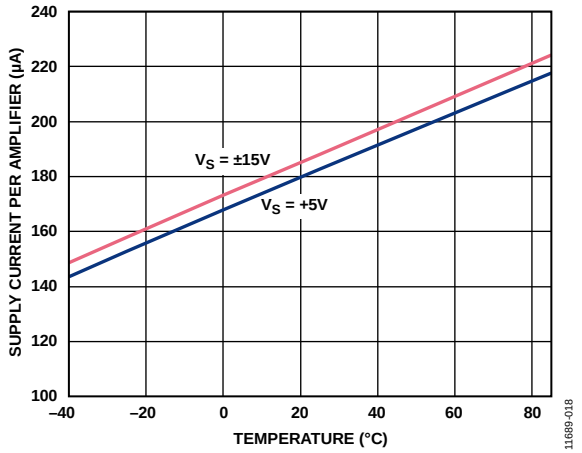

Figure 18. Supply Current vs. Temperature

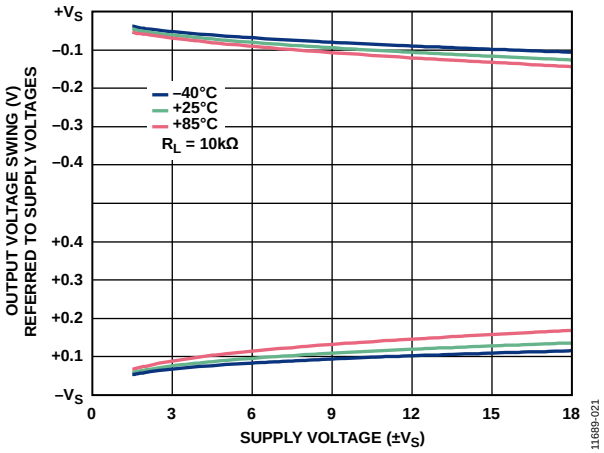

Figure 21. Output Voltage Swing vs. Supply Voltage, R_L = 10 kΩ

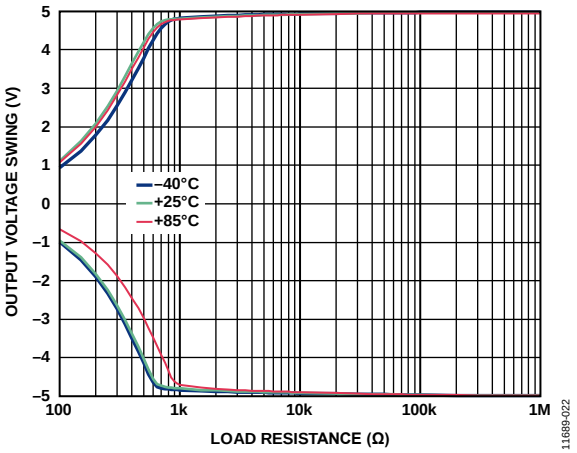

Figure 22. Output Voltage Swing vs. Load Resistance

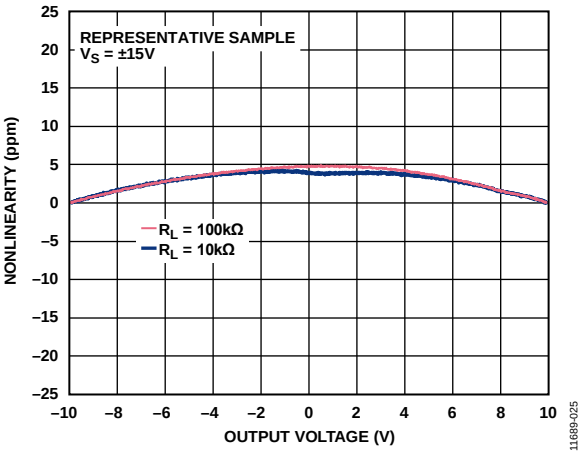

Figure 25. Nonlinearity, V_S = ±15 V

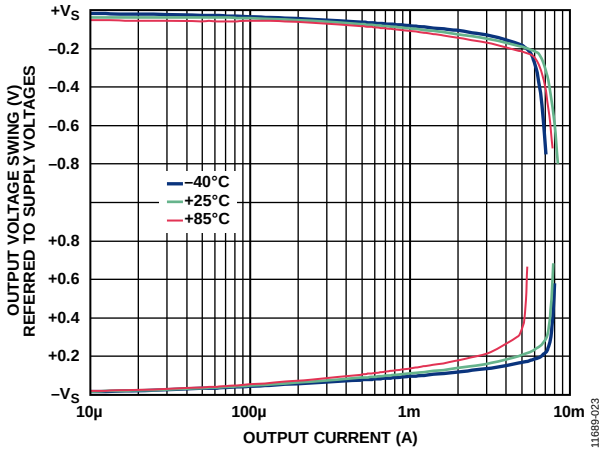

Figure 23. Output Voltage Swing vs. Output Current

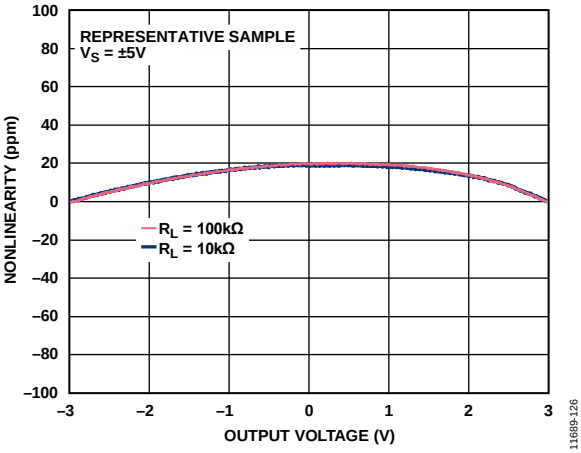

Figure 26. Nonlinearity, V_S = ±5 V

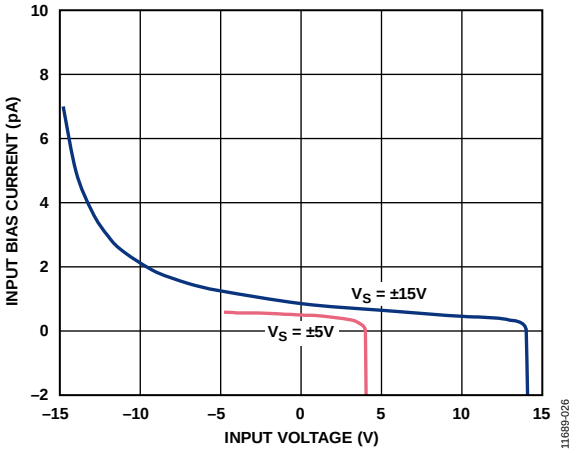

Figure 24. Input Bias Current vs. Input Voltage

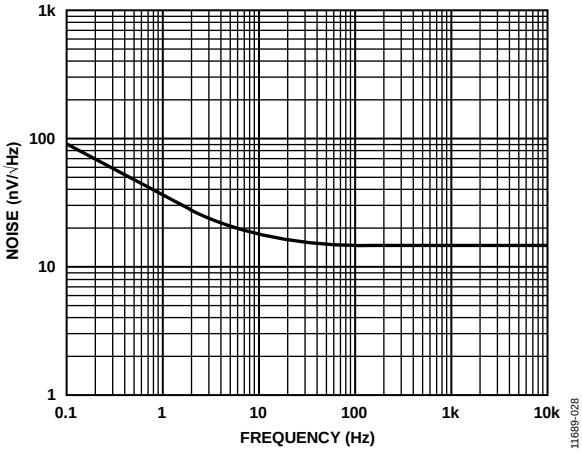

Figure 27. Voltage Noise Spectral Density vs. Frequency

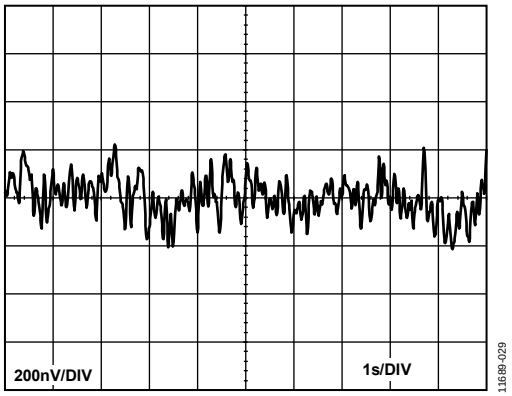

Figure 28. 0.1 Hz to 10 Hz Voltage Noise

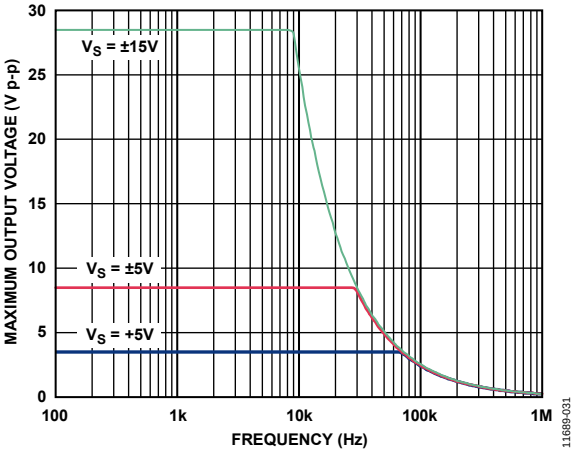

Figure 31. Large Signal Frequency Response

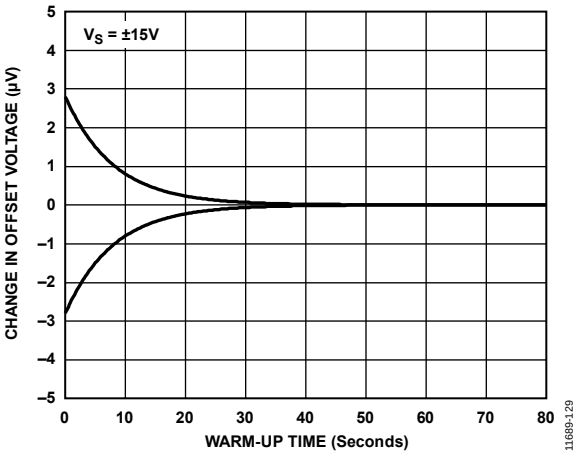

Figure 29. Change in Offset Voltage vs. Warm-Up Time

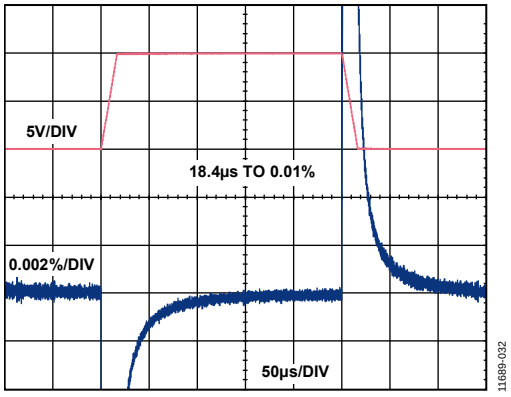

Figure 32. Large Signal Pulse Response and Settling Time, R_L = 10 kΩ, C_L = 100 pF

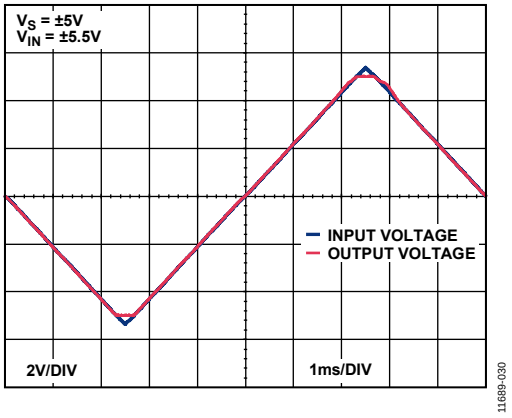

Figure 30. No Phase Reversal

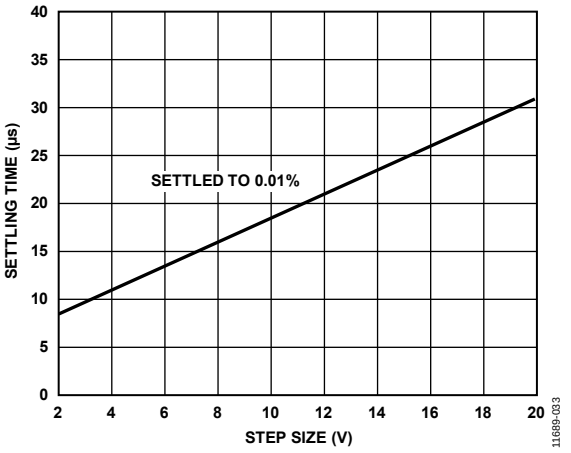

Figure 33. Settling Time vs. Step Size, R_L = 10 kΩ, C_L = 100 pF

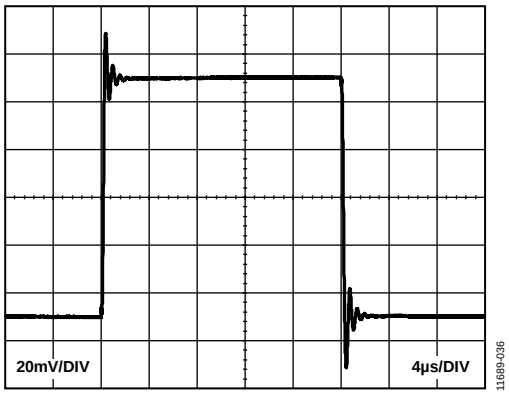

Figure 34. Small Signal Pulse Response, R_L = 10 kΩ, C_L = 100 pF

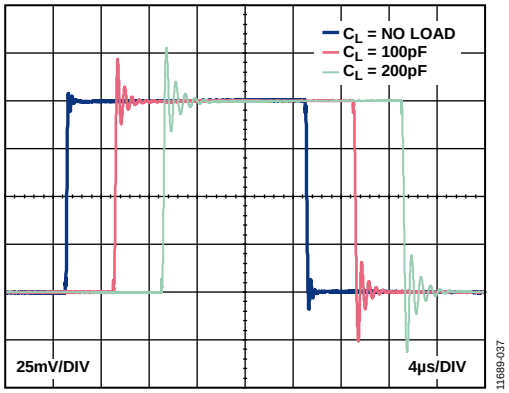

Figure 35. Small Signal Pulse Response with Various Capacitive Loads, R_L = No Load

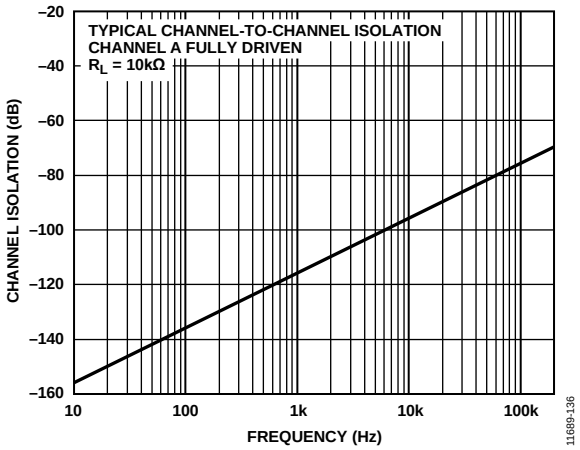

Figure 36. Channel Isolation vs. Frequency

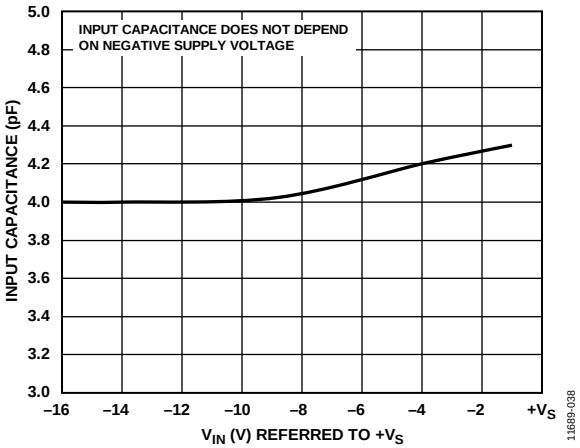

Figure 37. Input Capacitance vs. Input Voltage (V_{IN}) Referred to $+V_S$

THEORY OF OPERATION

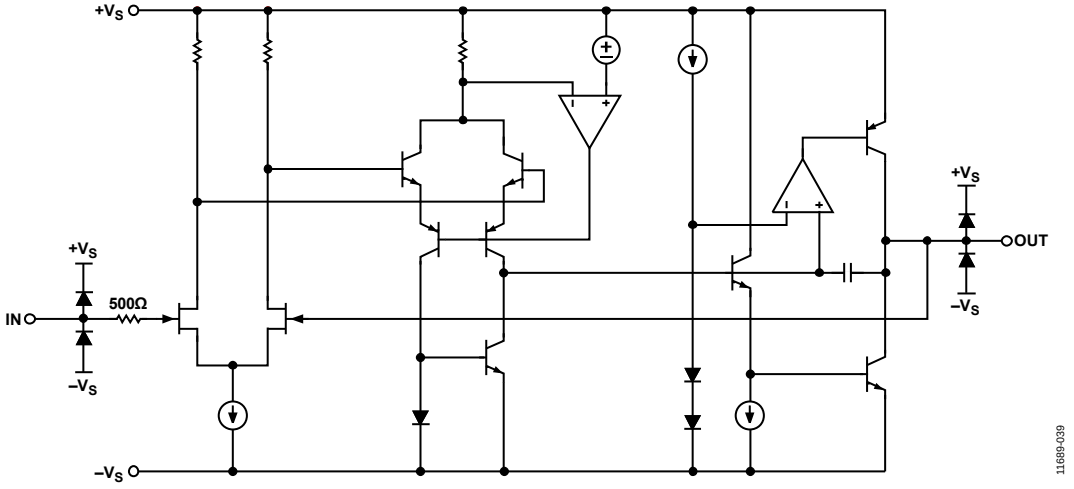

Figure 38. Simplified Schematic

OVERVIEW

The AD8244 is a precision, quad, FET input, unity-gain buffer that is designed to isolate very large source impedances from the rest of the signal chain. N-channel JFETs are used as the input transistors to provide a low offset (350 µV maximum), low noise (13 nV/√Hz typical), high impedance (more than 10 TΩ) input stage that operates right down to the negative supply voltage. Using a new drift trimming method, the B grade AD8244 is able to achieve very low offset voltage over temperature (0.545 mV maximum), and it introduces minimal system error over temperature. The AD8244 design is optimized for high precision applications, such as buffers for biopotential electrodes, where it is important that buffers have very high impedance inputs and channels that match closely. Because the AD8244 fits into a 10-lead package, whereas a quad op amp requires a minimum of 14 leads, routing space is reduced and parasitics from the feedback traces are eliminated. Furthermore, the flexible design and the high channel density of the AD8244 allow it to be used in the signal chain anywhere a unity-gain buffer is needed.

GUARDING

When using low input bias current FET input amplifiers, designers must pay careful attention to voltage gradients from the input node to adjacent conductors on the board. These gradients can create leakage currents that overwhelm the input impedance and bias current performance of the FET input. These leakage currents get much worse with contamination, humidity, and temperature. Guarding techniques can be used to protect against parasitic leakage currents by greatly reducing the voltage gradient seen by the input node. Physically, a guard is a low impedance conductor that surrounds a high impedance node and is raised to the voltage of that node. It serves to buffer leakage by diverting it away from the sensitive node and into the low impedance guard. A complication results from the fact that many traditional op amp pinouts place a supply pin next to the noninverting input. The only way to guard the input of one of these op amps is to route the guard trace between the input pin and the supply pin. Traces can be routed between pins for large packages, such as DIP or even SOIC; however, the board area consumed by these packages is prohibitive for many modern applications.

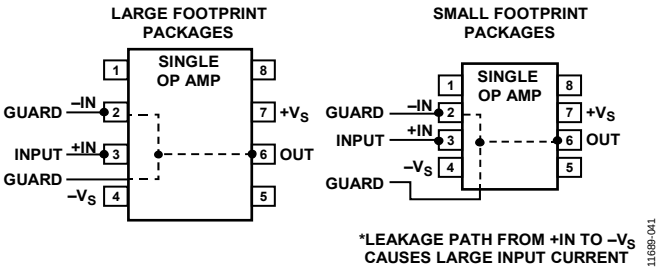

Figure 39. Single Op Amp Guarding Patterns

The AD8244 solves this problem with a unique pinout that naturally isolates the high impedance inputs from the low impedance nodes, such as the supplies and outputs of the other buffers. Additionally, the buffers of the AD8244 can be used to guard their own inputs, reducing the voltage gradient seen by the input to only the low offset voltage of the buffer. The AD8244 facilitates this by making guard traces easy to route without the need for traces to go between pins.

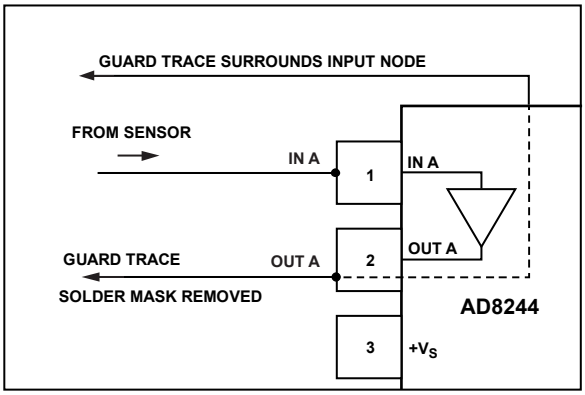

Figure 40. Guarding with the AD8244

INPUT PROTECTION

All terminals of the AD8244 are protected against ESD. In addition, the input structure allows for dc overload conditions up to a diode drop above the positive supply and a diode drop below the negative supply. Voltages more than a diode drop beyond the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, use an external resistor in series with each of the inputs to limit current for voltages beyond the supplies. In either scenario, the AD8244 input safely handles a continuous 6 mA current at room temperature.

For applications where the AD8244 encounters extreme overload voltages, as in cardiac defibrillators, use external series resistors and low leakage diode clamps, such as FJH1100 or BAV199L.

LAYOUT CONSIDERATIONS

The inputs of the AD8244 buffers are extremely high impedance. Shunt impedances from leakage resistance and parasitic capacitance in the printed circuit board (PCB) layout can severely degrade the performance of the JFET input. If a buffer output is used to surround the corresponding input node, leakage resistance and parasitic capacitance from the layout can be kept extremely low. Remove solder mask from the guard traces to guard against surface leakage due to contamination. In addition to the guard traces on the primary side, route a guard trace around any vias in the input net on the other side of the board as well. Keep the parasitic capacitance seen by the output small to maintain the optimum step response. Amplifiers used in the same signal path, such as buffering the voltage for two inputs of an in-amp or difference amplifier, must have matched impedance in the input traces. This includes matched length and symmetrical traces. Place any input resistors close to the AD8244 inputs to avoid interaction with trace parasitics. If one of the channels is not in use, connect the input to a voltage that is within its linear range to avoid overdrive conditions that can interfere with other channels. Leave the output unconnected. Place decoupling capacitors, such as 0.1 µF, near the AD8244. Larger capacitors, such as 10 µF, can be used farther away from the device.

DIFFERENTIAL SIGNAL CHAINS

The AD8244 can be used to buffer the inputs of difference amplifiers and instrumentation amplifiers to take advantage of qualities of the JFET input. In applications such as these, which use two channels of the AD8244 to buffer the positive and negative of a differential signal path, it is the mismatch between the channels, rather than the absolute error, that introduces error into the system. The AD8244 is designed so that the channels closely match and can be used in differential circuits with excellent results. Channel-to-channel matching errors are specified to aid in the design process. When driving the inputs of an instrumentation amplifier, difference amplifier, or other differential input circuit, the gain matching from channel to channel defines the common-mode rejection ratio (CMRR) error introduced to the system by the AD8244. The unit conversion is as follows:

$$CMRR\ (\text{dB}) = 20 \times \log_{10}(100/Gain\ Matching\ (\%))$$

The JFET pinch-off voltage can vary from channel to channel and cause additional mismatch when the JFET begins to saturate near the positive rail. The CMRR error is minimized by keeping the input voltage away from the positive input range limit. Because the input impedance is very high, the CMRR achieved in differential systems stays high, even with large or mismatched source resistance. See the Typical Performance Characteristics section for more information.

LOW OUTPUT IMPEDANCE vs. FREQUENCY

The closed-loop output impedance of the AD8244 increases at higher frequencies when the loop gain is reduced, as shown in Figure 12. The AD8244 drives 200 pF directly with slight ringing, as shown in Figure 35. By placing a small resistor in series with the output, the capacitive load drive of the AD8244 can be increased. For applications that need the AD8244 input performance and very low output impedance over frequency, such as driving a cable shield, a switching load, or a large amount of capacitance at high frequencies, an op amp can be added in a configuration, such as the one in Figure 41. This configuration takes advantage of the low op amp output impedance at low frequencies, and the load capacitor reduces the output impedance at high frequencies. Typically, $R_F \times C_F$ should be less than or equal to $R_O \times C_L$.

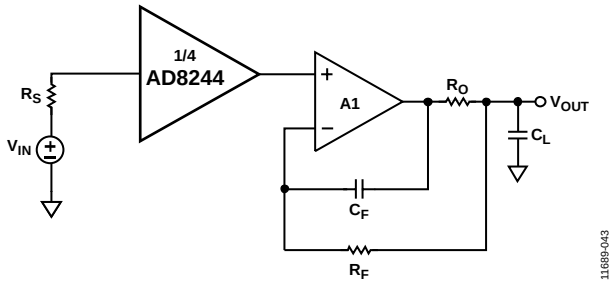

Figure 41. Adding an Op Amp for Low Output Impedance

APPLICATIONS INFORMATION

ELECTROCARDIOGRAM (ECG)

In an ECG system, mismatches between the source impedance of different leads, working against the input impedance of the front-end amplifier, can create unbalanced voltage dividers that reduce the system CMRR. When presented to a moderately high input impedance amplifier, the combined impedance of the skin, electrolyte, electrodes, and the protection resistors can be enough to cause power line noise pickup, current noise issues, and signal division. Dry electrode systems, which are becoming increasingly common and have significantly higher source impedance, are especially sensitive to these errors. Typically, a high input impedance, low bias current, FET input op amp is used to buffer the electrode signal before it is presented to an instrumentation amplifier. This buffer solves the majority of these problems; however, when an instrument is in the field, it can be subject to dust pickup and humidity. If the op amp input is not guarded, these environmental factors can create unwanted leakage currents that bring back the aforementioned issues from insufficient input impedance. The AD8244 pinout is configured to make it simple to guard the inputs from parasitic resistance and capacitance while it also drives the instrumentation amplifier inputs, creating a more robust design, while saving power and board space. The CMRR of the AD8244 driving an instrumentation amplifier initially depends on the gain matching for the chosen supplies and voltage range, as well as the instrumentation amplifier used, but it can be improved with design techniques such as right leg drive (RLD) or digital filtering.

FILTERING

In filtering applications, it is generally recommended to use capacitors such as C0G or NP0 ceramics for distortion and dielectric absorption performance. These types of capacitors do not have a high volumetric efficiency and are only available in values less than a few tens of nanofarads, depending on the case size and voltage rating. For a given cutoff frequency, using smaller capacitors requires larger resistor values. At low frequencies where the resistor values become very large, the bias current of a typical op amp can introduce significant offsets and additional noise. The subpicoampere bias current of the AD8244 allows resistor values in the tens of megaohms with no additional error while providing an excellent low power, small footprint solution for filter design. Between the four channels of the AD8244, a filter with more than eight poles can be implemented while using less space than the same filter with a quad op amp.

Sallen-Key Low-Pass Filter

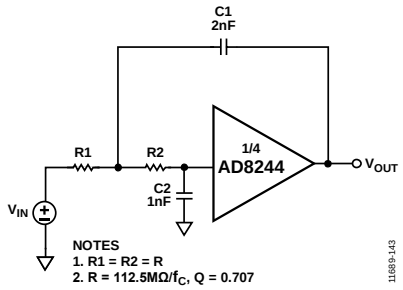

Figure 42. Sallen-Key Low-Pass Filter

The following equations describe the corner frequency, f_C, and quality factor, Q, for the low-pass filter case of the Sallen-Key topology, shown in Figure 42:

$$f_C = 1/(2\pi \sqrt{R1 \times R2 \times C1 \times C2})$$

$$Q = (\sqrt{R1 \times R2 \times C1 \times C2})/(C2 \times (R1 + R2))$$

For an example of a design with this topology, choose a filter where Q = 0.707 and R1 = R2 = R. This requires that C1 = 2 × C2. The corner frequency equation can now be simplified to

$$f_C = 1/(2\pi \times R \times C2 \times \sqrt{2})$$

If an available capacitor, such as 1 nF, is chosen for C2, R can be written in terms of the desired cutoff frequency:

$R = 1/(2\sqrt{2} \times \pi \times 1\ \text{nF} \times f_C) = 112.5\ M\Omega/f_c$ (that is, $R = 750\ \text{k}\Omega$ for $f_C = 150$ Hz)

Sallen-Key High-Pass Filter

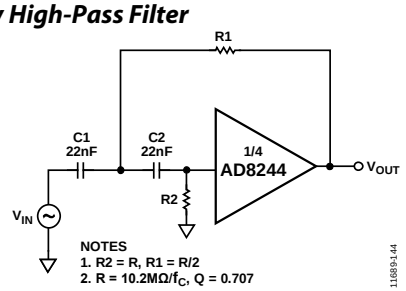

Figure 43. Sallen-Key High-Pass Filter

The high-pass filter case of the Sallen-Key topology has the same corner frequency equation as the low-pass filter. However, the equation for Q changes to

$$Q = (\sqrt{R1 \times R2 \times C1 \times C2})/(R1 \times (C1 + C2))$$

In this case, a Q of 0.707 is achieved with C1 = C2 = C, and 2 × R1 = R2 = R, which is a symmetrical result to the low-pass filter case.

The corner frequency then simplifies to

$$f_C = 1/(\sqrt{2} \times \pi \times R \times C)$$

For a low corner frequency, a larger available capacitor such as 22 nF can be chosen, yielding the following expression for R:

$R = 10.2\ M\Omega/f_c$ (that is, a 0.5 Hz filter requires R1 = 10 MΩ and R2 = 20 MΩ)

Twin-T Notch Filter

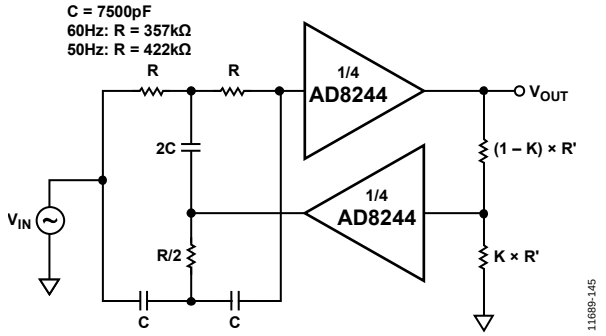

Figure 44. Twin-T Notch Filter

The following equations describe the parameters of the Twin-T notch filter with active feedback shown in Figure 44:

$$f_O = 1/(2\pi RC)$$

$$Q = 0.25/(1 - K)$$

where K is an attenuation factor from 0 to 1, as shown in Figure 44. A K of either 0 or 1 can be achieved with only one buffer.

One of the best things about this filter is that f_O and Q are independent, which allows for easy tuning of filter characteristics. However, designers use the Twin-T notch filter sparingly in production designs because of its sensitivity to component tolerances, which affect both the depth and the frequency of the notch. Reducing the Q is one way to ensure that the desired frequency has sufficient attenuation independent of component variance and drift; however, reducing the Q also linearly increases the distance between the pass bands. The notch depth can be improved and the stop-band width decreased simultaneously by cascading multiple filter stages.

To illustrate the benefit of cascading stages, Figure 45 shows the response of two filters, both designed to provide greater than 26 dB of attenuation at 60 Hz ± 5%, which allows for component tolerance. The single stage filter requires a Q of 0.5 and results in a −3 dB notch bandwidth of 120 Hz. The two stage filter has a Q of 2.25 for each stage, and the −3 dB notch bandwidth is reduced to about 40 Hz.

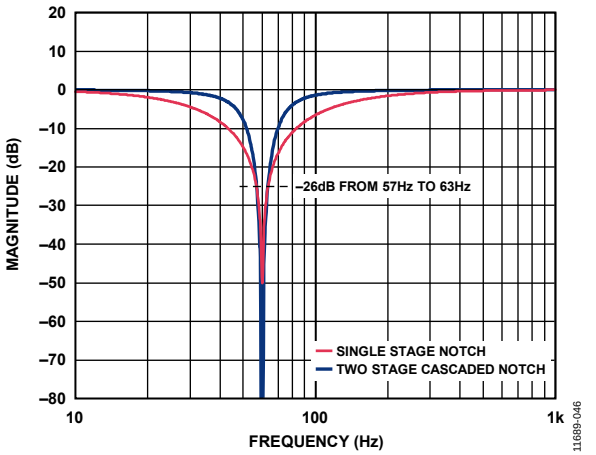

Figure 45. Cascading Notch Filters

PHOTODIODE AMPLIFIER

Photodiodes in precision circuits are typically measured in photovoltaic mode, in which there is no reverse bias voltage. Two benefits to this measurement mode are that there is no dark current, and the output is linearly related to the light intensity. However, in photovoltaic mode, the signal current can be very small, requiring a high gain transimpedance amplifier (TIA). There are a limited number of amplifiers suited for building TIAs for measuring photodiodes or other low current sensors, which can make it difficult to achieve high performance. Using an AD8244 as the interface to the photodiode eliminates the need for a low bias current op amp, allowing optimization of other parameters, such as precision, slew rate, output drive, board space, and cost. As with any composite amplifier, it is important to pay special attention to stability. The unity-gain crossover frequency of the op amp must be less than the AD8244 bandwidth for this configuration to be unity-gain stable. The noise gain of the op amp varies with the shunt resistance of the diode, which is temperature dependent.

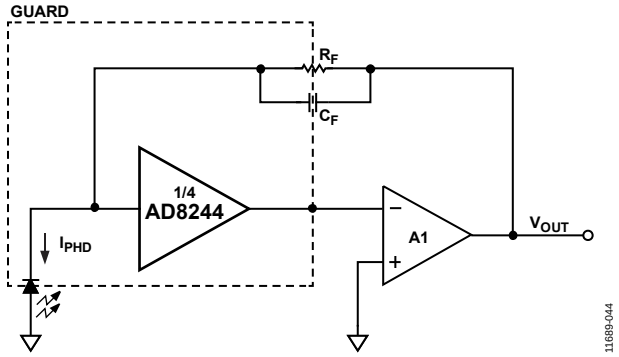

Figure 46. AD8244 in a Photodiode Application

LOW NOISE, JFET INPUT BUFFER

The voltage noise of the AD8244 can be reduced by placing multiple buffers in parallel. For example, two buffers in parallel reduce the voltage noise by √2, or all four buffers placed in parallel act as a buffer with ½ the noise. The trade-offs to this method are increased bias current, current noise, and input capacitance. Place a small resistor, such as 50 Ω, between the outputs to avoid extra current flow due to the slight differences between each output. For less power sensitive applications, these 50 Ω resistors can be omitted to boost the available output current.

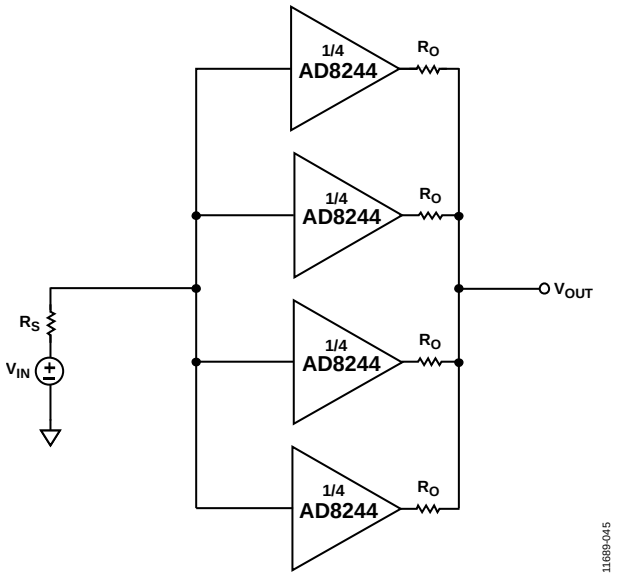

Figure 47. Reducing the Voltage Noise

OUTLINE DIMENSIONS

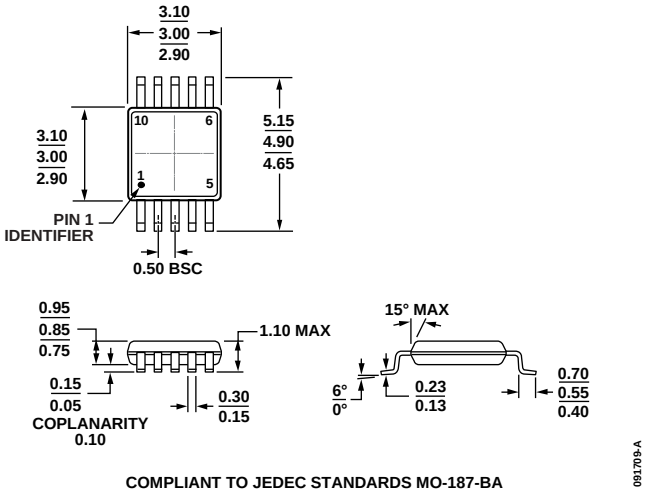

Figure 48. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8244ARMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP], Standard Grade	RM-10	Y54
AD8244ARMZ-R7	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP], Standard Grade, 7″ Tape and Reel	RM-10	Y54
AD8244BRMZ	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP], High Performance Grade	RM-10	Y55
AD8244BRMZ-R7	−40°C to +85°C	10-Lead Mini Small Outline Package [MSOP], High Performance Grade, 7″ Tape and Reel	RM-10	Y55
AD8244-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

NOTES

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